AY0438

32-Segment CMOS LCD Driver

FEATURES

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS process for: wide supply voltage range, low- power operation, high-noise immunity, wide temperature range
- CMOS and TTL-compatible inputs
- Electrostatic discharge protection on all pins
- Cascadable
- On-chip oscillator
- Requires only three control lines

APPLICATIONS

- Industrial displays
- Consumer product displays
- Telecom product displays
- Automotive dashboard displays

DESCRIPTION

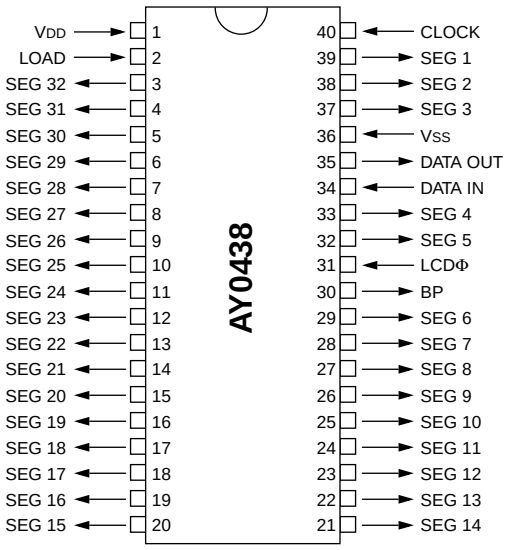
The AY0438 is a CMOS integrated device that drives a liquid crystal display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The AY0438 can drive any standard or custom parallel drive LCD display, whether it be field effect or dynamic scattering; 7-, 9-, 14- or 16-segment characters; decimals; leading + or -; or special symbols. Several AY0438 devices can be cascaded. The AC frequency of the LCD waveforms can either be supplied by the user or generated by attaching a capacitor to the LCD input, which controls the frequency of an internal oscillator.

The AY0438 is available in 40-lead dual in-line plastic and 44-lead PLCC packages. Unpackaged dice are also available.

PIN CONFIGURATION

40-Lead Dual In-line



44 PLCC

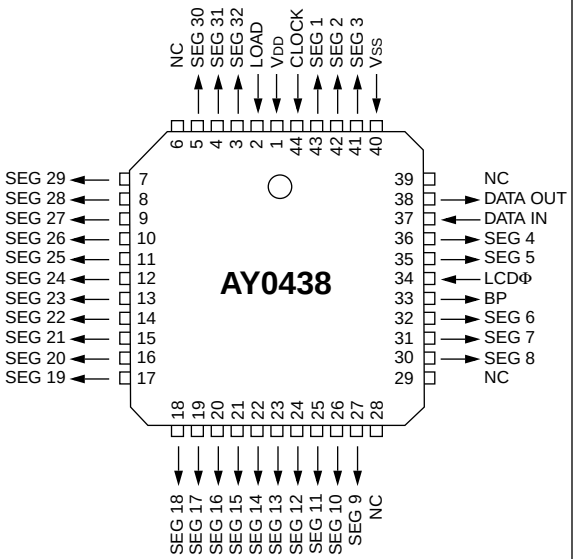


FIGURE 1: PIN DESCRIPTIONS

Pin # (PDIP Only)	Name	Direction	Description
1	V_{DD}	-	Supply voltage
2	Load	Input	Latch data from registers
3-29, 32, 33, 37-39	Seg 1-32	Output	Direct drive outputs
30	BP	Output	Backplane drive output
31	LCDΦ	Input	Backplane drive input
34	Data In	Input	Data input to shift register
35	Data Out	Output	Data output from shift register
36	V_{SS}	Ground	Ground
40	Clock	Input	System clock input

FIGURE 2: BLOCK DIAGRAM

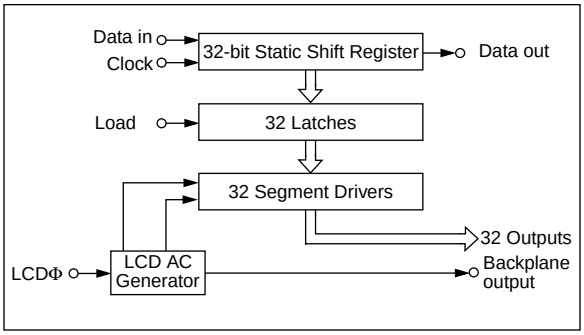


FIGURE 3: BACKPLANE AND SEGMENT OUTPUT

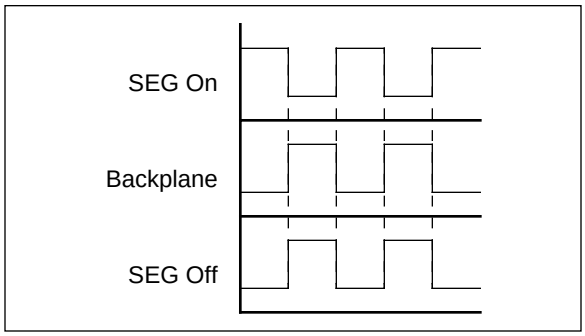
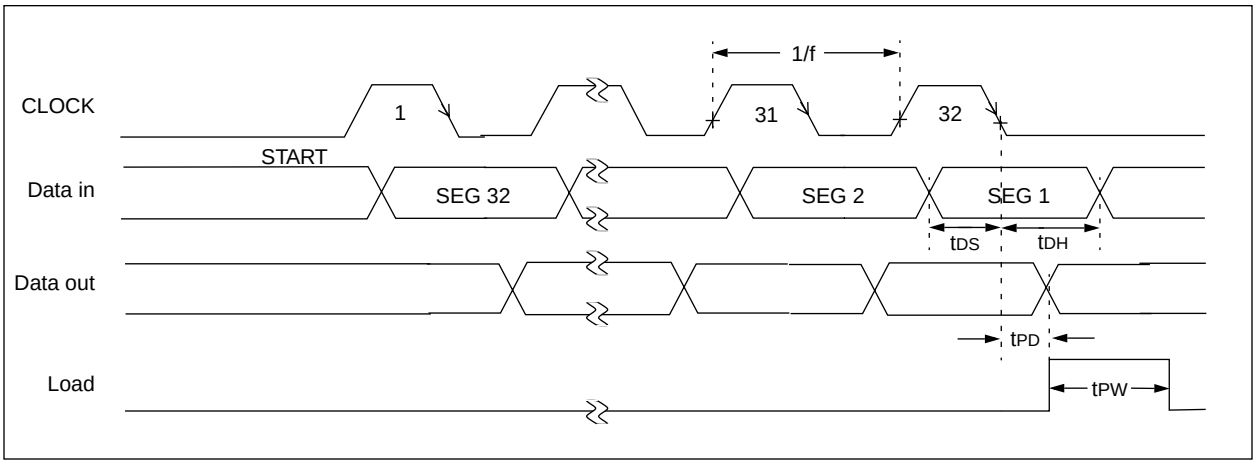


FIGURE 4: TIMING DIAGRAM



1.0 OPERATION:

1.1 Data In and Clock

The shift register shifts and outputs on the falling edge of the clock. Every clock falling edge does a logical left shift. As an example, if 32 clock pulses are supplied as in Figure 4, then the data input at the first clock will output at SEG 32, and the last data input (# 32) will output at SEG 1 when a LOAD signal is enabled (Figure 2). It is recommended that a complete 32 bit transfer be done every time the outputs are updated. A logic 1 at the Data In causes the corresponding segment to be enabled or visible, i.e. the output at Segment Output is 180° out-of-phase with the Backplane output (Figure 3).

1.2 Load

A logic 1 at the Load input (Figure 2) causes the parallel load of the data in the shift register into the latches that control the segment drivers. If the Load signal is tied high, then the latches become transparent and the segment drivers are always connected to the shift registers.

1.3 LCDϕ

LCDϕ can be driven by an external signal or by connecting a capacitor between LCDϕ and ground (GND), which will enable the on-chip oscillator required to generate the backplane output voltage. Figure 5 shows the relationship between capacitance value and output frequency. Leaving the LCDϕ input unconnected is not recommended. When driven by an external clock, the backplane output is in phase with the input clock. When cascading two AY0438 devices (Figure 6 and Figure 7), the backplane output can be generated using a capacitor to GND on the first AY0438. This backplane output can then be connected to the LCDϕ input of the second AY0438. The backplane output of the second device is then used to drive the backplane of the LCD module.

FIGURE 5: OSCILLATOR FREQUENCY GRAPH (TYPICAL @ 25°C)

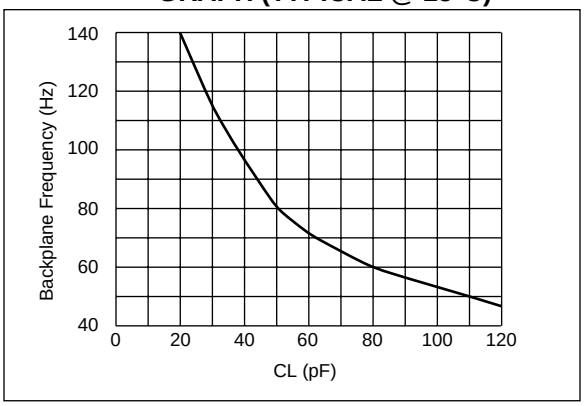


FIGURE 6: CASCADING TWO AY0438 DEVICES

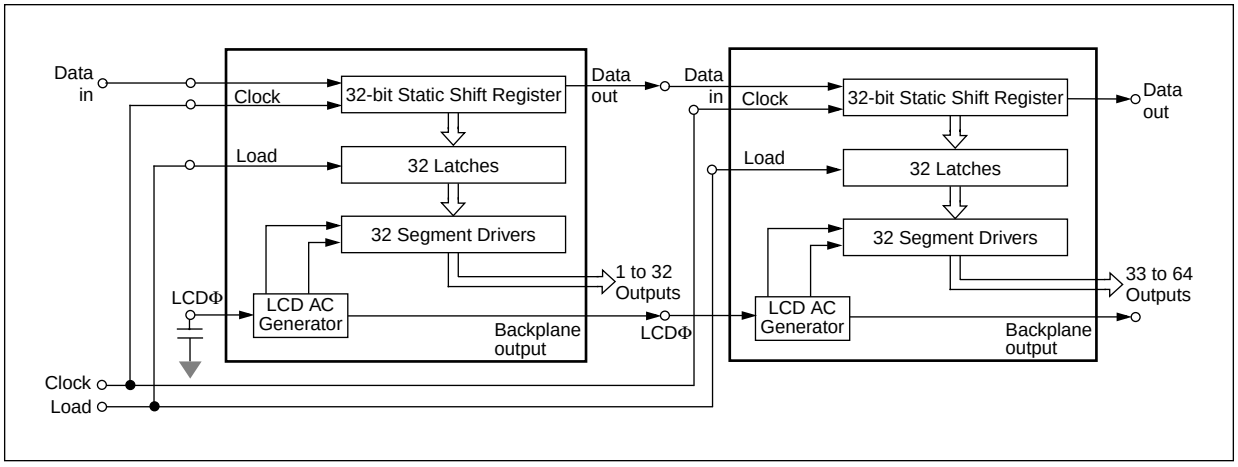
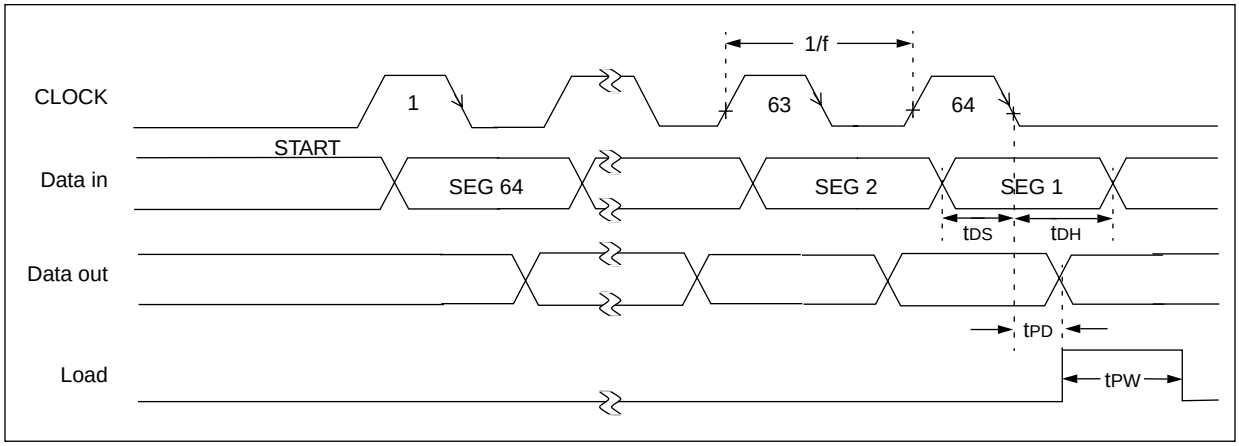


FIGURE 7: CASCADE TIMING DIAGRAM



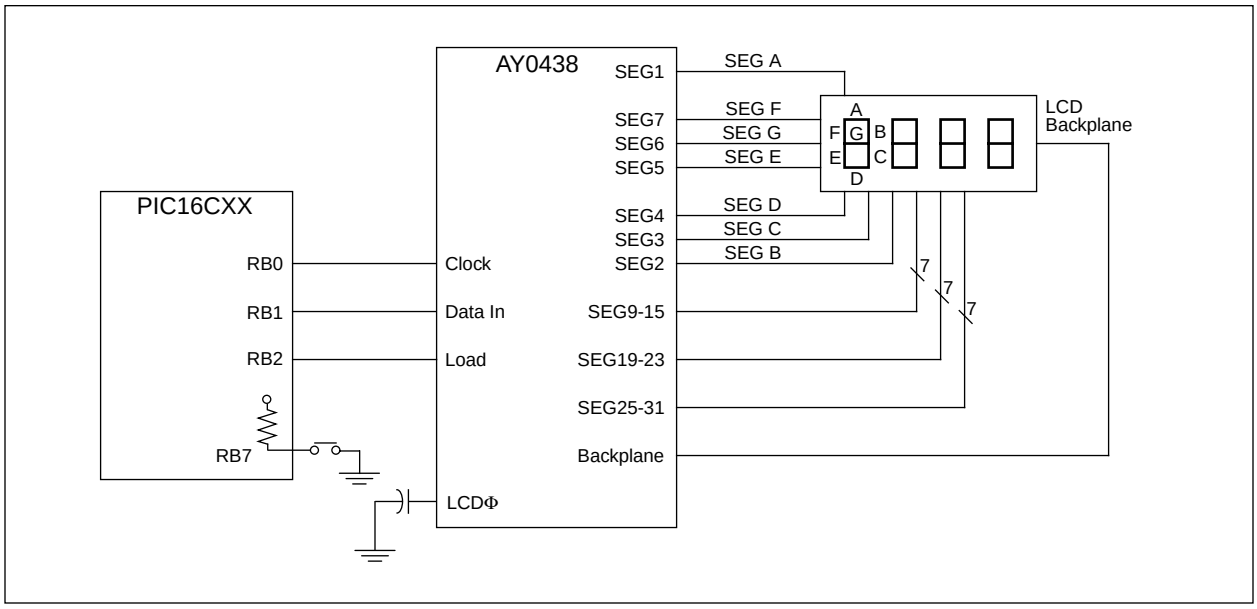
1.4 General

In order to avoid any race conditions, the Data In and Load signals should not be changed during a falling edge of the Clock. Figure 4 and Figure 7 show a typical timing diagram for a 32 segment and 64 segment LCD module.

1.5 Interfacing to a LCD Module and PIC16CXX Device

Figure 8 shows a typical layout of an AY0438 connected to a LCD module and interfaced to a PIC16CXX family device. Example 1 lists code used to program the PIC16CXX device. This code was complied using MPASM.

FIGURE 8: INTERFACING TO A LCD MODULE AND PIC16CXX DEVICE



EXAMPLE 1: EXAMPLE CODE

```
;*****************************************************************************
;This program shows an interface between a PIC16CXX device
;and the AY0438 LCD controller to control a 7 Segment
;4 digit LCD module.
;The PIC16CXX interface to the AY0438 Hardware:
;
;       PORTB bit 0 --> CLK
;       PORTB bit 1 --> DATA IN
;       PORTB bit 2 --> LOAD
;
;The LCD module is connected to the AY0438 as follows:
;       Most Significant digit  --> seg1 to seg7
;       3rd Significant digit   --> seg9 to seg15
;       2nd Significant digit   --> seg17 to seg 23
;       Least Significant digit --> seg25 to seg 31
;
```

```
;The DP are not connected, but can be connected to seg8, 16, 24 & 32.
;For each digit, the segments are connected as:
;       Seg A --> seg(8*n + 1)
;       Seg B --> seg(8*n + 2)
;       Seg C --> seg(8*n + 3)
;       Seg D --> seg(8*n + 4)
;       Seg E --> seg(8*n + 5)
;       Seg F --> seg(8*n + 6)
;       Seg G --> seg(8*n + 7)
;where n = 0, 1, 2 and 3 for MSD, 3rdSD, 2ndSD and LSD respectively.
;The firmware uses the values in registers:
;       MSD, THRDSD, SCNDSD and LSD   to determine the values to be
;pulsed to the AY0438.
;In this example, a pushbutton connected to PORTB bit 7
;is checked periodically to see if it has been pressed. If so,
;the LCD values in locations MSD to LSD are updated.
;*****************************************************************
        list p=16c71,f=inhx8m
;
;
MSD     equ     0x20
THRDSD  equ     0x21
SCNDSD  equ     0x22
LSD     equ     0x23
count   equ     0x24
temp    equ     0x25
PORTB   equ     0x06
#define CLK     PORTB,0
#define DATAIN  PORTB,1
#define LOAD    PORTB,2
#define UPDATELCD PORTB,7
w       equ     0
STATUS  equ     0x03
C       equ     0
RP0     equ     5
OPTION  equ     0x81
RBPU    equ     7
PCL     equ     0x02
PCLATH  equ     0x0A
;
;
        org     0
        goto    start
        org     0x10
;
;This DecodeValue table must reside in page 0 for this program to work
;
DecodeValue
        addwf   PCL
        retlw   B'00111111'     ;decode for 0
        retlw   B'00000110'     ;decode for 1
        retlw   B'01011011'     ;decode for 2
        retlw   B'01001111'     ;decode for 3
        retlw   B'01100110'     ;decode for 4
        retlw   B'01101101'     ;decode for 5
```

```
        retlw   B'01111101'     ;decode for 6
        retlw   B'00000111'     ;decode for 7
        retlw   B'01111111'     ;decode for 8
        retlw   B'01101111'     ;decode for 9
;
;
start
        clrf    PORTB
        bsf     STATUS,RP0      ;set portb 0,1&2 as outputs
        movlw   B'11111000'     ;       /
        movwf   PORTB           ;       /
        bcf     OPTION,RBPU     ;enable pull-up for switch
        bcf     STATUS,RP0
wait
        btfsc   UPDATELCD       ;see if update switch is low
        goto    wait            ;no then wait
        bcf     LOAD            ;make sure load is disabled
        movf    LSD,w           ;get least significant value
        clrf    PCLATH          ;PCH = 0
        call    DecodeValue     ;decode the value
        call    Send8           ;serially output the seg values
        movf    SCNDSD,w        ;get 2nd significant digit
        call    DecodeValue     ;decode it
        call    Send8           ;serially output it
        movf    THRDSD,w        ;get 3rd significant digit
        call    DecodeValue     ;decode it
        call    Send8
        movf    MSD,w           ;get Most significant value
        call    DecodeValue     ;decode it
        call    Send8           ;serially send it
        bsf     LOAD            ;toggle the LOAD line
        bcf     LOAD            ;to enable the latches
KeyReleased
        btfss   UPDATELCD       ;wait for key to be released
        goto    KeyReleased
        goto    wait            ;repeat loop.
;
;Send8, sends the 8 bits in the W register
Send8
        movwf   temp            ;save in temp
        movlw   .8              ;init count
        movwf   count           ;to 8
sendloop
        bcf     DATAIN          ;make sure DATAIN is low
        rrf     temp            ;rotate value through carry
        btfsc   STATUS,C        ;if bit clear then skip
        bsf     DATAIN          ;else set data bit
        bsf     CLK             ;toggle clock
        bcf     CLK             ;       /
        decfsz  count           ;see if 8 done
        goto    sendloop        ;no then do all
        return                  ;else return

        end
```

2.0 ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} ..... -0.3V to +12V

Inputs (CLK, Data In, Load) ..... V_{CC} to V_{DD} +0.3V

LCDΦ Input ..... -0.3V to V_{DD} +0.3V

Power Dissipation ..... 250 mW

Storage Temperature ..... -65˚C to +125˚C

Operating Temperature Industrial ..... -40˚C to +85˚C

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled “typical” is presented for design guidance only and is not guaranteed.

TABLE 2: DC CHARACTERISTICS

V_{DD} = +5V unless otherwise noted, T_A = 40°C to +85°C							
Characteristics		**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Supply Voltage		V_{DD}	+3.0	—	+8.5	V	
Supply Current		I_{DD}	—	25	60	µA	LCDΦ OSC < 15 kHz
			—	13	30	µA	LCDΦ OSC < 100 Hz
Input High Level		V_{IH}	0.5 V_{DD}	—	V_{DD}	V	
Input Low Level	Clock	$V_{IL}1$	0	—	0.1 V_{DD}	V	3.0V ≤ V_{DD} ≤ 8.5V
	Data,	$V_{IL}2$	0	—	0.1 V_{DD}	V	3.0V ≤ V_{DD} ≤ 8.5V
Input Leakage Current	Load	I_L	—	0.01	±10	µA	V_{IN} = 0V and +5.0V
Input Capacitance		C_I	—	—	5.0	pF	V_{DD} = +5.0V
Segment Output Voltage		V_{OH}	0.8 V_{DD}	—	V_{DD}	V	I_{OH} = -100 µA
		V_{OL}	0	—	0.1 V_{DD}	V	I_{OL} = 100 µA
LCDΦ Input High Level		V_{IN}	0.9 V_{DD}	—	V_{DD}	V	
LCDΦ Input Low Level		V_{IL}	0	—	0.1 V_{DD}	V	
LCDΦ Input Leakage		I_L	—	—	10	µA	V_{IN} = 0V and +5.0V
							V_{DD} = +5.0V

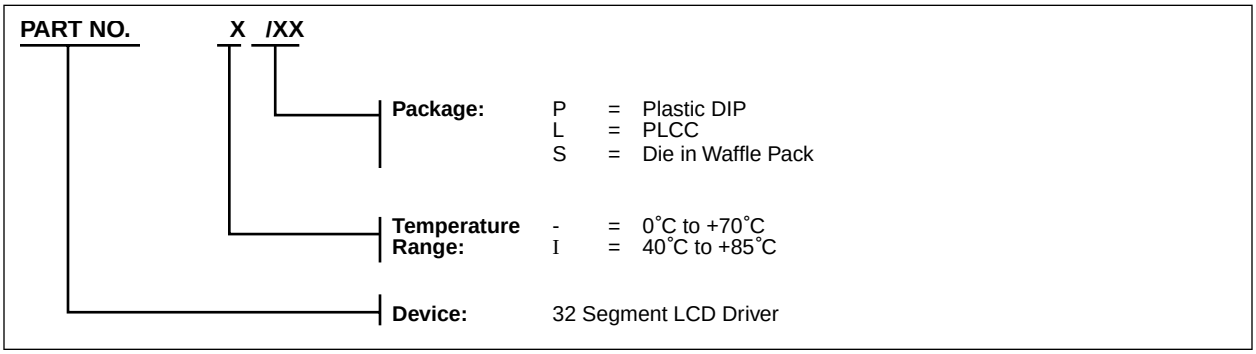
TABLE 3: AC CHARACTERISTICS

Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Clock Rate	f	DC	—	1.5	MHz	50% duty cycle
Data Set-up Time	t_{DS}	150	—	—	nsec	Data change to Clk falling edge
Data Hold Time	t_{DH}	50	—	—	nsec	
Load Pulse Width	t_{PW}	175	—	—	nsec	
Data Out Prop. Delay	t_{PD}	—	—	500	nsec	C_L = 55 pF

NOTES:

AY0438 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



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