# SSI 73M214
## Modem
## Analog Front End

June, 1990

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## DESCRIPTION

The SSI 73M214 is a complete analog front end IC for digital signal processor based V.22bis, V.22, Bell 212A, V.21, and Bell 103 compatible modems.

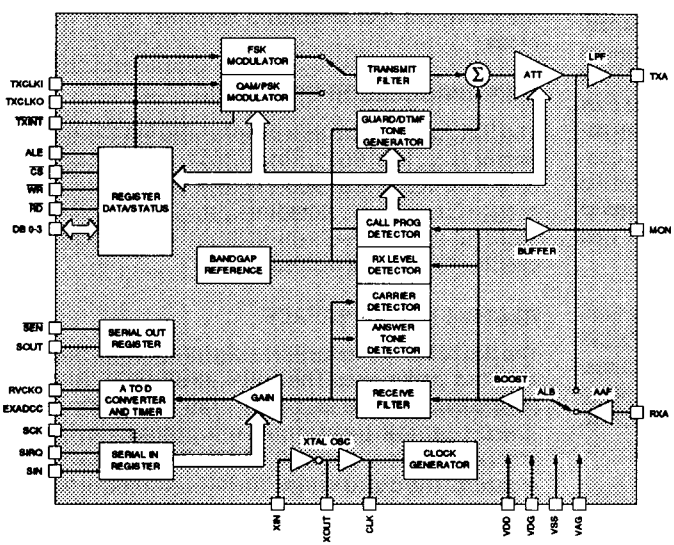
The 73M214 provides bandsplit filters, compromise equalization, and digitally controlled receive gain and transmit attenuation. An 8-bit A/D convertor is available for receive signal processing, and on-chip modulators provide the QAM, PSK, and FSK transmit signals, making it unnecessary for the DSP to perform the transmit functions. A tone generator is used to produce DTMF, answer, and guard tones while an analog loopback mode allows system testing. Carrier, answer, and call progress tone detection is provided.

The SSI 73M214 uses two busses to transfer data and control information. A 4-bit address/data multiplexed bus is used for connection to a control microprocessor (8031 typical) which performs the scrambler/descrambler, buffer/debuffer, system control, data, and user interface functions. A serial data bus transfers received digitized data as well as receiver status information to a standard DSP (7720 typical). The DSP also sends the 73M214 receive timing and gain control information over the serial bus. (Continued)

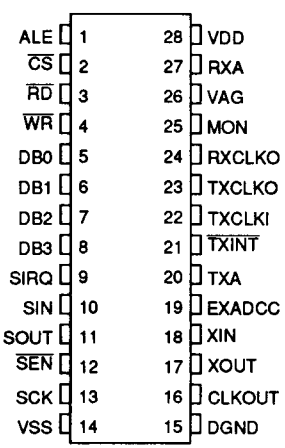
## FEATURES

- **Analog front end for DSP-based V.22bis modems**
- **Complete modulators for QAM/DPSK (V.22bis, V.22, Bell 212) and FSK (Bell 103 and V.21)**
- **Programmable receive gain/transmit attenuation**
- **8-bit ADC with reference, sample and hold**
- **Band split filters with compromise equalization**
- **Analog loopback test mode**
- **Serial interface for receive processing**
- **Parallel interface for transmitter and control**
- **Timer for transmit synchronization**
- **Programmable timer for receiver data clock recovery**
- **Carrier, call progress, and answer tone detectors**
- **Audio monitor for audible call status**
- **DTMF, guard tone, and answer tone generation**
- **Crystal oscillator with output buffer**
- **Low power CMOS (± 5V at < 250 mW)**
- **28-pin plastic DIP or PLCC surface mount package**
- **Controllable audio monitor**

## BLOCK DIAGRAM




## PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component

## DESCRIPTION (Continued)

The SSI 73M214 is ideal for use in self-contained or integral intelligent modem products requiring the benefits of 2400 bit/s full duplex operation while maintaining compatibility with existing standards at speeds down to 300 bit/s. By integrating the majority of the analog functions needed on a single CMOS IC, system complexity and cost is reduced without compromising performance or features.

## OPERATION

The SSI 73M214 provides the analog front end processing for a V.22bis/224 2400 bit/s modem. The SSI 73M214 includes band-split filters, fixed U.S. compromise line equalizer, programmable gain/attenuator for receive and transmit functions, FSK/QAM modulators, differential encoder, and an analog to digital converter. The 73M214 interfaces to an external digital signal processor and inexpensive control microprocessor to complete the modem function.

## FUNCTIONAL DESCRIPTION

The 73M214 allows selection of 300 bit/s, 600 bit/s, 1200 bit/s, or 2400 bit/s transmission modes. The 73M214 generates the bit rate clocks RVCKO (receive) and TXCKO (transmit) and a baud rate clock $\overline{\text{TXINT}}$. In the synchronous modes, there is a fixed phase relationship between TXCKO and $\overline{\text{TXINT}}$ (refer to figure of Transmit Timing). Each case here assumes that the receive timer is in internal timing mode, otherwise RVCKO is high. Register CR0 selects a mode (there are three synchronous modes and one asynchronous mode). In internal synchronous mode, the SSI 73M214 generates an accurate bit rate clock, TXCKO. This may be used for data transfers from the DTE to the microprocessor. The microprocessor sends the latest quadbit (or dibit), which is latched into the modulator on the falling edge of $\overline{\text{TXINT}}$. Pin TXCKI is ignored in internal synchronous mode. RVCKO is the receiver bit rate clock.

In external synchronous mode the data rate clock from the DTE should be connected to the TXCKI pin. TXCKI is used to generate phase locked clocks TXCKO and $\overline{\text{TXINT}}$ (TXCKI's falling edge synchronously resets an internal counter). RVCKO is the receiver bit rate clock.

## RECEIVE PROCESSING

The received signal from the line passes through an anti-alias filter with adjustable gain, then through a band-split filter with selectable compromise line equalization, after which it is amplified by a programmable gain stage. The analog signal is converted to an 8-bit, 2's complement number for the digital signal processor. The ADC output and AGC gain word are transferred serially between the DSP and SSI 73M214. A programmable timer is included for use in the data clock recovery loop. Answer tone, carrier, and imprecise call progress detectors are included for modem smart dialing capability.

## TRANSMIT PROCESSING

In QAM (DPSK) mode, the quadbit (dibit) is transfered to the SSI 73M214 where it is differentially encoded and then passed through a baseband filter. The baseband information is modulated up to 1200 Hz or 2400 Hz. A band-split filter shapes the modulator output and provides compromise line equalization. The transmitted spectrum has the recommended square root of 75% raised cosine shaping. Guard tone is added to the signal after the filter, and the programmable attenuator sets the transmit amplitude. Finally, a smoothing filter eliminates out-of-band energy generated by the switched-capacitor filters.

In FSK mode, a programmable tone generator acts as the modulator. The modulator output passes through the band-split and smoothing filters as in the QAM mode.

## MICROPROCESSOR INTERFACE

The SSI 73M214 acts as a peripheral to the microprocessor (e.g., Intel 8051, Zilog Z8601, Motorola 6801) on a 4-bit multiplexed address/data bus. Control and status information are stored in registers on the 73M214. Transmit data is also sent from the microprocessor over the bus in 4-bit nibbles.

## RECEIVE DSP INTERFACE

The SSI 73M214 interfaces to a digital signal processor over two serial ports. The serial interface is directly compatible with the NEC/OKI 7720 or 77C20. The 73M214 can also be interfaced with parallel bus signal processors using standard LSTTL 7400 series shift registers. The digital sample from the A/D convertor is

sent to the DSP on the serial output port, and the AGC gain value is sent from the DSP to the SSI 73M214 on the serial input port. Both serial ports transfer 16 bits simultaneously under timing control generated by the 73M214.

In slave mode TXCKO and $\overline{\text{TXINT}}$ are phase locked internally to RVCKO (RVCKO's falling edge synchronously resets an internal counter). Pin TXCKI is ignored in slave mode. If the internal receive timer is not being used, slave mode can be implemented by putting the SSI 73M214 in external synchronous mode and externally connecting the recovered receiver bit rate clock to TXCKI.

Asynchronous mode operation is the same as internal synchronous mode, except TXCKO and RVCKO are high.

### SERIAL DSP INTERFACE

Serial DSP Interface provides for communication between the DSP and the 73M214. A programmable receive timer block which provides for adjustment of the ADC sampling rate is included on the 73M214. It may be used as part of the data clock recovery loop. The receive timer control bits RvT1 and RvT0 (TR0) select one of four possible ADC modes; off, external timing, internal timing 7200 Hz, or internal timing 9600 Hz. The DSP through serial port SIN (bits 8-9) provides for adjustment to the internal sampling clock rates either 7200 Hz ± 1 µs or 9600 Hz ± 1 µs. The falling edge of $\overline{\text{SEN}}$ corresponds to the following events:

1) The signal on RXA is sampled and an 8-bit analog-to-digital conversion begins.
2) The previous 8-bit ADC sample and the status bits are loaded into a register for serial shifting out of port SOUT to the DSP.
3) The previous gain & timer bits from the DSP are latched into the 214 register and the current DSP serial word is shifted into port SIN.

Serial Output- 16-bit word - bit 0 (LSB) is shifted out first.

| BIT # | 15 - 12 | 11 | 10 | 9 | 8 | 7 - 0 |
|---|---|---|---|---|---|---|
| Output Data | Fast C.D. | Slow C.D. | A.T. | CPD | RCV Level | ADC Output |

Serial input - 10 bits - bit 0 (LSB) is shifted first.

| Bit # | 15 - 10 | 9 - 8 | 7 | 6 - 0 |
|---|---|---|---|---|
| Input Data | X | RCV Timer Control | X | Gain Word (Log) MSB-LSB |

### SERIAL DSP TIMING

The timing diagram for the serial receive processor interface is shown in Figure 3. Signal SIRQ is generated by the NEC/OKI 77C20 and must be high to send SIN data. If it is low during a serial transmission, SOUT remains active but SIN becomes inactive and the 73M214 will continue to use the last gain/timer value. SCK from the 73M214 is the serial shift clock.

### QAM/DPSK ENCODER/MODULATOR

The quadbits sent to the 73M214 are differentially encoded according to the CCITT V.22bis specification. The encoded quadbits are then passed through an FIR baseband filter. The baseband signal thus generated is modulated by the carrier at either 1.2 kHz or 2.4 kHz.

### FSK MODULATOR

The FSK modulator frequency modulates the data in a continuous phase manner. FSK operation is asynchronous and is determined by the control bits shown:

| REGISTER | D3 | D2 | D1 | DCR |
|---|---|---|---|---|
| CR0 | 1 | 1 | x | x |
| CR1 | 0/1 | x | x | 1 |
| CR3 | 0 | 0 | x | 0/1 |
| TR0 | x | x | 1 | 0 |
| TR1 | 1/0 | 1/0 | 1/0 | 1/0 |

### TONE GENERATOR

The tone generator will output a dual-tone (DTMF) or a single tone (FSK, answer tone, or guard tone) on the TXA line if the appropriate control bits are enabled. The control bits are found in register TR0 and TR1. The tone is specified by register TR1 - 16 dual-tone combinations and 7 single tones are possible. DTMF has priority over single tones. The tone generator consists of 4 blocks: tone selection and control, two programmable down counters, two three-level six-step square wave generators, and a 3-pole ladder filter with programmable gain and pole setting.

### BAND SPLIT FILTERS

The band-split filters provide attenuation for out-of-band noise components and near-end cross talk. The filters also provide some of the root 75% raised cosine shaping for minimum intersymbol interference. Transmit and Receive delay equalization can be bypassed by using the TxEQ and RvF1 bits. The receive filter can be bypassed for direct access to the ADC with the RvF0 bit.

### PROGRAMMABLE GAIN STAGE

The programmable gain stage is part of an AGC loop which is controlled by the receive digital signal processor. The gain increased monotonically with increasing gain word. The 7-bit gain setting covers a 48 dB range with 0.375 dB steps. Minimum gain of 0 dB corresponds to 0000000, maximum gain of 48 dB is 1111111.

### ADC

The 8-bit analog to digital converter provides a 2's complement representation of the sampled analog voltage. The sample and hold function is incorporated in this switched-capacitor ADC.

### TRANSMIT ATTENUATOR

The programmable transmit attenuator allows the control processor to set the transmit power level. If the attenuator control bits are set to 0000, the attenuator acts as a unity gain stage. The attenuation increments by 1 dB per bit.

In addition to the user programmable attenuator, there is an internally controlled attenuator for the QAM/DPSK modulated signal. The attenuation value is determined by the guard tone selected and assures that modulated data plus guardtone gives 0 dBm prior to the transmit attenuator regardless of the guard tone setting.

### DETECTORS

The special detect circuitry checks the received analog signal for special conditions. The conditions checked for are the presence of a carrier (i.e., energy in the receive band), the presence of an answer tone (2100 or 2225 Hz), and the presence of a call progress signal.

### IMPRECISE CALL PROGRESS DETECTOR

The call progress detector monitors activity on the line. This detector is an imprecise call progress detector- the on/off envelope of the signal is replicated as a 1/0 in the CPD bit of the SR register. The detector consists of a bandpass filter followed by a peak detector. The 3 dB points of the bandpass filter are 350 Hz and 620 Hz. Dial-tone, busy-signal, ringback and reorder are composed of at least one tone in this band.

### PRECISE ANSWER TONE DETECTOR

The receive filter output is fed to a highly selective frequency discriminator controlled by the ABT1 and ABT0 bits of the DCR register to detect 2100 and 2225 Hz answer back tones. The frequency discriminator is gated by the output of the carrier detector to provide amplitude discrimination.

### CARRIER DETECTOR

The carrier detector detects the presence of a signal in the receive band. When energy is detected the CAR bit of the SR register is set to "1." The detector uses a peak-to-peak amplitude detecting scheme which requires knowledge of the Peak/Rms ratio of the waveform to be detected. This information is obtained from the data rate control register (CR0) bits DR1 and DR0.

| DR1 | DR0 | Carrier Type | Peak/Rms |
|---|---|---|---|
| 0 | 0 | None | 1.414 |
| 0 | 1 | FSK | 1.414 |
| 1 | 0 | DPSK | 2.0 |
| 1 | 1 | QAM | 2.5 |

The fast carrier detect is an imprecise carrier detector that is derived from the short term peak-to-peak amplitude in the carrier detector. The detector output will be erratic for small signals with high peak-to-rms values. The fast carrier is output on the FCAR bit of the serial output port.

### RECEIVE LEVEL DETECTOR

The receive level detector indicates whether the signal present at RXA is too large to permit the use of the receive gain (RvGE) of 12 dB prior to the band-split filters. When the RvL bit of the SR register - "1," the signal is too large to use the gain.

A fixed, switchable 12 dB gain is provided ahead of the band-split filters to be used when the total received signal (received signal + near-end signal) is more than 12 dB below the maximum allowed input voltage.

### OUTPUT SMOOTHING FILTER

The output smoothing filter attenuates out-of-band frequency components that are generated by the switched capacitor filters on the chip.

### INPUT ANTI-ALIAS LOW PASS FILTER

The anti-alias low pass filter prevents aliasing of incoming frequency components into the passband of interest.

## PIN DESCRIPTION



### POWER

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| VDD | 28 | I | Positive voltage supply (+5V) |
| VSS | 14 | I | Negative voltage supply (-5V) |
| VAG | 26 | I | Analog Ground |
| VDG | 15 | I | Digital Ground |

### ANALOG INTERFACE

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| RXA | 27 | I | Receive analog input from line. |
| TXA | 20 | O | Transmit analog output to line. Modulator output as well as DTMF output uses this pin. |
| XIN | 18 | I | Crystal connection, 7.3728 MHz crystal, or externally generated 7.3728 MHz oscillator input. |
| XOUT | 17 | O | Crystal connection, 7.3728 MHz crystal. |
| CLKOUT | 16 | O | Crystal oscillator output echoed for system use. |
| MONITOR | 25 | O | Analog output for call progress tone monitoring. Can be muted (see Control Bits). |

### MICROPROCESSOR INTERFACE

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| DB0-DB3 | 5,6,7,8 | I/O | (Bi-directional, 3 state) Address/Data Bus. |
| $\overline{CS}$ | 2 | I | Chip Select. A low allows a read or write cycle to occur. DB0-DB3 can not be written to or read from if $\overline{CS}$ (latched) is not low. $\overline{CS}$ is latched on the falling edge of ALE. |
| $\overline{RD}$ | 3 | I | Read. A low requests a read of the 73M214 registers. Data cannot be ouput on DB0-DB3 unless both $\overline{RD}$ and the latched $\overline{CS}$ are low. |
| $\overline{WR}$ | 4 | I | Write. A low informs the 73M214 that data is available on DB0-DB3 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$ - no data is written unless both $\overline{WR}$ and $\overline{CS}$ are low. |
| ALE | 1 | I | Address strobe line for multiplexed addressed/data bus. The falling edge of ALE latches the address on DB0-DB3 and the chip select $\overline{CS}$. |

**TRANSMIT INTERFACE**

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| TXCKI | 22 | I | Transmit clock input, used for the external synchronous mode. In external synchronous mode, all clocks for the modulator are synchronized to this bit rate clock. |
| TXCKO | 23 | O | Bit rate transmit clock output, provided when the modulator is in a synchronous mode. In FSK, or modulator off modes, this pin is pulled high. |
| $\overline{\text{TXINT}}$ | 21 | O | Transmit interrupt, active low. Baud rate clock which requests a new quadbit for the modulator. Active in the 1200 or 2400 bit/s modes only. Forced high otherwise. |

**RECEIVE INTERFACE**

| NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| RVCKO | 24 | O | Bit rate receive clock output from receive timer. Output is active in 2400 or 1200 bit/s transmission when the internal timer is used and the modulator is operating in a synchronous mode. Otherwise the output is forced high. |
| SOUT | 11 | O | Output serial port - sends ADC/status bits to DSP. |
| SIN | 10 | I | Input serial port receive gain and timer bits from DSP. |
| SIRQ | 9 | I | Serial input request. SIRQ high signifies that data is available to shift into SIN port - SIRQ low causes SIN port to retain past data and not shift. SIRQ is latched by $\overline{\text{SEN}}$ falling edge. SIRQ does not affect the shifting of the SOUT port. |
| $\overline{\text{SEN}}$ | 12 | O | Serial enable pin. Enables serial shifting on SOUT and SIN ports. Signal is low for 16 cycles of SCK. |
| SCK | 13 | O | Shift clock generated on 73M214 for serial ports SIN and SOUT. Clock rate is 184 kHz and is resychronized to receive timer every $\overline{\text{SEN}}$ falling edge. |
| EXADCC | 19 | I | External ADC convert clock input which is required if the internal receive timer is not being used. The rising edge of EXADCC is aligned to an internal 922 kHz clock; it starts an ADC conversion and serial shifting over the SIN and SOUT ports. |

**REGISTER ADDRESSES**

The signals A0, A1, A2, and A3 (DB0-DB3 latched by ALE) are used to address the on chip registers.

| FUNCTION | REGISTER | D3 | D2 | D1 | D0 | A3-A0 |
|---|---|---|---|---|---|---|
| Transmit Control Register | CR0 | DR1 | DR0 | TxM1 | TxM0 | 0000 |
| Interface Control Register | CR1 | FBK | RvF1 | RvF0 | $\overline{\text{TxSQ}}$ | 0001 |
| Attentuation Control Register | CR2 | ATT3 | ATT2 | ATT1 | ATT0 | 0010 |
| Set-up Control Register | CR3 | TST | ALB | RvGE | ORIG | 0011 |
| Detect Control Register | DCR | ABT1 | ABT0 | MONEN | RST | 0100 |
| Status Register | SR | CAR | ATD | CPD | RvL | 0101 |
| Transmit Tone Control Reg. 0 | TR0 | RvT1 | RvT0 | ST | DTMF | 0110 |
| Transmit Tone Control Reg. 1 | TR1 | TRB3 | TRB2 | TRB1 | TRB0 | 0111 |
| Quadbit Register-QAM/DPSK | QBR | QB3 | QB2 | QB1 | QB0 | 1000 |

## REGISTER BIT DESCRIPTION

| TRANSMIT CONTROL REGISTER | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| CR0 | DR1 | DR0 | TXM1 | TXM0 |

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0, D1 | Transmit Modes (TXM0, TXM1) | D1 D0<br>0 0 | Asynchronous mode: Modulator clocks are derived from crystal. The 73K214 operates in the internal synchronous mode as described below. TXCKO and RVCKO are high in asynchronous mode. |
| | | 0 1 | Internal synchronous mode: Modulator clocks are derived from crystal. The SSI 73M214 generates an accurate bit rate clock, TXCKO. This may be used for data transfers from the DTE to the microprocessor. The microprocessor scrambles the data and sends the latest quadbit or (dibit) to the modulator as requested by the baud rate clock TXINT. The TXCKI pin is ignored in the internal synchronous mode. If the receive timer is enabled, RVCKO is a bit rate clock. If the receive timer is disabled, RVCKO is high. |
| | | 1 0 | External synchronous mode: Modulator clocks are synchronized to signal on TXCKI pin. The data rate clock from the DTE should be connected to the TXCKI pin. This clock is internally synchronized to a high speed clock. The synchronized signal is echoed on pin TXCKO and used to generate the quadbit interrupt signal TXINT. RVCKO is as described above. |
| | | 1 1 | Slave mode: Modulator clocks are synchronized to RVCKO signal. In slave mode with the receive timer enable, RVCKO signal is internally routed to TXCKI. If the receive timer is not being used, slave mode can be implemented by putting the SSI 73K214 in external mode and connecting the recovered bit rate clock to TXCKI. |

**REGISTER BIT DESCRIPTION** (continued)

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D2, D3 | Data Rates | D3 D2<br>0 0 | Modulator off: With the modulator off, carrier detect defaults to FSK settings, and the modular output is effectively shortened to ground. |
| | | 0 1 | Select FSK operating mode. The FSK modulation is performed by programming the tone generator output frequency. Operation is asynchronous, and the transmission mode control bits (CR0 - TXM1, TXM0) are ignored in FSK mode. TXCKO and RVCKO are high. |
| | | 1 0 | Select DPSK operating mode at 1200 bit/s. |
| | | 1 1 | Select QAM operating mode at 2400 bit/s. |

| INTERFACE CONTROL REGISTER | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| CR1 | FBK | RvF1 | RvF0 | $\overline{\text{TxSQ}}$ |

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0 | Tx squelch ($\overline{\text{TxSQ}}$) | 0 | Disables transmit output at TXA. Forces TXA output to ground. |
| | | 1 | Enables transmit output at TXA. |
| D1 | Receive Filter (RvF0) | 0 | Select normal mode. |
| | | 1 | Bypass receive filter to allow direct access to ADC. |
| D2 | Receive Filter Equalizer (RvF1) | 0 | Select normal mode. |
| | | 1 | Bypass Receive filter delay equalizer. |
| D3 (FBK) | Fallback | | Selects low speed options. (See Table 1.) |

**REGISTER BIT DESCRIPTION** (continued)

**Table 1: Rate/Mode Selections**

Register bits CR0 - DR1, DR0, TXM1, TXM0 and CR1 - FBK control the data clocks and modular mode. To enable DPSK/QAM modulation, FSK and Answer tones must be disabled. This table assumes the receive timer to be in internal timer mode (if not RVCKO is high) - see register TR0 - RVT1, RVT0.

| CR1 | CR0 | | | | MODULATOR MODE | DATA CLOCKS | | |
|---|---|---|---|---|---|---|---|---|
| FBK | DR1 | DR0 | TXM1 | TXM0 | | TXCKO | $\overline{\text{TXINT}}$ | RVCKO[1] |
| x | 0 | 0 | 0 | 0 | off | 1 | 1 | 1 |
| x | 0 | 0 | 0 | 1 | off | 1200 Hz | 1 | 1200 Hz |
| x | 0 | 0 | 1 | 0 | off | TsCKI | 1 | 1200 Hz |
| x | 0 | 0 | 1 | 1 | off | RVCKO | 1 | 1200 Hz |
| 0 | 0 | 1 | X | X | FSK(103) | 1 | 1 | 1 |
| 1 | 0 | 1 | X | X | FSK(V.21) | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | DPSK | 1 | 600 Hz | 1 |
| 0 | 1 | 0 | 0 | 1 | DPSK | 1200 Hz | 600 Hz | 1200 Hz |
| 0 | 1 | 0 | 1 | 0 | DPSK | RXCKI | 600 Hz | 1200 Hz |
| 0 | 1 | 0 | 1 | 1 | DPSK | RVCKO | 600 Hz | 1200 Hz |
| 1 | 1 | 0 | 0 | 0 | DPSK | 1 | 600 Hz | 1 |
| 1 | 1 | 0 | 0 | 1 | DPSK | 600 Hz | 600 Hz | 600 Hz |
| 1 | 1 | 0 | 1 | 0 | DPSK | TXCKI | 600 Hz | 600 Hz |
| 1 | 1 | 0 | 1 | 1 | DPSK | RVCKO | 600 Hz | 600 Hz |
| x | 1 | 1 | 0 | 0 | QAM | 1 | 600 Hz | 1 |
| x | 1 | 1 | 0 | 1 | QAM | 2400 Hz | 600 Hz | 2400 Hz |
| x | 1 | 1 | 1 | 0 | QAM | TXCKI | 600 Hz | 2400 Hz |
| x | 1 | 1 | 1 | 1 | QAM | RVCKO | 600 Hz | 2400 Hz |

[1]RVCKO pin is high if receive timer is not in internal mode-register bits TR0; D3, D2.

| ATTENUATION CONTROL REGISTER | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| CR2 | ATT3 | ATT2 | ATT1 | ATT0 |

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0, D1, D2, D3 | Transmit Attenuator | D3, D2, D1, D0<br><br>0000 to 1111 | Sets transmit attenuator which scales modulated data (and guard tone if enabled). Attenuation increments by 1 dB per LSB ATT = 0000 is unity gain, ATT = 1111 is 15 dB of Attenuation. |

| SET-UP CONTROL REGISTER | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| CR3 | TST | ALB | RvGE | ORIG |

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0 | Originate/Answer | 0 | Select answer mode. Answer mode set transmit path for high band modulation and filtering and connects the low band filter on the receive side. |
| | | 1 | Select originate mode. Originate mode sets the transmit path for low band modulation and filtering connects the high band filter on the receive side. |
| D1 | Receive filter gain (RvGE) | 0 | Receive path gain = 0 dB |
| | | 1 | Adds 12 dB of gain in the receive path prior to the band-split filter to enhance dynamic range. Care must be taken to ensure that the level at RXA does not exceed - 12 dBm when RvGE is enabled. The status bit RvL indicates the signal level at the receive band-split filter input. If RvL is low, the Receive filter gain can be safely enabled. |
| D2 | Analog Loopback (ALB) | 0 | Select normal mode. |
| | | 1 | Select analog loopback mode. A '1' causes the modulated data to pass through the transmit band-split filter (magnitude & delay section), through the attenuator, through transmit smoothing filter, into the receive anti-alias filter, bypassing the receive band-split filter (magnitude and delay), through the gain stage, into the ADC. The RXA input is floated, and the TXA is grounded. Detectors are active. |
| D3 | Test (TST) | 0 | Select normal mode. |
| | | 1 | Silicon Systems test mode. Not for customer use. |

| DETECT CONTROL REGISTER | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| DCR | ABT1 | ABT0 | MONEN | RST |

The Detect Control Register holds the control for the Special Detect circuits and some miscellaneous functions.

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0 | Reset (RST) | 0 | Normal mode. |
| | | 1 | Resets all Registers to the 0 state. |
| D1 | Monitor Enable (MONEN) | 0 | Monitor output disabled. |
| | | 1 | Enables echoing of the RXA signal on the MON pin. |
| D2, D3 | Answer Back Select (ABT0, ABT1) | D3, D2 | Selects which answer back tone or combination of tones will cause the Answer Tone status bit (ATD) to go high, as shown |
| | | 00/11 | Detect broadband from 2100 to 2225 Hz |
| | | 01 | Detect only 2225 Hz |
| | | 10 | Detect only 2100 Hz |

| STATUS REGISTER | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| SR | CAR | ATD | CPD | RvL |

The Status Register holds the special detect circuit outputs and are read-only. These status bits and a "fast" carrier detect bit are sent out on the serial interface.

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0 | Receive level indicator (RvL) | 0 | Signal peak amplitude is small enough to safely allow 12 dB pre-filter gain to be switched in. |
| | | 1 | Signal amplitude is too large to allow the 12dB gain. |
| D1 | Call progress detect (CPD) | 0 | No call progress detected. |
| | | 1 | Energy in call progress band present. |
| D2 | Answer tone detect (ATD) | 0 | No answer tone detected. |
| | | 1 | Valid answer back tone present. |
| D3 | Carrier Detect (CAR) | 0 | No energy in receive band detected. |
| | | 1 | Valid carrier present. |

| TRANSMIT TONE CONTROL REGISTER 0 | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| TR0 | RvT1 | RvT0 | ST | DTMF |

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0 | DTMF enable (DTMF) | 0 | Disables DTMF. |
| | | 1 | Activates DTMF. Selects dual tones. Output level is to be 0 dBm when attenuator setting is 0000. All detectors will be operating and should be ignored during DTMF. The tone pairs are determined by TR1 contents. |
| D1 | Single tone enable (ST) | 0 | Disables single tone transmit. |
| | | 1 | Selects single tones (FSK, Guard, or Answer). The tone frequency is determined by the bits in register TR1. |
| D2, D3 | Receiver Timer (RvT0, RvT1) | D3, D2 | The receive timer (RvT1, RvT0) selects one of four possible sampling rates: off, external timing, internal 7200 Hz, or internal 9600 Hz. The rising edge of an internal sampling clock initiates an analog-to-digital conversion and data transfer to the DSP. In the two internal modes, the sampling clock is generated by an on chip counter which can be controlled by bits 8 and 9 of the serial input word. |
| | | 00 | $\overline{SEN}$ is forced high. This state can be used for initializing the serial interface to the NEC 7720. ADC is stopped. |
| | | 01 | External timer EXADCC (synchronized internally) is the sampling clock. |
| | | 10 | Internal timer, 7200 Hz sampling rate |
| | | 11 | Internal timer, 9600 Hz sampling rate |

| TRANSMIT TONE CONTROL REGISTER 1 | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| TR1 | TRB3 | TRB2 | TRB1 | TRB0 |

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0 to D3 | DTMF Mode (TR0 - DTMF = 1) | 0000 to 1111 | Programs 1 of 16 DTMF tone pairs that will be transmitted when DTMF (TR0) bit is set. Tone Encoding is shown below. |

| Keyboard Equivalent | Register TR1 D3 | D2 | D1 | DO | Tones (Hz) Low | High |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 697 | 1209 |
| 2 | 0 | 0 | 1 | 0 | 697 | 1336 |
| 3 | 0 | 0 | 1 | 1 | 697 | 1477 |
| 4 | 0 | 1 | 0 | 0 | 770 | 1209 |
| 5 | 0 | 1 | 0 | 1 | 770 | 1209 |
| 6 | 0 | 1 | 1 | 0 | 770 | 1477 |
| 7 | 0 | 1 | 1 | 1 | 852 | 1336 |
| 8 | 1 | 0 | 0 | 0 | 852 | 1336 |
| 9 | 1 | 0 | 0 | 1 | 852 | 1477 |
| 0 | 1 | 0 | 1 | 0 | 941 | 1336 |
| * | 1 | 0 | 1 | 1 | 941 | 1209 |
| # | 1 | 1 | 0 | 0 | 941 | 1477 |
| A | 1 | 1 | 0 | 1 | 697 | 1633 |
| B | 1 | 1 | 1 | 0 | 770 | 1633 |
| C | 1 | 1 | 1 | 1 | 852 | 1633 |
| D | 0 | 0 | 0 | 0 | 941 | 1633 |

| D0 to D3 | Single Tone Mode (TR0 - ST = 1) | 0000 to 1111 | Programs 1 of 11 single tones that will be transmitted when ST (TR0) bit is set. Tone encoding is shown below. |
|---|---|---|---|

| Tone-Type | Register TR1 D3 | D2 | D1 | D0 | Tones (Hz) |
|---|---|---|---|---|---|
| FSK 103 | 0 | 0 | 0 | 0 | 2025 |
| FSK 103 | 0 | 0 | 0 | 1 | 2225 |
| FSK 103 | 0 | 0 | 1 | 0 | 1070 |
| FSK 103 | 0 | 0 | 1 | 1 | 1270 |
| FSK V.21 | 1 | 1 | 0 | 0 | 1850 |
| FSK V.21 | 1 | 1 | 0 | 1 | 1650 |
| FSK V.21 | 1 | 1 | 1 | 0 | 1180 |
| FSK V.21 | 1 | 1 | 1 | 1 | 980 |
| Guard | 0 | 1 | 0 | 0 | 1800 |
| Guard | 0 | 1 | 0 | 0 | 550 |
| Answer | 1 | 0 | 0 | 0 | 2225 |
| Answer | 1 | 0 | 0 | 1 | 2100 |

| QUADBIT REGISTER | | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| QBR | QB3 | QB2 | QB1 | QB0 |

The new quadbit for the QAM modulator is written to this register by the transmit microprocessor for every baud. Quadbits are latched into the modulator on the falling edge of TXINT. In 1200 bit/s mode, QB1 is internally forced to 0 and QB0 is forced to 1 so that only a dibit need be written in QB3, QB2. In 600 bit/s mode, QB1, QB0 are forced to 01, and QB3 is duplicated in QB2 so that only one bit need be written in QB3.

| BIT NO. | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| D0, D1 | Quadbits (QB0, QB1) | D1, D0 | The last two quadbits which determine the point within the quadrant in QAM. Forced to 01 in DPSK. Point in quadrant (I) |
| | | 0 0 | (1,1) |
| | | 0 1 | (3,1) [DPSK points] |
| | | 1 0 | (1,3) |
| | | 1 1 | (3,3) |
| D2, D3 | Quadbits (QB2, QB3) | D3, D2 | The first two quadbits as described in the V.22bis spec. (these bits determine the differential quadrant shift). Used as Dibit in DPSK Quadrant shift (I) |
| | | 0 0 | +90° |
| | | 0 1 | 0° |
| | | 1 0 | +180° |
| | | 1 1 | +270° |

**SERIAL INTERFACE DESCRIPTION**

| BIT NO. | 0 1 2 3 4 5 6 | 7 | 8 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|
| INPUT DATA | LSB ←GAIN WORD→ MSB | X | RCV TIMER CONTROL | X | X | X | X | X | X |

| BITS | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| 0-6 | GAIN WORD | 0000000-1111111 | Receive Gain from DSP for programmable Receive Gain stage. Step size is approximately 0.375 dB/bit with 48 dB of range. Transmitted LSB first. |

**SERIAL INTERFACE DESCRIPTION** (continued)

| BITS | NAME | CONDITION | DESCRIPTION |
|---|---|---|---|
| 7 | NONE | X | Not used |
| 8,9 | REC. TIMER CONTROL (internal modes only) | 8,9 | Used for timer control & correction of timing errors in the time base, $\overline{SEN}$, for start of ADC conversion. Sample rate is selected by TR0-RVT1, RVT0. Used only with internal modes. |
| | | 0,0 | 7200 Hz (or 9600 Hz) |
| | | 1,1 | 7200 Hz (or 9600 Hz) |
| | | 1,0 | 7200 Hz - 1 µs (or 9600 Hz - 1 µs) |
| | | 0,1 | 7200 Hz + 1 µs (or 9600 Hz + 1 µs) |
| 10 - 15 | NONE | XXXXXX | Not used |

| BIT NO. | 0 1 2 3 4 5 6 7 | 8 | 9 | 10 | 11 | 12 13 14 15 |
|---|---|---|---|---|---|---|
| OUTPUT DATA | LSB ← ADC 2's → MSB Complement output | RVL | CPD | AT | Slow CD | Fast CD |

| BITS | NAME | CONDITIONS | DESCRIPTIONS |
|---|---|---|---|
| 0-7 | ADC OUTPUT | 00000000-11111111 | 2's Complement coded output from 8-bit ADC ±3.75V F.S. |
| 8 | RVL (same as SR-RVL) | 0 | Receive level amplitude is small enough to allow 12 dB pre-filter gain to be used. |
| | | 1 | Receive level too large for 12 dB gain to be used. |
| 9 | CPD (same as Sr-CPD) | 0 | No call progress energy detected |
| | | 1 | Call progress energy detected |
| 10 | AT (same as SR-ATD) | 0 | No answer tone detected |
| | | 1 | Answer tone detected |
| 11 | SLOW CD (same as SR-CAR) | 0 | No carrier detected |
| | | 1 | Time qualified carrier detected |
| 12 - 15 | Fast CD | 0 | No carrier detected |
| | | 1 | Carrier detected |

**ABSOLUTE MAXIMUM RATINGS** - Operation above maximum ratings may damage the device

| PARAMETER | RATING | UNITS |
|---|---|---|
| Supply Voltage VDD | +7.5 | V |
| VSS | -7.5 | V |
| Storage Temperature | -65 to 150 | °C |
| Lead Temperature (10 sec.) | 260 | °C |
| Inputs | VSS -0.3 to VDD +0.3 | V |
| TTL Compatible Outputs | -0.3 to VDD +0.3 | V |
| TTL Compatible Outputs | ±3 | mA |
| Analog Outputs | VSS -0.3 to VDD +0.3 | V |
| Analog Outputs | ±3 | mA |

Notes: 1. All inputs and outputs are protected from static charge using built-in industry standard protection devices.

2. All outputs are short-circuit protected.

3. All voltages are referenced to GND.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|
| Positive Supply (VDD) | 4.75 | | 5.25 | V |
| Negative Supply (VSS) | -4.75 | | -5.25 | V |
| Ambient Temperature (TA) | 0 | | 70 | °C |
| External Components<br>VDD, VSS Bypass Capacitors (External to ground (VAG)) | 0.1 | | | µF |
| External Loads | | | | |
| Load Capacitance XIN, XOUT | 10 | | 50 | pF |
| Load Capacitance CLKOUT | | | 25 | pF |
| Digital Input Capacitance | | | 10 | pF |
| Digital Output Loading | | | 50 | pF |
| Analog Input Capacitance RXA | | | 26 | pF |
| Analog Input Resistance RXA | 100 | | | kΩ |
| Analog Loading, TXA Output (Vout = ±3Vpk) | | | 10k, 50 pF | |
| Analog Loading, MON Output (Vout = ±3Vpk) | | | 10k, 50 pF | |
| On-chip pull up/down Resistor<br>pull down: $\overline{CS}$, pull up: TXC KI, EXADCC | 20 | | | kΩ |
| Input Clock variation (7.3728 MHz Input XTAL) | -0.01 | | +0.01 | % |

## DC ELECTRICAL CHARACTERISTICS

(TA = 0 to 70°C, VDD = 5V, VSS = -5V Unless otherwise noted)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Current (IDD) | | | | 25 | mA |
| (ISS) | | | | 25 | mA |
| Input Low voltage (VIL) | | | | 0.8 | V |
| Input High Voltage (VIH) | | 2.0 | | | V |
| Input High Current (IIH) | Input voltage = VDD | | | 10 | µA |
| Input Low Current (IIL) | Input Voltage = 0V | | | -20 | µA |
| High Output Voltage (VOH) | Iout = -0.4 mA | 2.4 | | | V |
| Low Output Voltage (VOL) | Iout = 1.6 mA | | | 0.4 | V |



## DYNAMIC CHARACTERISTICS AND TIMING[1]

(TA = 0 to 70°C. VDD = 5V, VSS = -5V Unless otherwise noted)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Receive Signal Path | | | | | |
| Receive Gain | RvGE = 0<br>Gain word 0000000<br>Measured at input of ADC | | 0.0 | | dB |
| Receive Noise | RXA = 0<br>Boost 0dB<br>Gain word 0000000<br>0.3 to 3400 kHz bandwidth | | | 775 | µVrms |
| Receive Boost | RvGE = 0 | -0.2 | | 0.2 | dB |
| Receive Boost | RvGE = 1 | 11.8 | | 12.2 | dB |
| Programmable Gain Stage | | | | | |
| Gain Range | | 0.0 | | 48.0 | dB |
| Step Size | | 0.275 | 0.375 | 0.475 | dB |
| Gain Error | | | | 0.2 | dB |
| ADC | | | | | |
| Integral non-linearity | | | | 1/2 | LSB |
| Differential non-linearity | | | | 1/2 | LSB |
| Total input referred offset | | -4 | | +4 | LSB |
| Input voltage range | | -3.75 | | +3.75 | V |
| Input Anti-alias Low Pass Filter | | | | | |
| Receive Attenuation | | | | | |
| @ 4.0 kHz | | | -35 | | dB |
| @ 10.0 kHz | | | -60 | | dB |
| @ 12.0 kHz | | | -70 | | dB |
| @ 153.6 kHz | | | -55 | | dB |
| @ 921.6 kHz | | | -40 | | dB |

1) All dBm numbers refer to the signal power on the 2-wire telephone line as may be realized thru an external 2W/4W converter (hybrid). The hybrid gain from the line to the RXA pin should be 0 dB.

**DYNAMIC CHARACTERISTICS AND TIMING[1]** (continued)

| PARAMETERS | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Precise Answer Tone Detector | | | | | |
| Must Detect Level | | | | -43 | dBm |
| Must Reject Level | | -48 | | | dBm |
| Delay Time | | 40 | | 200 | ms |
| Hold Time | | 40 | | 100 | ms |
| Answer Tone Detect Frequency Range | | | | | |
| Must Accept | 2100 Hz to 2225 Hz | 2078 | | 2247 | Hz |
| Must Reject Low | Mode Selected | | | 2000 | Hz |
| Must Reject High | (ABT1, ABT0 = 00 or 11) | 2350 | | | Hz |
| Must Accept | 2100 Hz only | 2078 | | 2122 | Hz |
| Must Reject Low | Mode Selected | | | 2000 | Hz |
| Must Reject High | (ABT1, ABT0 = 01) | 2200 | | | Hz |
| Must Accept | 2225 Hz only | 2203 | | 2247 | Hz |
| Must Reject Low | Mode Selected | 2350 | | | Hz |
| Must Reject High | (ABT1, ABT0 = 01) | | | 2125 | Hz |
| Fast Carrier Detector | The following detect levels assume a waveform of the type shown is present in the receive band. | | | | |
| Must Detect | See Condition Table Below | | | -43 | dBm |
| Must Reject Level | | -48 | | | dBm |
| Delay Time | | 0 | | 20 | ms |
| Hold Time | | 0 | | 20 | ms |
| Slow Carrier Detector | The following detect levels assume a waveform of the type shown is present in the receive band. | | | | |
| Must Detect Level | See Condition Table Below | | | -43 | dBm |
| Must Reject Level | | -48 | | | dBm |
| Hysteresis | | 2 | | | dB |
| Delay Time | | 40 | | 205 | ms |
| Hold Time | | 40 | | 65 | ms |

**CONDITION TABLE**

| DR1 | DR0 | CARRIER TYPE | PEAK/RMS |
|---|---|---|---|
| 0 | 0 | None[2] | 1.414 |
| 0 | 1 | FSK | 1.414 |
| 1 | 0 | DPSK | 2.0 |
| 1 | 1 | QAM | 2.5 |

2) When the modulator is off, the carrier detector responds to sinusoids as might be found in answer back type tones.

| PARAMETERS | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Receive Signal Path | | | | | |
| Imprecise Call Progress Detector | | | | | |
| Must Detect Level | 460 Hz Input frequency | | | -35 | dBm |
| Must Reject Level | 460 Hz Input frequency | -45 | | | dBm |
| Hysteresis | 460 Hz Input frequency | 2 | | | dB |
| Delay Time | 460 Hz Input frequency | 40 | | 200 | ms |
| Hold Time | | 10 | | 40 | ms |
| Receive Level Indicator (SR-RVL) | | | | | |
| Must Detect Level | | | | 1.00 | Vpk |
| Must Reject Level | | 0.50 | | | Vpk |
| Hysteresis | | 2 | | | dB |
| Delay Time | | 40 | | 205 | ms |
| Hold Time | | 40 | | 65 | ms |
| Transmit Signal Path | | | | | |
| Transmit Output | Measured at TXA<br>Attenuator word 0000<br>Guard tones Off<br>V.52 511 bit data pattern | -0.8 | | 0.8 | dBV |
| QAM/DPSK Encoder/Modulator | | | | | |
| Carrier Suppression | Measured at TXA | 50 | | | dB |
| Modulation Frequency | 1200 or 2400 Hz | -0.1 | | +0.1 | % |
| Transfer Gain Variation | Measured at TXA<br>ATT = 0000 | -0.8 | | +0.8 | dB |
| Transmit Attenuator | | | | | |
| Attenuation Range | | 0 | | 15 | dB |
| Attenuation Error | Any setting | -0.2 | | 0.2 | dB |
| Modulator output attenuation | | | | | |
| Guard Tones Off | | -0.05 | | 0.05 | dB |
| 1800 Hz guard tone on | | 0.9 | | 1.1 | dB |
| 550 Hz guard tone on | | 1.65 | | 1.85 | dB |
| Tone Level | Specified for an attenuator setting of -9 dB (ATT = 1001) | | | | |
| Guard Tone 550 Hz | | -14.8 | | -12.8 | dBm |
| Guard Tone 1800 Hz | 0.4922 | -17 | | -15 | dBm |
| Answer Tone | 0.3182 | -10 | | -8 | dBm |
| FSK (103, V.21) | Nom (VPP) 0.777 | -10 | | -8 | dBm |
| DTMF (columns) | 0.777 | -7 | | -5 | dBm |
| DTMF (rows) | 1.098 | -9 | | -7 | dBm |
| DTMF (twist) | 0.872 | -3 | | -1 | dB |

**DYNAMIC CHARACTERISTICS AND TIMING[1]** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Harmonic Distortion | Distortion is specified below in dB relative to the fundamental frequency generated. | | | | |
| DTMF | (0 - 10 kHz bandwidth) | | | -29 | dB |
| FSK, V.21 | | | | -45 | dB |
| Guard Tone | | | | -31 | dB |
| Answer Tone | | | | -40 | dB |
| Output Smoothing Filter Transmitted energy | | | | | |
| 4.0 kHz | | | | -35 | dBm |
| 10.0 kHz | | | | -60 | dBm |
| 12.0 kHz | Guard tones disabled | | | -70 | dBm |
| 917.6 kHz | | | | -70 | dBm |
| 921.6 kHz | | | | -40 | dBm |
| Register Reset | Register Bit DCR - RST resets all register bits to the '0' state. Subsequent µP read/write's should wait until the internal 73K214 reset cycle end. | | | | |
| RST on | Time from reset bit written (rising edge $\overline{WR}$) until registers reset to '0' | | 4 | 10 | µs |
| RST off | Time from reset bit written (rising edge $\overline{WR}$) until next permissible µP register read/write | | 8 | 20 | µs |
| Clock Off Reset | The 73K214 will reset all control registers and status bits whenever the 7.3728 MHz clock is not present. This provides a "power on reset" capability which forces all control register bits to '0'. | | | | |
| Trst | Time from last clock transition to registers reset | 2 | | 100 | µs |
| Tact | Time from start of clock to activate state | 25 | | 40 | clocks |

**DYNAMIC CHARACTERISTICS AND TIMING[1]** (continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Microprocessor Bus Interface | | The timing necessary for the $\overline{CS}$ signal is the same as for address. | | | | |
| Intel 8051 µP | | | | | | |
| Address Before Latch | TAL | CL = 100 pF | 20 | | | ns |
| Address hold after Latch | TLA | | 10 | | | ns |
| Latch to $\overline{RD}/\overline{WR}$ control | TLC | | 30 | | | ns |
| $\overline{RD}/\overline{WR}$ to Latch | TCL | | 30 | | | ns |
| Data out from $\overline{RD}$ | TRD | | 120 | | | ns |
| ALE Width | TLL | | 40 | | | ns |
| Data float after Read | TRDF | | 0 | | 80 | ns |
| Read Width | TRW | | 150 | | 5000 | ns |
| Write Width | TWW | | 100 | | 5000 | ns |
| Data setup before write | TDW | | 100 | | | ns |
| Data hold after write | TWD | | 25 | | | ns |

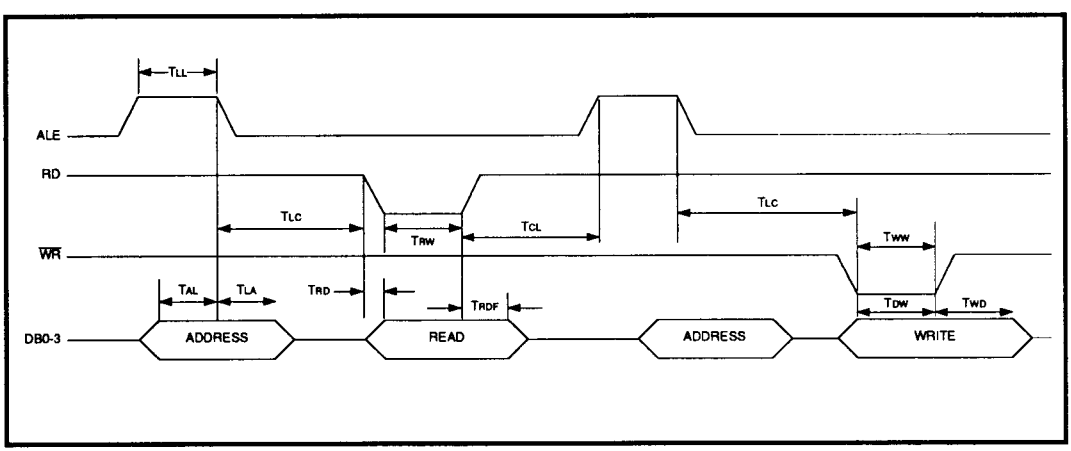



**Figure 1: Intel 8051 Bus Timing**

**DYNAMIC CHARACTERISTICS AND TIMING[1]** (continued)

| PARAMETERS | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Zilog 8601 | | Zilog interface requires externally inverting ALE and $\overline{RD}$, these pins then assume the functionality of Zilog pins $\overline{AS}$ and $\overline{DS}$ respectively. | | | | |
| Address before latch | TAL | CL = 100 pF | 20 | | | ns |
| Address hold after latch | TLA | | 10 | | | ns |
| Latch to $\overline{DS}$ control | TLC | | 30 | | | ns |
| Data out for $\overline{DS}$ | TRD | | 120 | | | ns |
| $\overline{AS}$ width | TLL | | 40 | | | ns |
| Data float after read | TRDF | | 0 | | 80 | ns |
| Read width | TRW | | 150 | | 5000 | ns |
| Write width | TWW | | 100 | | 5000 | ns |
| Data setup before write | TDW | | 100 | | | ns |
| Data hold after write | TWD | | 25 | | | ns |
| R/$\overline{W}$ hold after $\overline{DS}$ | TWH | | 20 | | | ns |

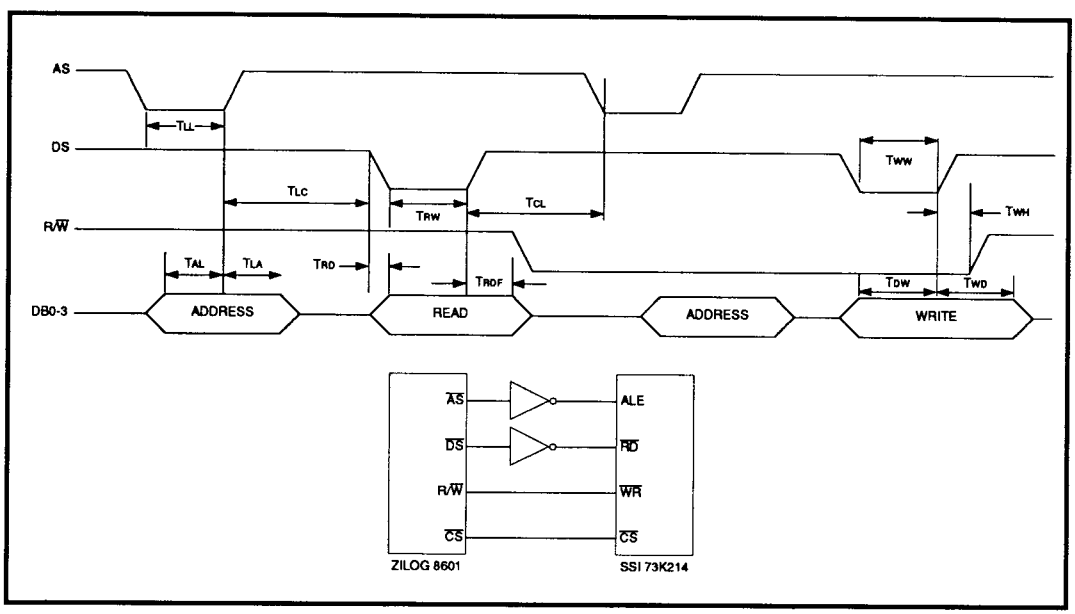



**Figure 2: Zilog 8601 Bus Timing**

**DYNAMIC CHARACTERISTICS AND TIMING[1]** (continued)

| PARAMETERS | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Serial DSP Interface** | | | | | | |
| SCKK falling to SOUT valid | TDCK | | | | 100 | ns |
| $\overline{SEN}$ edge to SCK edge | TSS | | 400 | | | ns |
| SIN setup before SCK | TADC | | 100 | | | ns |
| SIN hold after SCK | TACD | CL = 50 pF | 25 | | | ns |
| SIRQ setup before $\overline{SEN}$ | TSL | | 100 | | | ns |
| SIRQ hold after $\overline{SEN}$ | TLS | | 100 | | | ns |
| SCK width | TPW | | 800 | | | ns |
| SCK frequency | FSCK | | | 184 | | kHz |
| **Receiver Clocking** | | | | | | |
| RVCKO rising to $\overline{SEN}$ falling | TRS | | | 1.3 | | µs |
| EXADCC rising to $\overline{SEN}$ falling | TES | | .5 | 1.1 | 1.7 | µs |
| $\overline{SEN}$ low pulse width | TS | | | 86 | | µs |
| EXADCC frequency | FEXADCC | | | | 10.5 | kHz |
| **Transmit Timing** | | | | | | |
| TXCKO rising to $\overline{TXINT}$ falling | TOB | | 0 | | 500 | ns |
| TXCKI falling to TXCKO rising | TEO[1] | | -3 | +1 | +3 | µs |
| RVCKO falling to TXCKO rising | TRO[2] | | -3 | +1 | +3 | µs |

1) All dBm numbers refer to the signal power on the 2-wire telephone line as may be realized thru an external 2W/4W converter (hybrid). The hybrid gain from the line to the RXA pin should be 0dB.

2) When the modulator is off, the carrier detector responds to sinusoids as might be found in answer back type tones.

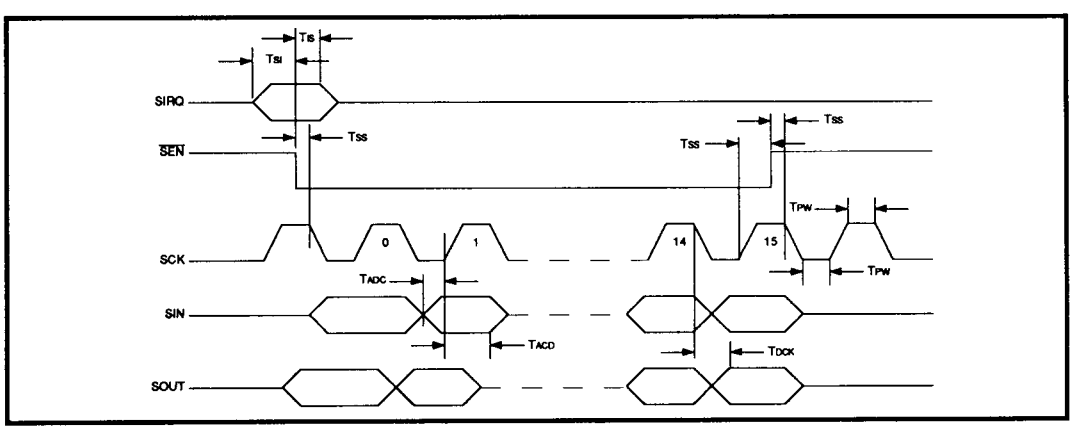



**Figure 3: Serial DSP Interface Timing**

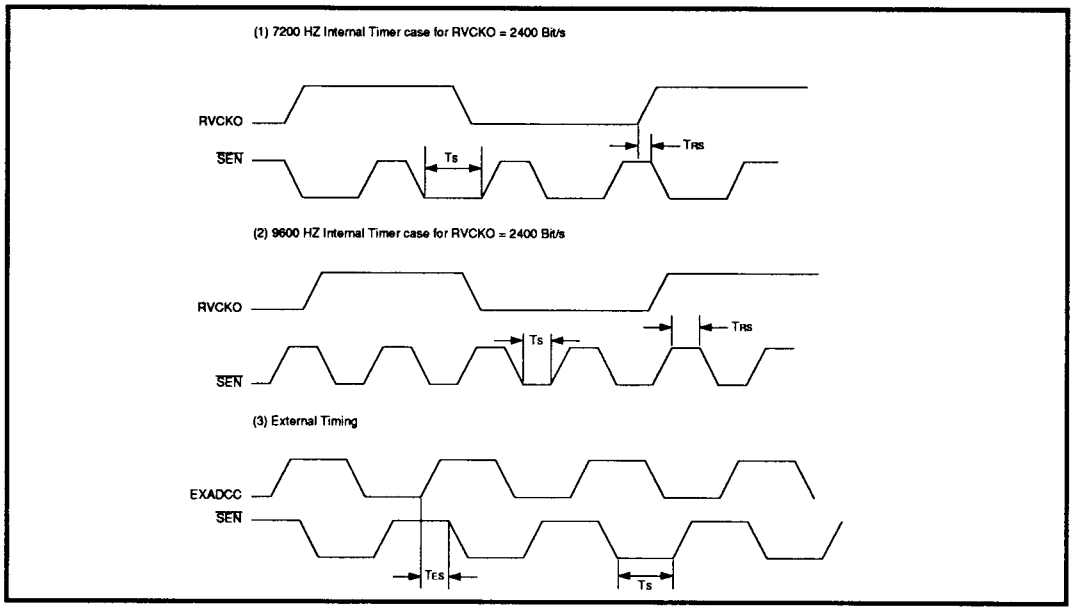



**Figure 4: Receive Clocking**

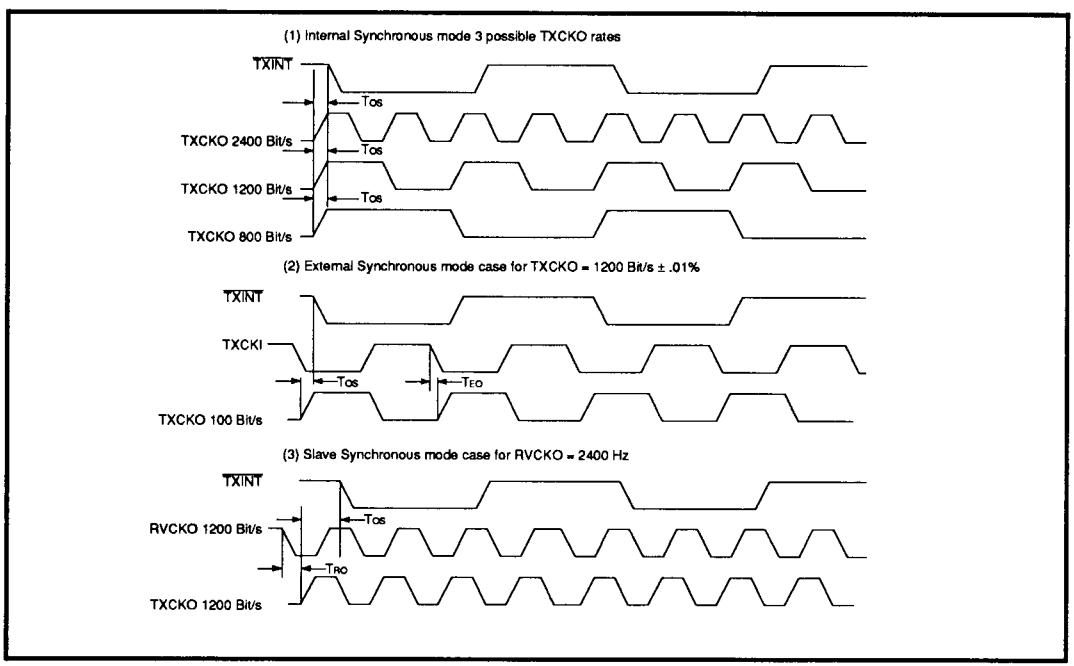



**Figure 5: Transmit Timing**

## APPENDIX A: V.21 Operation

The SSI 73M214 tone generator includes the V.21 tones (980/1180 Hz, 1650/1850 Hz). These tones can be accessed by setting ST-1 in TR0 and writing the appropriate bits in TR1 which select 1070/1270 Hz and 2025/2225 Hz. A difficulty arises because the high band V.21 tones will not pass through the high BPF required for V.22bis. Therefore, when V.21 FSK mode is selected (i.e., DR1, DR0 = 01, FBK = 1 in registers CR0, CR1), the BPFs center frequency and bandwidth are shifted to allow the V.21 signals to pass. Care must be taken in using this feature. Some settling time will be required when the filters shift to (from) FSK. Also, the answer tone detector will not function properly when the filters have been shifted. We recommend shifting the filters after answer tone has been detected.

## APPENDIX B: Using the RvT bits to synchronize the NEC 7720

To properly synchronize the serial interface to the 7720, the following procedure may be used after power up:

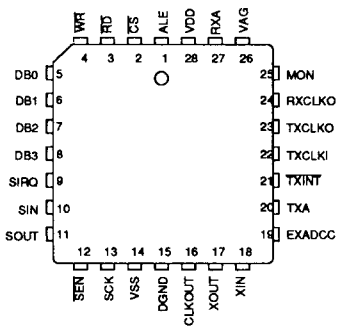
1. RESET the SSI 73M214 (write XXX 1 in Detect Register), this resets all control bits to 0, and therefore sets RvT1 = 0, RvT0 = 0.
2. WAIT 100 ms before changing RvT1, RvT0. This allows all serial clocks to cycle to an idle state. During this 100 ms, SEN will be high, and the 7720 should be reset during that time. (Other control registers may be written during this time.)

3

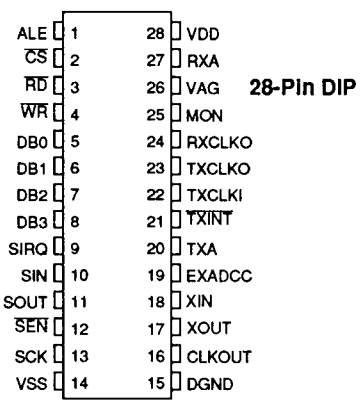
## PACKAGE PIN DESIGNATIONS

(TOP VIEW)

28-Pin PLCC




28-Pin DIP




## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 73M214 | | |
| Plastic Dual-In-Line | SSI 73M214-IP | 73M214-IP |
| Plastic Leaded Chip Carrier | SSI 73M214-IH | 73M214-IH |



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