WD90C61

Video Graphics Array Clock

Preliminary

DECEMBER 06, 1989

T-52-33-49

FEATURES

- Clock generation for IBM* compatible Western Digital Video Graphics Array (WD90C00)
- On-chip generation of six video clock frequencies (25.057, 28.189, 36.242, 16.108, 32.216 and 44.744 MHz) derived from 14.318MHz system clock reference frequency
- Pin selectable video clock among the six internally generated clocks and up to three externally supplied clocks.
- Dynamic frequency scaling control using Phase Lock Loops
- Selectable external clock inputs
- On-chip generation of four (36.242, 41.612, 37.586 and 44.744 MHz) memory clock frequencies
- Pin selectable memory clock among the four internally generated clocks
- CMOS technology
- Available in 20 pin PLCC package

DESCRIPTION

The Western Digital Video Graphics Array clock generator (WD90C61) is capable of producing different output frequencies dynamically under firmware control. The video output frequency is derived from14.318MHz system clock available in IBM† PC† /XT/AT† and Personal System/2† . It is designed to work with the Western Digital Video Graphics Array (WD90C00) for optimizing video subsystem performance.

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FUNCTIONAL DESCRIPTION:

The WD90C61 device generates the VCLK output according to the select inputs as shown in Table 1. The SEL0 and SEL1 inputs are latched with the SELEN strobe. VGATTL is an additional select input that selects frequencies suitable for VGA modes when left high and frequencies suitable for TTL modes when pulled low. Select input FCLKSEL overrides internal clock generation and passes through the FCLKIN clock input.

The MCLK output is generated according to the select inputs as shown in Table 2. The various VCLK and MCLK frequencies are achieved by multiplying the 14.318 MHz input frequency by a factor of N/32 (e.g., 44.74 is obtained with N = 100).

The VCLKE and MCLKE inputs can tristate the VCLK and MCLK outputs to facilitate board level testing. External filter components are attached to the MCAP and VCAP pins for the internal phase lock loops.

Table 1. VCLK Selection

VCLKE	FCLKSEL	VGATTL	SEL0	SEL1	VCLK Frequency
Open	1 or Open	1 or Open	0	0	25.057 MHz
Open	1 or Open	1 or Open	0	1	28.189 MHz
Open	1 or Open	1 or Open	1	0	EXTCLK pass-through
Open	1 or Open	1 or Open	1	1	36.242 MHz
Open	1 or Open	0	0	0	REFCLK pass-through
Open	1 or Open	0	0	1	16.108 MHz
Open	1 or Open	0	1	0	32.216 MHz
Open	1 or Open	0	1	1	44.744 MHz
Open	0	X	X	X	FCLKIN pass-through
0	X	X	X	X	DISABLED

Table 2. MCLK Selection

MCLKE	MCLKS0	MCLKS1	MCLK Frequency	Application
Open	1 or Open	1 or Open	44.744 MHz	WD90C00
Open	1 or Open	0	37.585 MHz	WD90C10
Open	0	1	36.242 MHz	PVGA1A
Open	0	0	41.612 MHz	PVGA1A
0	X	X	DISABLED	

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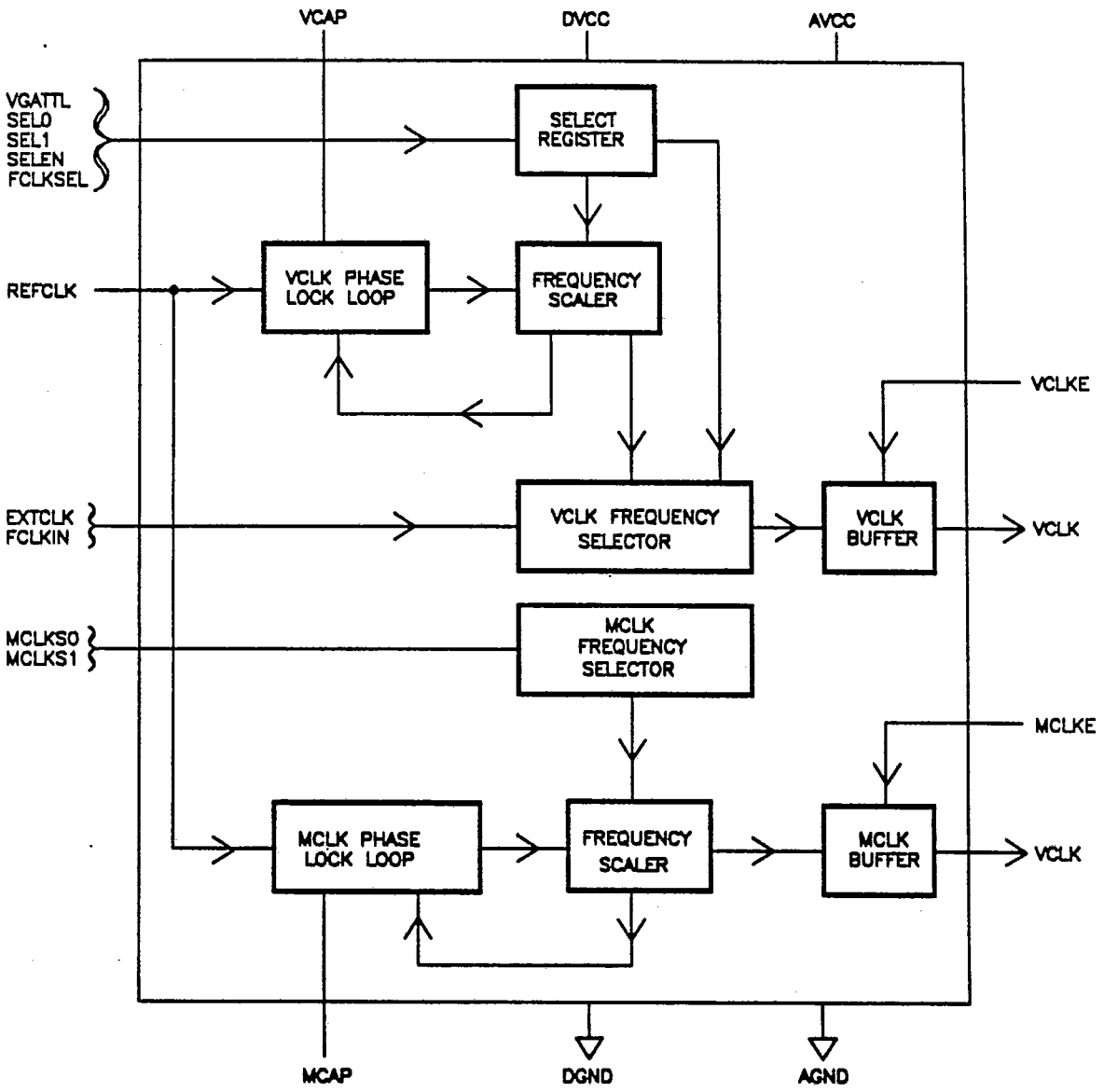

Figure 1. WD90C61 Functional Block Diagram

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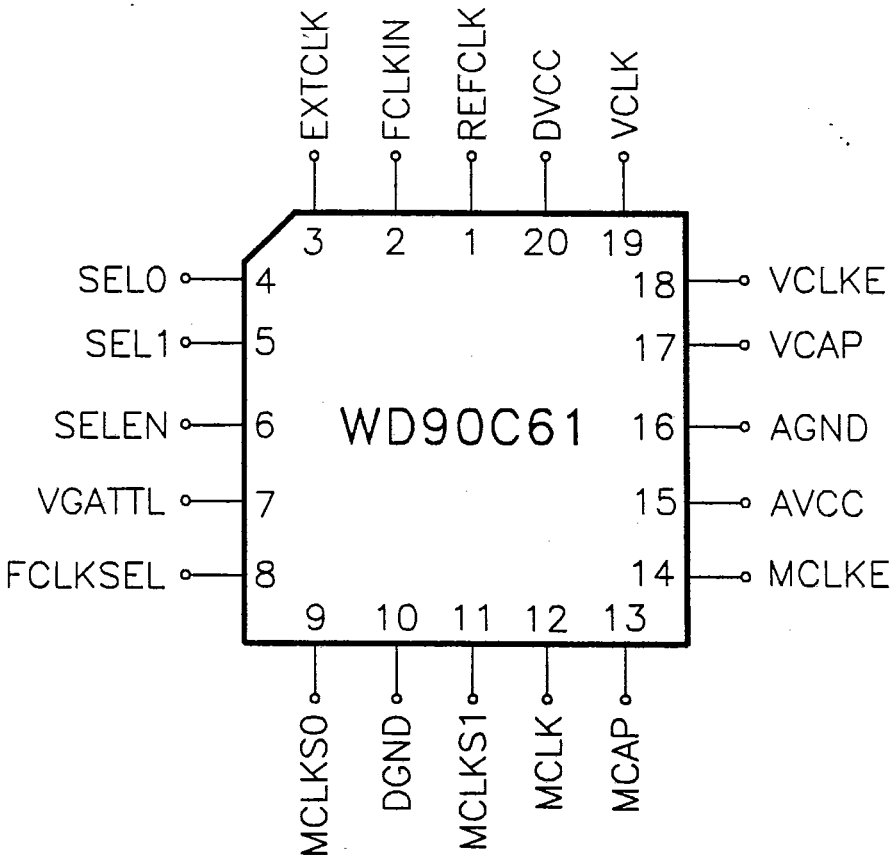

Figure 2. WD90C61 Pin Assignments

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Table 3. Pin List and Functions

PIN SYMBOL	PIN TYPE	PIN NO.	DESCRIPTION
REFCLK	IN	1	Reference Input Clock from system (14.318MHz)
FCLKIN	IN	2	Clock input from Feature Connector
EXTCLK	IN	3	External Clock input for an additional frequency
SEL0	IN	4	Control Input for VCLK selection
SEL1	IN	5	Control Input for VCLK selection
SELEN	IN	6	Strobe for latching SEL0 and SEL1
VGATTL	IN	7	Select input for VCLK selection - has an internal pullup resistor
FCLKSEL	IN	8	Select input for VCLK - has an internal pullup When pulled low, passes through FCLKIN
MCLKS0	IN	9	Select input for MCLK selection - has an internal pullup resistor
MCLKS1	IN	11	Select input for MCLK selection - has an internal pullup resistor
MCLK	OUT	12	Memory Clock (MCLK) output
MCAP	IN	13	External filter connection for MCLK generation
MCLKE	IN	14	Enable input for MCLK output - has an internal pullup resistor. When pulled low, tristates MCLK
VCAP	IN	17	External filter connection for VCLK generation
VCLKE	IN	18	Enable input for VCLK output - has an internal pullup resistor. When pulled low, tristates VCLK
VCLK	OUT	19	Video Clock (VCLK) output
DVCC	-----	20	Power supply for digital circuit
DGND	-----	10	Ground for digital circuit
AVCC	-----	15	Power supply for analog circuit
AGND	-----	16	Ground for analog circuit

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ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0^{o}C TO 70^{o}C
Storage temperature	-40^{o} C to 125^{o} C
Voltage on all inputs and outputs with respect to VSS	-0.5 to 7 Volts

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0^{o} to 70^{o} C
Power supply voltage	4.75 to 5.25 Volts

D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{CC} = 5V
V_{IH}	Input High Voltage	2.0	V_{CC}	V	V_{CC} = 5V
I_{IH}	Input Leakage Current	---	20	uA	$V_{IN} = V_{CC}$
V_{OL}	Output Low Voltage	---	0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Voltage	2.4	---	V	I_{OH} = 4.0mA
I_{CC}	Supply Current	---	25	mA	V_{CC} = 5V
R_{UP}	Internal Pullup Resistors (FCLKSEL, MCLKS0, MCLKS1, VGATTL, MCLKE, VCLKE)	25K	---	Ohm	V_{CC} = 5V
Cin	Input Pin Capacitance	---	8	pF	Fc = 1 MHz
Cout	Output Pin Capacitance	---	12	pF	Fc = 1 MHz

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AC CHARACTERISTICS

SELEN timing (Top waveform, Figure 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{pwen}	Enable Pulse Width	20	---	ns
t_{suen}	Setup Time Data to Enable	20	---	ns
t_{hden}	Hold Time Data to Enable	10	---	ns

Reference Input Clock (See Figure 3) **REFCLK = 14.318MHz**

SYMBOL	PARAMETER	MIN	MAX	UNITS
	Duty Cycle	42.5	57.5	%
t_r	Rise Time	---	10	ns
t_f	Fall Time	---	10	ns
	Phase Jitter	---	1	ns*

MCLK & VCLK Waveforms (See Figure 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS
	Duty cycle	40	60	%
t_r	Rise time	---	3	ns
t_f	Fall time	---	3	ns
	Phase Jitter	---	5	ns*

NOTE: Parameteric Test And Measurement Data is based upon the following details ;

* 1 Maximum jitter within a range of 30 us after triggering on a 400 MHz scope.
2 Output pin loading = 25pf.
3 Rise and fall time between 0.8 and 2.0 VDC.

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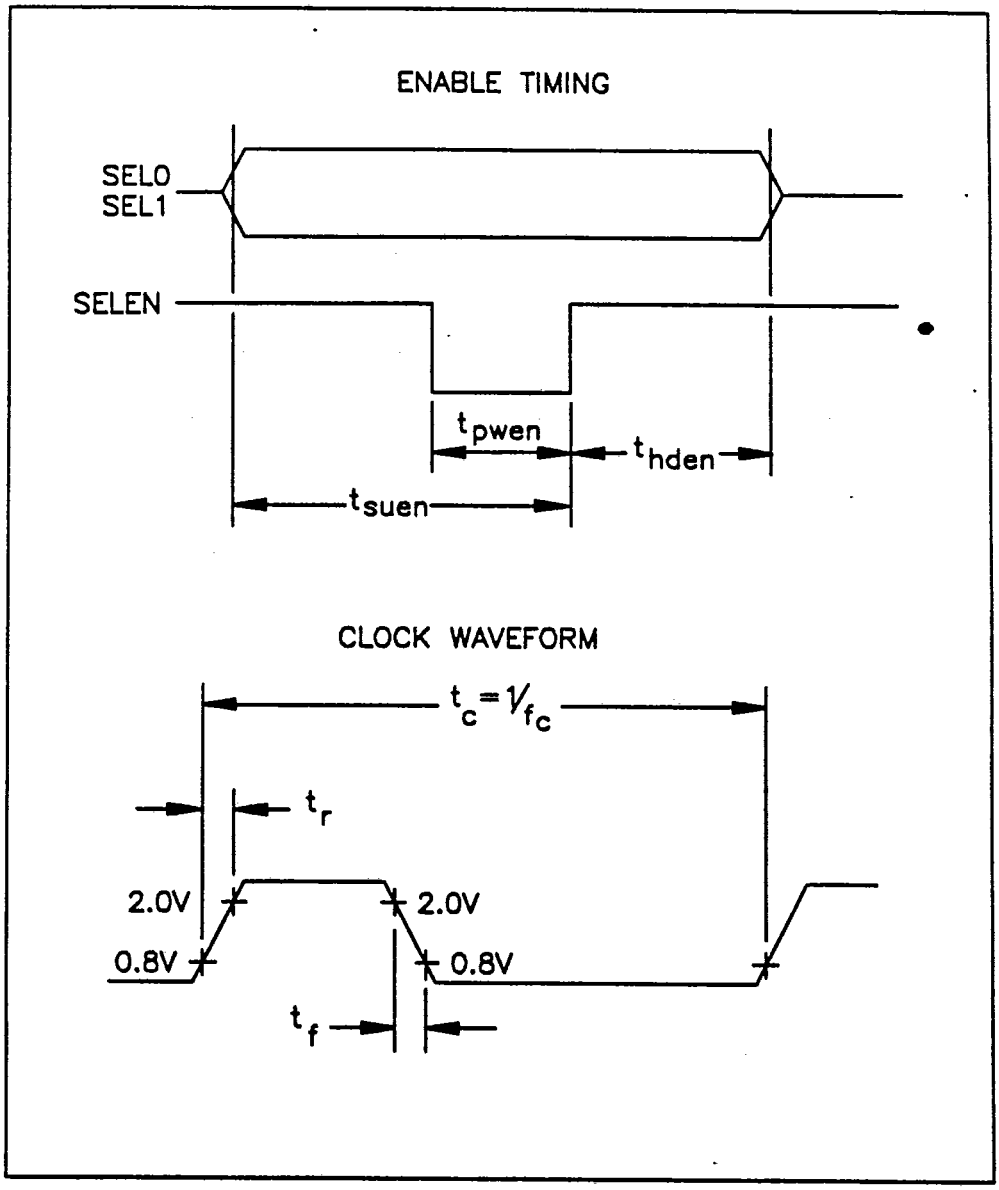

Figure 3. Waveforms

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SALES ORDER INFORMATION:

PACKAGE TYPE	WESTERN DIGITAL PART NUMBER
20-PIN PLCC	WD90C61JE00

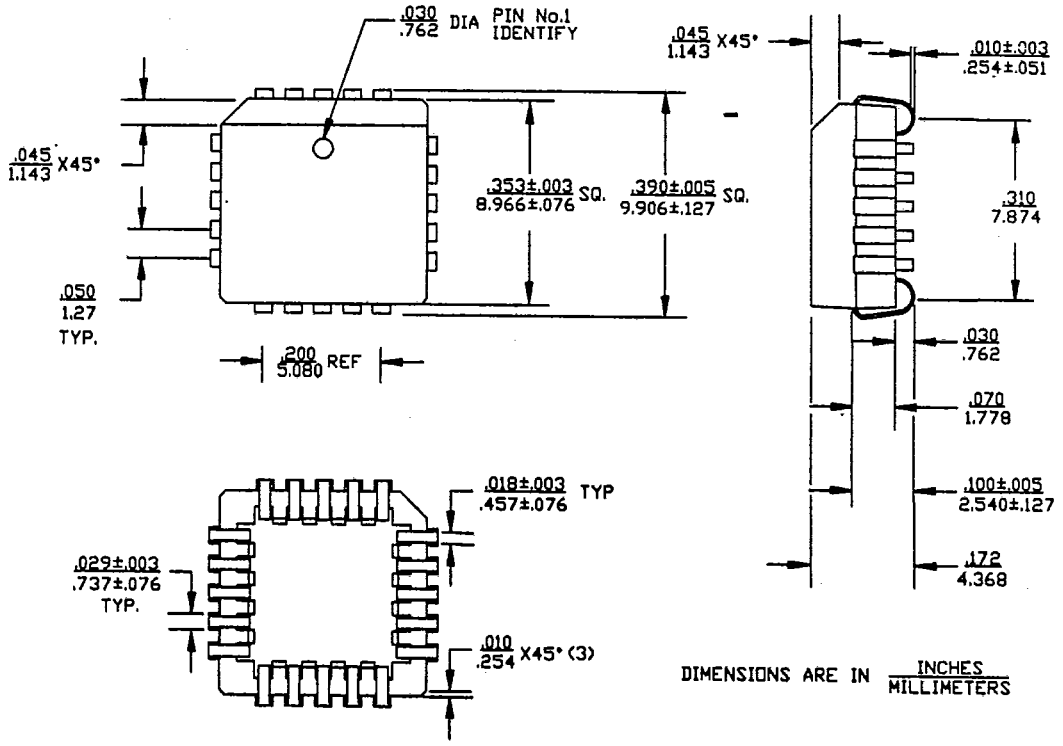

Figure 4. Packaging

APPLICATION DESCRIPTION

The typical application block diagram (refer to Figure 4) shows the Western Digital Video Graphics Array Clock (WD90C61) and the Western Digital Video Graphics Array (WD90C00), with external oscillators connected to a system bus.

The system bus provides a reference frequency to the WD90C61, which can dynamically select different video clock frequencies (VCLK) based upon the state of the mode control bits. The Western Digital Video Graphics Array (WD90C00) is normally designed with VCLK1 as an input pin. The configuration register bit 3 can be programmed to make it an output and provide the mode control latch enable (SELEN) pulse. This pulse can be used to select the desired VCLK frequency or external input frequency EXTCLK or REFCLK based on the state of the select pins. The FCLKIN and FCLKSEL pins can be connected to the clock and select pins from the Feature Connector.

MCLK frequencies can be selected by strapping the MCLKS0 and MCLKS1 inputs according to Table 2 of this data sheet.

The VGATTL input of the WD90C61 can be left open or strapped to ground to select the VCLK frequencies suitable for VGA or TTL modes.

The WD90C00's pin 73 (VCLK2) can be programmed to be configured as an output. This output can be controlled by software and so can be used as a frequency select input by the WD90C61. Please refer to the WD90C00 datasheet for more information.

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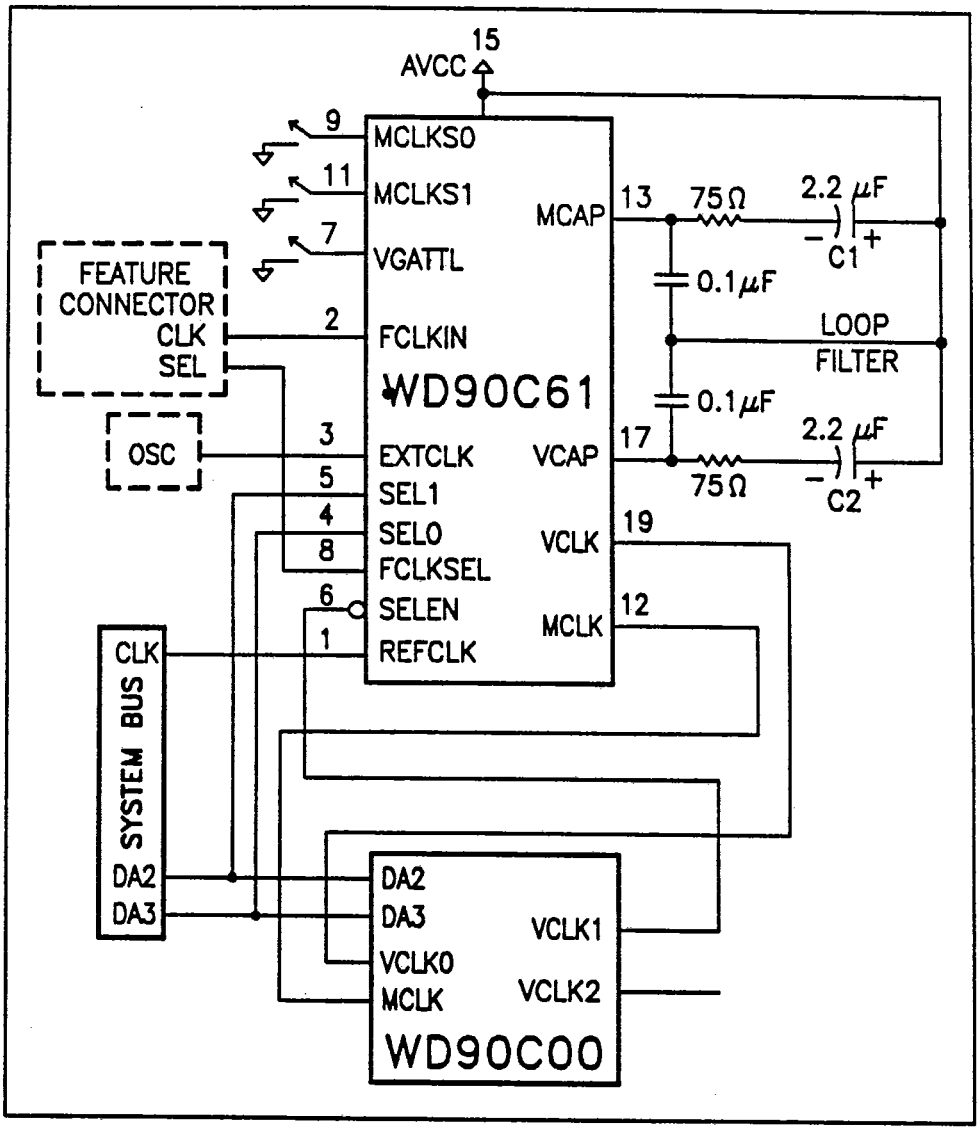

Figure 5. Typical Application

NOTES:

1. C1 and C2 are 2.2 uF, 25V, tant. capacitors.
2. 0.1 uF capacitors are ceramic capacitors.
3. 75-Ohm resistors are 1% metal film resistors.
4. WD90C00 is Western Digital Advanced Video Graphics Array