YAMAHA LSI

YM7109

MD96FX (9600bps FAX MODEM LSI)

■ OUTLINE

The YM7109 LSI is a one-chip modem for half-duplex synchronous data transfer at 9600 bps, 7200 bps, 4800 bps, 2400 bps, and 300 bps (CCITT V.29, V.27ter, V.21 ch2). With its built-in programmable dual tone originating function and programmable tone detection function, this LSI is designed for use with a public telephone line network and is ideal for modem applications for G3 facsimile machines.
In addition, the YM7109 is equipped with function for modulation into full duplex (CCITT V.21 and BELL 103) and a 75 bps (CCITT V.23 Backward channel) transmission function. It can thus also be used as the modem for telecommunications by personal computer or as a CAPTAIN adapter.
The YM7109 also has a built-in interface register which can connect to the data bus of a microprocessor, allowing reading and writing to and from that data bus. By accessing this interface register via a parallel interface, you can set the operating mode, set various parameters, read status flags, transfer the data to be transmitted or received, operate the modem and so on. The transfer of the transmit and receive data as well as modem operation can also be performed via a serial interface. The YM7109 is fabricated in 40-pin DIP, 64-pin QFP and 68-pin PLCC. Because of its low power consumption thanks to CMOS, the full capability of the LSI can be facilitated with 5V battery power supply, allowing much space to work with in terms of designing. This is a great plus for portability.

■ FEATURES

- CCITT V.29 (9600 bps/7200 bps) — Half duplex, synchronous
  V.27ter (4800 bps/2400 bps) — Half duplex, synchronous
  V.21 ch 2 (300 bps) — Half duplex, synchronous
  V.23 Backward — Channel (75 bps) Transmission only
  V.21 (300 bps) — Full duplex
- BELL 103 (300 bps) — Full duplex
- In CAPTAIN mode, full-duplex reception using V.27ter and full-duplex transmission using V.23 (75 bps) is possible.
- Compatible with the public phone line network (two-wire system)
- Dual tone originating function (programmable)
- Tone detection function (programmable)

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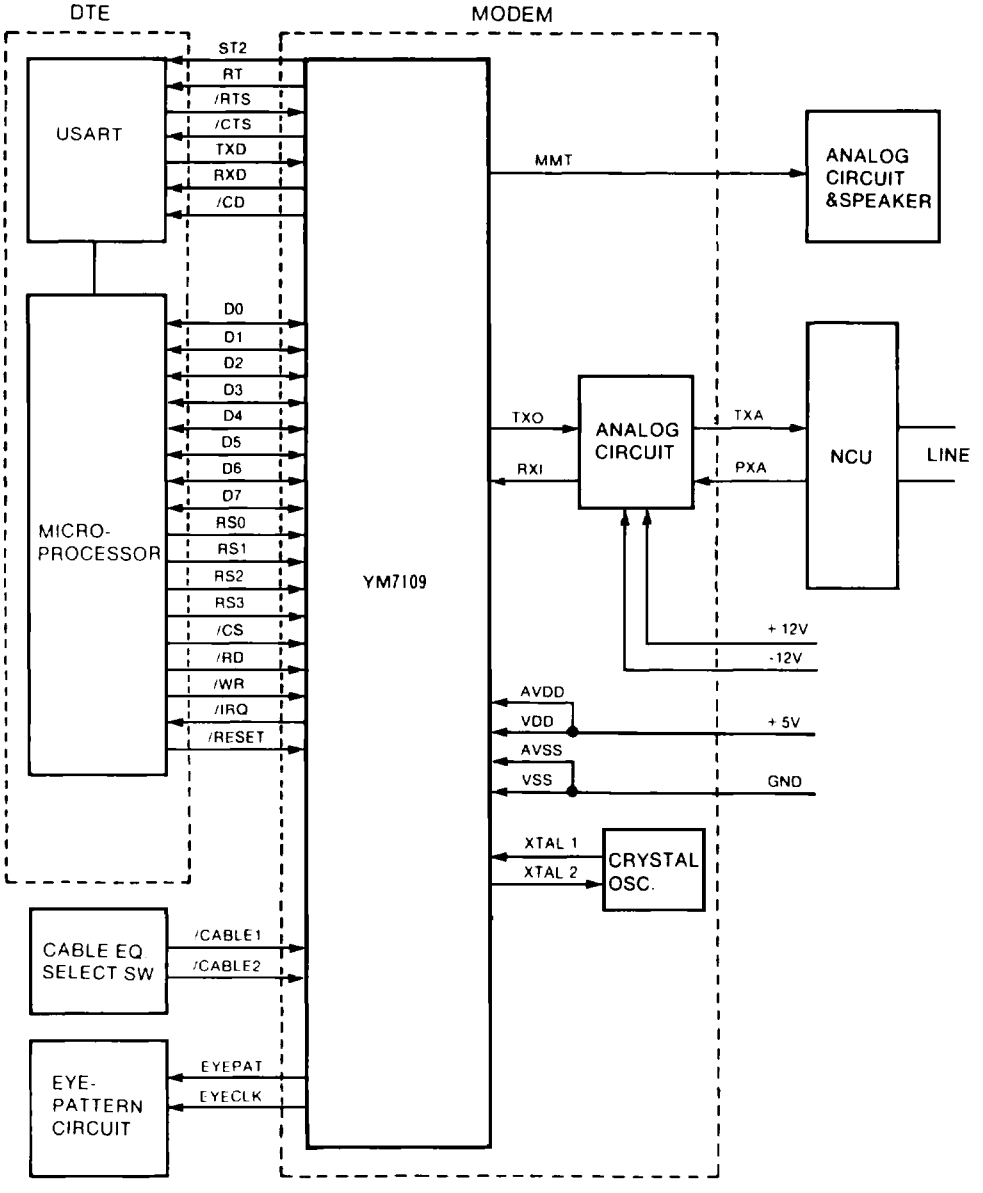
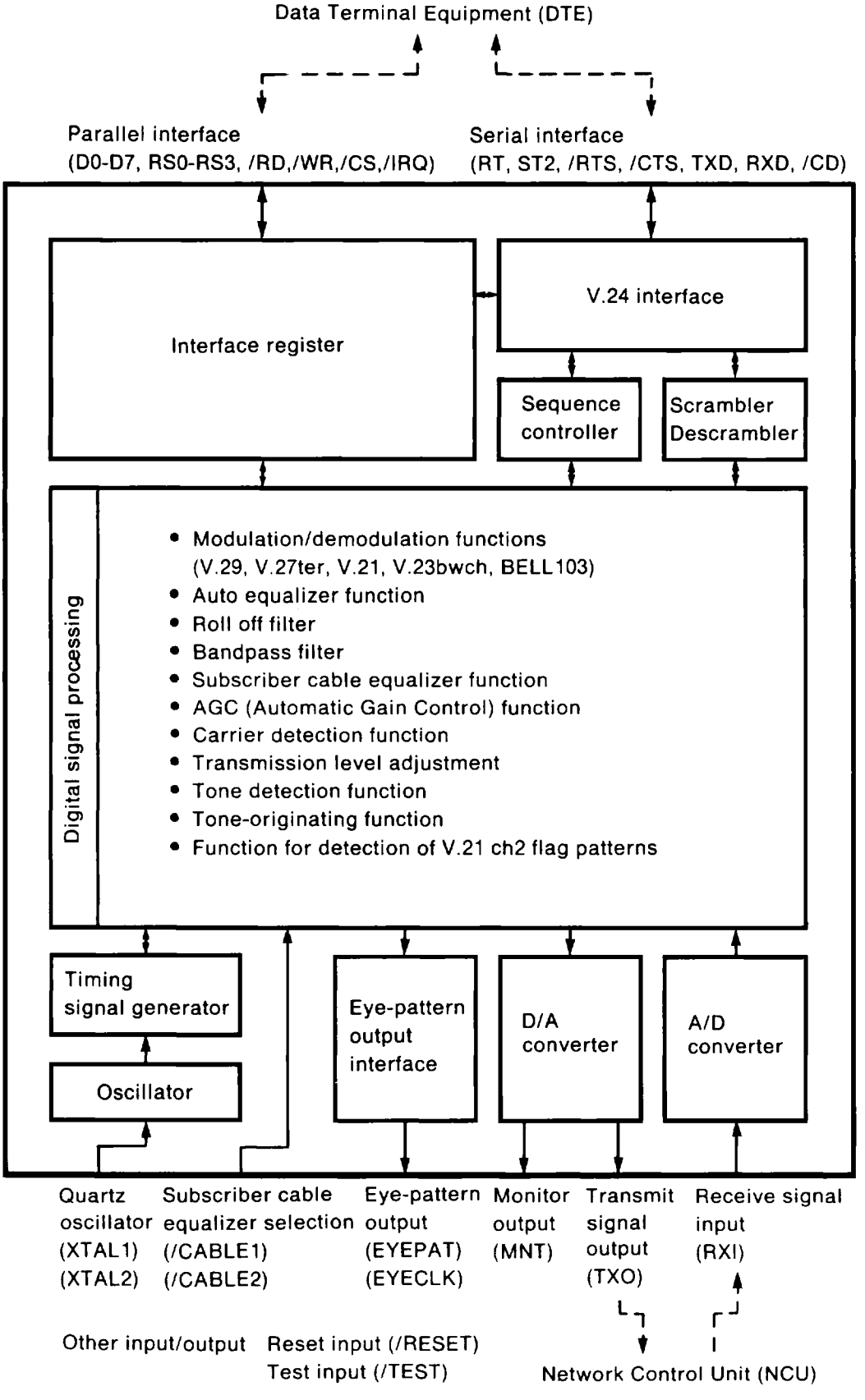
YM7109 CATALOG
CATALOG No.:LSI-2171092
1991. 10

- DTMF detection function (fixed)
- Function for detecting flag patterns of V.21 ch2
- Transmission level: 0 dBm to −15 dBm (programmable)
- Reception dynamic level: 0 dBm to −43 dBm (programmable)
- Auto equalizer function, and subscriber cable equalizer function
- Built-in bandpass filter for transmission and reception, A/D converter, D/A converter, and AGC (Automatic Gain Control)
- Parallel interface and serial (CCITT V.24) interface
- 40-pin DIP, 64-pin QFP and 68-pin PLCC package
- Low power consumption due to CMOS use
- 5V Type-A power supply

■SYSTEM BLOCK DIAGRAM



■ INTERNAL BLOCK DIAGRAM



■ OPERATING MODES AND COMMUNICATION PROTOCOLS

The YM7109 has the eight operating modes listed below:

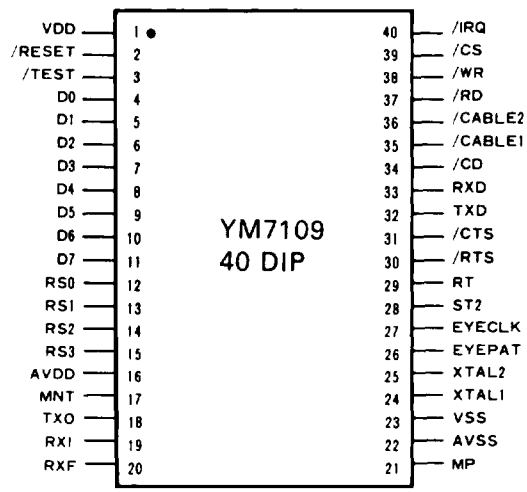
①9600 bps half-duplex reception/transmission: CCITT V.29
②7200 bps half-duplex reception/transmission: CCITT V.29
③4800 bps half-duplex reception/transmission: CCITT V.27ter
④2400 bps half-duplex reception/transmission: CCITT V.27ter
⑤300 bps half-duplex reception/transmission: CCITT V.21 ch2
⑥300 bps full-duplex reception/transmission: CCITT V.21 or BELL 103
⑦CAPTAIN full-duplex reception/transmission: CCITT V.27ter (4800 bps) and V.23 Backward CH (75 bps)
⑧TONE transmission and detection

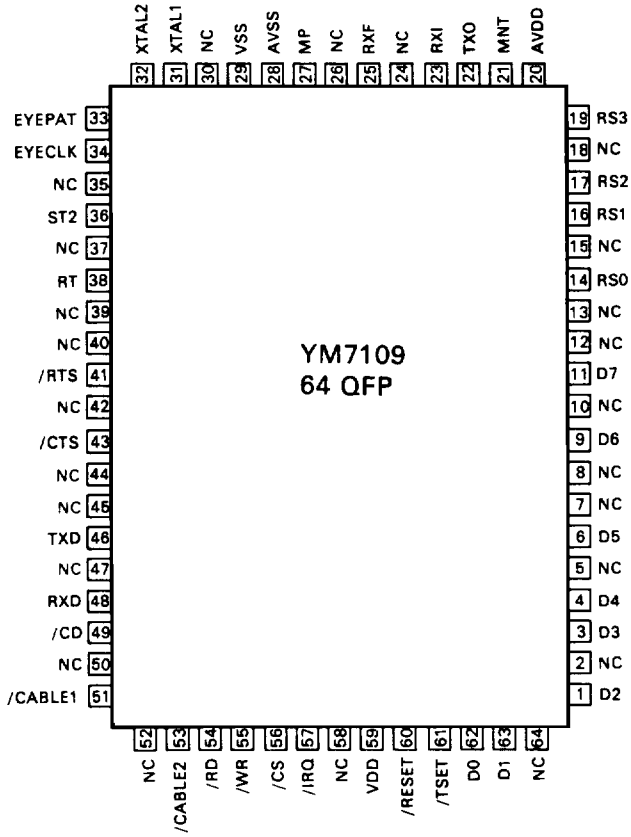
The protocols used in Modes ① through ⑦ conform either to the CCITT Recommendation or the BELL Standard. The specifications of these communication protocols are outlined below.

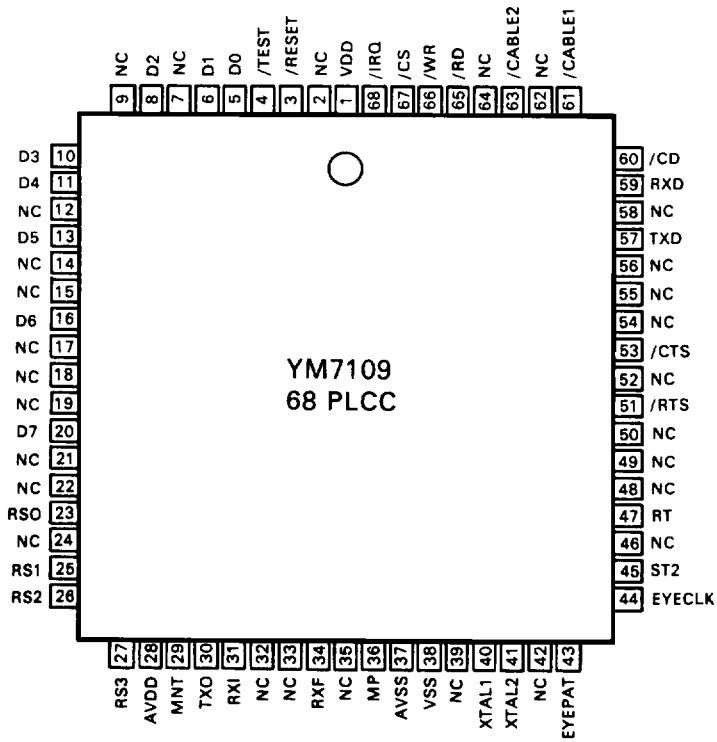
Protocol		Transfer Rate (bps)	Modulation Rate (Baud)	Carrier Frequency (Hz)	Modulation System	Communication Method
CCITT V.29		9600	2400	1700	16-QAM	Two-wire half-duplex synchronous
		7200	2400	1700	8-QAM	
CCITT V.27ter		4800	1600	1800	8-PSK	
		2400	1200	1800	4-PSK	
CCITT V.21	CH 1	300	300	Space 1180 Mark 980	FSK	Two-wire full duplex or Two-wire half duplex synchronous using CH 2
	CH 2	300	300	Space 1850 Mark 1650	FSK	
CCITT V.23 Backward CH		75	75	Space 450 Mark 390	FSK	Transmission only (Two-wire full duplex communication is possible in combination with V.27ter reception)
BELL 103	CH1	300	300	Space 1070 Mark 1270	FSK	Two-wire full duplex
	CH 2	300	300	Space 2025 Mark 2225	FSK	

■ TERMINAL DESCRIPTION

1. Pin Assignment




YM7109
64 QFP
1 D2
2 NC
3 D3
4 D4
5 NC
6 D5
7 NC
8 NC
9 D6
10 NC
11 D7
12 NC
13 NC
14 RS0
15 NC
16 RS1
17 RS2
18 NC
19 RS3
20 AVDD
21 MNT
22 TXO
23 RXI
24 NC
25 RXF
26 NC
27 MP
28 AVSS
29 VSS
30 NC
31 XTAL1
32 XTAL2
33 EYEPAT
34 EYECLK
35 NC
36 ST2
37 NC
38 RT
39 NC
40 NC
41 /RTS
42 NC
43 /CTS
44 NC
45 NC
46 TXD
47 NC
48 RXD
49 /CD
50 NC
51 /CABLE1
52 NC
53 /CABLE2
54 /RD
55 /WR
56 /CS
57 /IRQ
58 NC
59 VDD
60 /RESET
61 /TSET
62 D0
63 D1
64 NC


YM7109
68 PLCC
1 VDD
2 NC
3 /RESET
4 /TEST
5 D0
6 D1
7 NC
8 D2
9 NC
10 D3
11 D4
12 NC
13 D5
14 NC
15 NC
16 D6
17 NC
18 NC
19 NC
20 D7
21 NC
22 NC
23 RS0
24 NC
25 RS1
26 RS2
27 RS3
28 AVDD
29 MNT
30 TXO
31 RXI
32 NC
33 NC
34 RXF
35 NC
36 MP
37 AVSS
38 VSS
39 NC
40 XTAL1
41 XTAL2
42 NC
43 EYEPAT
44 EYECLK
45 ST2
46 NC
47 RT
48 NC
49 NC
50 NC
51 /RTS
52 NC
53 /CTS
54 NC
55 NC
56 NC
57 TXD
58 NC
59 RXD
60 /CD
61 /CABLE1
62 NC
63 /CABLE2
64 NC
65 /RD
66 /WR
67 /CS
68 /IRQ

PIN NAME	40 DIP	64 QFP	68PLCC
VDD	1	59	1
/RESET	2	60	3
/TEST	3	61	4
D0	4	62	5
D1	5	63	6
D2	6	1	8
D3	7	3	10
D4	8	4	11
D5	9	6	13
D6	10	9	16
D7	11	11	20
RS0	12	14	23
RS1	13	16	25
RS2	14	17	26
RS3	15	19	27
AVDD	16	20	28
MNT	17	21	29
TXO	18	22	30
RXI	19	23	31
RXF	20	25	34
MP	21	27	36
AVSS	22	28	37
VSS	23	29	38
XTAL1	24	31	40
XTAL2	25	32	41
EYEPAT	26	33	43
EYECLK	27	34	44
ST2	28	36	45
RT	29	38	47
/RTS	30	41	51
/CTS	31	43	53
TXD	32	46	57
RXD	33	48	59
/CD	34	49	60
/CABLE1	35	51	61
/CABLE2	36	53	63
/RD	37	54	65
/WR	38	55	66
/CS	39	56	67
/IRQ	40	57	68

NOTE:

NC Pin of 68 PLCC

2, 7, 9, 12, 14, 15, 17, 18, 19, 21, 22, 24, 32, 33, 35, 39, 42, 46, 48, 49, 50, 52, 54, 55, 56, 58, 62, 64

NC Pin of 64 QFP

2, 5, 7, 8, 10, 12, 13, 15, 18, 24, 26, 30, 35, 37, 39, 40, 42, 44, 45, 47, 50, 52, 58, 64

2. Terminal Functions

PIN NAME	TYPE	FUNCTION
VDD	PWR	Digital +5V power supply
VSS	GND	Digital ground level
XTAL1	XI	Quartz oscillator input or external clock input (9.8304 MHz)
XTAL2	XO	Quartz oscillator output
/RESET	DI	System Reset input (Reset when LOW)
/TEST	DIP	TEST mode input (normally HIGH or OPEN)
EYEPAT	DO	Eye-pattern serial output
EYECLK	DO	Eye-pattern clock output (4.9152 MHz)
ST2	DO	Transmitter element timing output
RT	DO	Transmitter/receiver element timing output
/RTS	DIP	Request-to-Send input (with built-in pull-up)
/CTS	DO	Clear-to-Send output
TXD	DIP	Transmit-Data input (with built-in pull-up)
RXD	DO	Receive-Data output
/CD	DO	Receive carrier detect output
D0 ~ D7	DIO	Data bus (8 bits)
RS0 ~ RS3	DI	Register selection input (4 bits)
/RD	DI	Read strobe input
/WR	DI	Write strobe input
/CS	DI	Chip select input
/IRQ	DOD	Interrupt-Request output (open drain output)
/CABLE1	DIP	Subscriber cable equalizer selection input
/CABLE2	DIP	(with built-in pull-up)
AVDD	PWR	Analog +5V power supply
AVSS	GND	Analog ground level
TXO	AO	Transmit signal analog output
RXI	AI	Receive signal analog input
RXF	AO	Capacitor terminal for AD conversion
MP	AO	Reference voltage terminal for AD conversion
MNT	AO	Analog output for the monitor

NOTE: The "/" prefix indicates an active-LOW signal.

DI: Digital input
DIP: Built-in pull up digital input
DO: Digital output
DO: Open drain output
DIO: Digital I/O
AI: Analog input
AO: Analog output

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (VSS shall be 0V)

ITEM	SYMBOL	RATING		UNIT
		Min.	Max.	
Supply voltage	VDD	−0.5	7.0	V
Input voltage	VI	−0.5	VDD + 0.5	V
Output voltage	VO	−0.5	VDD + 0.5	V
Storage temperature	TSTG	−50	+125	°C

2. Recommended Operating Conditions (VSS shall be 0V)

ITEM	SYMBOL	RATING			UNIT
		Min.	Typ.	Max.	
Supply voltage	VDD	4.75	5.0	5.25	V
Ambient operating temperature	Ta	0	25	70	°C
Clock frequency	fCLK	9.82942	9.83040	9.83138	MHz

3. D.C. Characteristics (The recommended operating conditions unless otherwise indicated)

ITEM	SYMBOL	TARGET PIN TYPE & MEASUREMENT CONDITIONS	RATING			UNIT
			Min.	Typ.	Max.	
High-level input voltage	VDIH	DI, DIP, DIO	2.0	—	—	V
Low-level input voltage	VDIL		—	—	0.8	V
Input leak current	ILDIH	DI	−10	—	+10	μA
High-level output voltage	VDOH	DO, DIO	VDD-1.0	—	—	V
Low-level output voltage	VDOL	@2.0mA	—	—	0.4	V
High-level clock input voltage	VCLKH	XI In case of external input without quartz oscillation	VDD-1.0	—	—	V
Low-level clock input voltage	VCLKL		—	—	1.0	V
Clock input leak current	ILCLK		−100	—	+100	μA
Analog input voltage range	VAI	AI	0.0	—	VDD	V
Analog input leak current	ILAI		−10	—	+10	μA
Open drain output current	IDOD	DOD @0.4V	4.0	—	—	mA
Output capacitance	CIO		—	—	12.0	pF
Output leak current	ILOUT	DIO, DOD When HIGH-zero	−10	—	+10	μA
Pull-up current	IPU	DIP	50	—	200	μA
Analog output voltage range	VAO	AO	0.0	—	VDD	V
Power current	IDD	PWR, GND	—	40	60	mA

4. A.C. Characteristics (The recommended operating conditions unless otherwise indicated)

ITEM	SYMBOL	CONDITIONS	RATING			UNIT
			Min.	Typ.	Max.	
Reset input pulse width	$T_{W(RESET)}$		1.0	—	—	msec
/CS setup time	$T_{S(CS)}$	For /RD, /WR	30	—	—	nsec
/CS hold time	$T_{H(CS)}$	Same as above	10	—	—	nsec
/RS setup time	$T_{S(RS)}$	Same as above	30	—	—	nsec
/RS hold time	$T_{H(RS)}$	Same as above	10	—	—	nsec
Write data setup time	$T_{S(WD)}$		75	—	—	nsec
Write data hold time	$T_{H(WD)}$		10	—	—	nsec
Write pulse width	$T_{W(WR)}$		75	—	—	nsec
Read data access time	$T_{A(RD)}$	$C_L = 100PF$	—	—	140	nsec
Read data hold time	$T_{H(RD)}$		10	—	50	nsec
Read cycle time	$T_{CYC(RD)}$		1	—	—	μsec
Write cycle time	$T_{CYC(WR)}$		1	—	—	μsec

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