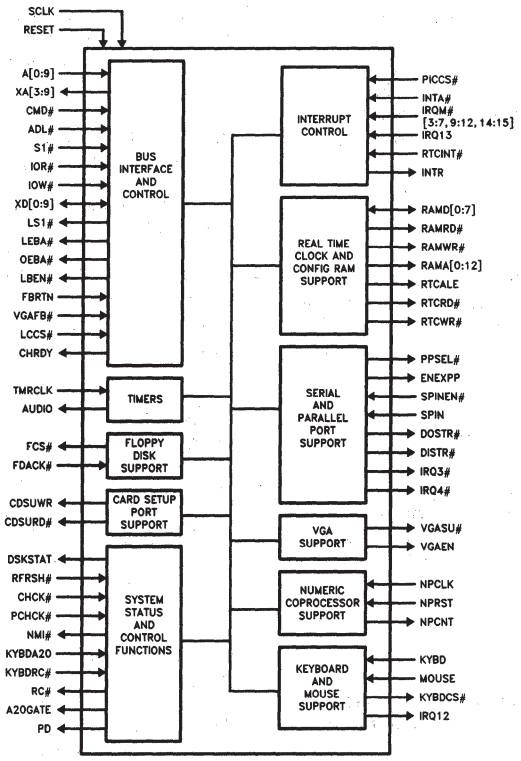
82304
LOCAL I/O SUPPORT CHIP

- **High-Integration—The 82304, 82303 and 82077 Floppy Disk Controller Replace 50 IC's in IBM Design**
- **Supports I/O Peripherals . . . Keyboard/ Mouse Controller, Serial/Parallel Ports, Configuration RAM, and Real Time Clock**
- **Integrates Two 8259 PIC's and All Associated Logic**
- **Integrates Programmable Timer Counters 0, 2 and 3**
- **Supports VGA Controller on the Local Channel**
- **Integrates the OS/2 Optimized HOT A20 and HOT RESET Functions**
- **Integrates Variety of System Status/ Control Ports and Functions**
- **Low Power CHMOS Technology/132-Pin PQFP Package**

The 82304 Local Channel Support Chip, along with its companion chip (the 82303) and the 82077 Floppy Disk Controller, significantly reduce system cost, design effort, and form factor constraints by replacing 50 IC devices in an equivalent IBM system.

The 82304 integrates logic to support local bus I/O peripherals and the VGA Controller. Also integrated are three programmable timer/counters, two "8259-like" programmable interrupt controllers, and a variety of system status/control ports and functions. Integrated along with the 8259 PIC's is all logic required to make the PIC's Microchannel architecture compatible.



290185-1

November 1988
Order Number: 290185-001

INTRODUCTION

The 82304 is a high integration device intended for Microchannel compatible system designs. It essentially integrates the 82306 Local Channel Support chip, two 8259 Programmable Interrupt Controllers, and a wide assortment of TTL circuitry. The 82304, in conjunction with its sister chip the 82303 and the 82077 Floppy Disk Controller, replaces approximately 50 IC devices in an equivalent IBM system. Included as an appendix to this data sheet is a functional logic diagram of the 82304 that should facilitate understanding of the part. Note that the 82304, 82303 and 82077 integrate a variety of system ports. For programming and register level details, please refer to the IBM Technical Reference Manual, 82077 data sheet, and 8259A data sheet.

BUS INTERFACE AND CONTROL

The Bus Interface and Control unit interfaces the 82304 to the Microchannel and peripheral busses. It inputs the unlatched Microchannel address, latches it for internal use, and makes the latched version available externally for other peripheral bus resources. It also provides signals to control an external 74F543 latching data transceiver that sits between the Microchannel and peripheral data busses. The bus interface unit also provides functions such as cycle extension on behalf of slower peripherals, and support of the Microchannel architecture's system feedback function.

SYSTEM TIMERS

The 82304 integrates the timers required for multitask time slice interrupt (timer 0), audio tone generation (timer 2), and "watch-dog" function (timer 3). These timers are accessed via ports 40, 42, 43, 44, and 47H.

FLOPPY DISK SUPPORT

The 82304 provides the decode signal required by the 82077 Floppy Disk Controller. The decode addresses ports 3F0–3F7H. The 82304 also inputs the 82077's DMA acknowledge in support of the system feedback function.

VGA SUPPORT

The 82304 supports the VGA setup and enable/disable functions. Specifically, bit 5 of integrated port 94H is used to put the VGA into setup mode, and this mode is reflected to the VGA on the 82304's VGASU# pin. Also, the 82304 integrates bit 0 of port 3C3H, which is used to enable/disable the system board VGA subsystem as indicated by the 82304's VGAEN output.

CARD SETUP PORT SUPPORT

The 82304 provides decoded read/write strobes for ports 96–97H. Port 96H is the card setup port, which is integrated on the 82303 chip. Port 97H is currently reserved by IBM.

INTERRUPT CONTROL

The 82304 integrates two 8259 Programmable Interrupt Controllers, and all additional logic required to make these interrupt controllers Microchannel architecture compatible. Specifically, the Microchannel definition requires that interrupts be active low and level sensitive. This allows a wire-OR system implementation. Integrated logic includes inverters for incoming interrupts, as the 8259 treats level sensitive interrupts as active high. Additionally, logic to inhibit the 8259's from being programmed in edge-triggered mode is integrated.

REAL TIME CLOCK AND CONFIGURATION RAM SUPPORT

The 82304 integrates all logic required to support an external battery backed up real time clock chip and static RAM. Note that while the IBM implementation supports a 2K RAM, the 82304 makes provision to support either a 2K or 8K RAM. The real time clock is accessed via ports 70–71H, while the RAM is accessed via ports 74–76H. (RAM data is accessed via port 76H, while ports 74H and 75H serve as an indirect address latch for the RAM.) The 82304 also integrates the logic required to enforce the Microchannel architecture's password security function. Specifically, writes to port 70H are monitored. If a write to 70H is attempting to access offsets 38–3FH in the real time clock chip's onboard RAM, and if the security bit in 92H indicates that these offsets are off limits, then no address latch signal is generated to the real time clock chip.

SERIAL AND PARALLEL PORT SUPPORT

The 82304 provides various functions in support of an external serial port chip (the 16550A), and a par-

allel port (integrated on the 82303 chip). The 82304 provides decoded read/writes strobes for the serial port chip, as well as converting a serial port interrupt into either IRQ3# or IRQ4#, depending on whether the serial port is configured as COMM1 or COMM2. When configured as COMM1, the serial port is decoded at ports 3F8–3FFH. As COMM2, the port is decoded from 2F8–2FFH. Configuration is done via the integrated system setup port 102H.

The 82304 generates a parallel port chip select that maps to LPT1, LPT2, or LPT3, depending on how system setup port 102H is programmed. As LPT1, the parallel port is decoded at ports 3BC, 3BD, 3BE, and 3BFH. LPT2 maps to ports 378, 379, 37A, and 37BH. LPT3 maps to 278, 279, 27A, and 27BH. The 82304 also generates a signal that indicates whether the parallel port is to operate in its normal output-only mode, or its "extended" bi-directional mode. The mode is selected via system setup port 102H.

NUMERIC COPROCESSOR SUPPORT

The 82307 DMA Controller, in response to a software command, issues a pulse to reset the 80387 or 80387SX Numeric Coprocessor. The 82304 inputs this pulse and effectively stretches it out to insure that the 80387 reset input pulse is long enough to meet its internal reset requirements. (Note that the 80387 reset pulse out of the 82304 must be externally synchronized to the 80387 clock so as to convey the system phase to the 80387.) The 82304 also manipulates CHRDY to extend the bus cycle that initiates the reset so as to tie up the CPU until the 80387's reset and initialization requirements are met.

KEYBOARD AND MOUSE SUPPORT

The 82304 provides a chip select for the 8742 Keyboard Controller. This decode maps to ports 60 and 64H. The 82304 also integrates the logic required to both latch and subsequently clear keyboard and mouse interrupts.

SYSTEM STATUS AND CONTROL FUNCTIONS

The 82304 integrates a variety of system status and control functions and ports. Integrated ports include:

- Port 61H System Control Port B
- Port 92H System Control Port A
- Port 91H Card Selected Feedback Register
- Port 94H System Board Setup Port
- Port 102H System Board POS Port
- Port 70H NMI Enable (Write Only)

The functions and register level details of these ports are documented in the IBM Technical Reference.

82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS

Symbol	Pin No.	Type	Description
SCLK	50	I	**INPUT CLOCK:** Tied to same clock as host CPU.
RESET	64	I	**SYNCHRONIZED POWER-UP RESET:** Resets 82304 and synchronizes internal clock to system phase.
A[0:9]	85–81, 78–74	I	**MICROCHANNEL ADDRESS:** Address Lines are internally latched.
XA[3:9]	73–67	O	**PERIPHERAL BUS ADDRESS:** These are latched versions of the Microchannel address.
CMD#	97	I	**MICROCHANNEL CMD# INPUT**
ADL#	100	I	**MICROCHANNEL ADL# INPUT**
S1#	1	I	**MICROCHANNEL S1# INPUT**
IOR#, IOW#	96, 95	I	**82304 READ AND WRITE STROBES**
XD[0:7]	94–90, 88–86	I/O	**BI-DIRECTIONAL DATA BUS**
LS1#	131	O	**LATCHED VERSION OF MICROCHANNEL S1# INPUT**
LEBA#, OEBA#	130, 129	O	**EXTERNAL 74543 DATA BUFFER CONTROL SIGNALS:** These signals control data timing on the peripheral data bus.
LBEN#	52	O	**LOCAL (PERIPHERAL) BUS ENABLE:** The 82304 generates this in response to address decodes of peripheral bus ports. It is typically "OR"ed with other system qualifiers to enable the peripheral bus data buffer.

82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS (Continued)

Signal Name	Pin No.	I/O	Description
FBRTN	41	I	**SYSTEM FEEDBACK:** This input receives the OR of the system feedback signals of the Microchannel slots. It is internally latched and "OR"ed with other feedback sources, and the result made available via a Port 91H read (Bit 0).
VGAFB#	42	I	**VGA FEEDBACK.**
LCCS#	37	I	**LOCAL CHANNEL CHIP SELECT:** Activated for the I/O address range 0–3FFH (CPU or DMA master) or 100–3FFH (Microchannel Master). LCCS# is internally latched.
CHRDY	5	O	**CHANNEL READY:** The 82304 deasserts CHRDY to extend accesses to certain peripheral bus resources, specifically the keyboard controller, real time clock and serial port. Also, CHRDY is used to tie up the CPU during numeric coprocessor resets.
TMRCLK	45	I	**1.193 MHz CLOCK INPUT:** Drives clock inputs of system timers 0 and 2.
AUDIO	128	O	**OUTPUT OF SYSTEM TIMER 2 GATED BY BIT 1 OF PORT 61H:** It drives the Microchannel audio sum node.
FCS#	46	O	**FLOPPY DISK CONTROLLER (82077) CHIP SELECT:** Responds to I/O range 3F0–3F7H.
FDACK#	49	I	**FLOPPY DISK CONTROL DMA ACKNOWLEDGE:** Internally latched and "OR"ed with other system feedback sources.
VGASU#	44	O	**VGA SETUP:** Puts the VGA into setup mode when active, according to Bit 5 of Port 94H.
VGAEN	43	O	**VGA ENABLE:** Enables/Disables motherboard VGA according to Bit 0 of Port 3C3H.
CDSUWR	126	O	**CARD SETUP WRITE STROBE:** Active High command generated during writes to Port 96–97H.
CDSURD#	125	O	**CARD SETUP READ STROBE:** Active low command generated during reads from Port 96–97H.
DSKSTAT	127	O	**FIXED DISK STATUS:** Controls the fixed disk activity light. It is active when either Bit 6 or Bit 7 of Port 92H is set.
RFRSH#	51	I	**REFRESH CYCLE INDICATOR:** Diagnostics can monitor refresh activity via Bit 4 of Port 61H.
CHCK#	54	I	**MICROCHANNEL CHECK INDICATOR:** Used to report adapter errors.
PCHCK#	55	I	**DRAM PARITY ERROR:** Driven in response to motherboard memory parity errors.
NMI#	53	O	**NON-MASKABLE INTERRUPT REQUEST TO CPU:** This acts as an open drain output that allows for an external wire "OR" with other NMI sources.
KYBDA20	60	I	**A20 GATE SIGNAL OUT OF THE KEYBOARD CONTROLLER:** Internally "OR"ed with the alternate A20 switch incorporated in Bit 1 of Port 92H.
KYBDRC#	58	I	**CPU RESET SIGNAL OUT OF THE KEYBOARD CONTROLLER:** It is internally "OR"ed with the alternate reset function of Bit 0 of Port 92H.
RC#	59	O	**RESET CPU:** Resets CPU via Port 92H (Bit 0) or the KYBDRC# input.
A20GATE	57	O	**A20 GATE SIGNAL:** The "OR" of Bit 1 of Port 92H and the KYBDA20 input.

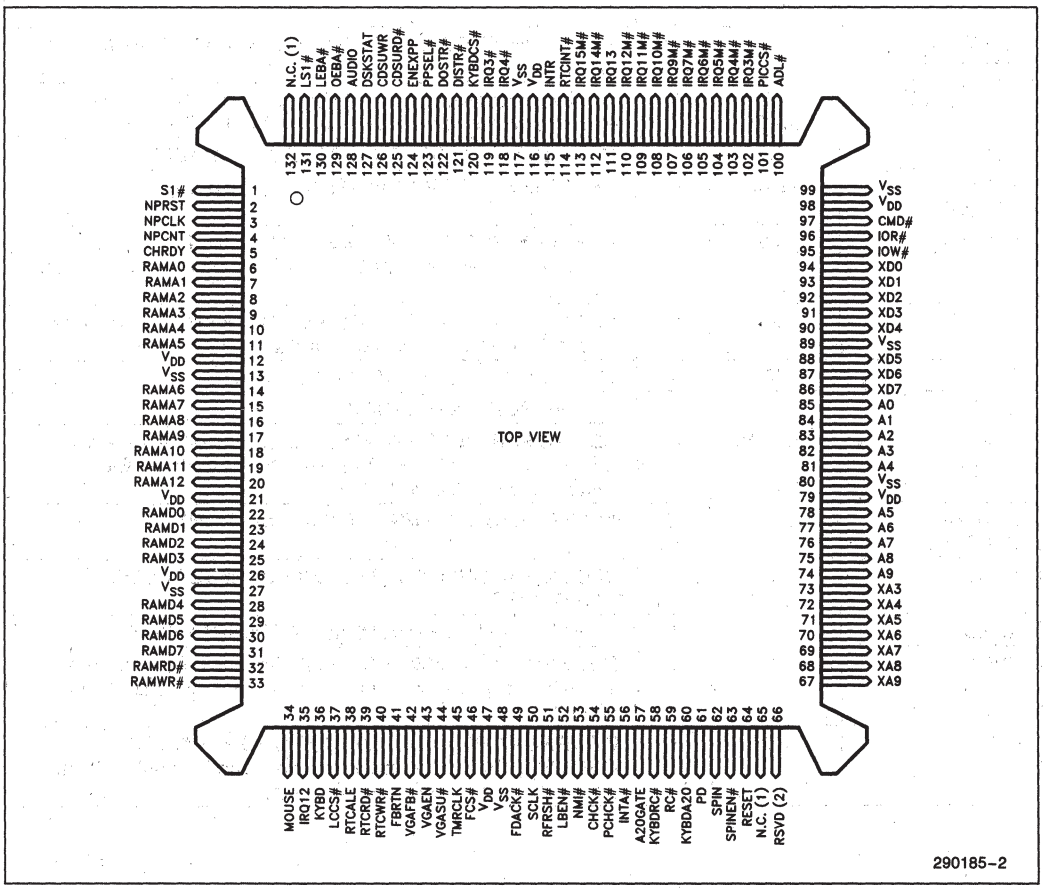
82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS (Continued)

Signal Name	Pin No.	I/O	Description
PD	61	O	**POS DECODE:** An active high decode of system board setup ports 100, 101, 103–107H. (Port 102H is integrated on the 82304.)
PICCS#	101	I	**CHIP SELECT FOR THE INTEGRATED 8259 PROGRAMMABLE INTERRUPT CONTROLLERS (PIC)**
INTA#	56	I	**INTERRUPT ACKNOWLEDGE:** Generated by the bus controller during interrupt acknowledge cycles.
IRQM# [3:7, 9:12, 14:15]	102–110, 112–113	I	**MICROCHANNEL INTERRUPT INPUTS.**
IRQ13	111	I	**INTERRUPT INPUT USED TO REPORT NUMERIC COPROCESSOR ERRORS.**
RTCINT#	114	I	**INTERRUPT INPUT FROM REAL TIME CLOCK.**
INTR	115	O	**MASKABLE INTERRUPT REQUEST TO CPU.**
RAMD[0:7]	22–25, 28–31	I/O	**REAL TIME CLOCK AND CONFIGURATION RAM DATA BUS.**
RAMRD#, RAMWR#	32, 33	O	**READ/WRITE STROBES TO CONFIGURATION RAM:** Generated during accesses to Port 76H.
RAMA[0:12]	6–11, 14–20	O	**CONFIGURATION RAM ADDRESS BUS:** Internal RAM address latches are written to via Ports 74–75H.
RTCALE	38	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.**
RTCRD#, RTCWR#	39, 40	O	**REAL TIME CLOCK READ/WRITE STROBES.**
PPSEL#	123	O	**PARALLEL PORT CHIP SELECT:** Maps to LPT1, LPT2, or LPT3 as controlled by Bits 5 and 6 of system board setup Port 102H.
ENEXPP	124	O	**PARALLEL PORT EXTENDED MODE ENABLE:** This mode is controlled via bit 7 of system board setup Port 102H.
SPINEN#	63	I	**SERIAL PORT INTERRUPT ENABLE.**
SPIN	62	I	**SERIAL PORT INTERRUPT.**
IRQ3#, IRQ4#	119, 118	O	**SERIAL PORT INTERRUPT:** Configured to either COMM1 (IRQ4#) or COMM2 (IRQ3#). Selection is done via Bit 3 of system board setup Port 102H.
DOSTR#, DISTR#	122, 121	O	**WRITE/READ STROBES FOR SERIAL PORT.**
NPCLK	3	I	**CLOCK FOR NUMERIC PROCESSOR RESET PULSE STRETCHER.**
NPRST	2	I	**NUMERIC PROCESSOR RESET REQUEST INPUT**
NPCNT	4	O	**NUMERIC PROCESSOR COUNT:** Numeric processor reset signal typically synchronized externally and fed to 80387 or 80387SX.
KYBD	36	I	**INTERRUPT REQUEST INPUT FROM KEYBOARD CONTROLLER:** It is internally latched, and then subsequently cleared by a keyboard controller read.

82304 LOCAL CHANNEL SUPPORT CHIP PIN DEFINITIONS (Continued)

Signal Name	Pin No.	I/O	Description
MOUSE	34	I	**INTERRUPT REQUEST INPUT FROM KEYBOARD CONTROLLER'S MOUSE PORT:** It is internally latched and subsequently cleared by a keyboard controller read.
KYBDCS#	120	O	**KEYBOARD CONTROLLER CHIP SELECT.**
IRQ12	35	O	**LATCHED VERSION OF MOUSE INPUT INTERRUPT REQUEST.**
V_{DD}	12, 21, 26, 47, 79, 98, 116		**POWER.**
V_{SS}	13, 27, 48, 80, 89, 99, 117		**GROUND.**
NC	65, 132		**NO CONNECT.**
RSVD	66		**RESERVED.**

82304 132-Pin PQFP Pinout



290185-2

NOTES:
1. N.C. pins must be left not connected.
2. This pin is reserved . . . must be tied to ground in system.

82304 Parametrics

Absolute Maximum Ratings*

Case Temperature Under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to any Pin with
Respect to Ground .... −0.3V to +(V_{CC} +0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Electrical Characteristics T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	SCLK
V_{IH}	Input High Voltage	V_{CC}−0.8		V	SCLK
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA (Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA (Note 1)
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA (Note 2)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA (Note 2)
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	TRI-STATE Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

NOTES:
1. DSKSTAT, XA[3:9], XD[0:7].
2. All outputs other than those listed in Note 1.

82304 A.C. Electrical Specifications T_C = 0°C to +70°C, V_{CC} = 5V ±10%

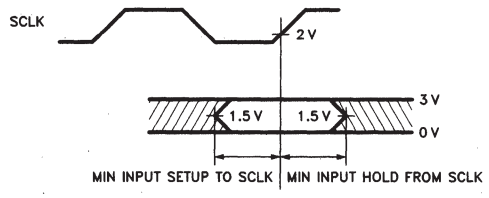
Symbol	Parameter	KIT-16		KIT-20		KIT-25		C_L (pF)	Notes
		Min	Max	Min	Max	Min	Max		
T_1	SCLK Period	31.25		25		20			
T_{2A}	SCLK High/Low Time	12		10		8			
T_{2B}	SCLK High/Low Time	8		6.5		6			
T_3	Reset Setup	10		10		10			
T_4	Reset Hold	3		3		3			
T_5	Reset Pulse Width	500		500		500			
T_6	RC# Pulse Width	75	150	75	150	75	150	50	
T_7	TMRCLK High/Low Time	300		300		300			
T_8	PICCS#, FDACK# Setup	30		30		30			
T_9	PICCS#, FDACK# Hold	0		0		0			
T_{10}	IOR#, IOW#, INTA# Pulse Width	170		170		170			

82304 A.C. Electrical Specifications T_C = 0°C to +70°C, V_{CC} = 5V ±10% (Continued)

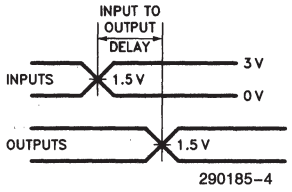
Symbol	Parameter	KIT-16		KIT-20		KIT-25		C_L (pF)	Notes
		Min	Max	Min	Max	Min	Max		
T_{11}	Write Data Setup	25		25		25			
T_{12}	Write Data Hold	10		10		10			
T_{13}	Read Data Valid Delay	0	90	0	90	0	90	100	
T_{14}	Read Data Float Delay	0		0		0		100	
T_{15}	RAMD[0:7] to XD[0:7] Delay		36		36		36	100	
T_{17}	CHRDY Delay	0	80	0	80	0	80	25	
T_{18}	CHRDY Inactive Pulse Width	280		280		230		25	5
T_{19}	Address Decode Delays from ADL# ↓	0	62	0	62	0	62	50	1
T_{20A}	Write Strobe Delays from IOW# ↓	0	40	0	40	0	40	50	2
T_{20B}	CDSUWR, DOSTR# Delays from IOW# ↑	0	35	0	35	0	35	50	
T_{20C}	RTCWR#, RAMWR# Delay from CMD# ↑	0	33	0	33	0	33	50	
T_{21}	Read Strobe Delays	0	40	0	40	0	40	50	6
T_{22}	RTCALE Min Pulse Width	120		120		110		50	3
T_{23}	XA[3:9] Delay from ADL# ↓		35		35		35	100	5
T_{24}	S1#, LCCS#, A[0:9] Setup to ADL# ↑	30		30		30			
T_{25}	FBRTN Setup to CMD# ↓	15		15		15			
T_{26}	VGAFB# Setup to CMD# ↑	15		15		15			
T_{27}	LEBA# Delay from CMD#		26		26		26	25	
T_{28}	OEBA# Delay from CMD# ↓		30		30		30	25	
T_{30}	CHRDY ↓ Delay		38		38		38	25	4
T_{31}	NPCNT ↑ Delay	128 NPCLKS		128 NPCLKS		128 NPCLKS		50	5
T_{32}	CHRDY ↑ Delay	192 NPCLKS		192 NPCLKS		192 NPCLKS		25	5
T_{33}	NPCLK High/Low Time	12		12		12			
T_{34}	LS1# Delay from ADL# ↓		35		35		35	50	

NOTES:
1. Address decodes include FCS#, PPSEL#, KYBDCS#, PD and LBEN#.
2. Write strobes include RTCWR#, COSUWR#, DOSTR#, and RAMWR#.
3. Read strobes include RTCRD#, CDSURD#, DISTR# and RAMRD#.
4. From later or NPRST ↑ or CMD# ↓.
5. Functional Specification . . . Not tested.
6. CMD# ↑ causes RTCWR# ↑ and RAMWR# ↑, while IOW# ↑ causes RAMD[0:7] to float. The 82304 insures that CMD#-to-RAMWR#/RTCWR# is at least 5 ns faster than IOW# to RAMD[0:7] float, assuming loading on RAMD[0:7] is greater than or equal to loading on RAMWR# or RTCWR#. This provides a minimum of 5 ns data hold time for the real time clock and SRAM, assuming CMD# and IOW# reach the 82304 at the same instant. Typically, more than 5 ns is provided, since IOW# is generated from, and thus delayed from CMD#.
7. Specification applies to software reset generated via port 92H.

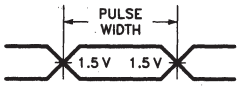
82304 DRIVE LEVELS/MEASUREMENT POINTS FOR A.C. SPECIFICATIONS



290185-3

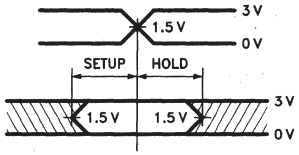


290185-4



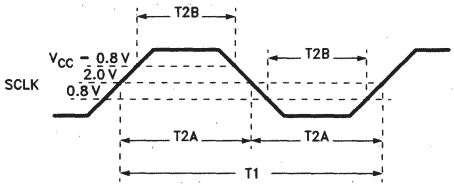
290185-5

Input/Output Pulse Widths,
Input Clock (Other than SCLK)
HIGH/LOW Times

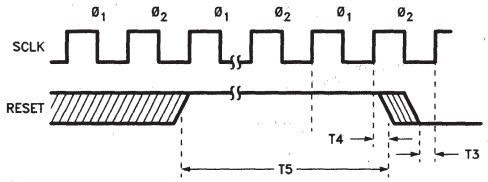


290185-6

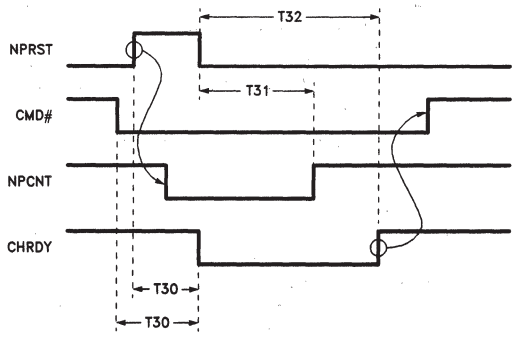
Input Setup and Hold to
another Input (Other than SCLK)



290185-7

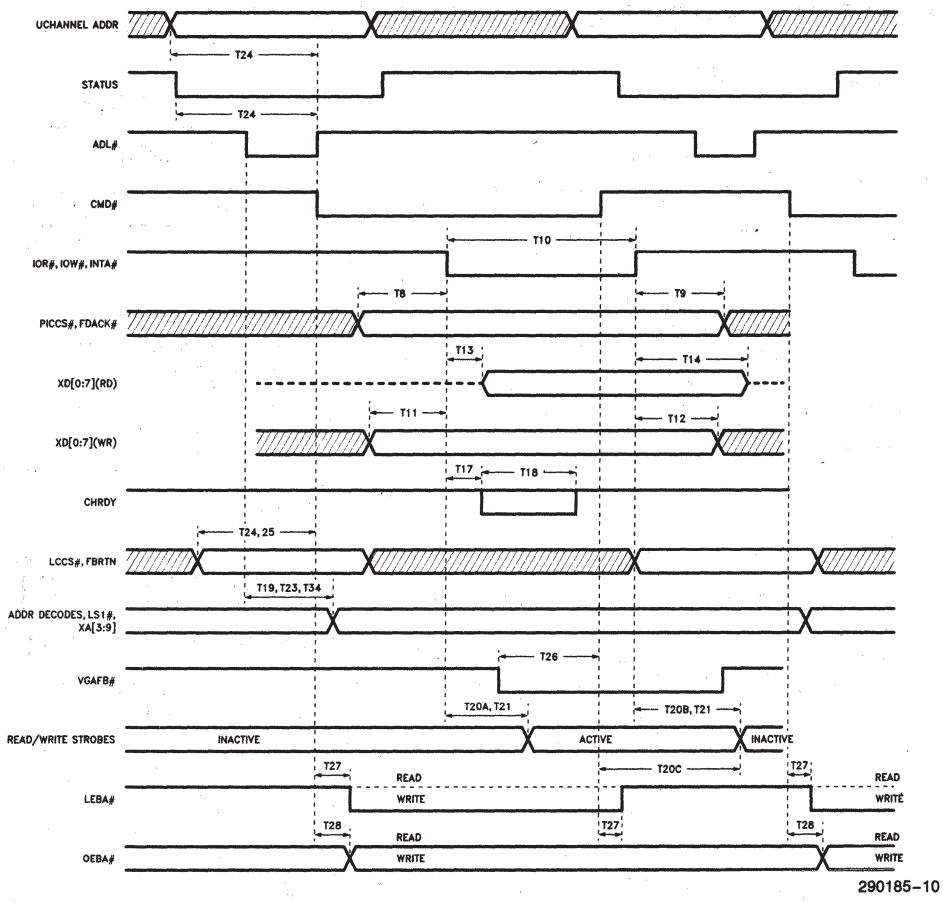


290185-8

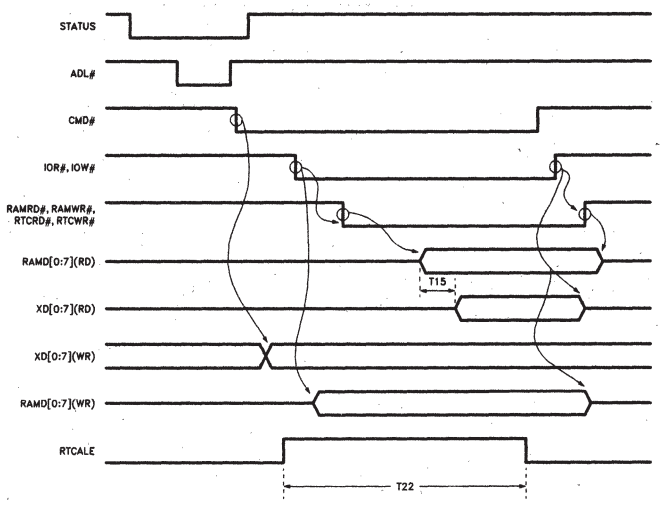


290185-9

NOTE:
Input Waveforms have $T_R \leq 2.0$ ns from 0.8V to 2.0V.



290185-10



290185-11

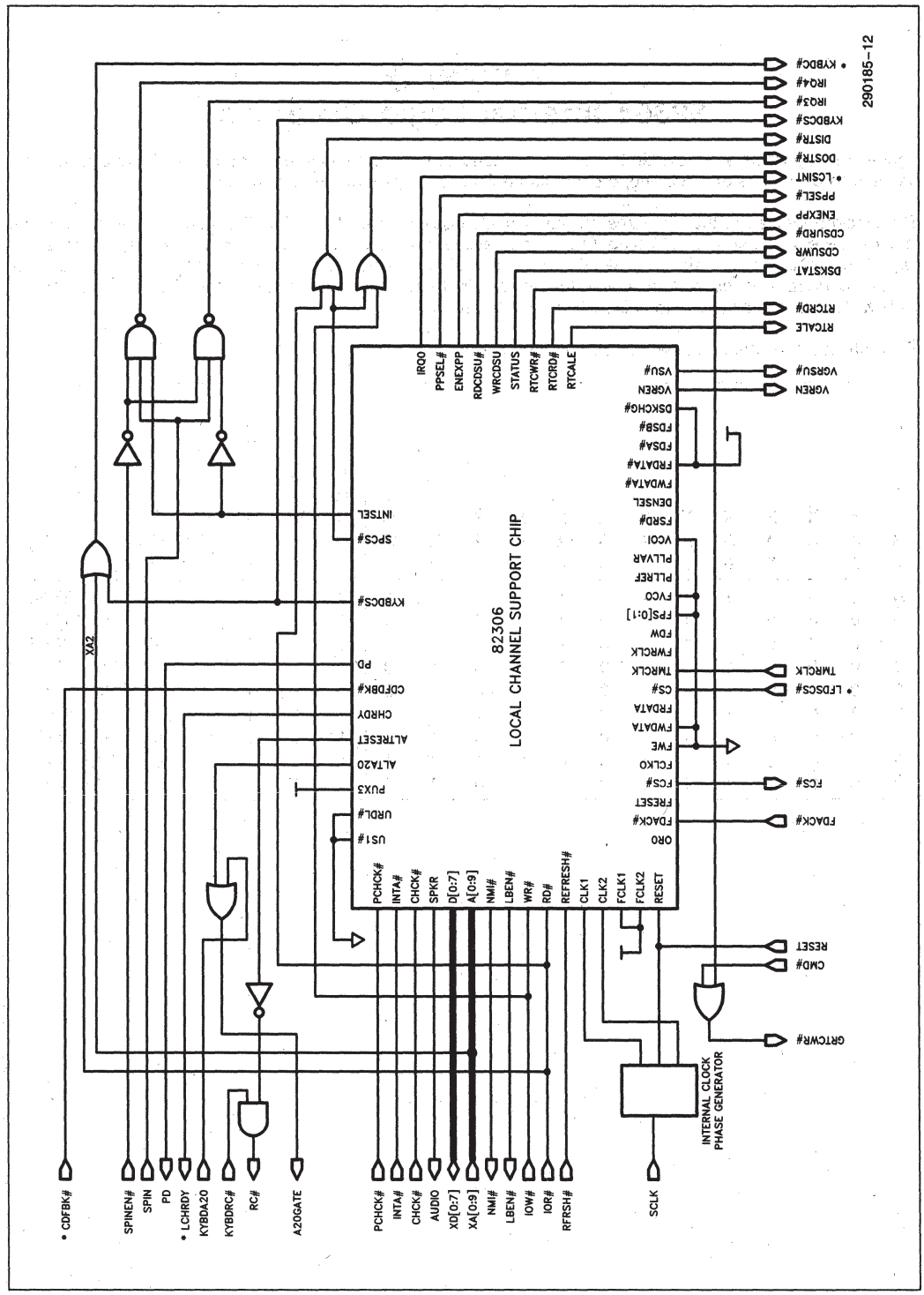
APPENDIX
82304 Internal Logic Diagrams

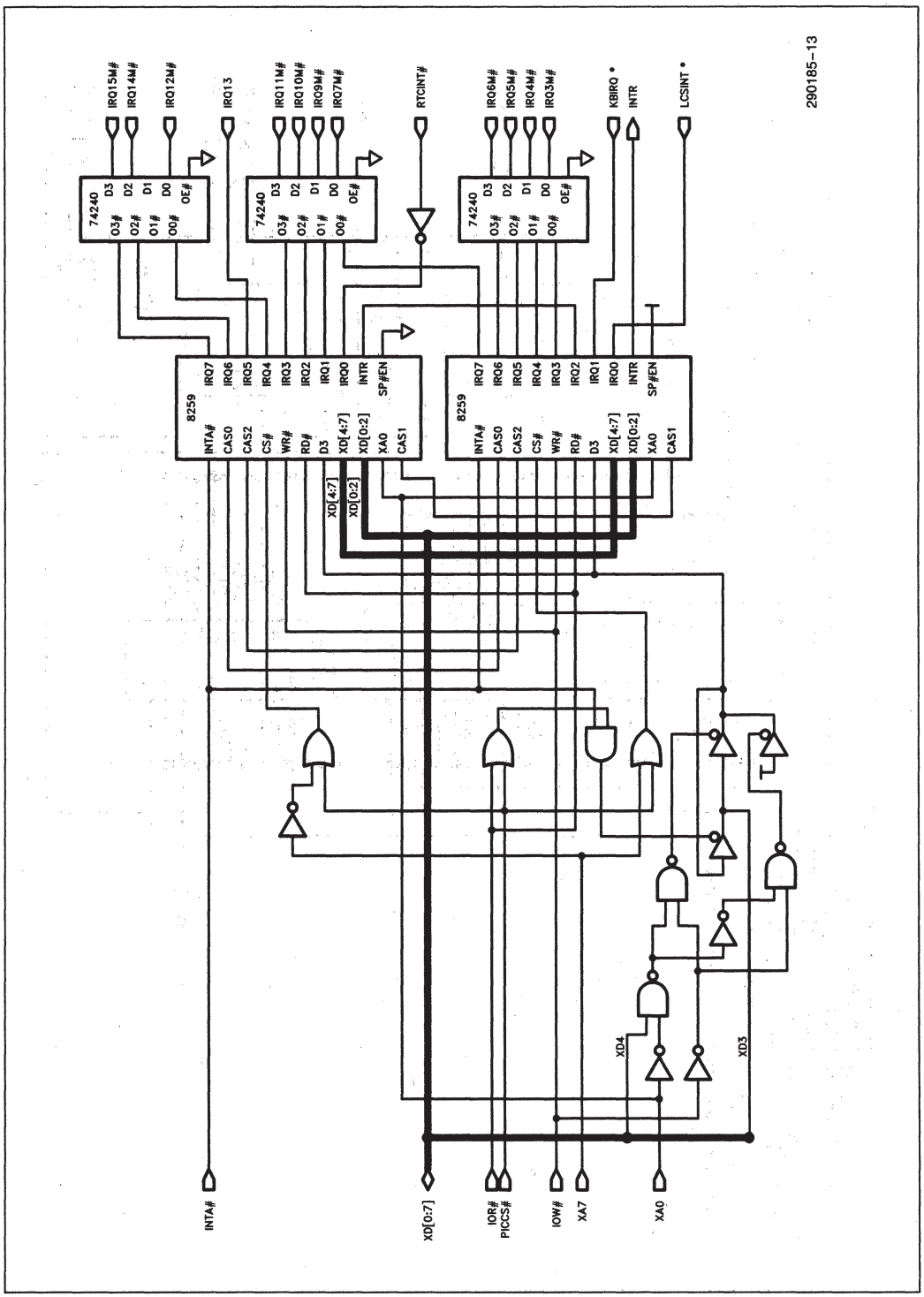
These logic diagrams are provided to aid in understanding the basic functionality of the 82304, and should not be used to estimate signal loading, propagation delays, or any other timing behavior.

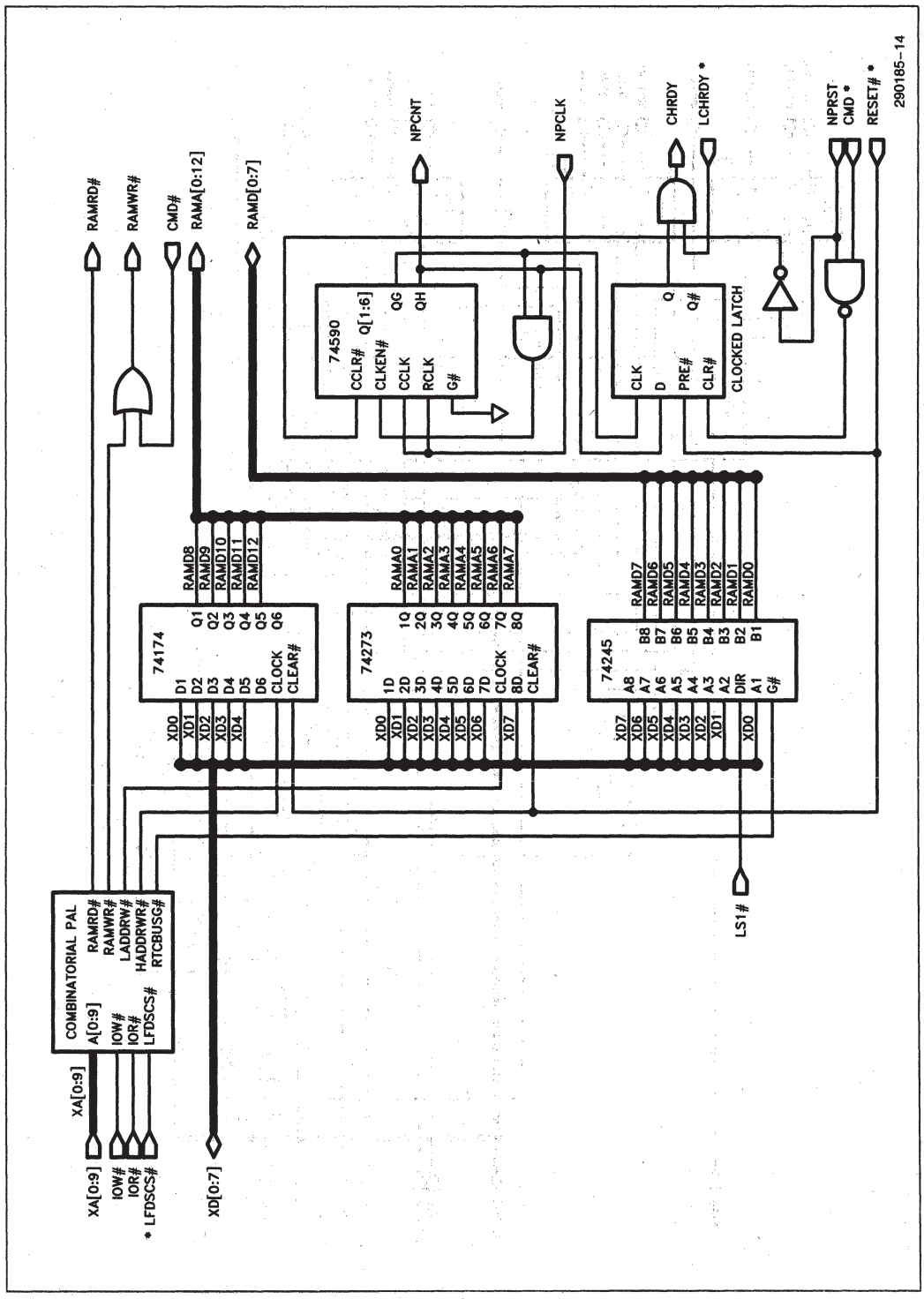
The clocked latches in the diagrams are functionally equivalent to 7474 type TTL latches. The transparent latches are equivalent to 74373 type TTL latches except that the gate input is active low rather than active high. The signals marked with asterisks (*) are not actually available external to the 82304, but simply serve as page-to-page references. Note however, that the XA[0:9] internal address bus is not marked with an asterisk. Only XA[3:9] are available externally, while XA[0:2] are not.

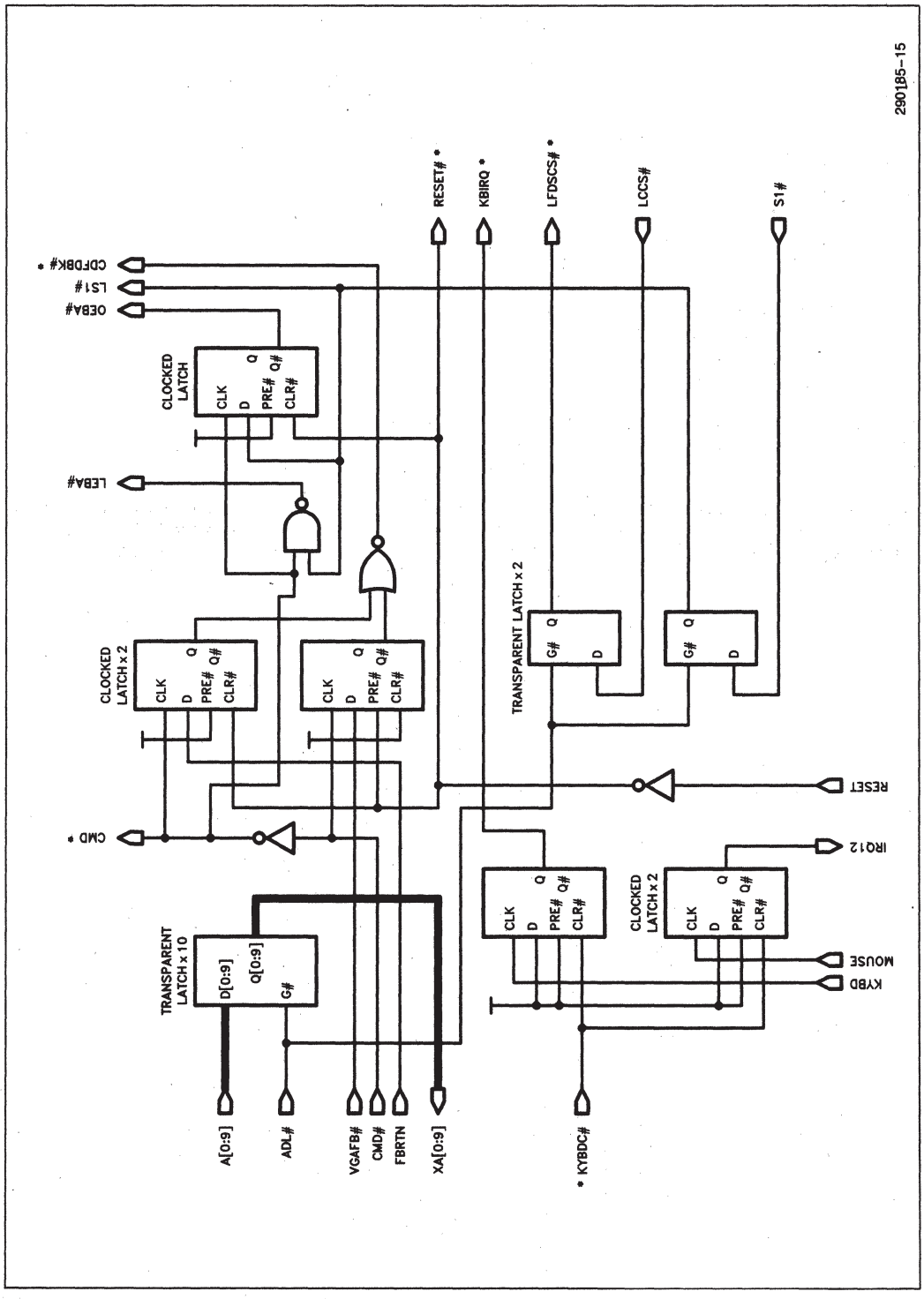
The truth table for the combinatorial PAL is as follows:

LFDSCS#	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	IORC#	IOWC#	RAMRD#	RAMWR#	HADDRWR#	LADDRWR#	RTCBUSG#	
0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	1	1	1	76H READ
0	0	0	0	1	1	1	0	1	1	0	1	0	1	0	1	1	1	76H WRITE
0	0	0	0	1	1	1	0	1	0	1	1	0	1	1	0	1	1	75H WRITE
0	0	0	0	1	1	1	0	1	0	0	1	0	1	1	1	0	1	74H WRITE
0	0	0	0	1	1	1	0	0	0	0	1	0	1	1	1	1	0	70H WRITE
0	0	0	0	1	1	1	0	0	0	1	1	0	1	1	1	1	0	71H WRITE
0	0	0	0	1	1	1	0	1	1	0	1	0	1	1	1	1	0	76H WRITE
0	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	1	0	71H READ
0	0	0	0	1	1	1	0	1	1	0	0	1	1	1	1	1	0	76H READ


82306
LOCAL CHANNEL SUPPORT CHIP
INTERNAL CLOCK PHASE GENERATOR
290185-12
• KYBDC#
IRQ4#
IRQ3#
KYBDCS#
DISTR#
DOSTR#
• LCSINT
PPSEL#
ENEXPP
CDSURD#
CDSUWR
DSKSTAT
RTCRD#
RTCALE
VSU#
VGREN
DSKCHG#
FDSB#
FDSA#
FRDATA#
FWDATA#
DENSEL
FSRD#
VCOI
PLLVAR
PLLREF
FVCO
FPS[0:1]
FDW
FWRCLK
TMRCLK
CS#
FRDATA
FWDATA
FWE
FCLKO
FCS#
FRESET
FDACK#
ORQ
IRQO
PPSEL#
ENEXPP
RDCDSU#
WRCDSU
STATUS
RTCWR#
RTCRD#
RTCALE
INTSEL
SPCS#
KYBDCS#
PD
CDFDBK#
CHRDY
ALTRESET
ALTA20
PUX3
URDL#
US1#
PCHCK#
INTA#
CHCK#
SPKR
D[0:7]
A[0:9]
NMI#
LBEN#
WR#
RD#
REFRESH#
CLK1
CLK2
FCLK1
FCLK2
RESET
XA2
VGRSU#
VGREN
TMRCLK
• LFDSCS#
FCS#
FDACK#
RESET
CMD#
GRTCWR#
• CDFBK#
SPINEN#
SPIN
PD
• LCHRDY
KYBDA20
KYBDRC#
RC#
A20GATE
PCHCK#
INTA#
CHCK#
AUDIO
XD[0:7]
XA[0:9]
NMI#
LBEN#
IOW#
IOR#
RFRSH#
SCLK


290185-13
IRQ15M#
IRQ14M#
IRQ12M#
IRQ13
IRQ11M#
IRQ10M#
IRQ9M#
IRQ7M#
RTCINT#
IRQ6M#
IRQ5M#
IRQ4M#
IRQ3M#
KBIRQ *
INTR
LCSINT *
74240
D3
D2
D1
D0
OE#
O3#
O2#
O1#
O0#
8259
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
IRQ2
IRQ1
IRQ0
INTR
SP#EN
INTA#
CAS0
CAS2
CS#
WR#
RD#
D3
XD[4:7]
XD[0:2]
XA0
CAS1
XD4
XD3
INTA#
XD[0:7]
IOR#
PICCS#
IOW#
XA7
XA0


290185-14
RAMRD#
RAMWR#
CMD#
RAMA[0:12]
RAMD[0:7]
NPCNT
NPCLK
CHRDY
LCHRDY *
NPRST
CMD *
RESET# *
74590
CCLR#
CLKEN#
CCLK
RCLK
G#
QG
QH
Q[1:6]
CLOCKED LATCH
CLK
D
PRE#
CLR#
Q
Q#
74174
74273
74245
RAMD8
RAMD9
RAMD10
RAMD11
RAMD12
RAMA0
RAMA1
RAMA2
RAMA3
RAMA4
RAMA5
RAMA6
RAMA7
RAMD7
RAMD6
RAMD5
RAMD4
RAMD3
RAMD2
RAMD1
RAMD0
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
CLOCK
CLEAR#
DIR
G#
LS1#
COMBINATORIAL PAL
A[0:9]
IOW#
IOR#
LFDSCS#
RAMRD#
RAMWR#
LADDRW#
HADDRWR#
RTCBUSG#
XA[0:9]
XD[0:7]
* LFDSCS#


290185-15
RESET# *
KBIRQ *
LFDSCS# *
LCCS#
S1#
CDFDBK# *
LS1#
OEBA#
CLOCKED LATCH
CLK
D
PRE#
Q
Q#
CLR#
LEBA#
CLOCKED LATCH x 2
TRANSPARENT LATCH x 2
G#
RESET
CMD *
IRQ12
TRANSPARENT LATCH x 10
D[0:9]
Q[0:9]
MOUSE
KYBD
A[0:9]
ADL#
VGAFB#
CMD#
FBRTN
XA[0:9]
* KYBDC#