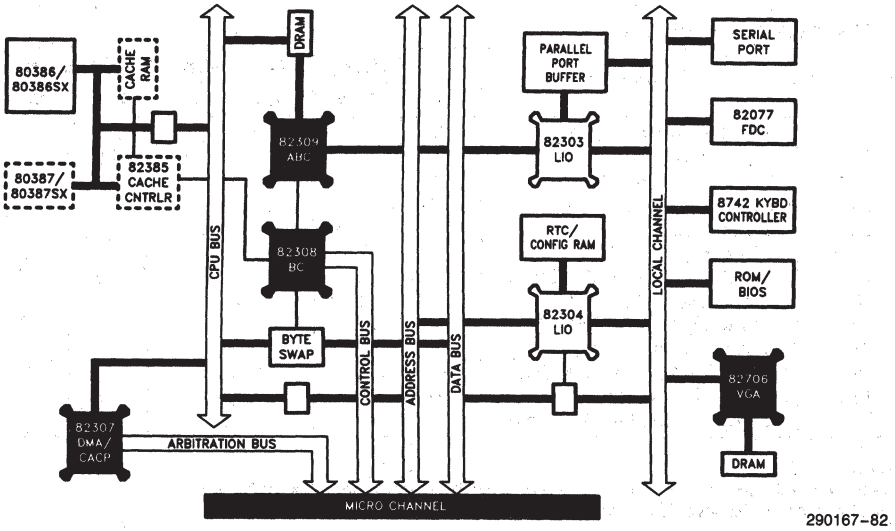
ADVANCE INFORMATION

82311
HIGH INTEGRATION Micro Channel COMPATIBLE PERIPHERAL CHIP SET

- **High Integration VLSI Components to Implement Micro Channel™ Compatible Motherboard**
- **Single Architectural Solution for 80386 16 MHz, 20 MHz and 25 MHz Systems and 80386SX 16 MHz Systems**
- **Full Compatibility with IBM Micro Channel Architecture**
- **Zero-Wait State Performance**
- **Cache Interface (82385) for Highest Performance Compatible System Implementation with 80386**
- **Supports up to 16 MB of Memory on Motherboard**
  — Extended Memory for OS/2 Support
- **100% IBM Compatible VGA Graphics**
- **Flexible Memory Architecture Support**
  — Up to 4 Banks of Interleaved Page Memory
  — 256K, 1M, 4M DRAM Support
- **Supports the 82077 Single Chip Floppy Disk Controller, Which Supports 3½" and 5¼" Disk Drives**
- **Keyboard and BIOS Support from 3rd Party**
- **Numeric Coprocessor(s) Interface (80387, 80387SX)**
- **Surface Mount Packaging for Small Footprint Design (0.025" Pitch)**
- **Low Power CHMOS Technology**
- **Available in 100 & 132-Pin Plastic Quad Flat Pack Packages.**
  (See Packaging Spec. # 231369)

Intel's peripheral chip family is designed to support the new generation of Micro Channel compatible systems. Intel's Micro Channel compatible peripheral solution consists of highly integrated VLSI components designed to support 80386 systems up to 25 MHz, as well as 16 MHz 80386SX systems.

The Intel solution is based on the high performance IBM Model 80 register model but it is highly integrated to provide full compatibility across all models. The specifications for 82311 VLSI components conform to architectural specifications defined for the Micro Channel Bus Architecture. The VLSI components are implemented in 1.5 micron CHMOS technology and packaged in space saving surface mount JEDEC flat pack packages.



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INTRODUCTION

The new generation of Personal Computer systems from IBM offers significant technological advantages over the PC/AT and XT systems. The most significant advancement is in the *Architectural* definition of the bus—Micro Channel Bus. Unlike the AT bus, the Micro Channel is well defined in terms of bus protocol timings. To create a compatible Micro Channel system requires adherence to the Micro Channel timings and electrical drive characteristics.

All IBM Micro Channel models have increased system functionality included on the motherboard. In the older PC/AT architecture, such functionality required the addition of peripheral cards. Specific features added to the motherboard include the Serial Port, Bi-directional Parallel Port and Video Graphics Control.

Micro Channel ARCHITECTURE

The Micro Channel Bus is defined to support an open architecture providing Multi-Master capability, Multi-Device arbitration with fairness, arbitration capability and easy configurability of the total system (Programmable Option Select-POS). Providing full details about the Micro Channel Bus Architecture is beyond the scope of this document. Please refer to IBM Technical Reference Manuals on Micro Channel systems.

To provide Multi-Master capability as defined in the Micro Channel Architecture, each Master device is responsible for driving the Address, Data, arbitration and control signals. For operation reliability and compatibility there are significant constraints in terms of timing and drive levels. These constraints are well documented in IBM's Technical Reference Manual for Micro Channel systems. Intel's chip set is designed to meet the Micro Channel timings.

The Micro Channel has four modes of Memory and I/O Bus cycles. These are Default cycle, Synchronous Extended cycle, Asynchronous Extended cycle and Matched Memory cycle. Each of these bus cycles is supported by the Intel Peripheral chip set.

COMPATIBILITY METRICS

The Intel chip set provides full compatibility with the IBM Micro Channel solution. All Bus cycles comply with the Micro Channel timings. Selection of buffers for drive level with minimum delays to meet Micro Channel timings are specified in the Intel *Designers Guide for Micro Channel Compatible Implementation.*

MEMORY PERFORMANCE

With the Intel chip set, Micro Channel compatible motherboards can be designed to provide zero-wait performance. Performance is predicated on memory design and DRAM speed selection. The Intel chip set offers flexible memory design support to meet various cost/performance goals.

SYSTEM CONSIDERATIONS

System Components

82303	Local I/O Support Chip
82304	Local I/O Support Chip
82307	DMA/CACP Controller
82308	Micro Channel Bus Controller
82309	Address Bus Controller
82706	VGA Graphics Controller
82077	Floppy Disk Controller

Note that the above names/numbers are frequency independent; i.e., they refer to a generic functional VLSI device. To actually implement for example, a 20 MHz system, however, requires an 82311-20 Chip Set as opposed to an 82311-16 Chip Set. The 25 MHz version of the 82308 (dubbed the 82308HS-25) cannot be used at 16 MHz or 20 MHz.

To implement a minimum configuration Micro Channel compatible motherboard, each of the seven system components listed above are required in addition to the following components:

- 80386 or 80386SX Microprocessor
- TTL Buffers for Various Buses in the System
- 8742 Keyboard Controller with Firmware for 101 and 102 Keyboard Interface
- Battery-Backed Real Time Clock with CMOS RAM
- Serial Port
- Memory

— ROM BIOS
— DRAMs for Main Memory
— DRAMs for VGA

- System Clock Sources
- Mechanical Connectors/Components

The Intel solution is supported by a fully compatible BIOS firmware from a third-party vendor.

82311 CHIP SET SYSTEM CLOCK REQUIREMENTS

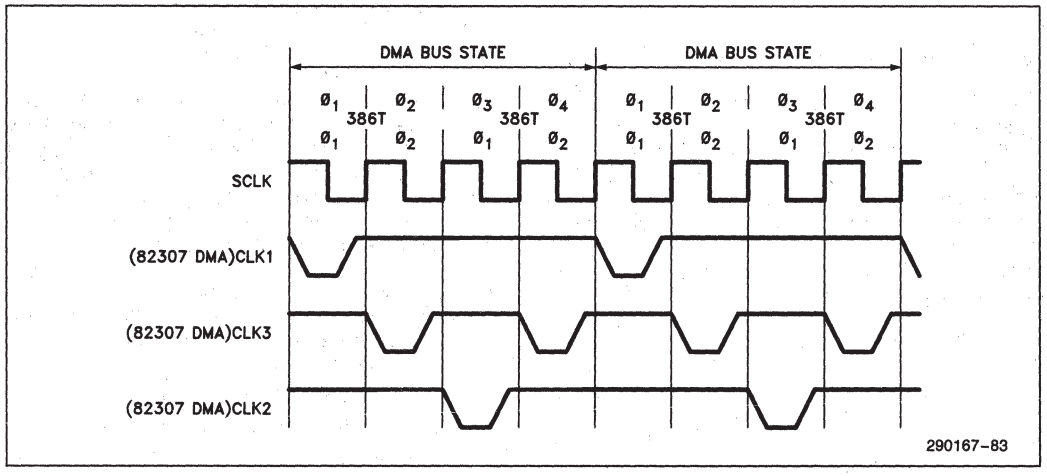
- Introduction
- Clock Definitions
- Clock Requirements

INTRODUCTION

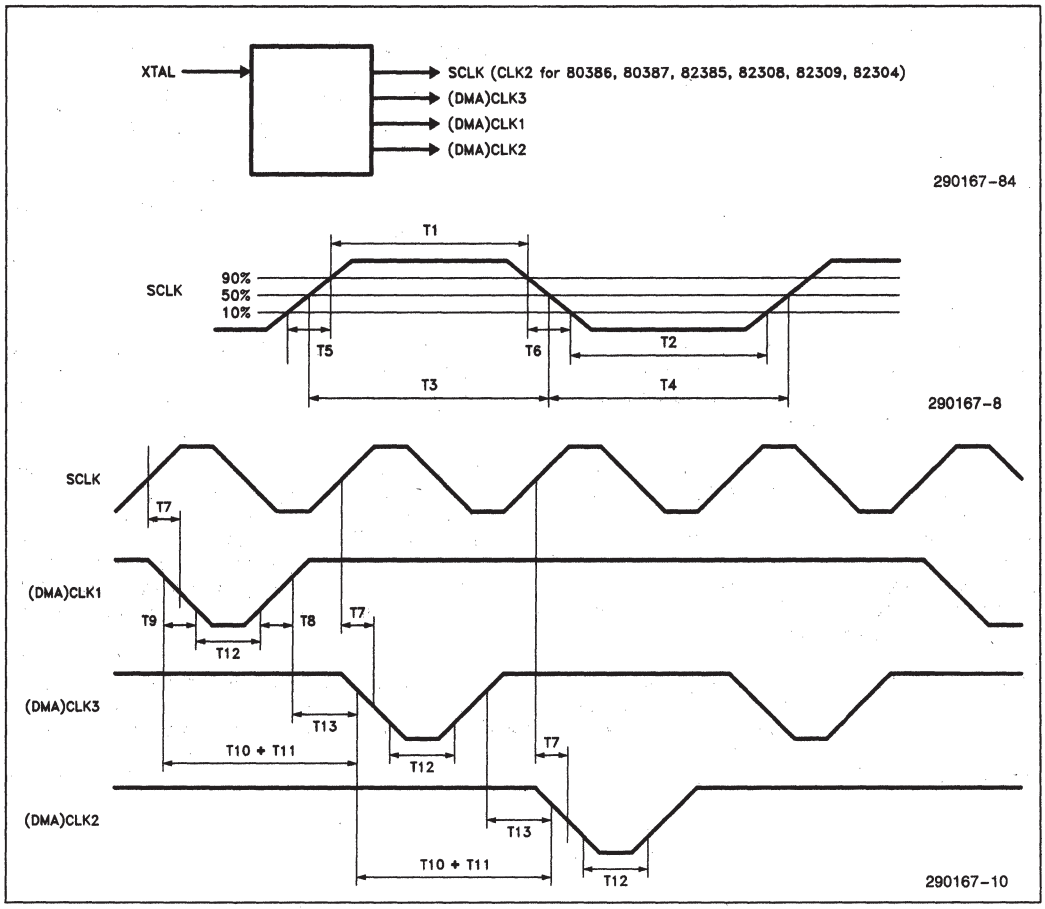
This section describes the basic clocking scheme of the host CPU (80386 or 80386SX), LIO (82304), DMA (82307), BC (82308) and ABC (82309). Although each component spec individually describes its own clock requirements, this section describes the synchronous relationship that exists between them. (Note that several other clocks exist in a Micro Channel system. However, this section describes only those clocks that are synchronously related to the CPU clock.)

The clocking scheme essentially divides the DMA bus state into four phases as depicted in the figure. Note that there is a direct 2-to-1 mapping of 80386 state to DMA state. The DMA (82307) comprehends phases by inputting distinct, active low, non-overlapping clock phases. The Address Bus Controller, Bus Controller and LIO device learn the system phase by synchronously sampling the falling edge of RESET, as described in the component specifications.

BASIC FOUR-PHASE CLOCKING REQUIREMENT



CLOCK CIRCUIT DEFINITION



SYSTEM CLOCK REQUIREMENTS

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		Notes
		Min	Max	Min	Max	Min	Max	
T1	SCLK High Time (90%)	8		6.5		5.5		
T2	SCLK Low Time (10%)	8		6.5		5.5		
T3	SCLK High Time (50%)	12		10		9		1
T4	SCLK Low Time (50%)	12		10		9		1
T5	SCLK Rise Time		3.5		3.5		3.5	
T6	SCLK Fall Time		3.5		3.5		3.5	
T7	SCLK-To-DMACLK(N) Skew	−2	3	−2	3	−2	3	2
T8	DMACLK(N) Rise Time		2		2		2	
T9	DMACLK(N) Fall Time		2		2		2	
T10	SCLK Period							
T11	DMACLK-To-DMACLK Skew	−2	2	−2	2	−2	2	2
T12	DMACLK Low Time	15		15		12		
T13	DMACLK Non-Overlap Time	4		4		2		

NOTES:
1. Needed to enforce a duty cycle between 40% and 60% (45% and 55% at 25 MHz).
2. Limiting skew to this level is recommended.

Micro Channel INTERFACE AND SPECIFICATIONS

INTRODUCTION

This section describes the interface between the host CPU (80386, 80386SX), DMA (82307), Bus Controller (82308) and Micro Channel Bus. This interface provides 100% compliance to published Micro Channel timings, driver type requirements, drive levels, and drive current capability. Timings meet the full capacitive load allowed on the Micro Channel.

The Micro Channel Specifications included in this section assume the specific TTL Data, Address, and Command Path interfaces depicted in the accompanying figures. Timing analysis was based on the Bus Controller AC specifications included in the 82308 Bus Controller section. Worst case TTL analysis was used, except when two related signals share a path through the same physical chip. (For example, since MMCCMD#, S0#, and S1# propagate through the same 74F241 package in an 80386 system, one signal will not experience a worst case delay while the other sees a best case. Rather, it is assumed that the signals will track within 2 ns of each other.) For this reason, it is important to follow the recommendations detailed at the end of this section in the Interface Logic Notes.

The F and AS TTL logic is typically specified into a 50 pF load, worst case delays were derated at 1 ns per 50 pF for loads greater than 50 pF. As an example, the 74F241 published maximum delay is specified as 7 ns. To meet Micro Channel bus loading of 250 pF, a 4 ns derating factor was added, resulting in an effective worst case delay of 11 ns.

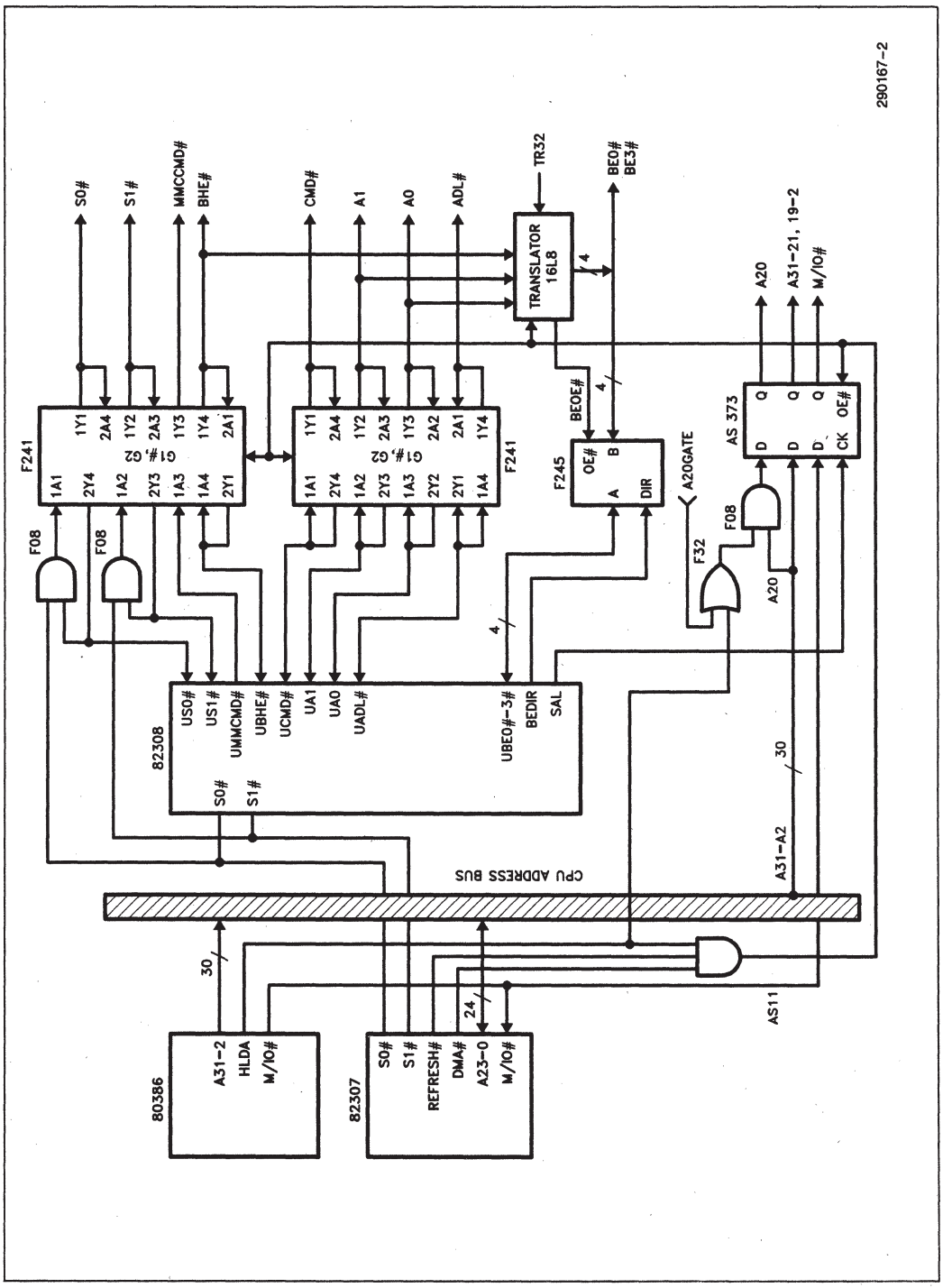
DEFAULT CYCLE SPECIFICATIONS — ALL KITS

Symbol	Parameter	Min	Max
T1	Status active from ADDR,M/IO#,REFRESH#	10	
T2	CMD# active from Status active	55	
T3	ADL# active from ADDR,M/IO#,REFRESH#	45	
T4	ADL# active to CMD# active	40	
T5	ADL# active from Status active	12	
T6	ADL# pulse width	40	
T7	Status hold from ADL# inactive	25	
T8	ADDR,M/IO#,REFRESH#,SBHE# hold frm ADL# INACTIVE	25	
T9	ADDR,M/IO#,REFRESH#,SBHE# hold frm CMD# ACTIVE	30	
T10	Status hold from CMD# active	30	
T11	SBHE# setup to ADL# inactive	40	
T12	SBHE# setup to CMD# active	40	
T13	CDDS16/32 active from ADDR,M/IO#,REFRESH#		55
T14	CDSFDBK# active from ADDR,M/IO#,REFRESH#		60
T15	CMD# active from ADDRESS valid	85	
T16	CMD# pulse width	90	
T17	Write data setup to CMD# active	0	
T18	Write data hold from CMD# inactive	30	
T19	Status to Read Data valid (Access Time)		125
T20	Read Data valid from CMD# active		60
T21	Read Data hold from CMD# inactive	0	
T22	Read Data bus tri-state from CMD# INACTIVE		40
T23	CMD# active to next CMD# active	190	
T23A	CMD# inactive to next CMD# active	80	
T23B	CMD# inactive to next ADL# active	40	
T24	Next Status active from Status Inactive	30	
T25	Next Status active to CMD# Inactive		20
T26	CHRDY INACTIVE FROM ADDR VALID		60
T27	CHRDY INACTIVE FROM STATUS ACTIVE		30
T28	CHRDY RELEASE FROM CMD# ACTIVE		30
T28D	READ DATA VALID FROM CMD# ACTIVE		160
T29S	READ DATA VALID FROM CHRDY RELEASE		60
T31	BE#(0–3) from Addr valid (32-Bit Masters Only)		40
T32	BE#(0–3) active from SBHE#,A0,A1 active		30
T33	BE#(0–3) active to CMD# active	10	

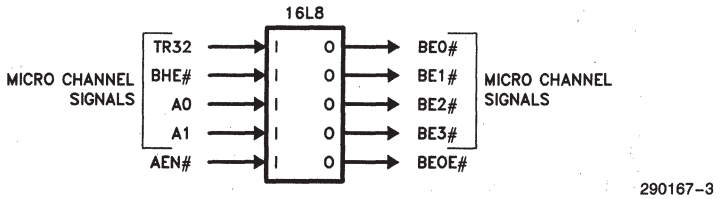
MATCHED MEMORY CYCLE SPECIFICATIONS — ALL KITS

Symbol	Parameter	Min	Max
T1	ADDR VALID TO STATUS ACTIVE	10	
T2	Status valid to MMCCMD# active	82	
T3	ADDR hold from MMCCMD# active	20	
T4	Status hold from MMCCMD# active	25	
T5	CDDS16/32 active from ADDR valid		55
T6	MMCR# active from ADDR valid		55
T7	CDSFDBK# active from ADDR valid		60
T8	ADDR valid to MMCCMD# active	100	
T9	MMCCMD# pulse width	85	
T10	Write Data valid to MMCCMD# active	0	
T11	Write Data hold from MMCCMD# inactive	30	
T12A	Read Data valid from Status active		145
T12B	for non-aligned xfers (16b < = = > 32b)		145
T13A	Read Data valid from MMCCMD# active		60
T13B	for non-aligned xfers (16b < = = > 32b)		60
T14	Read Data hold from MMCCMD# inactive	0	
T15	Read Data off dly from MMCCMD# inactive		40
T16	MMCCMD# active to next MMCCMD# active	180	
T17	CDCHRDY valid from ADDR valid		70
T18	CDCHRDY valid from Status active		30
T23	Status inactive pulse width	30	
T24	MMCCMD# inactive to Status active	5	
T25	MMCCMD# inactive pulse width	85	
T26	MMCCMD# ACTIVE TO NEXT STATUS ACTIVE	90	

80386 SYSTEM ADDRESS/COMMAND PATH



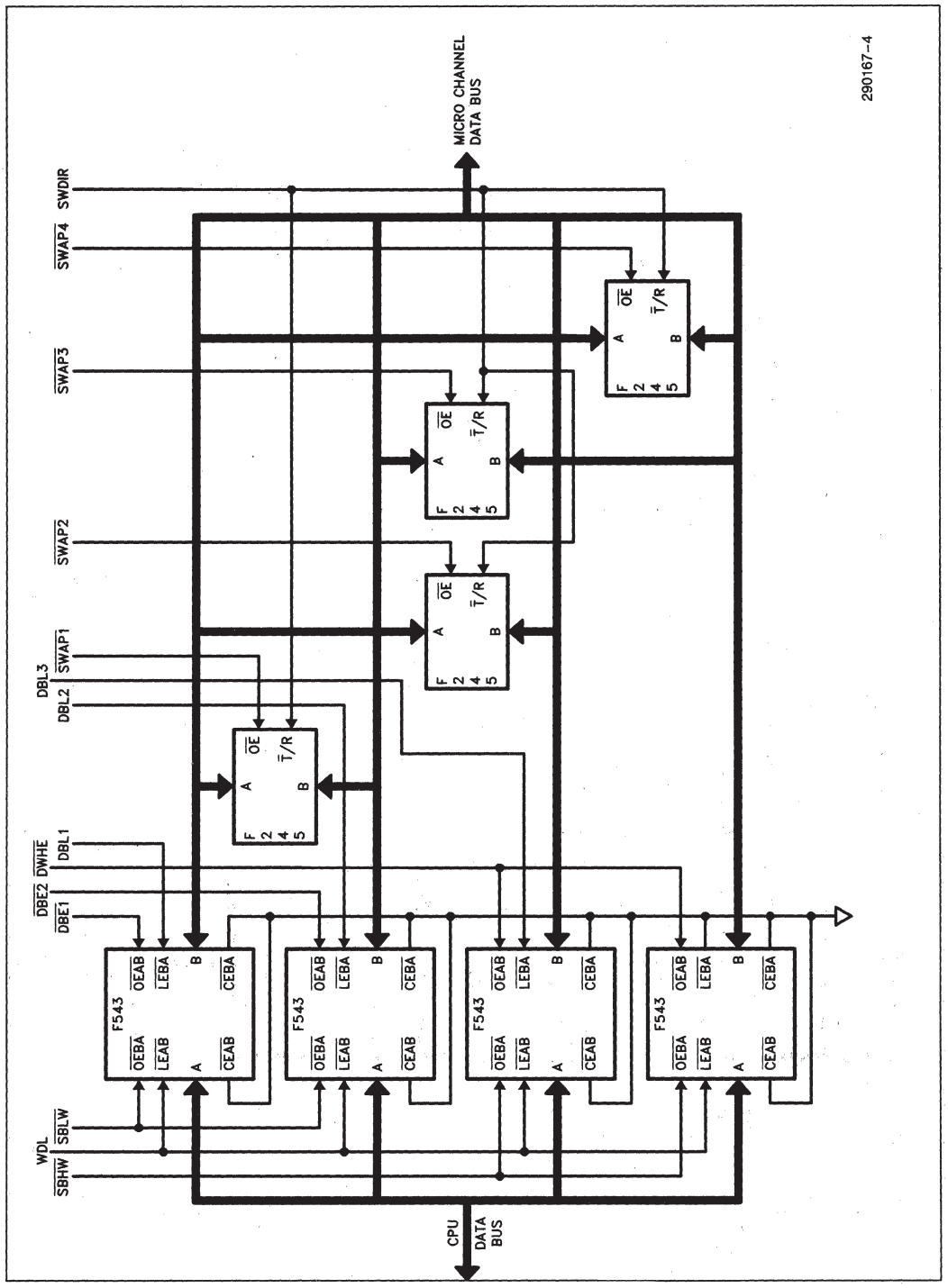
80386 SYSTEM BYTE ENABLE TRANSLATOR PAL



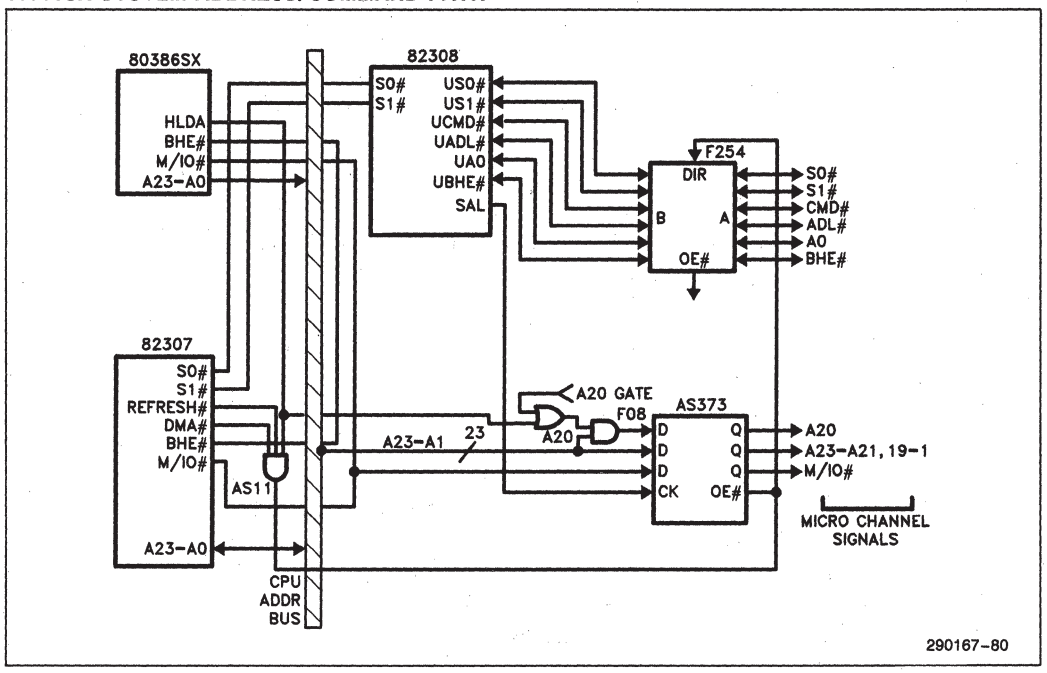
TR32	AEN#	BHE#	A1	A0	BE3#	BE2#	BE1#	BE0#	BEOE#
1	1	0	0	0	1	1	0	0	1
1	1	0	0	1	1	1	0	1	1
1	1	0	1	0	0	0	1	1	1
1	1	0	1	1	0	1	1	1	1
1	1	1	0	0	1	1	1	0	1
1	1	1	0	1	1	1	0	1	1
1	1	1	1	0	1	0	1	1	1
1	1	1	1	1	0	1	1	1	1
0	X	X	X	X	TS	TS	TS	TS	0
X	0	X	X	X	TS	TS	TS	TS	0

TS = TRISTATE

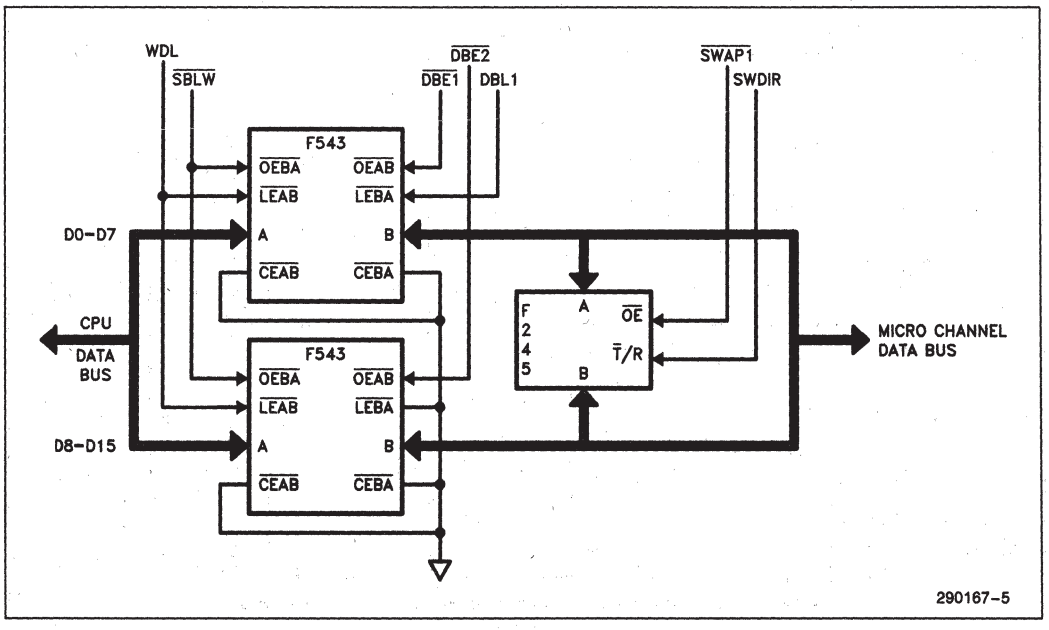
80386 SYSTEM DATA PATH



80386SX SYSTEM ADDRESS/COMMAND PATH



80386SX SYSTEM DATA PATH



Micro Channel Interface Logic Notes

80386 SYSTEM

1. The F08 gates in the S0#, S1# path are required at 20 MHz and at 25 MHz. They should not be used at 16 MHz.
2. In an 82385 system, the A20 gate logic is on the 80386 local bus, and is thus not required on the 82385 local bus as shown in the diagram.
3. The F08 gates in the S0#, S1# path and the F08 in the A20 path should all be from the same TTL package.
4. It is important that S0#, S1#, BHE#, and MMCCMD# go through the same F241 package, and that CMD#, ADL#, A0, and A1 go through the same package.

80386SX SYSTEM

1. The F08 gates in the S0#, S1# path and in the A20 path should all be from the same package.

PLASTIC PACKAGING INFORMATION

(See Packaging Spec. Order # 231369)

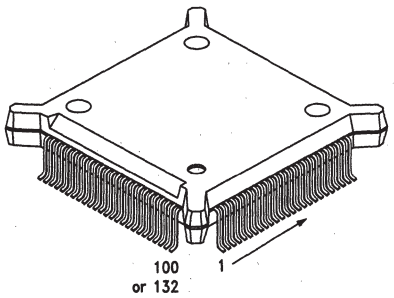
Introduction

The individual components of Intel's Micro Channel Compatible Peripheral Chip Sets come in JEDEC standard Gull Wing packages (25 MIL pitch), with "bumpers" on the corners for ease of handling. Please refer to the accompanying table for the package associated with each device, and to the individual component specifications for pinouts. (Note that the individual pinouts are numbered consistently with the numbering scheme depicted in the accompanying figures.)

MICRO CHANNEL COMPATIBLE PERIPHERAL FAMILY COMPONENT PACKAGES

Component	Package
82303	100 Pin PQFP
82304	132 Pin PQFP
82306	100 Pin PQFP
82307	132 Pin PQFP
82308	100 Pin PQFP
82309	100 Pin PQFP
82706	132 Pin PQFP
82077	68-Pin PLCC, See Component Data Sheet

PLASTIC QUAD FLAT PACK (PQFP)



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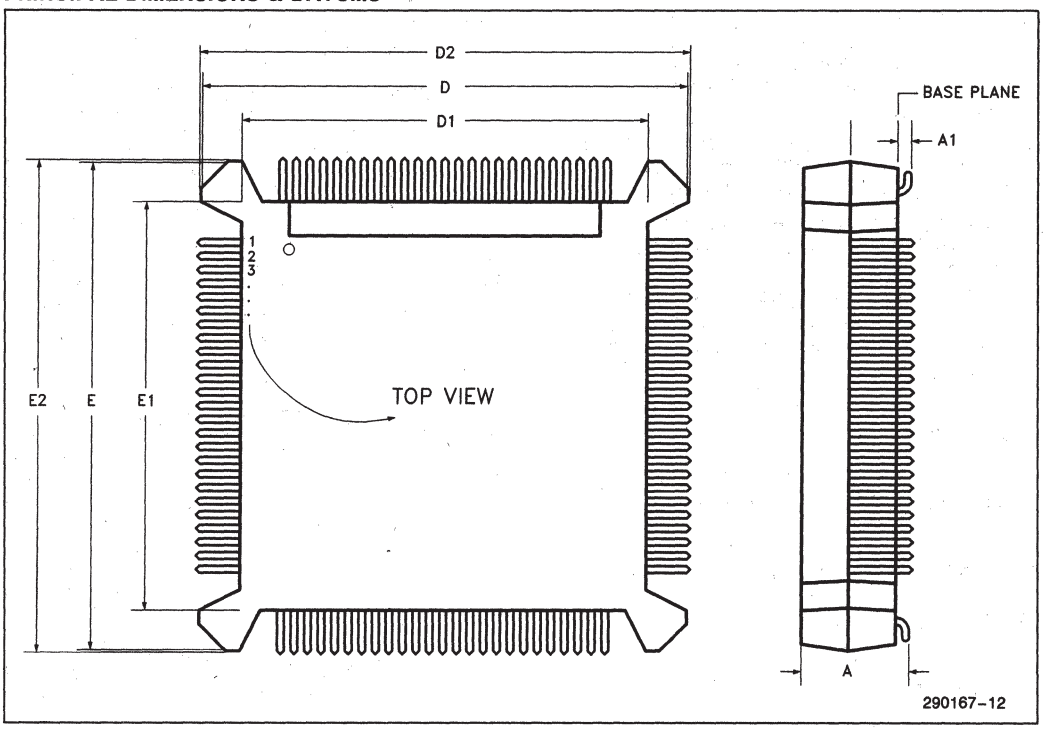
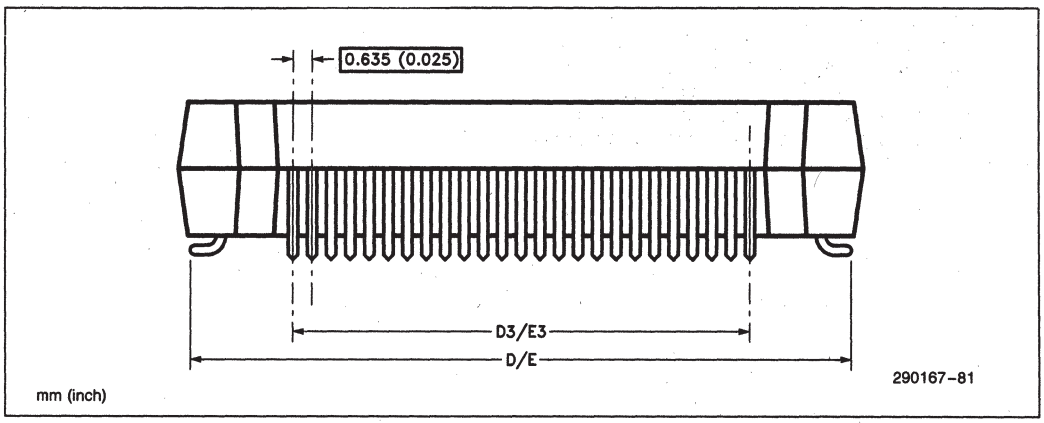
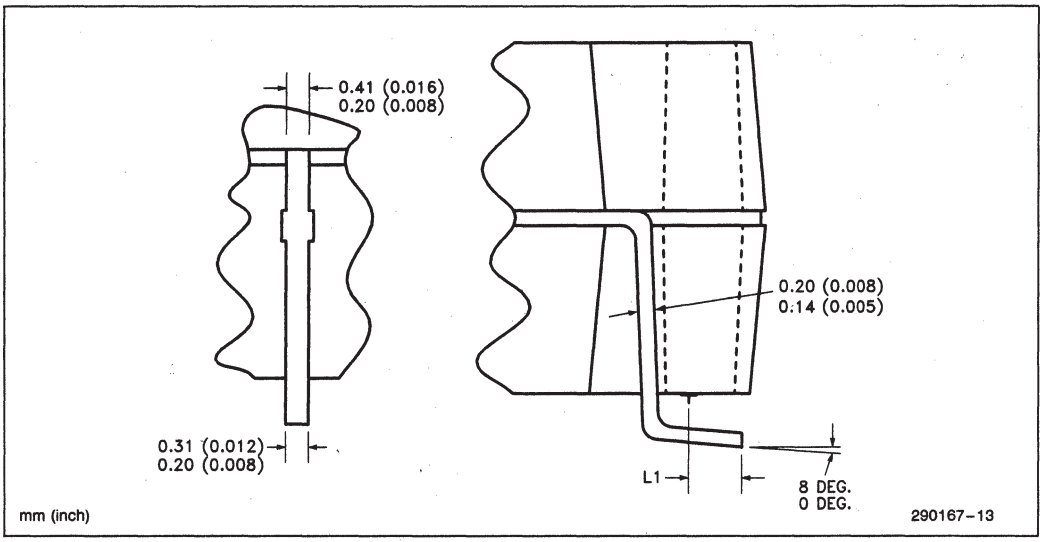
PRINCIPAL DIMENSIONS & DATUMS



TERMINAL DETAILS



TYPICAL LEAD



Case Outline Drawings
Plastic Fine Pitch Chip Carrier

		0.025 inch Pitch				0.84 mm Pitch			
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
N	Lead Count	100		132		100		132	
A	Package Height	0.160	0.170	0.160	0.170	4.06	4.32	4.06	4.32
A1	Standoff	0.020	0.030	0.020	0.030	0.51	0.76	0.51	0.76
D, E	Terminal Dimension	0.875	0.885	1.075	1.085	22.23	22.48	27.31	27.56
D1, E1	Package Body	0.747	0.753	0.947	0.953	18.97	19.13	24.05	24.21
D2, E2	Bumper Distance	0.897	0.903	1.097	1.103	22.78	22.94	27.86	28.02
D3, E3	Lead Dimension	0.600 Ref		0.800 Ref		15.24 Ref		20.32 Ref	
L1	Foot Length	0.020	0.030	0.020	0.030	0.51	0.76	0.51	0.76
		Inch				mm			

REVISION HISTORY

The A.C. Specifications of the 82306, 82307, 82308 and 82309 chips have been modified with respect to the 82310 Data Sheet Order Number 290167-001. These modifications apply to the 16 MHz and 20 MHz kits only.

82306 Spec Revisions

— T1 changed from 14 ns to 15 ns at 16 MHz . . . from 12 ns to 15 ns at 20 MHz

— T2 changed from 10 ns to 4 ns at 16 MHz . . . from 7 ns to 4 ns at 20 MHz

— T16 changed from 180 ns to 230 ns at 16 MHz and 20 MHz

— T20 changed from 200 ns to 120 ns at 16 MHz and 20 MHz

82307 Spec Revisions

— T1 changed from 14 ns to 15 ns at 16 MHz . . . from 12 ns to 15 ns at 20 MHz

— T2 changed from 10 ns to 4 ns at 16 MHz . . . from 7 ns to 4 ns at 20 MHz

— T33 cap load C(L) changed from 50 pF to 25 pF

82308 Spec Revisions

— T5A changed from 37 ns to 30 ns at 16 MHz and 20 MHz

— T6A broken into two specs . . . T6A for FLUSH, and T6C for SNOOP#

— T44 broken into two specs . . . T44A for Setup to SCLK and T44B for Setup to UCMD# . . . T44A left at 0 ns, but T44B changed to 3 ns

— T47C changed from 35 ns to 40 ns

82309 Spec Revisions

— T18A changed from 45 ns to 30 ns at 16 MHz

— T18B changed from 50 ns to 38 ns at 16 MHz

— T18C changed from 50 ns to 35 ns at 16 MHz

— T27B changed from 30 ns to 33 ns

— T32B changed from 50 ns to 55 ns

— T32E (Min) changed from 8 ns to 4 ns

— T32E (Max) changed from 30 ns to 27 ns

— T32G (Min) changed from 6 ns to 4 ns

— T32I changed from 50 ns to 40 ns

— T33 (Min) changed from 8 ns to 5 ns

— T34 (Min) changed from 6 ns to 3 ns

— T34 (Max) changed from 26 ns to 27 ns

— T35 changed to 115 ns to 100 ns at 16 MHz and from 90 ns at 20 MHz

— T45 changed from 26 ns to 32 ns