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82495DX/82490DX A HIGH PERFORMANCE 2ND LEVEL CACHE FOR THE Intel486™ DX CPU

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AGENDA

- System Model
- Objectives
- The Product
- Architecture
- Performance
- Conclusions

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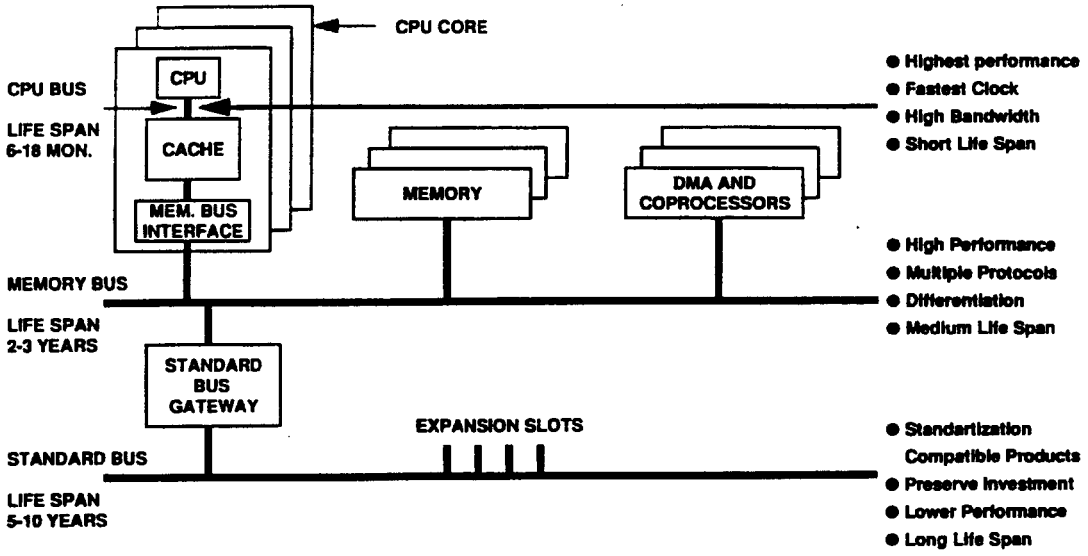
SYSTEM MODEL



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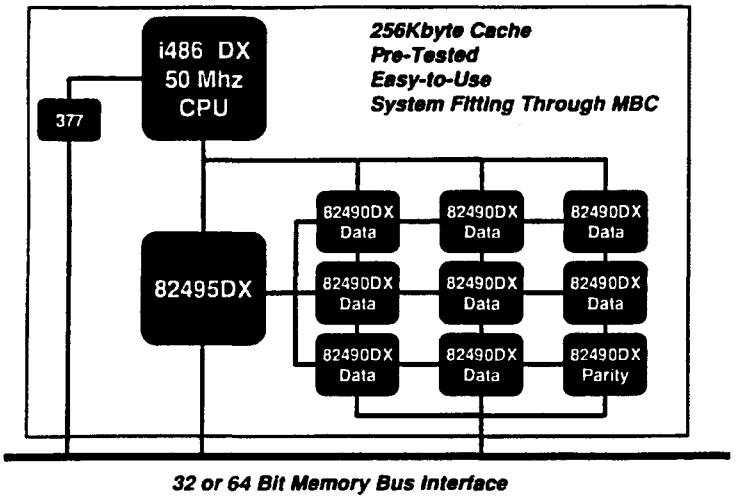
82495DX/490DX CACHE OBJECTIVES

- **Deliver High Performance**
  - 50 Mhz, Zero Wait-State RDs/WRs
  - Concurrent CPU/MEM Bus Transactions
  - Large Cache Size (upto 512Kbytes)
  - Two-Way Set Associative
- **Simplify Multi-Processing Designs**
  - Hardware Cache Consistency
- **High Integration**
  - Minimum Number of Devices
- **Provide Flexible Memory Bus Interface**
  - User Differentiated
  - Synchronous / Asynchronous
- **Software Transparent**

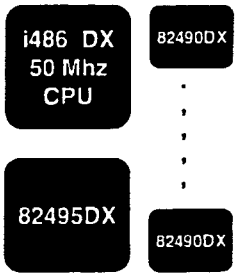
THE PRODUCT

MARKET: HIGH-END DESKTOPS / SERVERS

Intel486™ DX 50Mhz CPU-Cache Module



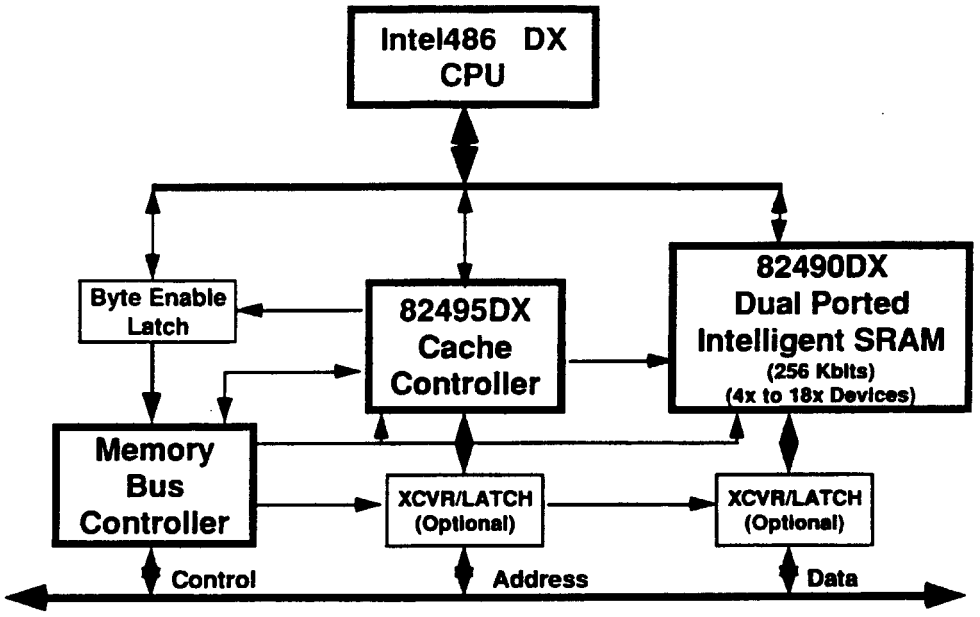
50 Mhz CPU-Cache Chip Set



82495DX/490DX CACHE FEATURES

- **Two Chip Set**
  - Controller (82495DX)
  - Dual Ported Intelligent SRAM (82490DX)
- **Cache Sizes: 128, 256, 512 Kbytes**
- **0-WS Support for 50 Mhz Intel486™ DX CPU**
- **Multi-Processing Support**
  - Write-Back Snoopy Cache, MESI-Consistency
  - 2-way Set Associative,
    Most-Recently-Used (MRU) Way Prediction
  - Multi-level Consistency Through Inclusion
- **Flexible Memory Bus Interface**
  - Synchronous / Asynchronous, 32/64/128 Bits
- **Available as Components / CPU-Cache Module**

CPU / CACHE CORE



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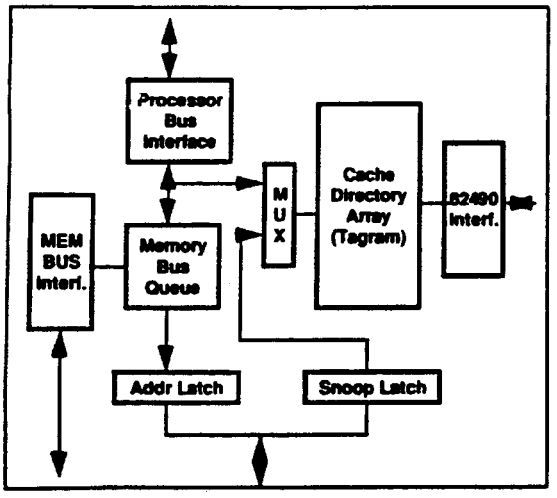
CACHE HIGHLIGHTS

82495DX - CACHE CONTROLLER



- **Integrated Tags and Cache Control**
- **Cache Consistency**
  - MESI on Memory Bus
  - Inclusion on CPU Bus
- **Two Way Associative**
  - MRU Prediction / Correction
  - In Lock-step with 82490DX
- **Innovative / Flexible MBC Interface**
  - 4 / 8 Transaction Burst
  - Sync / Async Snoops
  - With / Without Write-Allocation
  - Pipelined

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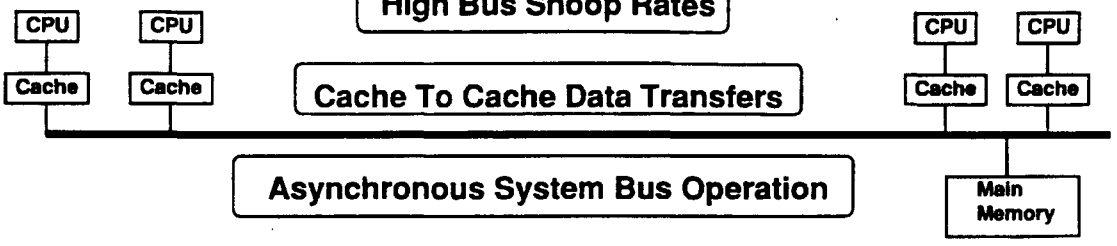
MULTIPROCESSING FEATURES

Hardware-Based MESI Consistency Protocol

Allocate On Write To Minimize Bus Traffic

High Bus Snoop Rates



Consistency With CPU-L1-Cache by Inclusion

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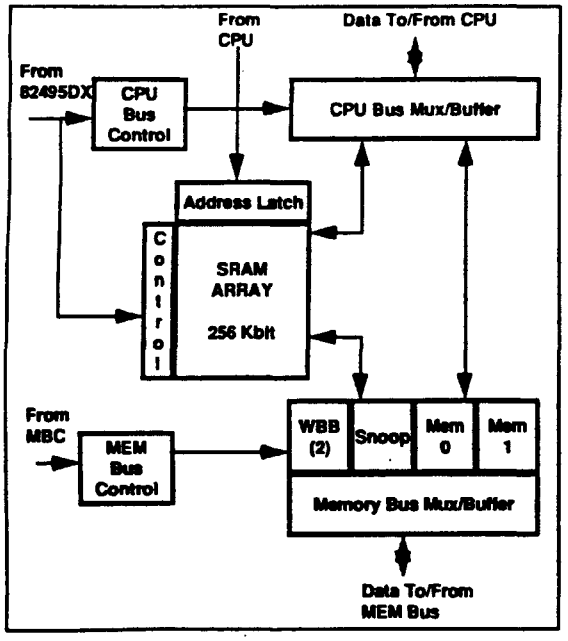
CACHE HIGHLIGHTS

82490DX - DUAL PORTED INTELLIGENT SRAM



- **2-WAY SRAM ARRAY (256 Kbits)**
  - MRU Prediction
- **Line Wide Buffers (upto 128Bytes)**
  - Write-Throughs, Line-Fill
  - Write-Back (2), Snoop
  - One CLK Array Access
- **Dual Ported**
  - CPU / MEM Bus concurrency
- **Line-Size: 16 / 32 / 64 / 128 Bytes**
- **MEM-BUS: 32 / 64 / 128 Bits Wide**
- **SYNC / ASYNC Interface**

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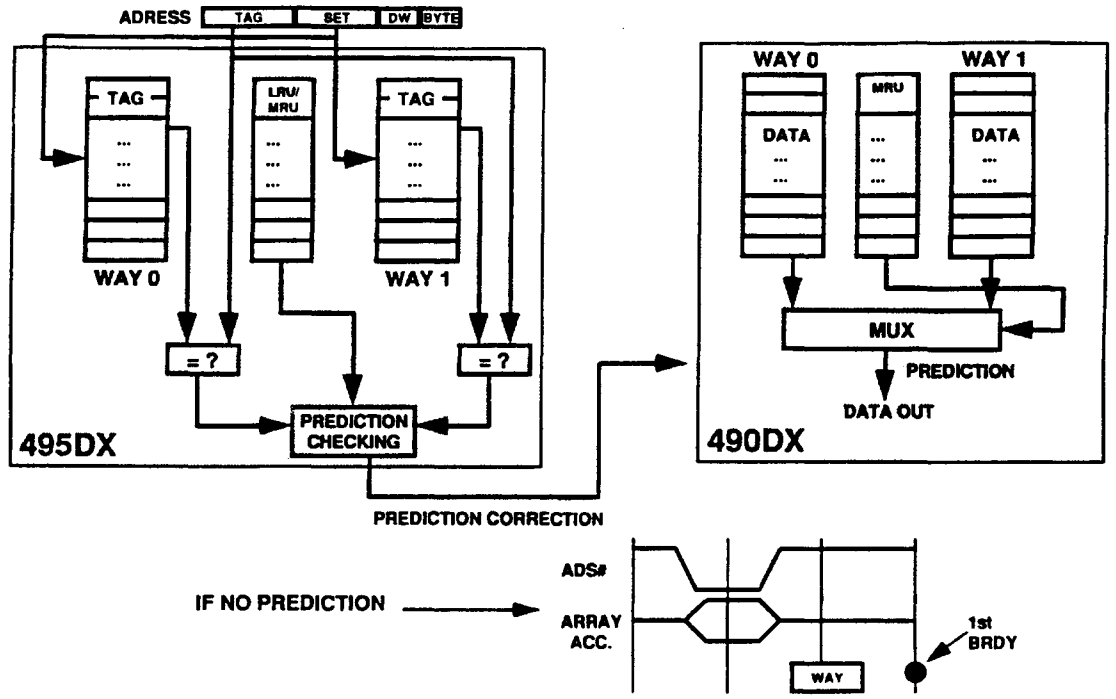
MRU-WAY-PREDICTION



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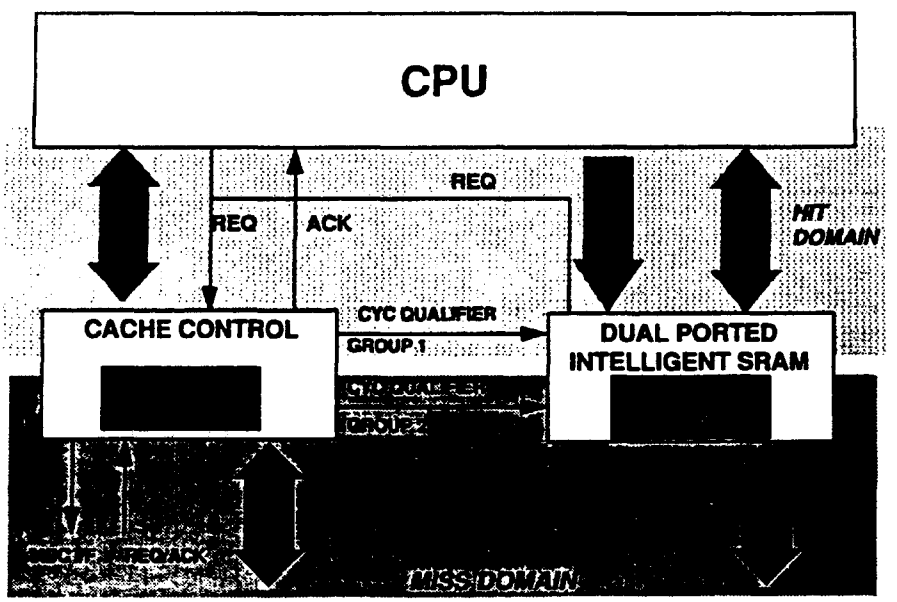
TUNED CPU/CACHE INTERFACE

50 MHZ, 2-WAY, 0-WAIT-STATE



TUNED INTERFACE

OPTIMIZED FOR MODULES

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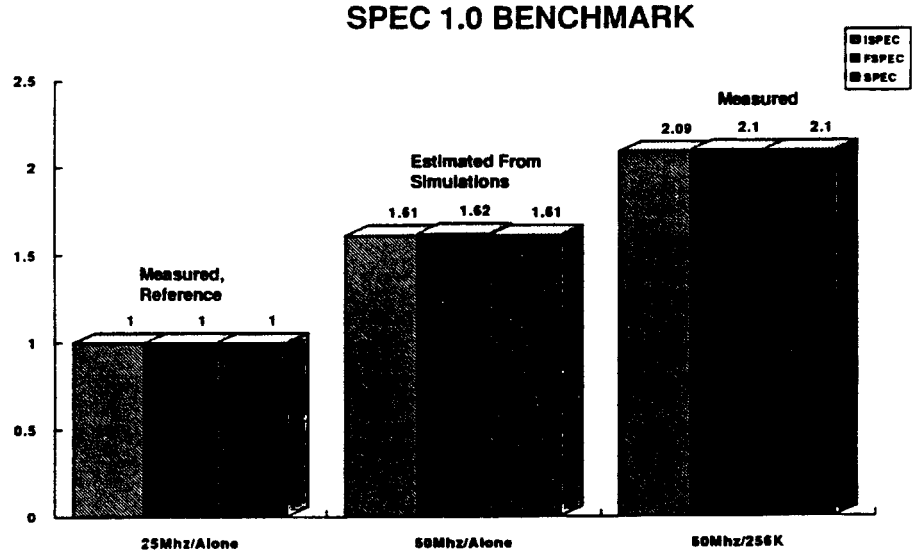
PERFORMANCE

IMPROVEMENT VS 25 MHZ STAND-ALONE Intel486™ DX SPEC 1.0 BENCHMARK



BUS: @ 25 Mhz, PH=2WS, PM=5WS, BURST=1,2,1

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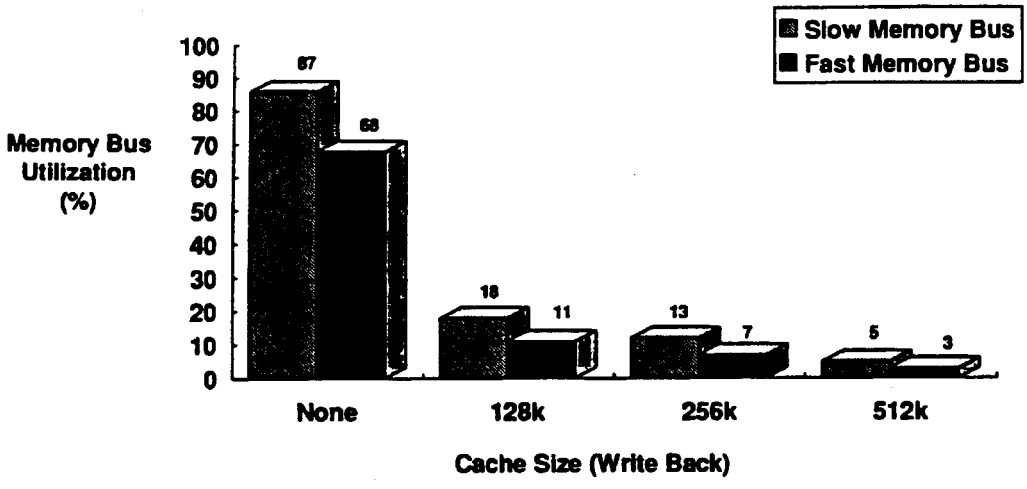
BUS UTILIZATION

Average Of 9 Program Traces: 6 Unix, 3 DOS Data From Performance Simulations



Fast Bus: Ph=1WS, Pm=4WS, Burst=1,1,1
Slow Bus: Ph=4WS, Pm=10WS, Burst=2,2,2

CONCLUSIONS

- **A High Performance Cache For The Intel486™ DX Was Presented**
- **It Offers**
  - **High Integration**
    Cache Controller,Dual-Ported-Intelligent-SRAM
  - **High Performance**
    50 Mhz, 2-Way-Cache, 0-WS
    TUNED CPU BUS
    MODULE READY
  - **Multi-Processing**
    Write-Back
    MESI Cache Consistency