CY7C9101

CMOS 16-Bit Slice

Features

- **Fast**
  - **— CY7C9101–30 has a 30-ns (max.) clock cycle (commercial)**
  - **— CY7C9101–35 has a 35-ns (max.) clock cycle (military)**
- **Low power**
  - **— I_{CC} (max. at 10 MHz) = 60 mA (commercial)**
  - **— I_{CC} (max. at 10 MHz) = 85 mA (military)**
- **V_{CC} margin of 5V ±10%**
- **All parameters guaranteed over commercial and military operating temperature range**
- **Replaces four 2901s with carry look-ahead logic**
- **Eight-function ALU performs three arithmetic and five logical operations on two 16-bit operands**
- **Infinitely expandable in 16-bit increments**
- **Four status flags: carry, overflow, negative, zero**
- **Capable of withstanding greater than 2001V static discharge voltage**
- **Pin compatible and functional equivalent to AM29C101**

Functional Description

The CY7C9101 is a high-speed, expandable, 16-bit-wide ALU slice that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C9101 is basic, yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C9101, as shown in the logic block diagram, consists of a 16-word by 16-bit dual-port RAM register file, a 16-bit ALU, and the necessary data manipulation and control logic.

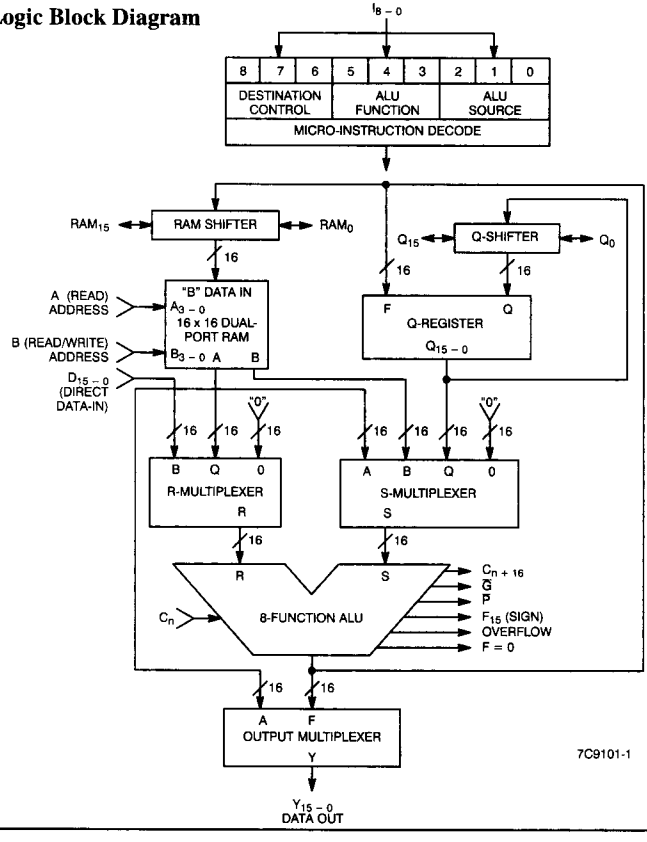
The function performed is determined by 9-bit instruction word (I_8 to I_0), which is usually input via a micro-instruction register.

The CY7C9101 is expandable in 16-bit increments, has three-state data outputs as well as flag outputs, and can implement either a full look-ahead carry or a ripple carry.

The CY7C9101 is a pin-compatible, functional equivalent for the Am29C101 with improved performance. The 7C9101 replaces four 2901s and includes on-chip carry look-ahead logic.

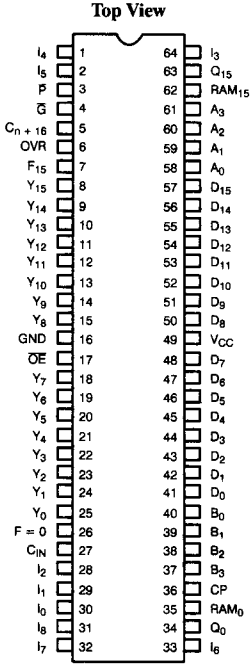
Fabricated in an advanced 1.2-micron CMOS process, the CY7C9101 eliminates latch-up, has ESD protection greater than 2000V, and achieves superior performance with low power dissipation.

Logic Block Diagram



Pin Configurations

Top View



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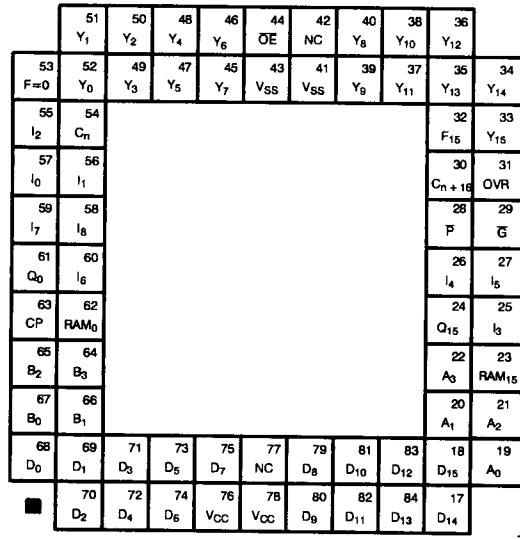
Pin Configurations (continued)

PGA
Top View



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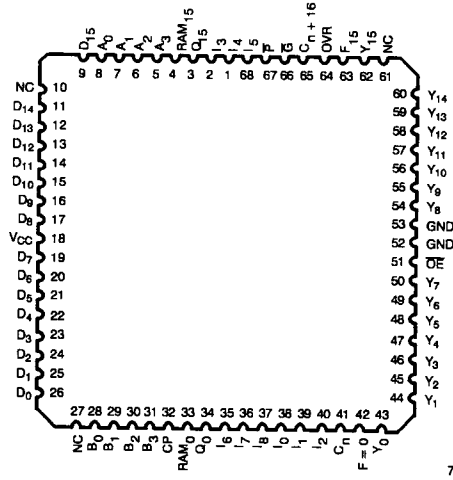
LCC/PLCC
Top View



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Selection Guide

		CY7C9101–30 CY7C9101–35	CY7C9101–40 CY7C9101–45
Minimum Clock Cycle (ns)	Commercial	30	40
	Military	35	45
Maximum Operating Current at 10 MHz (mA)	Commercial	60	60
	Military	85	85

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 30 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)

Latch-Up Current (Outputs) ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Note:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_3 - A_0$	I	RAM Address A. This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) A port.
$B_3 - B_0$	I	RAM Address B. This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) B port. When data is written back to the register file, this is the destination address.
$I_8 - I_0$	I	Instruction Word. This 9-bit word is decoded to determine the ALU data sources ($I_{0,1,2}$), the ALU operation ($I_{3,4,5}$), and the data to be written to the Q register or register file ($I_{6,7,8}$).
$D_{15} - D_0$	I	Direct Data Input. This 16-bit data word may be selected by the $I_{0,1,2}$ lines as an input to the ALU.
$Y_{15} - Y_0$	O	Data Output. These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latch, as determined by the code on the $I_{6,7,8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the $Y_{15} - Y_0$ outputs. A HIGH level on this signal places the output drivers at the high-impedance state.
CP	I	Clock. The LOW level of CP is used to write data to the RAM register file. A HIGH level of CP writes data from the dual-port RAM to the A and B latches. The operation of the Q register is similar; data is entered into the master latch on the LOW level of CP and transferred from master to slave during CP = HIGH.
Q_{15} RAM_{15}	I/O	These two lines are bidirectional and are controlled by $I_{6,7,8}$. They are three-state output drivers connected to the TTL-compatible CMOS inputs.
Q_{15} RAM_{15} (cont.)	I/O	Output Mode: When the destination code on lines $I_{6,7,8}$ indicates a left shift (UP) operation, the three-state outputs are enabled and the MSB of the Q register is output on the Q_{15} pin and likewise, the MSB of the ALU output (F_{15}) is output on the RAM_{15} pin. Input Mode: When the destination code indicates a right shift (DOWN), the pins are the data inputs to the MSB of the Q register and the MSB of the RAM, respectively.
Q_0 RAM_0	I/O	These two lines are bidirectional and function similarly to the Q_{15} and RAM_{15} lines. The Q_0 and RAM_0 lines are the LSB of the Q register and the RAM.
C_n	I	Carry In. The carry in to the internal ALU.
C_{n+16}	O	Carry Out. The carry out from the internal ALU.
$\overline{G}, \overline{P}$	O	Carry Generate, Carry Propagate. Outputs from the ALU that may be used to perform a carry look-ahead operation over the 16 bits of the ALU.
OVR	O	Overflow. This signal is the logical exclusive-OR of the carry in and the carry out of the MSB of the ALU. This indicates when the result of the ALU operation has exceeded the capacity of the ALU's two's complement number range.
F = 0	O	Zero Detect. Open drain output that goes HIGH when the data on outputs ($F_{15} - F_0$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic assumed).
F_{15}	O	Sign. The MSB of the ALU output.

Description of Architecture

General Description

The CY7C9101 general block diagram is shown on the first page of this datasheet, in the Logic Block Diagram section. Detailed block diagrams (*Figures 1* through *3*) show the operation of specific sections as described below. The device is a 16-bit slice consisting of a register file (16-word by 16-bit dual-port RAM), the ALU, the Q register, and the necessary control logic. It is expandable in 16-bit increments.

Register File

The dual-port RAM is addressed by two 4-bit address fields ($A_3 - A_0$, $B_3 - B_0$) that cause the data to simultaneously appear at the A or B (internal) ports. If the A and B addresses are the same, the data at the A and B ports will be identical.

Data to be written to RAM is applied to the D inputs of the 7C9101 and is passed (unchanged) through the ALU to the RAM location specified by the B-address word. New data is written into the RAM by specifying a B address while RAM write enable (RAM EN) is active and the clock input is LOW. RAM EN is an internal signal decoded from the signals $I_{6,7,8}$. As shown in *Figure 1*, each of the 16 RAM inputs is driven by a three-input multiplexer that allows the ALU output ($F_{15} - F_0$) to be shifted one bit position to the left or right, or not shifted at all. The RAM_{15} and RAM_0 I/O pins are also inputs to the 16-bit, 3-input multiplexer.

During the left-shift (upshift) operation, the RAM_{15} output buffer and RAM_0 input multiplexer are enabled. For the right-shift (downshift) operation, the RAM_0 output buffer and the RAM_{15} input multiplexer are enabled.

The A and B outputs of the RAM drive separate 16-bit latches that are enabled when the clock is HIGH. The outputs of the A latch go to the three multiplexers that feed the two ALU inputs ($R_{15} - R_0$ and $S_{15} - S_0$) and the chip output ($Y_{15} - Y_0$). The B latch outputs are directed to the multiplexer that feeds the S input to the ALU.

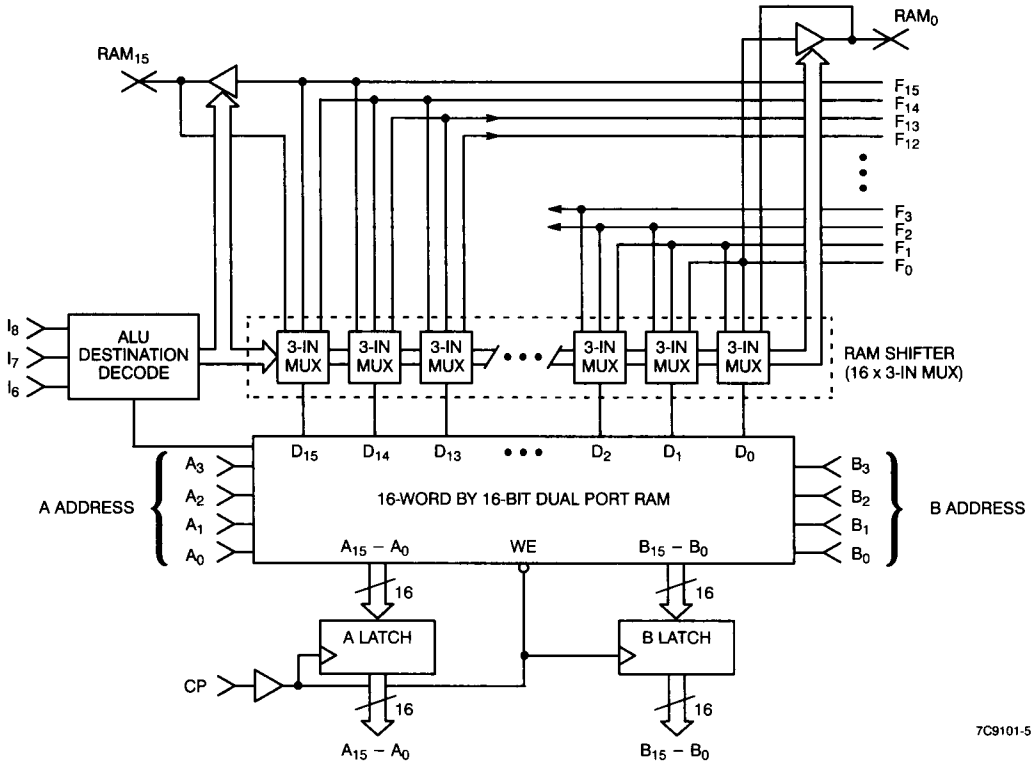


Figure 1. Register File

Description of Architecture (continued)

Q Register

The Q register is mainly intended for use as a separate working register for multiplication and division routines. It may also function as an accumulator or temporary storage register. Sixteen master-slave latches are used to implement the Q register. As shown in *Figure 2*, the Q-register inputs are driven by the outputs of the Q shifter (sixteen 3-input multiplexers, under the control of $I_{6,7,8}$). The function of the Q register input multiplexers is to allow the Q register to be shifted either left or right, or loaded with the ALU output ($F_{15} - F_0$). The Q_{15} and Q_0 pins (I/O) function similarly to the RAM_{15} and RAM_0 pins described earlier. Data is entered into the master latches when the clock is LOW and is transferred to the slave (output) at the clock LOW-to-HIGH transition.

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on the two 16-bit input operands, R and S. The R input multiplexer selects between data from the RAM A port and data at the external data input, $D_{15} - D_0$. The S input multiplexer selects between data from the RAM A port, the RAM B port, and the Q register. The R and S multiplexers are controlled by the $I_{0,1,2}$ inputs as shown in *Table 1*. The R and S input multiplexers each have an "inhibit capability," offering a state where no data is passed. This is equivalent to a source operand consisting of all zeros. The R and S ALU source multiplexers are configured to allow eight pairs of combinations of A, B, D, Q, and "0" to be selected as ALU input operands.

The ALU input functions, which are controlled by $I_{3,4,5}$, are shown in *Table 2*. Carry look-ahead logic is resident on the 7C9101, using the ALU carry in (C_n) input and the ALU carry propagate ($\overline{P}$), carry generate ($\overline{G}$), carry out (C_{n+16}), and overflow outputs to implement carry look-ahead arithmetic and determine if arithmetic overflow has occurred. Note that the carry in (C_n) signal affects the arithmetic result and internal flags only; it has no effect on the logical operations.

Control signals $I_{6,7,8}$ route the ALU data output ($F_{15} - F_0$) to the RAM, the Q register inputs, and the Y outputs as shown in *Table 3*. The ALU result MSB (F_{15}) is output so the user may examine the sign bit without needing to enable the three-state outputs. The F = 0 output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open drain output that may be wire ORed across multiple 7C9101 processor slices. *Figure 3* shows a block diagram of the ALU.

The ALU source operands and ALU function matrix are summarized in *Table 4* and separated by logic operation or arithmetic operation in *Tables 5* and *6*, respectively. The $I_{0,1,2}$ lines select eight pairs of source operands and the $I_{3,4,5}$ lines select the operation to be performed.

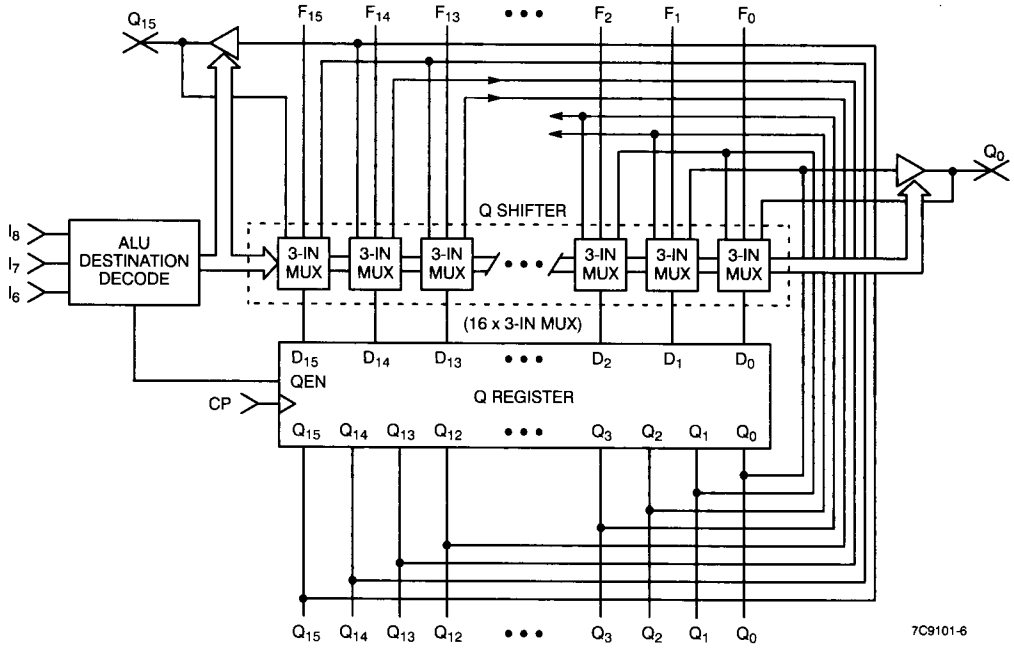


Figure 2. Q Register

Description of Architecture (continued)

Conventional Addition and Pass-Increment/Decrement

When the carry in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation. In logical operations, the carry in (C_n) will not affect the ALU output.

Subtraction

Recall that in two's complement integer coding − 1 is equal to all ones, and that in one's complement integer coding zero is equal to all ones. To convert a positive integer to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In *Table 6* the symbol − Q represents the two's complement of Q, so the one's complement of Q is then − Q − 1.

Table 1. ALU Source Operand Control

Mnemonic	Micro Code I_2	I_1	I_0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Table 2. ALU Function Control

Mnemonic	Micro Code I_5	I_4	I_3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
XOR	H	H	L	6	R XOR S	R ⊻ S
XNOR	H	H	H	7	R XNOR S	$\overline{R \veebar S}$

Table 3. ALU Destination Control

Mnemonic	Micro Code I_8	I_7	I_6	Octal Code	RAM Function Shift	Load	Q-Reg. Function Shift	Load	Y Output	RAM Shifter RAM_0	RAM_{15}	Q Shifter Q_0	Q_{15}
QREG	L	L	L	0	X	None	None	F ⇧ Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F ⇧ B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F ⇧ B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 ⇧ B	DOWN	Q/2 ⇧ Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2 ⇧ B	X	None	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F ⇧ B	UP	2Q ⇧ Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F ⇧ B	X	None	F	IN_0	F_{15}	X	Q_{15}

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output that is in the high-impedance state.
A = Register addressed by A inputs.
B = Register addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Description of Architecture (continued)

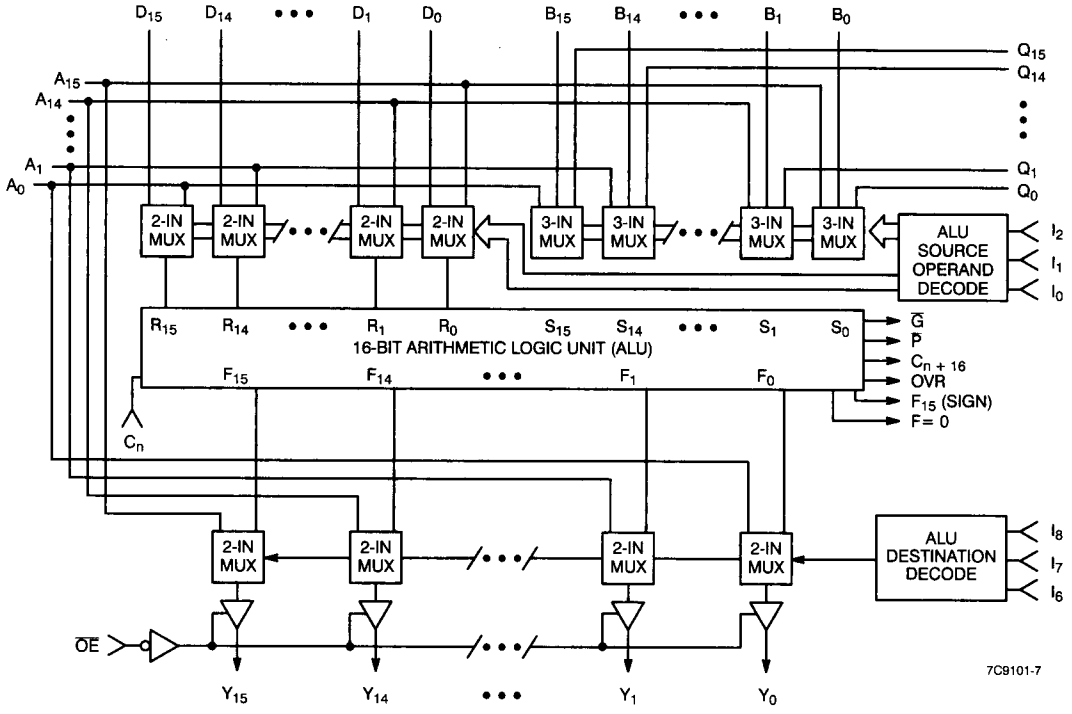


Figure 3. ALU

Table 4. Source Operand and ALU Function Matrix

Octal I_{543}	I_{210} Octal	0	1	2	3	4	5	6	7
	ALU Source	A	A	O	O	O	D	D	D
	ALU Function	Q	B	Q	B	A	A	Q	O
0	C_n = L R plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ⊻ Q	A ⊻ B	Q	B	A	D ⊻ A	D ⊻ Q	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ⊻ = EX-OR

Description of Architecture (continued)

Table 5. ALU Logic Mode Functions

Octal I_{543}, I_{210}	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee Q$
60	XOR	$A \veebar Q$
61		$A \veebar B$
65		$D \veebar A$
66		$D \veebar Q$
70	XNOR	$\overline{A \veebar Q}$
71		$\overline{A \veebar B}$
75		$\overline{D \veebar A}$
76		$\overline{D \veebar Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

Table 6. ALU Arithmetic Mode Functions

Octal I_{543}, I_{210}	C_n = 0 (LOW)		C_n = 1 (HIGH)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q − 1	PASS	Q
13		B − 1		B
14		A − 1		A
27		D − 1		D
22	1's Comp.	− Q − 1	2's Comp. (Negate)	− Q
23		− B − 1		− B
24		− A − 1		− A
17		− D − 1		− D
10	Subtract (1's Comp.)	Q − A − 1	Subtract (2's Comp.)	Q − A
11		B − A − 1		B − A
15		A − D − 1		A − D
16		Q − D − 1		Q − D
20		A − Q − 1		A − Q
21		A − B − 1		A − B
25		D − A − 1		D − A
26		D − Q − 1		D − Q

Electrical Characteristics Over Commercial and Military Operating Range[2]

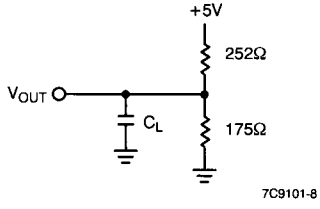
V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 3.4 mA All Outputs Except F = 0		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.		− 10	10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V All Outputs Except F = 0		− 3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V		16		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max.			+40	μA
		V_{OUT} = V_{SS} to V_{CC}		− 40		μA
I_{SC}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0V All Outputs Except F = 0			− 85	mA
$I_{CC}(Q_1)$[4]	Supply Current (Quiescent)	$V_{SS} \le V_{IN} \le V_{IL}$ or $V_{IH} \le V_{IN} \le V_{CC}$; $\overline{OE}$ = HIGH	Commercial		30	mA
			Military		35	mA
$I_{CC}(Q_2)$[4]	Supply Current (Quiescent)	$V_{SS} \le V_{IN} \le 0.4V$ or $3.85V \le V_{IN} \le V_{CC}$; $\overline{OE}$ = HIGH	Commercial		25	mA
			Military		30	mA
I_{CC}(Max.)[4]	Supply Current	V_{CC} = Max., f_{CLK} = 10 MHz; $\overline{OE}$ = HIGH	Commercial		60	mA
			Military		85	mA

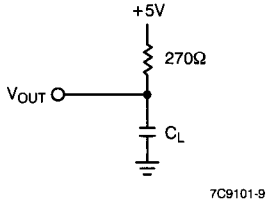
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Output Loads Used for AC Performance Characteristics[6, 7]



All Outputs Except Open Drain



Open Drain (F = 0)

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given frequency, use $I_{CC}(Q_1) + I_{CC}(AC)$ where $Icc(Q_1)$ is shown above and $I_{CC}(AC)$ = (3 mA/MHz) × Clock Frequency for the commercial temperature. $I_{CC}(AC)$ = (5 mA/MHz) × Clock Frequency for military temperature range.
5. Tested initially and after any design or process changes that may affect these parameters.
6. C_L = 50 pF includes scope probe, wiring, and stray capacitance.
7. C_L = 5 pF for output disable tests.

Table 7. Logic Functions for CARRY and OVERFLOW Conditions

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+16}	OVR
0	R + S	$\overline{P_0 - P_{15}}$	$\overline{G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_1 - P_{15}G_0}$	C_{16}	$C_{16} \veebar C_{15}$
1	S − R	◀ Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions ▶			
2	R − S	◀ Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions ▶			
3	$R \vee S$	HIGH	HIGH	LOW	LOW
4	$\overline{R \wedge S}$				
5	$\overline{R} \wedge S$				
6	$\overline{R \veebar S}$				
7	$R \veebar S$				

Definitions (+ = OR)

$P_0 - P_{15} = P_{15}P_{14}P_{13}P_{12}P_{11}P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$
$P_0 = R_0 + S_0$
$P_1 = R_1 + S_1$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$, etc.

$G_0 - G_{15} = G_{15}G_{14}G_{13}G_{12}G_{11}G_{10}G_9G_8G_7G_6G_5G_4G_3G_2G_1G_0$
$G_0 = R_0S_0$
$G_1 = R_1S_1$
$G_2 = R_2S_2$
$G_3 = R_3S_3$, etc.
$C_{16} = G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_0 - P_{15}C_n$
$C_{15} = G_{14} + P_{14}G_{13} + P_{14}P_{13}G_{12} + \ldots + P_0 - P_{14}C_n$

6 LOGIC

CY7C9101−30 and CY7C9101−40 Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the commercial (0°C to 70°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See the Electrical Characteristics section for loading circuit information.

This data applies to parts with the following numbers:
CY7C9101−30PC CY7C9101−30JC CY7C9101−30GC CY7C9101−40PC CY7C9101−40JC CY7C9101−40GC

Cycle Time and Clock Characteristics

CY7C9101	−30	−40
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	30 ns	40 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	33 MHz	25 MHz
Minimum Clock LOW Time	20 ns	25 ns
Minimum Clock HIGH Time	10 ns	15 ns
Minimum Clock Period	30 ns	40 ns

Combinatorial Propagation Delays (C_L = 50 pF)[8]

To Output	Y		F_{15}		C_{n+16}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0		Q_0	
From Input	Y		F_{15}		C_{n+16}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_{15}		Q_{15}	
Speed (ns)	30	40	30	40	30	40	30	40	30	40	30	40	30	40	30	40
A, B Address	37	47	36	47	35	44	32	41	35	46	32	42	32	40	—	—
D	29	34	28	34	25	32	25	30	29	36	21	26	27	33	—	—
C_n	22	27	22	27	20	25	—	—	22	26	22	26	24	30	—	—
I_{012}	32	40	32	40	30	38	28	36	34	42	26	32	27	35	—	—
I_{345}	34	43	33	42	33	42	27	35	34	40	32	42	29	38	—	—
I_{678}	19	22	—	—	—	—	—	—	—	—	—	—	22	26	22	26
A Bypass ALU (I = 2XX)	25	30	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock (LOW to HIGH)	31	40	30	39	30	38	27	34	28	37	34	34	27	35	20	23

Note:
8. A dash indicates a propagation delay path or set-up time constraint does not exist.

Set-Up and Hold Times Relative to Clock (CP) Input[8]

	CP: Set-Up Time Before H ⇂ L		Hold Time After H ⇂ L		Set-Up Time Before L ⇂ H		Hold Time After L ⇂ H	
Speed (ns)	30	40	30	40	30	40	30	40
A, B Source Address	10	15	3[9]	3[9]	30[10]	40[10]	0	0
B Destination Address	10	15	⇂ Do Not Change[11] ⇂				0	0
Data	—	—	—	—	22	28	0	0
C_n	—	—	—	—	16	22	0	0
$I_{0,1,2}$	—	—	—	—	26	35	0	0
$I_{3,4,5}$	—	—	—	—	29	37	0	0
$I_{6,7,8}$	10	12	⇂ Do Not Change[11] ⇂				0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	11	14	0	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101–30	$\overline{OE}$	Y	18	16
CY7C9101–40	$\overline{OE}$	Y	22	19

Notes:

9. Source addresses must be stable prior to the clock HIGH-to-LOW transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
10. The set-up time prior to the clock LOW-to-HIGH transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock LOW-to-HIGH transition, regardless of when the clock HIGH-to-LOW transition occurs.
11. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."

CY7C9101–35 and CY7C9101–45 Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the military (– 55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See the Electrical Characteristics section for loading circuit information.

This data applies to parts with the following numbers:
CY7C9101–35DMB CY7C9101–35LMB CY7C9101–35GMB
CY7C9101–45DMB CY7C9101–45LMB CY7C9101–45GMB

Cycle Time and Clock Characteristics[2]

CY7C9101	–35	–45
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	35 ns	45 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	28 MHz	22 MHz
Minimum Clock LOW Time	23 ns	28 ns
Minimum Clock HIGH Time	12 ns	17 ns
Minimum Clock Period	35 ns	45 ns

Combinatorial Propagation Delays (C_L = 50 pF)[2, 8]

To Output	Y		F_{15}		C_{n+16}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0		Q_0	
From Input	Y		F_{15}		C_{n+16}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_{15}		Q_{15}	
Speed (ns)	35	45	35	45	35	45	35	45	35	45	35	45	35	45	35	45
A, B Address	41	52	40	51	38	48	37	45	40	48	36	46	36	43	—	—
D	31	37	31	36	29	36	28	32	33	40	23	32	30	35	—	—
C_n	25	30	24	29	23	27	—	—	24	29	23	27	26	31	—	—
I_{012}	36	44	35	43	33	41	31	38	38	46	29	38	30	38	—	—
I_{345}	38	48	37	47	37	46	31	38	38	45	36	45	33	41	—	—
I_{678}	21	24	—	—	—	—	—	—	—	—	—	—	24	28	24	28
A Bypass ALU (I = 2XX)	28	33	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock (LOW to HIGH)	35	44	34	43	34	42	30	37	34	40	28	38	30	37	21	25

Set-Up and Hold Times Relative to Clock (CP) Input[2, 8]

	CP:							
	Set-Up Time Before H ⧫ L		Hold Time After H ⧫ L		Set-Up Time Before L ⧫ H		Hold Time After L ⧫ H	
Speed (ns)	35	45	35	45	35	45	35	45
A, B Source Address	12	17	3[9]	3[9]	35[10]	45[10]	0	0
B Destination Address	12	17	⧫ Do Not Change[11] ⧫				1	1
D	—	—	—	—	25	30	0	0
C_n	—	—	—	—	19	24	0	0
I_{012}	—	—	—	—	30	37	0	0
I_{345}	—	—	—	—	33	40	0	0
I_{678}	12	16	⧫ Do Not Change[11] ⧫				0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	13	15	1	1

Output Enable/Disable Times[2]

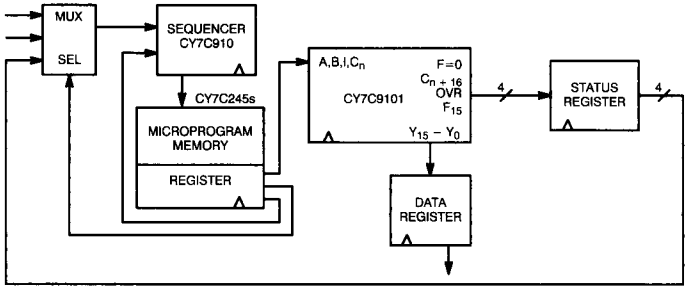
Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101–35	$\overline{OE}$	Y	20	17
CY7C9101–45	$\overline{OE}$	Y	23	20

Applications

Minimum Cycle Time Calculations for 16-Bit Systems

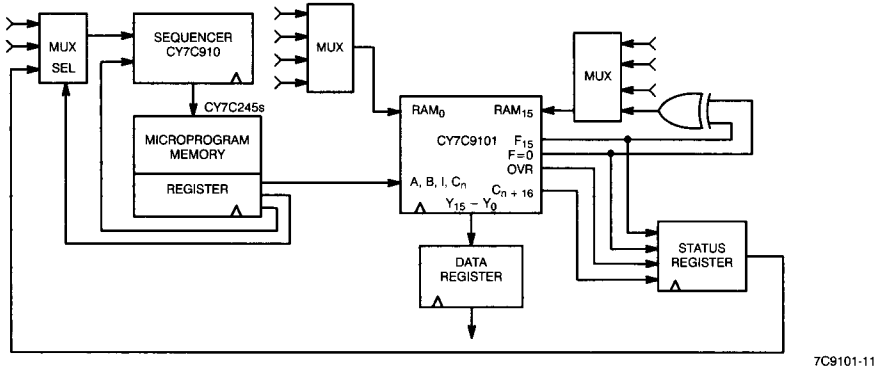
Speed used in calculations for parts other than CY7C9101 and CY7C910 are representative for available MSI parts.



Pipelined System, Add Without Simultaneous Shift

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
Register	Set-Up	4	CY7C910	CC to Output	22
		53 ns	CY7C245	Access Time	20
					66 ns

Minimum Clock Period = 66 ns



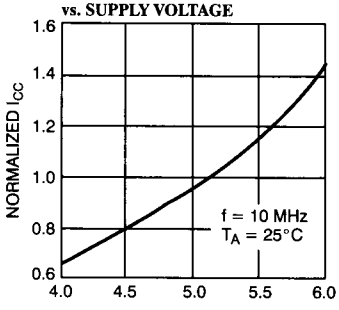
Pipelined System, Simultaneous Add and Shift Down (Right)

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C9101	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
XOR and MUX	Prop. Delay, Select to Output	20	CY7C910	CC to Output	22
			CY7C245	Access Time	20
CY7C9101	RAM_{15} Set-Up	11			66 ns
		80 ns			

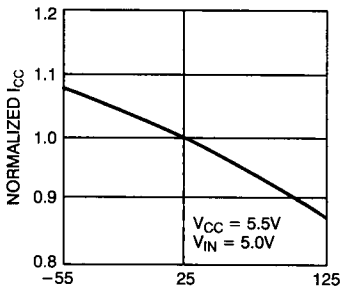
Minimum Clock Period = 80 ns

Typical DC and AC Characteristics

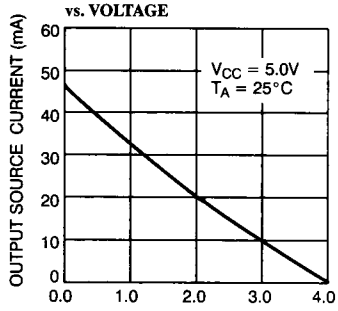
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



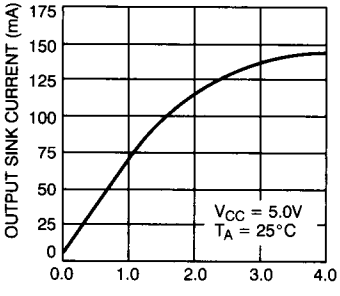
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



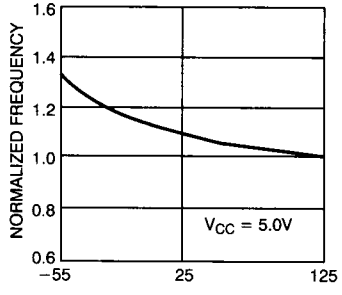
OUTPUT SOURCE CURRENT vs. VOLTAGE



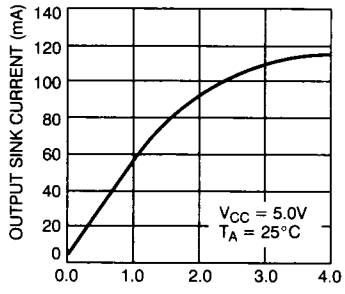
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



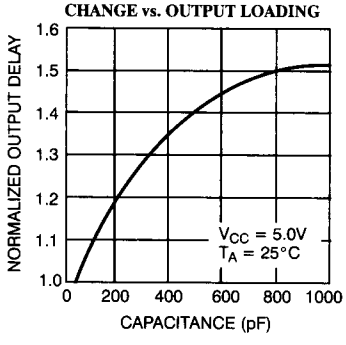
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



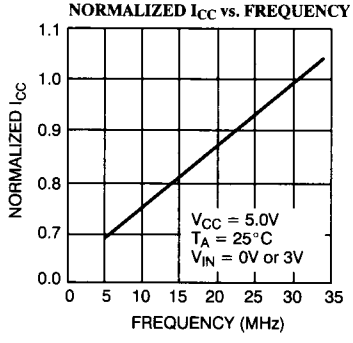
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL OUTPUT DELAY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



7C9101-12

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C9101-30GC	G68	68-Pin PGA (Cavity Down)	Commercial
	CY7C9101-30JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C9101-30PC	P29	64-Lead (900-Mil) Molded DIP	
35	CY7C9101-35DMB	D30	64-Lead (900-Mil) Bottombraze	Military
	CY7C9101-35GMB	G68	68-Pin PGA (Cavity Down)	
	CY7C9101-35LMB	L81	68-Square Leadless Chip Carrier	
40	CY7C9101-40GC	G68	68-Pin PGA (Cavity Down)	Commercial
	CY7C9101-40JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C9101-40PC	P29	64-Lead (900-Mil) Molded DIP	
45	CY7C9101-45DMB	D30	64-Lead (900-Mil) Bottombraze	Military
	CY7C9101-45GMB	G68	68-Pin PGA (Cavity Down)	
	CY7C9101-45LMB	L81	68-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{SC}	1, 2, 3
$I_{CC}(Q_1)$	1, 2, 3
$I_{CC}(Q_2)$	1, 2, 3
I_{CC}(Max.)	1, 2, 3

Combinational Propagation Delays

Parameter	Subgroups
From A, B Address to Y	7, 8, 9, 10, 11
From A, B Address to F_{15}	7, 8, 9, 10, 11
From A, B Address to C_{n+16}	7, 8, 9, 10, 11
From A, B Address to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From A, B Address to F = 0	7, 8, 9, 10, 11
From A, B Address to OVR	7, 8, 9, 10, 11
From A, B Address to $RAM_{0,15}$	7, 8, 9, 10, 11
From D to Y	7, 8, 9, 10, 11
From D to F_{15}	7, 8, 9, 10, 11
From D to C_{n+16}	7, 8, 9, 10, 11
From D to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From D to F = 0	7, 8, 9, 10, 11
From D to OVR	7, 8, 9, 10, 11
From D to $RAM_{0,15}$	7, 8, 9, 10, 11
From C_n to Y	7, 8, 9, 10, 11
From C_n to F_{15}	7, 8, 9, 10, 11
From C_n to C_{n+16}	7, 8, 9, 10, 11

Combinational Propagation Delays (continued)

Parameter	Subgroups
From C_n to F = 0	7, 8, 9, 10, 11
From C_n to OVR	7, 8, 9, 10, 11
From C_n to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{0,1,2}$ to Y	7, 8, 9, 10, 11
From $I_{0,1,2}$ to F_{15}	7, 8, 9, 10, 11
From $I_{0,1,2}$ to C_{n+16}	7, 8, 9, 10, 11
From $I_{0,1,2}$ to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From $I_{0,1,2}$ to F = 0	7, 8, 9, 10, 11
From $I_{0,1,2}$ to OVR	7, 8, 9, 10, 11
From $I_{0,1,2}$ to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{3,4,5}$ to Y	7, 8, 9, 10, 11
From $I_{3,4,5}$ to F_{15}	7, 8, 9, 10, 11
From $I_{3,4,5}$ to C_{n+16}	7, 8, 9, 10, 11
From $I_{3,4,5}$ to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From $I_{3,4,5}$ to F = 0	7, 8, 9, 10, 11
From $I_{3,4,5}$ to OVR	7, 8, 9, 10, 11
From $I_{3,4,5}$ to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{6,7,8}$ to Y	7, 8, 9, 10, 11
From $I_{6,7,8}$ to $RAM_{0,15}$	7, 8, 9, 10, 11
From $I_{6,7,8}$ to $Q_{0,15}$	7, 8, 9, 10, 11
From A Bypass ALU to Y (I = 2XX)	7, 8, 9, 10, 11
From Clock LOW to HIGH to Y	7, 8, 9, 10, 11
From Clock LOW to HIGH to F_{15}	7, 8, 9, 10, 11
From Clock LOW to HIGH to C_{n+16}	7, 8, 9, 10, 11
From Clock LOW to HIGH to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to F = 0	7, 8, 9, 10, 11
From Clock LOW to HIGH to OVR	7, 8, 9, 10, 11
From Clock LOW to HIGH to $RAM_{0,15}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to $Q_{0,15}$	7, 8, 9, 10, 11

Set-Up and Hold Times Relative to Clock (CP) Input

Parameter	Subgroups
A, B Source Address Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
A, B Source Address Hold Time After H ⧫ L	7, 8, 9, 10, 11
A, B Source Address Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
A, B Source Address Hold Time After L ⧫ H	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
B Destination Address Hold Time After H ⧫ L	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
B Destination Address Hold Time After L ⧫ H	7, 8, 9, 10, 11
D Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
D Hold Time After L ⧫ H	7, 8, 9, 10, 11
C_n Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
C_n Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{012} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{012} Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{345} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{345} Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{678} Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
I_{678} Hold Time After H ⧫ L	7, 8, 9, 10, 11
I_{678} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{678} Hold Time After L ⧫ H	7, 8, 9, 10, 11
RAM_0, RAM_{15}, Q_0, Q_{15} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
RAM_0, RAM_{15}, Q_0, Q_{15} Hold Time After L ⧫ H	7, 8, 9, 10, 11

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