National Semiconductor

DP802513
TROPIC™ MEMCS_16 Signal Decoder

General Description

The DP802511, DP802512 and DP802513 form the majority of the MEMCS_16 circuitry that is responsible for notifying the ISA bus (by way of MEMCS_16) that it can execute 16-bit bus transfers with the DP8025 TROPIC.

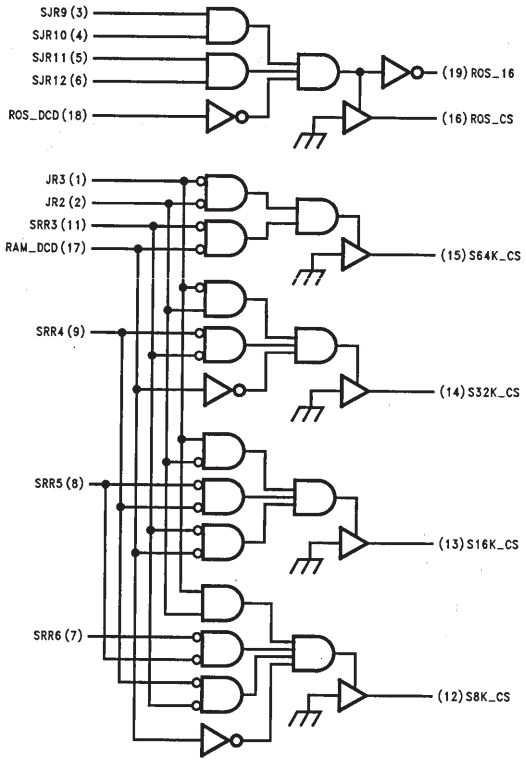
The areas of the architecture that will benefit most from the increased performance of 16-bit transfers are the shared memory interface and the host boot ROM (if so designed). For the boot ROM it is a relatively simple matter of matching the jumpered configuration bits SD9–SD15 (BIOS/MMIO base address) with the system address (SA) lines. The MEMCS_16 signal's maximum propagation delay from the SA lines is about 25 ns (assuming 8 MHz IBM® PC-AT®).

The shared memory interface RAM size is determined by jumper bits SD2 and SD3. These indicate the block size decoded to the shared memory MEMCS_16 circuitry. The address of this shared memory interface is software selectable. In order for the hardware to respond to the proper memory address it must shadow the RAM Relocation Register of the TROPIC's memory mapped I/O space. The data programmed into the RAM Relocation Register is latched into this shadowing register and used in conjuction with the system address lines to determine which address range contains the shared memory interface.

Features

- High speed: t_{PD} = 7.0 ns (max)
- Single chip custom logic solution
- Replaces glue logic

Logic Diagram



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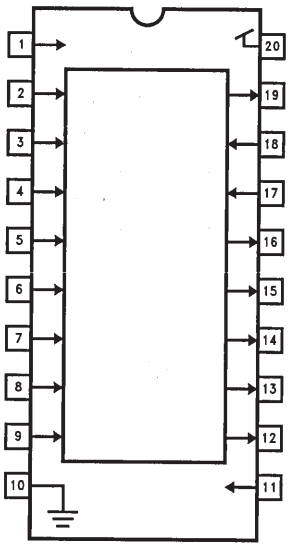
Block Diagram



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Functional Description

The DP802513 TROPIC MEMCS_16 Signal Decoder is manufactured using National's high speed ASPECT II bipolar TTL process and provides further decode of a 128k block decode for generation of the MEMCS_16 signal on the ISA bus. The ROS_CS (Read Only Storage) signal is a decode of an 8k boundary that is wire-ORed externally with the four RAM decode outputs. The ROS_16 signal is an identical decode as for ROS_CS above, except that it is not wire-ORed to the MEMCS_16 signal. Its purpose is to notify the RAM relocation register strobe circuitry (DP802511) that the required address (1E00) is in the ROM address area.

Depending upon the position of the jumpers JR02 and JR03, for user selectable shared RAM size, the device provides a decode of either 8k, 16k, 32k or 64k for MEMCS_16 generation. These signals are all output enabled and wire-ORed.

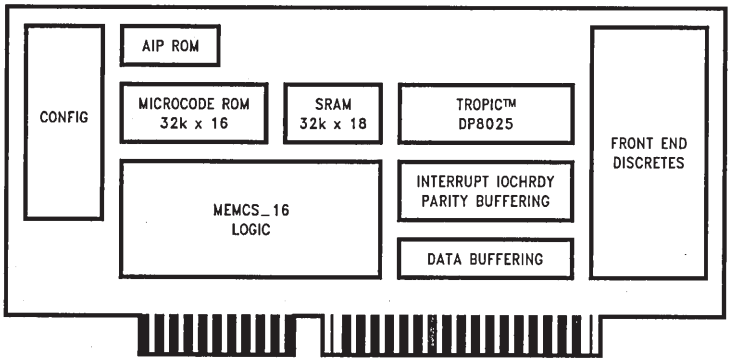

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FIGURE 1. TROPIC 16-Bit ISA Token Ring Workstation Adapter

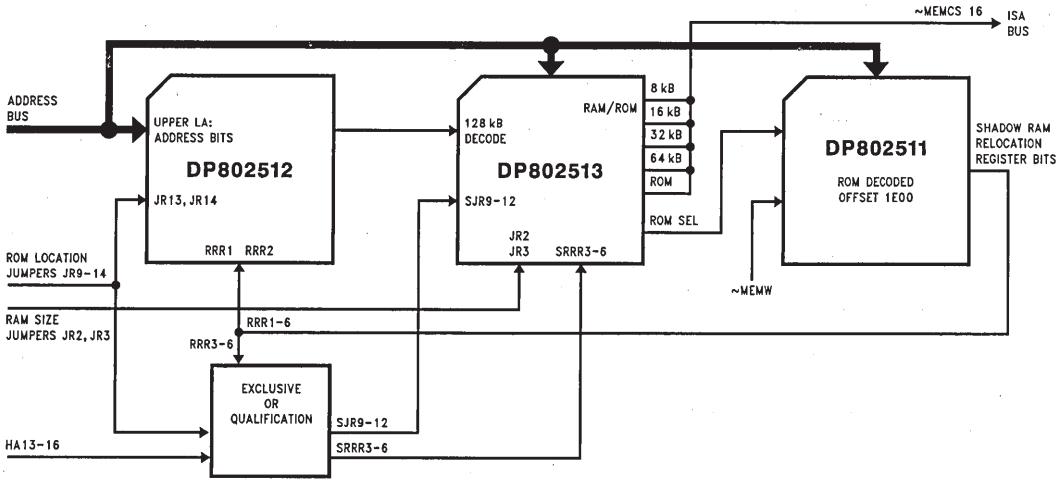

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FIGURE 2. MEMCS_16 Logic

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
Input Voltage	−1.5V to V_{CC} + 7.0V
Off-State Output Voltage (V_O) (Note 2)	−1.5V to V_{CC} + 5.5V
Input Current	−10.0 mA to +5.0 mA
Output Current (I_{OL})	100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

Symbol	Parameter	Commercial			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	0	25	75	°C

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 3)				0.8	V
V_{IH}	High Level Input Voltage (Note 3)		2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA			−1.2	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 24 mA			0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OL} = −3.2 mA	2.7			V
I_{OZL}	Low Level Off State Output Current	V_{CC} = Max, V_O = 0.4V			−50	μA
I_{OZH}	High Level Off State Output Current	V_{CC} = Max, V_O = 2.4V			50	μA
I_{OS}	Output Short Circuit Current (Note 4)	V_{CC} = 5V, V_O = 0V	−50		−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Output Open		125	180	mA
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V		8		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V		8		pF

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: V_O must not exceed V_{CC} + 1V.

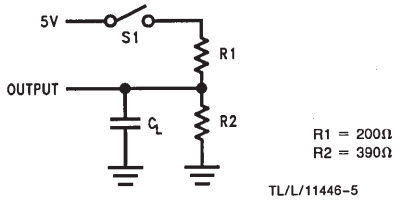
Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 4: To avoid invalid readings in other parameter tests it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Commercial			Units
			Min	Typ	Max	
t_{PD}	Input to Output	C_L = 50 pF, S1 Closed			7.0	ns
t_{PZXI}	Input to Output Enabled via Control Logic	C_L = 50 pF, Active High: S1 Open Active Low: S1 Closed	3.0		7.0	ns
t_{PXZI}	Input to Output Disabled via Control Logic	C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed	3.0		7.0	ns

Test Load



R1 = 200Ω
R2 = 390Ω

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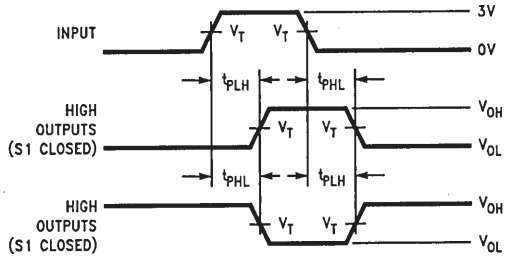
Test Waveforms

Propagation Delay



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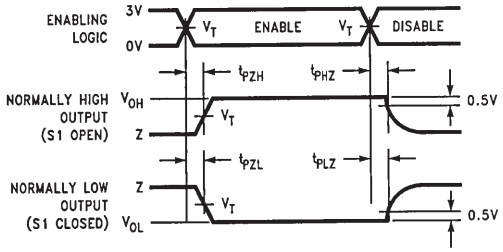
Enable and Disable



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