i960® Microprocessor

Performance Brief

October 1998

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1.0 Introduction

This report describes the results of performance benchmarks for the Intel® i960® microprocessor family. The benchmark results were obtained from Intel's web-based Remote Evaluation Facility (REF) located at the following URL:

- http://developer.intel.com/design/i960/testcntr/

The REF site allows users to evaluate the i960 processor family using provided benchmarks. Users can also download application-specific benchmark programs. The REF is a protected web site that allows the establishment of specific user accounts.

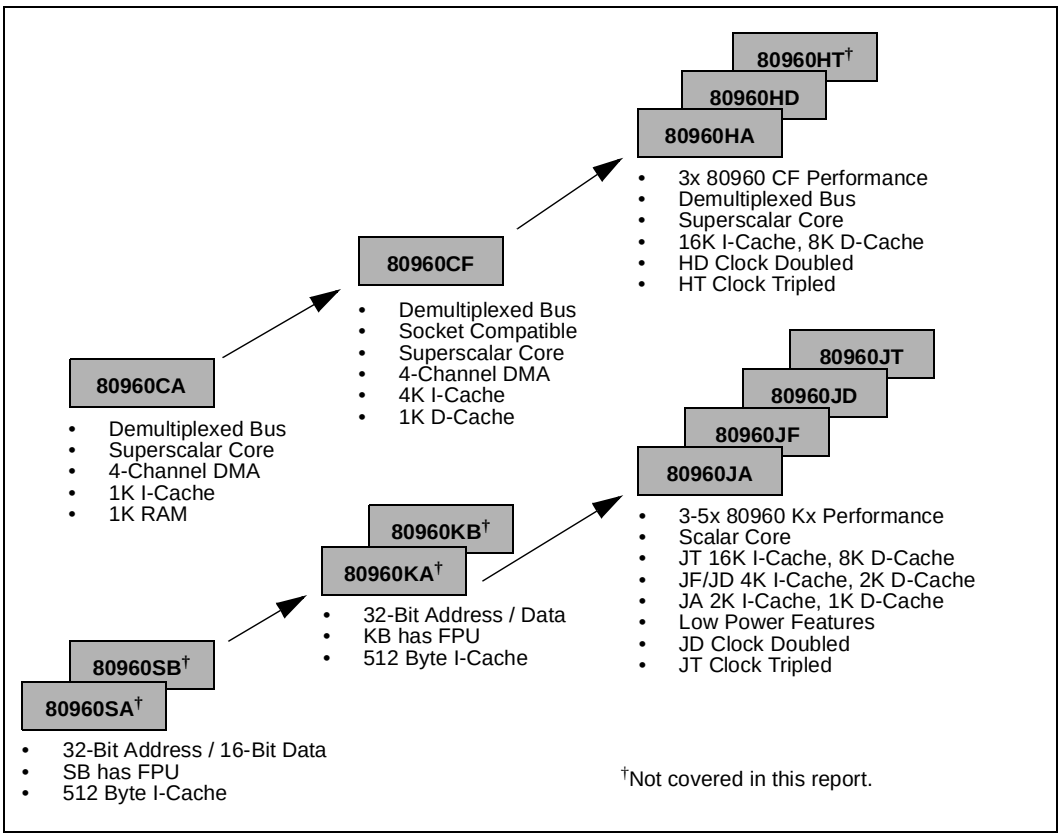
The benchmark results in this report are indicators only and should not be the sole deciding factor in microprocessor selection. The performance benefits described in this report are not guaranteed for any particular implementation of an i960 microprocessor in an embedded application. The results published in this report were obtained using Cyclone evaluation platforms for the i960 processor. The results should not be compared with other published microprocessor performance measurements. Variations in microprocessor platforms can significantly impact the results of performance benchmarks.

The i960 microprocessors covered in this report are:

- 80960CA, 80960CF, 80960JA, 80960JF, 80960JD, 80960JT, 80960HA, and 80960HD.

Figure 1 compares the features of the members of the i960 microprocessor family.

Figure 1. i960® Family Features Comparison

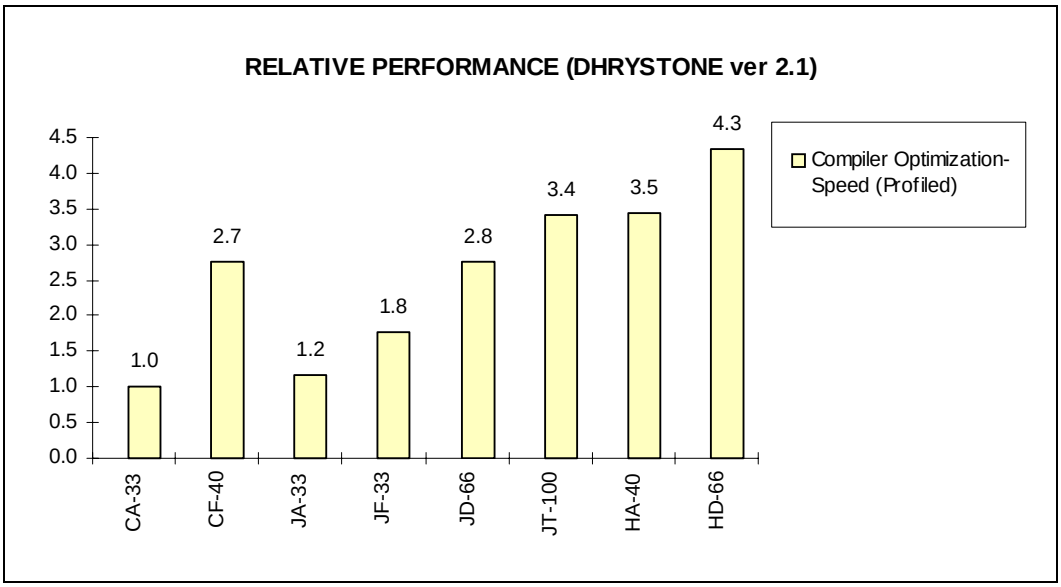


The basis of the comparison is a set of synthetic benchmark programs executed on all i960 microprocessors.

Why synthetic benchmarks? The best indicator of performance is obtained using a customer's own benchmark program or, in the absence of that, resembling the actual application. Developing a benchmark, however, takes time and money and may not be feasible for all customers. Also, a customer who is considering microprocessor performance may not have completed development of an application program. Due to these constraints, developers may use synthetic benchmarks as one indicator of microprocessor performance. The results of synthetic benchmark performance should not be the sole factor in selecting a microprocessor.

Benchmark data in this report is presented using simple bar charts. Figure 2 provides an example that shows the relative performance of various i960 microprocessors.

Figure 2. Relative Performance of i960® Microprocessors (not frequency normalized)



The programs used in this report were selected based on their general acceptance and well-known behavior, and because they are written in the C programming language. Each was chosen to provide an approximate, relative measurement of the performance of the microprocessor/compiler combination.

The benchmark programs used include Dhrystone*, Dhrystone MIPS, Single Precision Whetstone*, and Double Precision Whetstone.

2.0 i960® Microprocessor REF Product Highlights

Intel's web-based Remote Evaluation Facility (REF) is located at the following URL:

http://developer.intel.com/design/i960/testcntr/

i960 processor REF product highlights include:

- Private, password-protected accounts for storing your source files
- Easy-to-use Web interface
- Allows executing code on any of the following i960 processors: SA, SB, KA, KB, CA, CF, JA, JD, JF, JT, HA, HD
- 80960 processor speeds benchmarked in this report are as follows:
  - HD-66 - 33 MHz external clock, 66 MHz core clock
  - HA-40 - 40 MHz external clock, 40 MHz core clock
  - JT-100 - 33 MHz external clock, 100 MHz core clock
  - JD-66 - 33 MHz external clock, 66 MHz core clock
  - JF-33 - 33 MHz external clock, 33 MHz core clock
  - JA-33 - 33 MHz external clock, 33 MHz core clock
  - CF-40 - 40 MHz external clock, 40 MHz core clock
  - CA-33 - 33 MHz external clock, 33 MHz core clock
- Benchmark programs provided as example projects include:
  - Dhrystone
  - Single Precision Whetstone
  - Double Precision Whetstone
- Source file compilation using the Intel CTOOLS Development Suite
- CTOOL compiler supports C and C++ programming language
- Easy-to-use timers for measuring the speed of your programs and subroutines or timing your critical code sections
- Three levels of optimization are available for compiling code (NONE, SPEED, and SIZE)
- Links to on-line manuals for CTOOLS and processors

3.0 Methodology

There are several choices in memory technology when designing a microprocessor memory subsystem. DRAM is the predominant read/write memory technology. ROM, Flash, and EPROM are predominant technologies for read-only (or read-mostly) memory subsystems. SRAM subsystems may be expensive beyond practicality, as code and data size of applications continue to grow beyond 1 Mbyte.

The system designer must work within the bounds of these available memory technologies. For example, if a system designer must use 60 ns DRAM technology, the relevant question of performance is: How fast can the microprocessor execute using 60 ns DRAM?

A 32-bit microprocessor memory subsystem typically resembles one of the three subsystems described in Table 1.

Table 1. Typical 32-bit Microprocessor Memory Systems

Cost	Performance	Code Size	Description
High	High	Small to Moderate	Code and data are located in fast SRAM. SRAM provides access times on the order of 10 - 35 ns. Not a common design, but relatively simple to implement. Practical for applications that have little code and are not cost-sensitive.
Moderate	Moderate to High	Moderate to Large	Code and data are located in DRAM. The code and initialized data are loaded from a backplane bus or inexpensive ROM at initialization. Mainstream, inexpensive DRAM technology typically provides 60 to 70 ns access time and fast page mode access capability. The system designer can trade off interface cost and performance using different degrees of complexity such as burst mode support and interleaving. Performance may also be enhanced in these systems with a small, fast SRAM dedicated to frequently accessed data.
Low	Low to Moderate	Large	Code is executed from ROM. Data is located in DRAM. The system designer can increase performance by interleaving the ROM subsystem. Because this design is driven by low cost, a DRAM subsystem is typically implemented at the lowest possible cost.

Microprocessor performance is influenced by several elements; these are categorized below as either intrinsic or extrinsic:

- Intrinsic elements generally are not or cannot be varied for performance analysis purposes. These properties are inherent to the microprocessor:
  - — Architecture and internal implementation (e.g., cache size, instruction set, registers)
  - — Efficiency of the external memory interface (e.g., instruction fetch bandwidth)
  - — Compiler efficiency (assuming that the best compiler is selected with the highest optimization enabled)
- Extrinsic elements can be varied depending on application requirements, performance, and cost constraints:
  - — Clock speed
  - — Bus bandwidth (memory wait states)

Because many factors influence microprocessor performance, it is necessary to choose an equitable reference or baseline for a fair performance comparison. For this performance report, memory technology and clock speed are used as the common reference for measuring the performance of widely available industry benchmark programs.

4.0 Benchmark Programs

Table 2. Benchmark Program Descriptions

Program	Description	Units of Measure
Dhrystone	Tests integer performance. String manipulation is a common action in this program. Version 2.1 is used here.	Thousands of Dhrystones per second
Dhrystone MIPS	Measures instructions per second, based on Dhrystone v 2.1	Millions of instructions per second
Whetstone	Measure of floating-point performance. Includes single and double precision floating-point performance.	Millions of Whetstones per second

5.0 Development Workstation/Operating System

- Host: NCR S26 personal computer with a Pentium® Pro processor at 200 MHz
- OS: Windows* NT 4.0 Service Pack 3
- Memory: 130 Mbytes
- Hard disk size: 2 Gbytes
- Video: ATI Mach64*, 1 Mbyte memory

Note: The host and operating system specified above do not influence the performance benchmarks contained in this report. The platform and operating system are used to execute the GNU compiler, download code to the 80960 evaluation boards, and store results of each benchmark run.

5.1 Compiler/Assembler/Linker

The software used to compile the benchmark code for this report is the GNU960 v6.0.6

The compiler optimizations used for the web-based i960 Remote Evaluation Facility include the NONE, SIZE, and SPEED options. These options are used to define the neccesary compiler optimization switches, as follows:

- NONE: No compiler optimizations, the -O0 option
- SIZE: For non-profiling, the -O4 option
- SPEED: For profiling, the two pass compile option (provides program-wide optimization)

Refer to the *iC960 Compiler User's Guide* (order number 651230) for further details on optimization options.

5.2 Target Hardware

All performance numbers were obtained using a Cyclone Evaluation Platform (Cyclone EP) From Cyclone Microsystems with 8 Mbyte of 60 ns interleaved DRAM

The Cyclone EP is a stand-alone, general purpose evaluation and development tool for Intel's family of i960 embedded processors. The main board provides the capability to install one of several i960 microprocessor modules. A design engineer can install different CPU modules to evaluate the various i960 microprocessors in one system environment. This type of environment is desirable when evaluating CPU performance.

Further information on 80960 Cyclone Evaluation Platforms can be found at the following URLs:

- http://www.cyclone.com/
- http://support.intel.com/support/processors/i960/evalboards/eval_faq.htm

5.3 Memory Interface Configurations

These DRAM access times are specific to the 80960 Cyclone Evaluation Platform. Table 3 was obtained from the *Cyclone i960® Microprocessor Evaluation Platform User's Guide* (order number 272577).

Table 3. DRAM Access Times

Frequency (MHz)	Operation	DRAM Speed (ns)	Clock Cycles	Wait States (x1,x2,x3,x4)	Sustained Bandwidth[1] (Mbytes/sec)
16	Read	60, 70	3,1,1,1	1,0,0,0	36
20	Read	60, 70	3,1,1,1	1,0,0,0	45
25	Read	60	3,1,1,1	1,0,0,0	66
25	Read	70	4,1,1,1,1[2]	2,0,0,0	50
33	Read	60, 70	4,1,1,1,1[2]	2,0,0,0	66
40	Read	60	4,1,1,1,1[2]	2,0,0,0	80
40	Read	70	5,2,2,2,1[2]	3,1,1,1	53
16	Write	60, 70	3,2,2,2	1,1,1,1	25.6
20	Write	60, 70	3,2,2,2	1,1,1,1	32
25	Write	60	3,2,2,2	1,1,1,1	44.5
25	Write	70	4,2,2,2,1[2]	2,1,1,1	36
33	Write	60, 70	4,2,2,2,1[2]	2,1,1,1	48
40	Write	60	4,2,2,2,1[2]	2,1,1,1	58
40	Write	70	4,2,2,2,1[2]	2,1,1,1	53

NOTES:
1. Bandwidths stated are sustained bandwidths, not peak.
2. The extra cycle is the overhead of DRAM precharge. DRAM precharge time impacts back-to-back cycles only.

6.0 Relative Performance of the 80960 Microprocessor Family

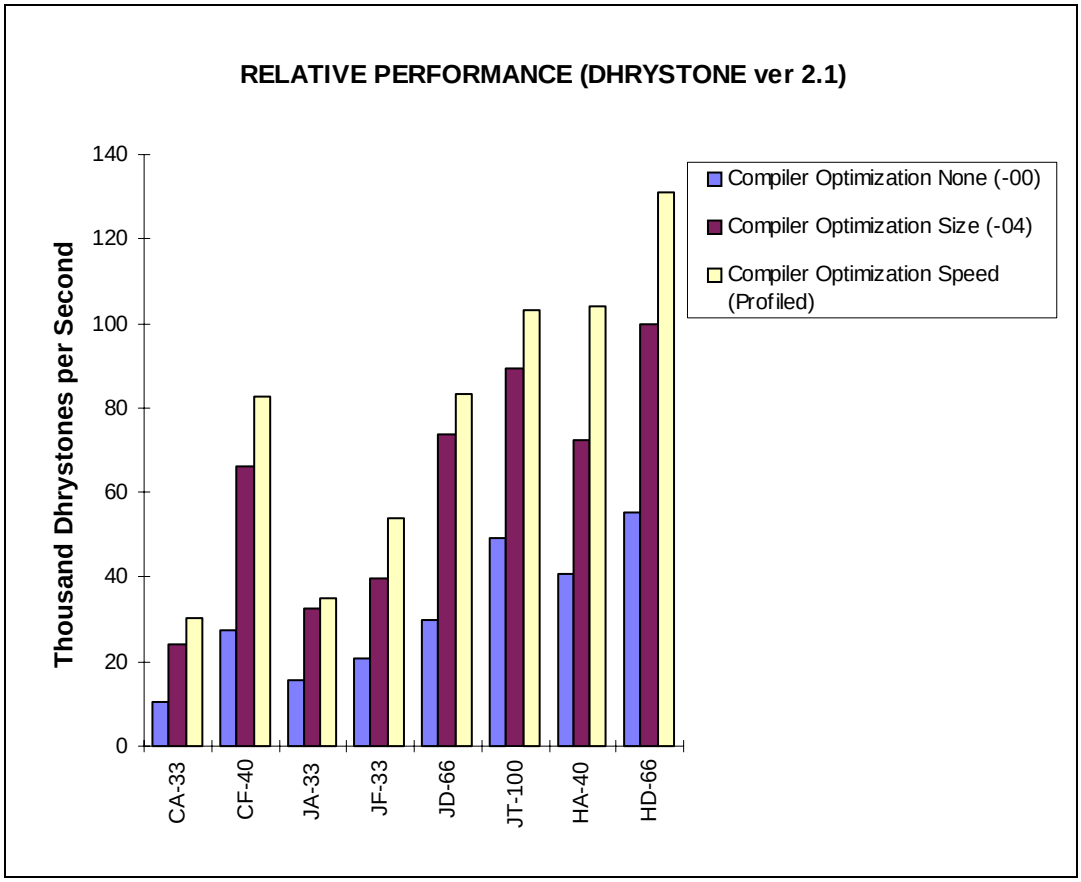
Note: These results are not frequency normalized.

The following graphs show the relative performance of the i960 microprocessor family.

6.1 Dhrystone Version 2.1

Memory:	Interleaved 60 ns DRAM	
Wait State Profile:	16/20/25 MHz:	10111
	33/40 MHz:	20121
Unit of Measure:	Thousand/Second	(Larger is better)

Figure 3. Dhrystone Version 2.1 Performance

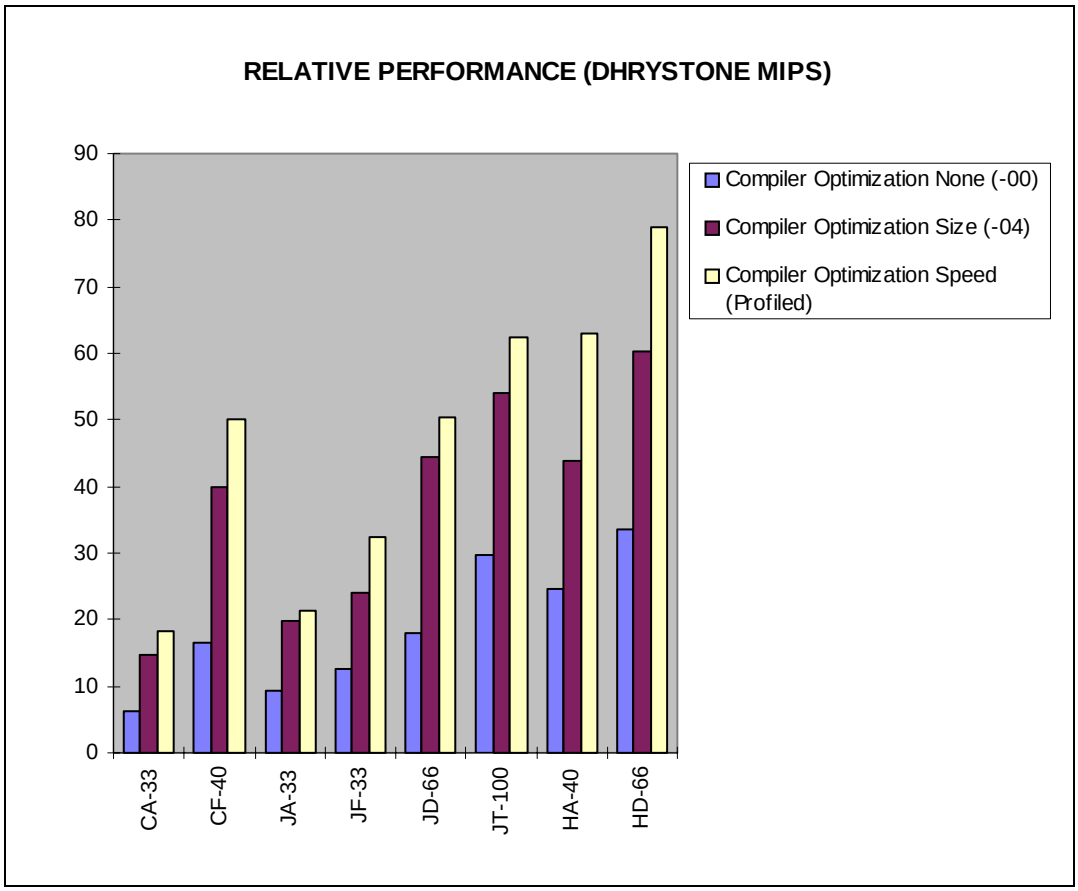


6.2 Dhrystone MIPS

Memory:	Interleaved 60 ns DRAM	
Wait State Profile:	16/20/25 MHz:	10111
	33/40 MHz:	20121
Unit of Measure:	MIPS	(Larger is better)

Note: MIPS performance numbers are extrapolated from Dhrystone v 2.1 performance numbers and supplied for indication only. Dhrystone MIPS = Dhystones per second (ver 2.1) divided by 1657.

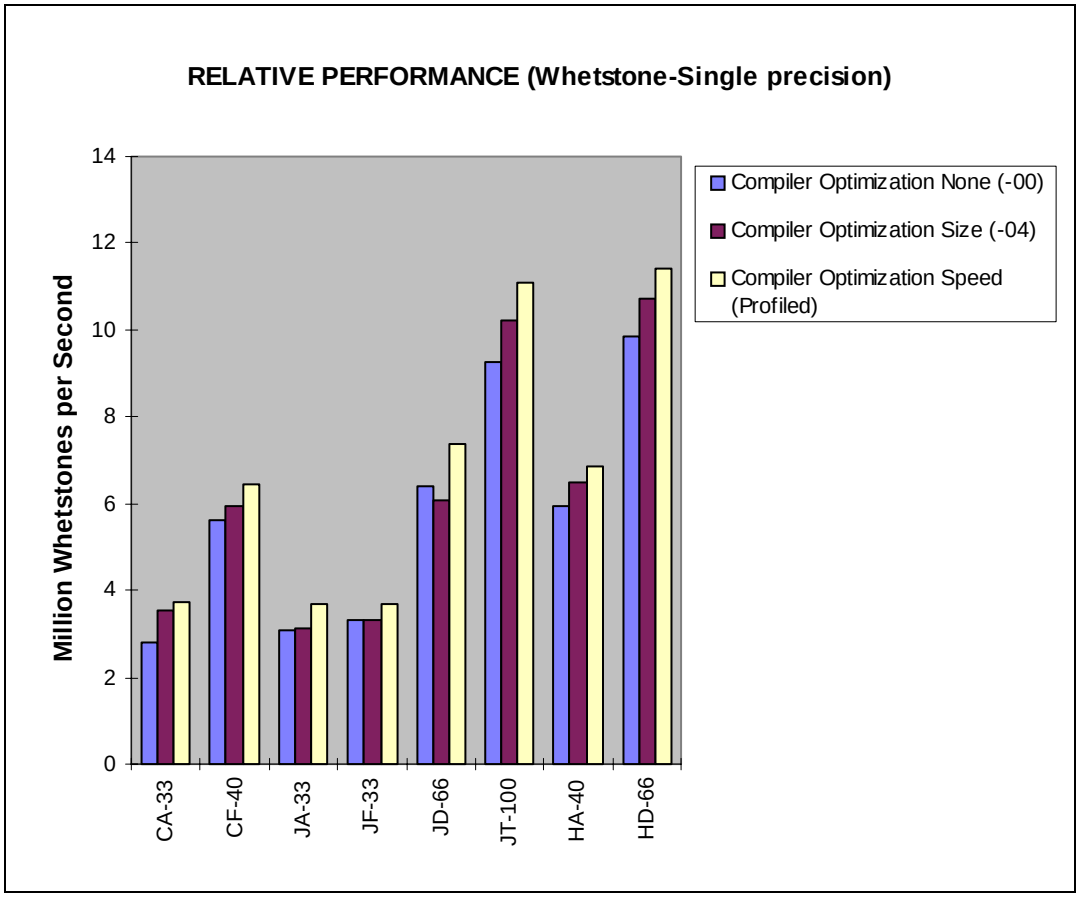
Figure 4. Dhrystone MIPS Relative Performance



6.3 Whetstone Single Precision

Memory:	Interleaved 60 ns DRAM	
Wait State Profile:	16/20/25 MHz:	10111
	33/40 MHz:	20121
Unit of Measure:	Million Whetstones per Second	(Larger is better)

Figure 5. Whetstone-Single Precision Relative Performance



6.4 Whetstone Double Precision

Memory:	Interleaved 60 ns DRAM	
Wait State Profile:	16/20/25 MHz:	10111
	33/40 MHz:	20121
Unit of Measure:	Million Whetstones per Second	(Larger is better)

Figure 6. Whetstone Double Precision Relative Performance