Integrated Circuit Systems, Inc.

ICS2494
ICS2494A

Dual Video/Memory Clock Generator

Features

- World standard **ICS2494A** has been reconfigured to allow 8 memory frequencies.
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Provision for external frequency input
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 20-pin DIP or SOIC

New Features

- Buffered XTAL Out
- Integral loop filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Frequency change detection circuitry which enhances new frequency acquisition and eliminates problems caused by programs that rewrite frequency information.
- Improved pinout - easier board layout.

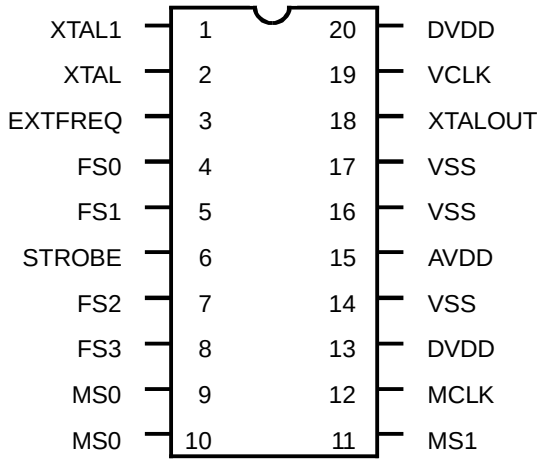
Applications

- VGA-Super VGA-XGA video adapters
- Workstations
- 8514A-TMS34010-TMS34020
- Motherboard

Description

The Dot Clock Generator is an integrated circuit dual phase-locked loop frequency synthesizer capable of generating sixteen video dot clock frequencies and eight memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2494/94A** provides a low-power, small-footprint, low-cost solution to the generation of video dot clocks. Outputs are compatible with XGA, VGA, EGA, MCGA, CGA, MDA, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single-level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

Pin Configuration



20-Pin DIP or SOIC

Notes:

1. In applications where the external frequency input is not specified, EXTFREQ must be tied to V_{SS}.
2. ICS2494/94AM(SOIC) pinout is identical to ICS2494/94AN(DIP).

Circuit and Application Options

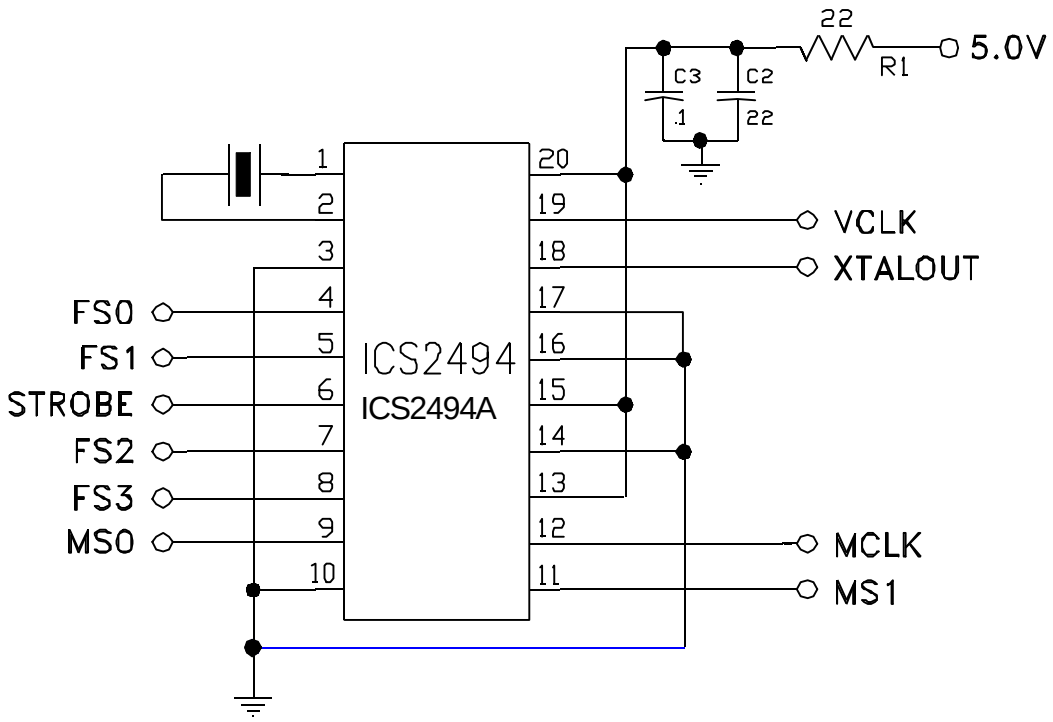
The **ICS2494/94A** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 2. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into **XTAL1**. Pin 2 must be left open.

Power Supply Conditioning

The **ICS2494/94A** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 volt analog supply is available, although the improved performance comes at a cost of an extra component. The cost of the discretes used in Figure 2, however, are less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all VDDs may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS minimized the effect of packaging and minimized the interaction of the digital and analog supply currents.

Figure 1

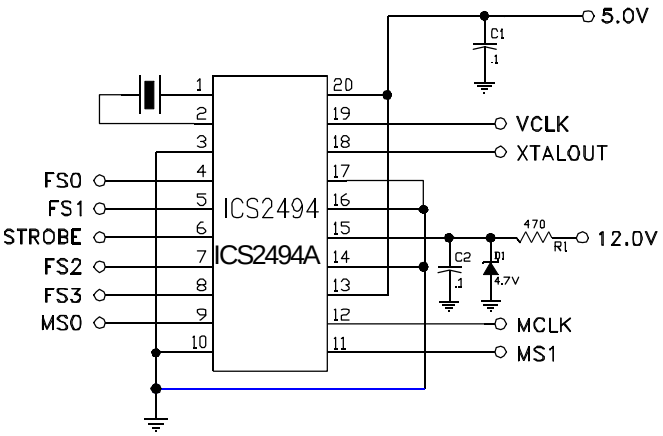


Applications

Layout Considerations

Utilizing the **ICS2494/94A** in video graphics adapter cards or on PS2 motherboards is simple but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2494/94A** do not share its ground. In applications utilizing a multi-layer board, VSS should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital VSS and VDD connections to permit extended frequency VCLK operation to 135 MHz. However, in all cases, all VSS and VDD pins should be connected.

Figure 2



Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (1)** and **XTAL2 (2)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2494/94A**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (1)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (1)**, and keep the lead length of the capacitor to **XTAL1 (1)** to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity.

The **ICS2494/94A** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (2)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2494/94A** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (18)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK (19) or MCLK (12)** and other components in the system should be kept as short as possible. The **ICS2494/94A** outputs have been designed to minimize overshoot. In addition it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2494/94A**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

Digital Inputs

FS0 (4), FS1 (5), FS2 (7), and **FS3 (8)** are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (6)**, when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **MS0 (9)**, **MS1 (11)** and **MS2 (3)** are the corresponding memory select inputs and are not strobed.

Absolute Maximum Ratings

Supply Voltage . . . . . V_{DD} . . . . . -0.5V to +7V
Input Voltage. . . . . V_{IN} . . . . . -0.5V to V_{DD}+0.5V
Output Voltage . . . . . V_{OUT} . . . . . -0.5V to VDD+0.5V
Clamp Diode Current . . . . . V_{IK} & I_{OK} . . . . . ±30mA
Output Current per Pin . . . . . I_{OUT} . . . . . ±50mA
Operating Temperature . . . . . T_o . . . . . 0 °C to 70 °C
Storage Temperature . . . . . T_S . . . . . -85 °C to +150 °C
Power Dissipation. . . . . P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <=V_{DD}.

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.0	5.5	V	
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{dd} = 5V
V_{IH}	Input High Voltage	2.0	V_{dd}	V	V_{dd} = 5V
I_{IH}	Input Leakage Current	-	10	*u*A	V_{in} = V_{cc}
V_{OL}	Output Low Voltage	-	0.4	V	I_{ol} = 4.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{oh} = 4.0 mA
I_{DD}	Supply Current	-	35	mA	V_{dd} = 5V, VCLK = 80 MHz
R_{UP} *	Internal Pull-up Resistors	50	200	K Ohm	V_{dd} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pull-ups: FS0-3, MS0-1, STROBE.

Frequency Pattern Availability

ICS offers the largest variety of standard frequency patterns in the industry, supporting all popular VGA controller devices. The attached listing provides the selection as of this publication date. Contact your local ICS sales office for latest frequency pattern availability.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. $T_C = 1/ F_C$
3. All units are in nanoseconds (ns).
4. Rise and fall time is between 0.8 and 2.0 VDC.
5. Output pin loading = 25pF
6. Duty cycle is measured at 1.4V.
7. Supply Voltage Range = 4.0 to 5.5 Volts
8. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK AND VCLK TIMINGS			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns

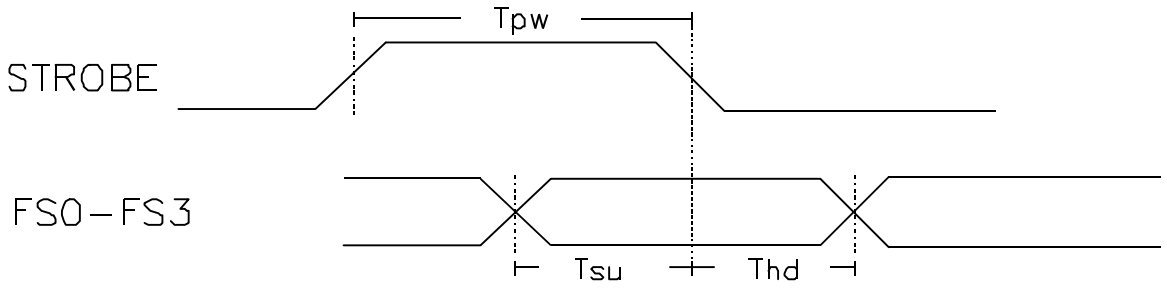
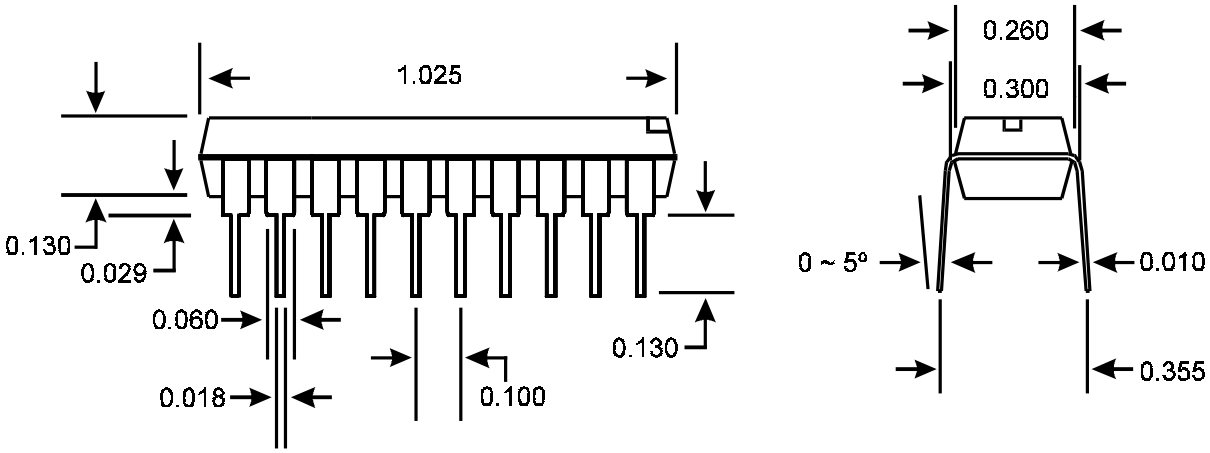


Figure 3

Package Dimensions



20-Pin DIP Package

Ordering Information

ICS2494AN-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

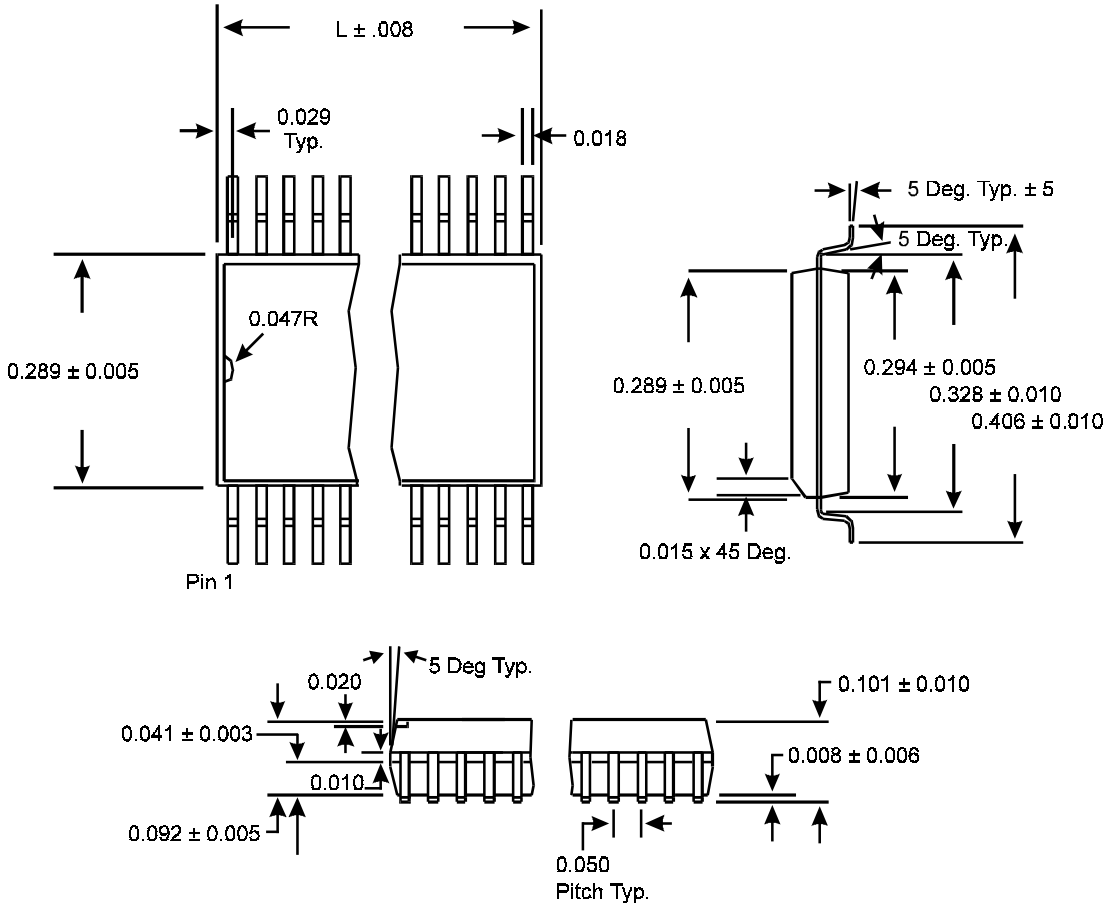
Package Type

N=DIP (Plastic)

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard Device; GSP=Genlock Device



SOIC Packages (wide body)

LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	0.354	0.404	0.454	0.504	0.604	0.704	0.804

Ordering Information

ICS2494AM-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device