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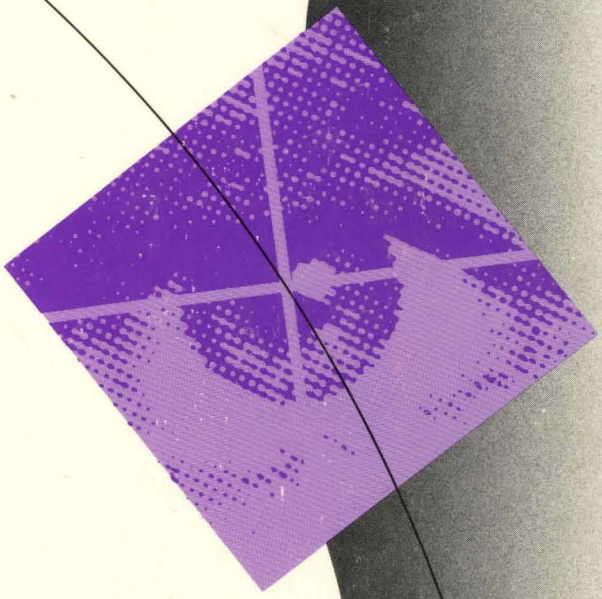

BROOKTREE

Graphics and Imaging Products/Application Literature Cross Reference List

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Bt101	1, 2, 3, 6, 10, 11, 12
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Bt102	1, 2, 3, 6, 10, 11, 12
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INTRODUCTION

Brooktree's Application Engineering Department is a responsive team that provides a diverse range of technical product support services. Our customers benefit from these services throughout their product's life cycle; initial design evaluation, prototype development, qualification and production.

We recognize the importance of customers having access to technical product information during a critical design phase to assure time-to-market design success. Several factory-direct access channels, such as the fax, telex and the toll-free telephone numbers, are printed on the front page of all technical product literature. The Technical Hotline (800 VIDEO IC) provides immediate access to technical personnel regarding a product question or literature inquiry. Other services include on-site design support or factory analysis of any issues you may have.

This Applications Handbook contains information to support you throughout your design effort. This information is compiled in sections which include application notes, article reprints and a summary of relevant industry standards.

Application Notes

Application notes provide transfer of technical information which is critical for correct operation or use of a product. The information may cover several levels of a product application, ranging from specific device use to system use techniques. Application notes are written to respond to product applications, provide solutions to recurring field difficulties, or clarify correct design techniques. New application notes are continually produced to meet new product applications.

Other Brooktree publications, such as the product databook and datasheets, contain application sections reflecting the latest information specific to a particular product.

Industry Standards

Industry trends will continue to push VLSI technology to incorporate more functionality into a system. This growth will evolve into VLSI subsystems that meet established protocol standards. Brooktree recognizes the importance of standards that support open architecture. Protocol standards provide a vital link between the software and hardware, reducing development time and system cost.

The Industry Standards section contains several standards relevant to the transmission, manipulation and display of images. The Electronic Industry Association (EIA) publishes bulletins, recommendations, and standards applicable to broadcast television and display systems. The electrical specifications for display standards such as RS330, RS343A, RS170, and RS170A are reproduced in this section.

The International Telecommunications Union (ITU) is the governing body of several committees, including the Consultative Committee of International Radio (CCIR). The recommendation CCIR 601-1 defines the digital encoding standards for television signals while report CCIR 624-1 lists the electrical specifications for universal worldwide broadcast television signals.

A reference address list of other standard publishing organizations and agencies is furnished at the end of the this section. The standards in this section have been reproduced with written permission from the authoritative governing body.

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TABLE OF CONTENTS

Getting the Best Performance from Video Digital-to-Analog Converters

When using high speed analog and digital logic, proper component selection, hardware, and printed circuit board layout become paramount in obtaining stable and noise-free performance.

Because VIDEODACs and RAMDACs contain part digital and part analog circuitry, the analog output signal is subject to degradation from power supply noise, ground loops, radiated pickup and magnetic coupling. The mixture of digital and analog circuitry often requires unique solutions due to the harmonic content of the waveforms. This application note will provide guidelines for both the design engineer and the printed circuit board designer to obtain the best performance from a VIDEODAC or RAMDAC.

For additional and more detailed product-specific layout considerations, refer to the individual product datasheets.

Ground Planes

In designing a board with high speed TTL logic, one should always use a ground plane under digital signal traces to minimize radiated noise and crosstalk.

Best performance from VIDEODACs is obtained by separating this ground plane into two separate areas (designated as digital ground and analog ground), with at least a 1/8" gap between the areas. The digital ground plane should encompass the area under all the digital logic including signal traces leading up to the DAC but excluding any ground pins on the DAC. The analog ground plane area should include all ground pins on the DAC, all reference circuitry (external reference if used, current setting resistors, etc.), the output traces and output connector(s).

The digital and analog ground plane areas should be connected at the lowest impedance source.

Power Planes

It is good design practice for dense PCB layout with high speed logic to include a power plane layer to minimize voltage drops, aid power supply decoupling and improve noise margins.

For best DAC performance, the power plane should be separated into two areas, designated as analog and digital power, which lay on top of the analog and digital ground planes, respectively. The digital power plane will supply power to all digital logic on the board and the analog power plane will supply all power pins of the DAC, together with power for any reference circuitry.

It is important that portions of the digital power plane area do not overlay portions of the analog ground plane area and that portions of the analog power plane area do not overlap portions of the digital ground plane. This will prevent PCB plane-to-plane noise coupling. Finally the analog and digital power plane areas should be tied together at a single point with a wire through a ferrite bead (such as Fair-Rite part no. 2743001111).

Power and ground return connections from the board to an external power supply should be made to the digital power and ground areas to minimize the DC current flowing through the ferrite beads connecting the analog and digital areas together.

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Supply Decoupling

Printed Circuit Boards

A four layer sandwich structure, with power and ground planes inside the board and signals on the top and bottom of the board, provides good high frequency decoupling by virtue of the distributed capacitance between the power and ground planes.

The addition of 0.1 μF ceramic capacitors at a density of one cap per one or two square inches is usually enough for lower frequency decoupling. For best DAC performance, a 0.1 μF ceramic capacitor should be placed as close to each DAC power pin as possible for bypassing the analog power and ground plane areas. For operation beyond 75 MHz, a 0.1 μF ceramic capacitor paralleled with a 0.001 μF chip capacitor is recommended.

If the display has "ghosting" problems, additional capacitance in parallel with the power supply and COMP capacitors may fix the problem.

Breadboards

In breadboards with a ground plane and point to point wiring for power, best DAC performance is achieved with chip capacitors in the 0.01 μF to 0.1 μF range connected between the power pins and ground (see discussion about sockets on next page). Also, in breadboards with point to point power wiring, a ferrite choke such as Ferroxcube part no. VK20019/4B should be placed between the DAC power pins and the power source for the digital logic. Breadboards with a prefabricated ground plane should have this plane cut into analog and digital areas as indicated in the earlier discussion on ground planes.

Signal Interconnect

Digital Inputs

The digital input signals to the DAC should be isolated from the analog output(s) analog reference inputs to the DAC. Also, the digital input signals should run over the digital ground and power plane areas of the board (see earlier discussion on power and ground planes).

To minimize data undershoot, ringing, and resultant data feedthrough noise, interconnect distances should be kept as short as possible to the DAC inputs (less than 3 inches). Data feedthrough noise is also proportional to edge speed, so in lower speed applications, use of lower speed logic will reduce data related noise on the DAC output. Also, one should avoid running long clock lines to the DAC since this is another source of noise pickup.

Finally, in some applications, use of parallel termination resistors at the DAC inputs can reduce digital noise. The terminating resistors, if used, should be the low inductance film type and should be connected to the digital ground and power planes.

Analog Inputs

The DAC should be located as close as possible to its output connector(s) to minimize noise pickup on the analog output traces. It is usually more difficult to control the characteristic impedance on boards, though minimizing the output line length will minimize reflections due to impedance mismatch. DAC reference circuitry should be kept close to the DAC to avoid stray pickup. DAC output signals should overlay the analog ground plane and not the analog power plane to maximize high frequency power supply rejection.

It is important to note that while DACs contain circuitry to reject power supply noise, this rejection decreases with increasing frequency. As an example, with a 0.01 μF compensation capacitor, the power supply rejection on CMOS DACs flattens out to 20 dB at frequencies around 1 KHz. This means that if the user powers the DAC from a 20 KHz switching power supply with 100 mV of noise at 20 KHz and harmonics, about 10 mV of this supply noise will be on the DAC output. If the designer does not use linear supplies, close attention should be paid to reducing supply noise and one should consider using a three terminal regulator for DAC power.

Bypass Capacitors

Probably the single most important external components which affect the noise performance of a DAC, are the capacitors used to bypass the power supplies.

It is important to realize that the high frequencies generated by the logic will not be filtered by most capacitors. At these frequencies, most capacitors look like inductors. For example, a 0.1 µF capacitor with 1/4 inch of lead length will self resonate at around 10 MHz, beyond this frequency it will look inductive. Therefore, the criterion for measuring the effectiveness of a given bypass capacitor is to note its lead inductance. In addition, bypass capacitors should be installed in printed circuit boards with the shortest leads possible, consistent with reliable operation.

Probably the most effective capacitor is the distributed capacitance between power and ground planes. However, this capacitance is usually too small to sustain large current surges without excessive voltage change. Ceramic chip capacitors are the next most effective for bypassing applications and are highly recommended. The drawback to using chip capacitors in PCB applications is their tendency to crack during high shock or wide temperature ranges.

The third most effective capacitor type is the radial lead ceramic capacitor. Distributed capacitor inductance must be balanced by a large-value tantalum or electrolytic capacitor.

In summary, there is no one right answer to bypassing which will suit all applications. However, the principle to keep in mind is that bypassing capacitors in conjunction with the distributed power supply plane inductance will determine the effectiveness of the decoupling.

Avoiding Latch-Up

Latch-up is a common concern with CMOS devices where power supply differentials or sequences can induce the CMOS device to draw excessive current. Observe the following precautions to avoid latch-up in CMOS devices:

1. Tie all VAA pins together at the package pins.
2. Hold all logic inputs low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants which could delay VAA power to the device.

Latch-up can be prevented by assuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5v.

ESD Considerations

Correct ESD sensitive handling procedures are required to prevent device damage which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Attenuation Beads

Ferrite beads are recommended to suppress interference due to the fast switching times of the DACs and decoupling noise on the power plane from getting to the DAC output. Some recommended attenuation beads are Ferroxcube part no. VK20019-4B, Fair-Rite part no. 2743001111, and Philips part no. 431202036690. Figures 1 and 2 are the impedance and typical damping curves for several Ferroxcube brand wide band chokes.

Analog Output Protection

CMOS VIDEODACs and RAMDACs have no intrinsic protection on the analog outputs against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low capacitance, fast switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

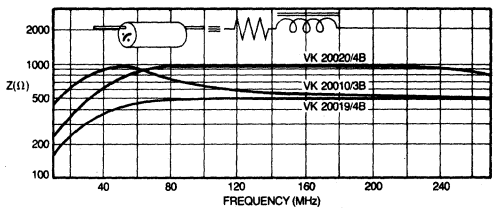

Figure 1. Impedance Curves of Wide-Band Chokes.

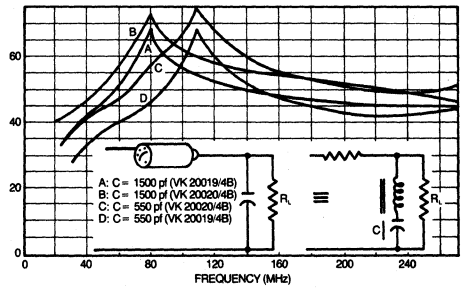

Figure 2. Typical Damping curves for VK Chokes with Additional Parallel Ceramic Capacitors.

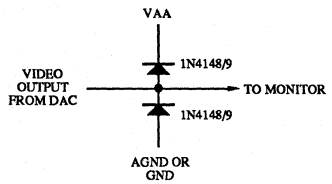

Figure 3. Output Protection Circuit.

VIDEODAC Essentials

A raster based graphics display terminal is comprised of a graphics controller, a frame buffer to hold the refresh data, optional color look-up tables, VIDEODACs, and a CRT monitor. The VIDEODAC subsystem has special requirements and performance parameters that will define the overall quality of the graphics presentation.

A simplified block diagram of a color graphics terminal using a color lookup table and three VIDEODACs is shown in Figure 1. A monochrome or black and white monitor will use one lookup table and one VIDEODAC. The interface to the computer system is the graphics display controller. The graphics controller generates all the timing and interface signals to the video RAM, the color lookup tables, the VIDEODACs and the deflection circuitry for the CRT.

The new generation of monolithic integrated circuits includes the color lookup RAM and the DAC, either as a single group or as a triple RAM and DAC combination (RAMDAC).

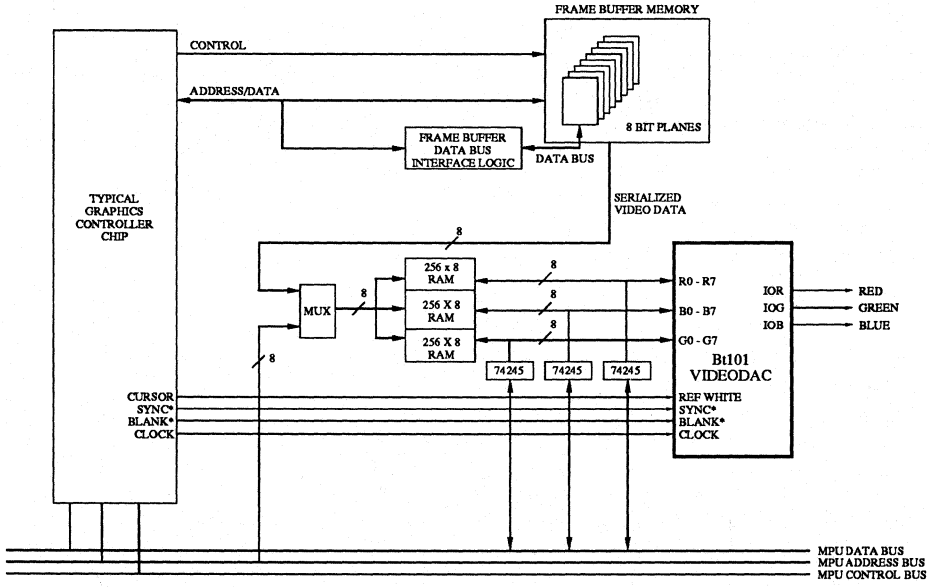

Figure 1. Simplified Block Diagram of a Color Graphics Terminal.

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Video Waveform

A standard input signal (EIA standard RS-343A) has been defined for raster scan video monitors which are commonly used for computer graphics. This standard defines the voltage level for each component of the video signal, as illustrated below in Figure 2. Note that the entire video signal is divided into three segments: sync, setup, and intensity information. A color CRT monitor requires three of these signals, one each for red, green, and blue.

In a color graphics system, the green video signal has a peak-to-peak amplitude of 1.0 volts. The red and blue video signals have a peak-to-peak amplitude of either 1.0 volts or 0.714 volts, depending on whether they have sync information present or not. Typically, sync information is present only on the green channel.

Sync information is defined to be 0.286v ± 0.05v, or 40+ IRE units. Sync is used to provide horizontal and vertical synchronization information to the CRT monitor. Separate sync monitors will have a fourth channel dedicated just to sync information.

The setup, which is the difference between the blank level and the reference black level, is defined as 7.5 ± 2.5 IRE units, or 0.054 ± 0.018 volts. At this level the CRT beam is visibly shut off, allowing it to retrace across the screen at the blank level to begin the next scan line.

Intensity information, the interval between reference black and reference white, is assigned 92.5 ± 2.5 IRE units, or 0.660 ± 0.018 volts. It is typically composed of 16 discrete levels when 4-bit DACs are used, or 256 discrete levels when 8-bit DACs are used. Thus, the DACs ultimately determine the number of colors available.

Table 1 illustrates the total number of available colors (color palette) for various DAC resolutions when used in a color graphics system. To substantially reduce system costs, most systems compress data through the use of lookup table RAMs, allowing the user to display typically only 16 or 256 simultaneous colors of the total available color palette.

DAC Bits	DAC Output Steps	Color Palette
1	2	8
2	4	64
3	8	512
4	16	4096
5	32	32,768
6	64	262,144
7	128	2,097,152
8	256	16,777,216

Table 1.

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

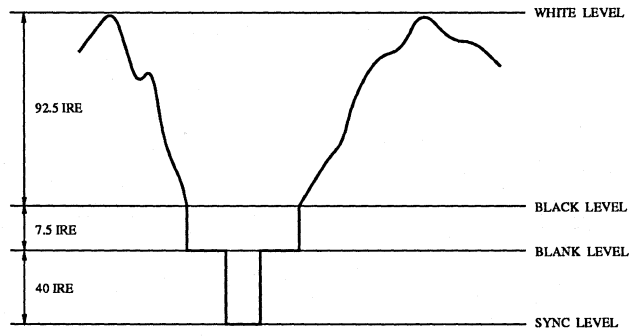

Figure 2. Standard Voltage Levels of RS-343A.

VIDEODAC

The VIDEODAC converts the digital information to analog signals for the color guns in the CRT. A VIDEODAC has several important parameters that will determine the overall performance of the display system. The update rate of the DAC sets the speed at which the pixels or dots can be displayed across the screen. The overall system speed is determined by the time it takes to scan across the screen and the time the monitor is blanked for retrace. Table 2 illustrates some of the common graphics resolutions and their video line rates.

Logic Interface

The type of logic interface can determine the overall system speed and the number of power supplies required. For a TTL type of system, the Schottky S series or the FAST series of logic must be used to obtain speeds up to 75 MHz. The regular Schottky families, such as LS or ALS, can be used in most cases up to 40 MHz. If the DAC is also compatible with CMOS logic levels, the 74HC series of gates can be used to 40 MHz. For speeds higher than 80 MHz, ECL logic is typically used. The 10K, 10KH, and 100K series will perform up to 125, 250, and 300 MHz respectively.

Resolution	Video Rate	Line Rate	# of 256K RAMs per Bit Plane
512 x 512	20 MHz	31.5 KHz	1
640 x 400	20 MHz	24 KHz	1
640 x 480	25 MHz	31.5 KHz	2
768 x 576	35 MHz	37 KHz	2
1024 x 800	66 MHz	52 KHz	4
1024 x 1024	80 MHz	63 KHz	4
1152 x 900	95 MHz	58 KHz	4
1280 x 1024	110 MHz	65 KHz	5
1600 x 1200	165 MHz	75 KHz	8
2048 x 1536	260 MHz	100 KHz	12
2048 x 2048	360 MHz	128 KHz	16

Table 2. Common Graphics Resolutions and Line Rates. (60 Hz Non-Interlaced Refresh Rate)

DAC Resolution

DAC resolution is a measure of how many individual steps there are between end points and a measure of how accurate each step relates to the next one. A 4-bit DAC output will have 16 discrete levels at 41.2 mV intervals, while an 8-bit DAC will have 256 discrete levels at 2.5 mV intervals (assuming 0.66 volts of color information). A typical 8-bit VIDEODAC will have a differential non-linearity of ±1 LSB or ±2.51 mV which determines the width of each step. The end result is a higher resolution and a smaller differential non-linearity value, which produces a more accurate control over the CRT beam intensity and the color quality.

In a TTL and CMOS system, only a single 5 volt power supply will be required. An ECL system will require a termination plane and a -5.2 volt power supply. An ECL-TTL system will need a termination plane, and a +5 volt and -5.2 volt power supply.

DAC Termination

The VIDEODAC's output signal must interface properly with a video monitor and be able to drive a 75 ohm coax (the standard input impedance for the video monitors). Since the DAC is a current source, and the relation V = IR determines the signal level, the output is terminated into a 75 ohm load to develop the output voltage levels. As speeds increase, ringing and reflections in the cable may distort the waveform causing the termination at the monitor to be insufficient in maintaining the signal quality.

If termination is at the source and at the load, some VIDEODACs will allow double termination. In such an instance, a 75-ohm resistor is placed near the output pin of the DAC to ground and the terminating impedance of the monitor serves as the load resistor. A diagram of the connections is shown in Figure 3.

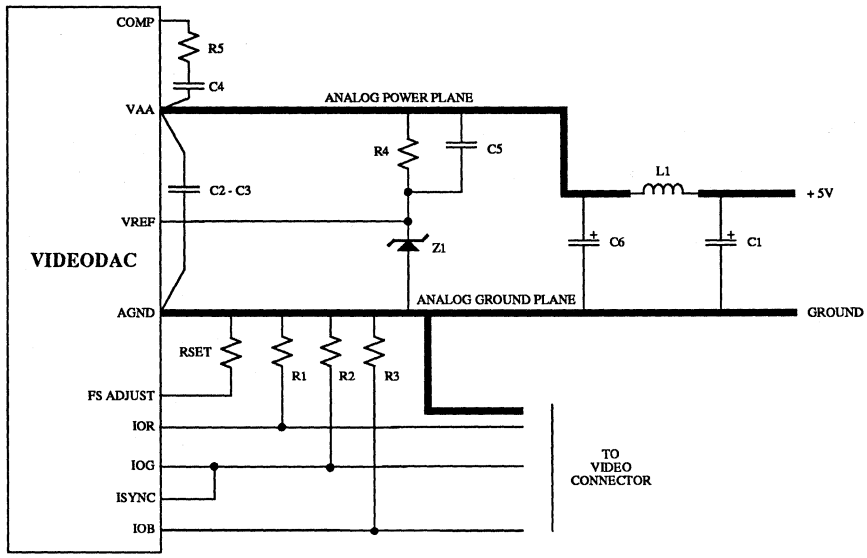

Figure 3. Typical Connection Circuit.

Glitch Impulse

Glitch impulse is a term used to define the area under the voltage-time curve of a single DAC step until the level has settled out to within the specified error band of the final value (the linearity error). Glitch impulse is important where subtle level changes can produce significant transients, and is different from settling impulse which involves large amplitude changes.

Depending on the type of internal logic design in the DAC, the glitch energy can be very low (< 50 pV-sec) for a segmented architecture to as much as 250 pV-sec for a R-2R network. For many DACs, maximum glitch energy will occur when a transition is made between segments (which have the worst switching skew), where the count goes from 0111 1111 to 1000 0000. This is where all the internal registers will change and the current sources are turning on and off. Low glitch energy is necessary to avoid pixel color change or blurred pixels across the CRT. Figure 4 shows a typical DAC output glitch.

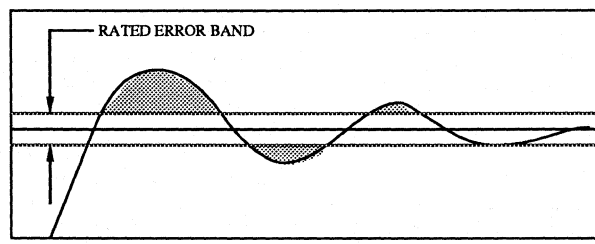

Figure 4. DAC Output Glitch.

In a video system, if the glitch energy is sufficiently low and consistent across all codes, it will be integrated over a period of time and will have no effect on the CRT screen. Other glitches generated by the DAC such as data feedthrough and DAC-to-DAC noise, may have a cumulative affect since the waveforms may not be repetitive. Therefore, good design practices in PC board design include power supply decoupling, and avoidance of running digital signal lines near the DAC analog circuitry and output to the monitor. A suggested component placement is shown in Figure 5.

DAC-to-DAC skews greater than 1/4 pixel interval can result in perceived color shift and resolution loss.

Rise/Fall Times

How fast a DAC output can switch from one voltage step to the next voltage step is measured from the 10% to 90% transition of the output waveform. In video applications, the faster the DAC the smaller this number will be. For a 30 MHz DAC, 3 to 10 ns would be typical, while for a 125 MHz DAC, 1 to 3 ns would be common. For very high speed DACs in the 250 MHz or greater speed range, rise and fall times under 1 ns are necessary. The output voltage slew rate is also a function of the load capacitance/termination and the addition of small values of capacitance can some times be used to reduce overshoot and ringing when very fast DACs are used. DAC rise/fall times are at least twice as fast as the monitor they drive to avoid degradation of the convolved transition time.

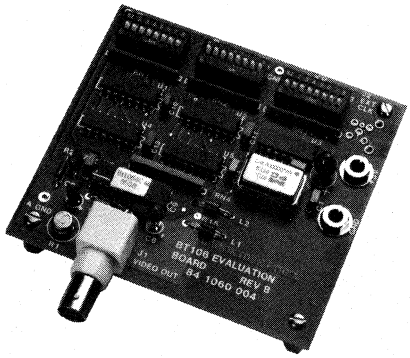

Figure 5. Typical Evaluation Module.

Settling Time

Settling time is a measurement of how fast a DAC output voltage from the mid-transition, settles to the desired value within an error band (e), typically ± 1/2 LSB.

In video applications, settling time is of moderate importance, since the CRT phosphors are being excited and the eye will not respond to the very small differences in light intensity of the pixel on the screen. Settling times greater than a pixel interval result in loss of color rendition or palette resolution.

Settling time is an important parameter if the DAC is being used in an instrumentation environment where it is necessary to have very accurate voltages as the input code is changed. Figure 6 describes both rise/fall time and settling measurements.

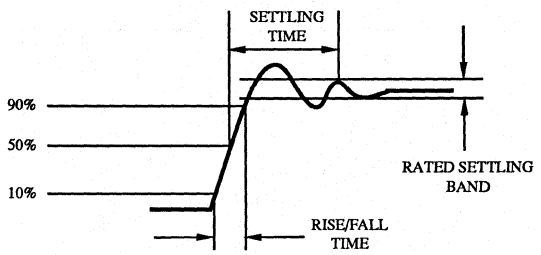

Figure 6. Rise/Fall Time and Settling Measurements.

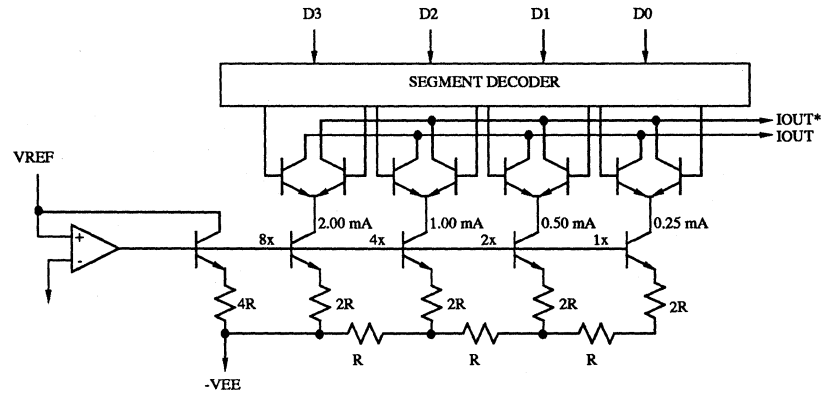

Figure 7. Typical R-2R DAC Network (4-Bit DAC).

DAC Internal Architecture

To generate the individual current steps, the simplest form of a DAC will use an R-2R summing resistor network. For an 8-bit DAC, eight current sources are used in a binary fashion to generate 256 output steps. While a minimal number of components are used, the weaknesses of this design are: 1) the resistor ladder tolerances are critical, 2) the individual current steps range from large to small values, and 3) the temperature tracking of resistor pairs. Due to device tolerances, in order to obtain less than ± 1 LSB integral linearity error and ± 1 LSB of differential linearity error, it is necessary to match the resistors by laser trimming resistor links.

Figure 7 illustrates a typical R-2R DAC network. An improved type of circuit architecture, called a segmented DAC, offers low glitch energy and no trimming of resistors to obtain the needed accuracy. The segmented DAC utilizes the fact that monolithic transistors and resistors of the same geometry can match closely to each other and that cumulative geometry errors can be effectively averaged over the monolithic device area.

Some segmented DACs may use 256 individual current source transistors or a combination of segmentation for the higher order bits and an R-2R network for the lower order bits where speed, tolerance and area determines the partition. Figure 8 shows a fully segmented DAC circuit topology.

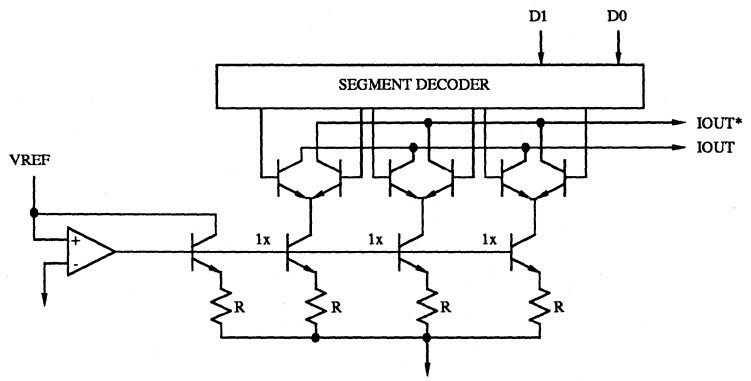

Figure 8. Segmented DAC Topology (2-Bit DAC).

Comparison of NTSC, PAL and SECAM Video Formats

There are several international standards for specifying the amplitude and video components of a waveform for use with television and video monitors which use a subcarrier for color or chrominance information.

In North America and Japan, the NTSC format is the standard, while PAL and SECAM video formats are used in Europe. A comparison of the various video levels is shown in Table 1 for reference, and Figure 1 is a drawing of a composite video waveform. The newer international standards specify a voltage amplitude of 0.714 volts between the blanking level and the white level for the video portion of the waveform (blanked video signal) and is defined as having 100 IRE units. The black to blank level (typically referred to as the setup) is used to shut off the beam during the retrace time and varies between the formats. The total amplitude is about 140 IRE units (143 IRE units for PAL and SECAM) from sync tips to reference white for monochrome, with a saturated subcarrier.

An older standard known as RS170A is also used in the United States and differs from RS343A level for the voltage level from blank to white. The RS170A blanked video level is 1.00 volts as compared to the RS343A, PAL, and SECAM levels of 0.714 volts.

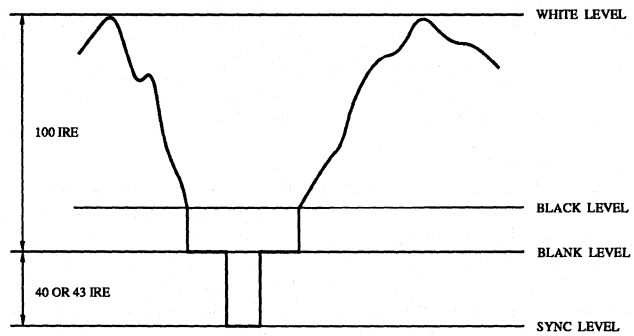

Figure 1. Composite Video Waveform.

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The monochrome version of the RS170A standard (RS170) does not have a subcarrier for color or chrominance information.

The sync levels (40 IRE units for NTSC and 43 IRE units for PAL and SECAM) are sufficiently close enough in tolerance that the 40 IRE levels of Brooktree's VIDEODACs and RAMDACs will meet the PAL and SECAM tolerance.

The RS343A standard is commonly used for computer graphics, and of the four standards previously mentioned, it and RS170 are the only ones that do not use a subcarrier for color or chrominance information. Rather, three separate signals (red, green, and blue) are generated, each containing intensity and blanking information. Typically, only the green channel contains sync information.

To assist users who need to determine the output current when terminated into 75-ohm and 37.5-ohm (doubly-terminated 75-ohm) loads, a comparison chart is shown in Table 1. Brooktree DACs are specified to drive doubly-terminated 75-ohm loads, while many competitor DACs can only drive a singly-terminated 75-ohm load and develop the proper video output voltage level.

	Video Output Levels	IRE Units	Volts	mA (typ.) (75-ohm load)	mA (typ.) (37.5-ohm load)
NTSC RS-343A*	Blank to White	100 IRE	0.714 ± 0.1	9.52	19.04
	Blank to Black	7.5 ± 5 IRE	typ. 0.054	0.714	1.43
	Blank Level		0	0	0
	Blank to Sync	typ. 40 IRE	- 0.286 ± 0.05	- 3.81	- 7.62
NTSC RS-170*	Blank to White	100 IRE	1.0 ± 0.05	13.33	26.67
	Blank to Black	7.5 ± 2.5 IRE	typ. 0.075	1	2
	Blank Level		0	0	0
	Blank to Sync	40 ± 5 IRE	typ. - 0.4	- 5.33	- 10.67
NTSC RS-170A**	Blank to White	100 IRE	1.0 ± 0.05	13.33	26.67
	Blank to Black	7.5 ± 2.5 IRE	typ. 0.075	1	2
	Blank Level		0	0	0
	Blank to Sync	40 ± 5 IRE	typ. - 0.4	- 5.33	- 10.67
PAL**	Blank to White	100 IRE	typ. 0.714	9.52	19.04
	Blank to Black	0 IRE	0v	0	0
	Blank Level		0v	0	0
	Blank to Sync	typ. 43 IRE	typ. - 0.307	- 4.09	- 8.19
SECAM**	Blank to White	100 IRE	typ. 0.714	9.52	19.04
	Blank to Black	0 to 7 IRE	0 to 0.049	0	0
	Blank Level		0	0	0
	Blank to Sync	typ. 43 IRE	typ. - 0.307	- 4.09	- 8.19

*no color or chrominance subcarrier -- requires three channels for RGB.
**uses color or chrominance subcarrier -- Bt102 is suggested VIDEODAC.

Table 1. Comparison Of Video Formats.

Other items of interest when comparing the various video formats are the number of lines per frame, field frequency, and normal video bandwidth:

	RS170A	PAL	SECAM
Number of lines per frame	525	625	625
Field frequency	60	50	50
Luminance Bandwidth (MHz)	4.2	5	6
Chrominance Subcarrier (MHz)	3.58	4.43	4.3 to 4.4
Chrominance Bandwidth (MHz)	0.5 to 1.5	1.3	1.3

Table 2. Comparison of Video Formats.

Since chrominance subcarrier formats generate output levels between blank and sync levels (to generate color burst information during the back porch time), the sync and blank control inputs to most DACs cannot be used in such applications. The 20 IRE gap between sync and the most negative color burst level represents a 15% loss in gray scale range just to encode the sync.

This can be improved by asserting sync information through an external current sink rather than through the DAC data bits. Figure 2 shows a circuit using a transistor array (3227) biased off a negative supply voltage. The delay through the external sync switch should roughly match that through the DAC including any pipeline delays. Fast CMOS switches (4316 type) can perform the same function using resistor summing (rather than current summing), with some attendant degradation in output impedance match or return loss (3% or 30 dB is common for industrial grade, while 10% or 20 dB suffices for consumer applications).

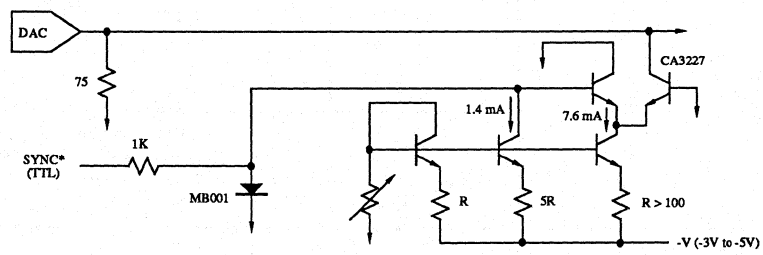

Figure 2. External Sync Circuit for NTSC RS170A, PAL, and SECAM.

Component Analog Video Formats

In recent years, the trend has been toward component analog video (CAV) formats, much like the RGB format of most computer graphics systems.

The major video equipment CAV formats currently in use are summarized in Table 3 at a standard color saturation level of 75%, which is the common "legal" limit to the chrominance subcarrier's amplitude range in the NTSC format.

GRB is the matrix decoded version of NTSC with sync added to all three channels, which may be extended to 700 mV gray scale at 100% saturation with a PLUGE offset for monitor black/white adjust. Reversal of the non-complex RGB to GRB format is consistent with the green signal corresponding to the Y or luminance signal in the other color difference (B - Y and R - Y) formats.

The BetaCam and MII are the popular Sony and Matsushita formats respectively, each of which come in 3 or 2 wire versions and involve the Component Time Division Multiplexed (CTDM or CTCM) nomenclature in the latter case.

The Society for Motion Picture and Television Engineers (SMPTE) and the European Broadcasting Union (EBU) have adopted their own color difference formats in order to remove brand name association. Most CAV formats sample the color difference components at half the rate or bandwidth of the luminance signal (the common 4:2:2 hierarchy, not to be confused with the RS-422 interface). Most CAV formats have no use for the 7.5 IRE setup used in NTSC, which represents a 7.5% loss in dynamic range. Hence, the newer CAV standards (GRB and SMPTE/EBU) call for no setup pedestal.

Format	Video Output Function	Signal Amplitude (Volts)	Comments
GRB	G, R, B Sync	+ 0.700 - 0.300	at 100% saturation, 0% setup three wire = (G + sync), (R + sync), (B + sync)
BetaCam*	Y Sync R - Y, B - Y	+ 0.714 - 0.286 ± 0.350	at 75% saturation, 7.5% setup on Y only three wire = (Y + sync), (R - Y), (B - Y)
BetaCam*	Y Sync CTDM R - Y CTDM B - Y Sync	+ 0.714 - 0.286 ± 0.350 ± 0.350 - 0.630	at 100% saturation, 7.5% setup on Y only two wire = (Y + sync), CTDM [(R - Y), (B - Y + sync)]
MII†	Y Sync R - Y B - Y	+ 0.700 - 0.300 ± 0.324 ± 0.324	at 100% saturation, 7.5% setup on Y only three wire = (Y + sync), (R - Y), (B - Y)
MII†	Y Sync CTCM R - Y CTCM B - Y Sync	+ 0.700 - 0.300 ± 0.350 ± 0.250 - 0.650	at 75% saturation, 7.5% setup on Y only two wire = (Y + sync), CTCM [(R - Y), (B - Y + sync)]
SMPTE	Y Sync PB PR	+ 0.700 - 0.300 ± 0.350 ± 0.350	at 100% saturation, 0% setup three wire = (Y + sync), PB, PR

*Trademark of Sony Corporation.
†Trademark of Matsushita Corporation.

Table 3. Popular Component Analog Video Output Formats.

Using the Overlay Palettes on Brooktree RAMDACs

What are Overlay Palettes?

Brooktree RAMDACs usually include an overlay palette, consisting of one or more registers, in addition to the normal color palette RAM. For triple RAMDACs, each overlay register contains 12 or 24 bits of color information (for triple 4-bit or triple 8-bit D/A converters, respectively). For single RAMDACs, each overlay register contains 8 bits of color information (assuming an 8-bit D/A converter).

To support the overlay palette, besides the normal pixel input ports, the RAMDACs have palette selection inputs, OLx. These inputs specify, on a pixel basis, whether color information is to be provided by the color palette RAM or one of the overlay registers.

Why are Overlays Useful?

In many instances, the graphics application software is primarily concerned with the generation and manipulation of images in the frame buffer. The system software, on the other hand, is usually responsible for cursor movement, menu insertion and deletion, and user messages, with minimal concern about the graphics image.

The use of one or two additional bit planes for overlays enables the system software to control user interface graphics independently of the graphics image. Graphics performance is improved, as the image in the frame buffer need not be modified each time the cursor is moved or a menu is displayed or removed. The problem of cursor avoidance during the image drawing process is also solved by implementing the cursor using an overlay approach.

Generating Overlay Information

Overlay information may be generated by using additional bit planes in the frame buffer, which are interfaced directly to the overlay inputs of the RAMDAC. Thus, the designer is able to keep the graphics data and overlay data in separate memory, simplifying software and increasing graphics performance.

If a VLSI graphics processor is used, the cursor output may be connected to the one of the overlay inputs of the RAMDAC. Thus, whenever the graphics controller outputs cursor information, the appropriate overlay register is automatically selected. Additional bit planes or external hardware may still be used for menus, grids, alphanumeric overlays, etc., by using any other overlay inputs of the RAMDAC.

Some high performance graphics systems implement hardware cursors using discrete or VLSI logic. Again, the cursor information may interface directly to one of the overlay inputs of the RAMDAC. Additional bit planes or hardware, connected to the other overlay inputs may be used for any additional overlay functions. Four bits of overlay can emulate an enhanced graphic adaptor window atop the main graphics image.

Summary

Overlays provide a means of simplifying the implementation of user interface mechanisms such as cursors, menus, and any type of graphics or text information that is to be displayed independent of the main graphics image.

The separation of system user interface software and graphics generation software will usually increase graphics performance and simplify software interfacing to the graphics system.

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Expanding VGA Graphics With the Bt471/475/476/477/478 Family

The IBM Personal System/2 introduces graphics display versatility to personal computer software and calls for more versatile digital-to-analog converters to take advantage of the greater software power. The Bt471/475/476/477/478 family of pin compatible RAMDACs support the basic capabilities of the IBM hardware as well as several added performance features which help differentiate board-level products in the compatible PC and expansion board markets.

The Bt47x family features more palette colors, higher speeds, overlay planes, simultaneous composite video and read-back, and surface mount packaging. These features afford the board designer flexibility and component savings for positioning his product in a dynamic marketplace.

Performance Features

Enhancements to the IBM hardware implementation (based on their Video Graphics Array) include:

A. Programmable choice of 262 thousand or 16.7 million color palette. On the Bt477 and Bt478, a single pin programs the length of the palette word to be either 6 or 8 bits per color channel. For business graphics or false color renderings 6 bits is adequate, but for presentation graphics of subtly shaded objects, 8 bits per channel is now standard on most Computer Aided Engineering (CAE) workstations and the Apple Macintosh II. More precise color segmentation can compensate for monitor inconsistencies (such as gamma effect) and reduce the "cartoon" appearance of color-limited palettes.

B. A 4-bit overlay port on the Bt471, Bt475, Bt477 and Bt478 makes special effects, such as cursors, borders, or even full EGA windows easy to implement on pixel-by-pixel boundaries, without the additional microprocessor burden of updating the pixel read mask for special effects.

C. A fully synchronous read-mask feature eliminates the need to externally synchronize the MPU write strobe to the pixel clock.

D. Support of both sync and MPU read-back on the Bt471, Bt475, Bt477, and Bt478 provides direct compatibility with RS-343 monitors without sacrificing future software system or self testing capabilities. The IMS® G171 device offers one or the other of these features, but not both, in one unit. Selectable setup levels (0 or 7.5 IRE) allow the user to optimize the retrace intensity for each monitor assuring international hardware compatibility. The Bt475 and Bt477 include on-chip comparators on the analog outputs for diagnostic capability, eliminating the need for external analog comparators.

E. The Bt47x family also offers a choice of more stable voltage references, or a cheaper current reference that is 100% compatible with the existing PS/2 hardware. The Bt475 and Bt477 offer an on-chip voltage reference, or the option of using an external voltage or current reference.

F. More robust output capability for driving doubly terminated cables greater distances (or looped through more monitors) with crisper transitions and lower reflection "ghosts". Brooktree guarantees linearity in terms of peak errors (not RMS) under doubly-terminated conditions. The coaxial medium between the DAC output and the monitor input calls for superior pulse fidelity to reduce amplitude ringing and monitor mistermination which can make pixels appear fuzzy, jittery or to have shadows.

G. An efficient 44-pin PLCC surface mount package occupies less board area than the 28-pin DIP counterpart. The lower PLCC profile improves power supply feedthrough and grounding as well by lowering package inductance 50%.

H. The Bt476 offers a pin-compatible solution to the IMS G176, and is available in both the 44-pin PLCC and the 28-pin DIP package.

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Implementing Enhanced Graphic Overlays

The PS/2 graphics format is distinguished by its higher vertical resolution, variable frame rate, and its 8-bit pixel architecture. To take advantage of multi-frequency monitors, the IBM 8514A resorts to interlacing at higher resolutions to provide near megapixel displays at a reasonable price, supporting interlaced 1024 x 768 resolution at a 43.5 Hz refresh rate. Since interlacing compromises display phosphor response to reduce flicker, faster pixel rates are desirable to achieve 60 Hz refresh rates without flicker or smearing. Non-interlaced 60 Hz formats of 1024 x 768 or 1024 x 1024 can be supported by the 80 MHz Bt47x family.

The non-interlaced formats keep the full 640 pixel horizontal resolution of the previous CGA, EGA and PGC formats while giving the preferred 4:3 aspect with 480 vertical lines at a frame rate of 60 to 70 hertz (320 x 200 with pixel replication). The 8-bit pixel word size provides for 256 simultaneous colors from a palette of 262K colors (6 bits per channel) or 16.7 million colors (8 bits per channel with the Bt477 or Bt478).

As the power of the VGA to do complex graphic operations in real time becomes fully supported by the software industry, it will be possible to mix various formats on screen to create sophisticated windows, cursors and overlays. The independent palette access provided by the overlay ports on the Bt471, Bt475, Bt477, and Bt478 will enable parallel generation of graphic effects without imposing additional MPU limitations.

The use of a read mask in the IMS G171 to generate special effects is fully supported (internally synchronous) in the Bt47x family, but its update rate is limited by the MPU write cycle time of 3 to 4 pixel clocks. This means that the mask effect will appear no finer than several pixels on the screen. This may save palette RAM size but prohibits high resolution overlays such as an EGA style window over a large part of the viewing screen. In situations where pixel frequency must be agile and independent of the MPU clock, the synchronous buffering of the Bt47x family prevents corruption of the palette contents, something that can occur with asynchronous IMS G171s when the pixel clock is not locked to the MPU clock.

The four overlay inputs to the color palette can be loaded and invoked in the same manner as the standard palette. An additional register select pin (RS2) is provided for loading and reading back the overlay values. In the read mode the overlay inputs override the P0 - P7 pixel inputs, so any unused pixel and overlay inputs should be tied low. This parallel palette access simplifies cursor or cross hair generation to where a single chip (such as the Bt431) can manage this function with direct connection to the overlay inputs of the Bt471, Bt475, Bt477, or the Bt478.

With proper synchronization and raster scaling through the feature connector common on EGA cards, direct superposition of an EGA image over a VGA display is possible without burdening the VGA interface. This multi-path approach to high resolution windows is inherently faster and more interactive than software driven techniques and compares with hardware window features found on the more sophisticated graphics systems processors. This technique can be done on a pixel-by-pixel or bit-by-bit basis so that the full resolution capability of the multi-frequency monitor can be used.

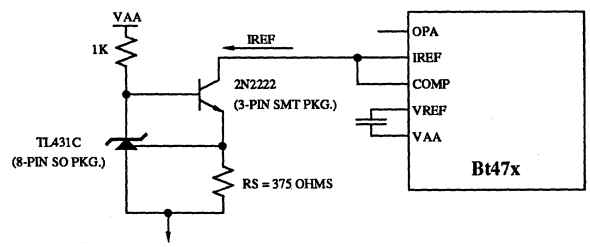

Figure 1. External Current Reference.

Suitable References

The quality of the image produced by the DAC can depend on the stability and regulation of its reference. The Bt47x SMD family offers the user a choice of current or voltage references so that either drop-in compatibility or optimum performance can be provided. The 28-pin DIP version of the Bt476 supports only the current reference mode and is 100% compatible with the IMS G176.

The Bt47x SMD family uses the voltage reference in a closed feedback loop control circuit which provides each individual current cell with a stable voltage reference. This common voltage reference can be externally decoupled at the compensation pin to minimize noise disturbance due to current switching. The combination of closed-loop stability, direct reference decoupling, and compatibility with low temperature coefficient voltage references gives the Bt47x family superior amplitude stability and noise immunity. This results in cleaner images on the graphics display monitor.

Figure 1 shows a typical current reference circuit for the Bt47x family. These components are available in surface mount packages, but notice the current reference approach requires 2 additional passive components. The simplest 4 mA current reference available, a Motorola MCL1304 or Siliconix CR430 type JFET device, offers only ± 15% to ± 25% accuracy, which would only be tolerable in analog-EGA applications or where the monitor contrast adjustment could compensate.

Setup and Sync

While the IBM-PC graphics standards have always provided for separate TTL synchronization lines, traditional analog monitors work with composite synchronization super-imposed on the green video channel. The Bt471/475/477/478 devices provide composite sync on all channels by asserting a low pulse on the SYNC* pin, which turns off an internal 40 IRE pedestal on each video channel.

Blank assertion in the composite format is more reliable (from a noise standpoint) if a 7.5 IRE pedestal distinguishes the black and blank voltage levels. This setup level provides for blacker-than-black CRT beam retraces which reduce visible retrace lines on bright displays. For this reason a selectable setup pedestal is provided to optimize the sync and blank interface for most multi-frequency analog monitors and various international raster video formats (NTSC, PAL, SECAM, CCIR, etc).

Optimum Termination

The analog interface between the RAMDAC and the display monitor must have transmission line properties to assure proper pixel definition on the display. Where TTL monitors can tolerate pulse ringing and cable echoes due to their binary nature, analog displays must settle to within 1% amplitude accuracy well within the pixel duration to render 6- or 8-bit color values faithfully. Double termination of the coaxial cable with the characteristic impedance of the cable is desirable since it lowers the lumped time-constant at the DAC node and attenuates signal reflections from the monitor (or loop through nodes), which can produce pixel smearing or ghosting with cables longer than 2 meters.

A lower termination resistance at the DAC node neutralizes the connector and cable capacitance but forces the DAC to put out as much as 30 mA to produce 1v peak to peak at the monitor input. A lower time constant produces faster transitions and settling, which means crisper pixels on the display with truer color rendition.

Figures 2 and 3 depict the 64 code steps of the IMS G171 and Bt471 driving a 75-ohm doubly-terminated load. A Tektronix 2465 scope (300 MHz BE) was used in the expanded sweep mode to highlight the mid-scale glitch that occurs during the binary 31 to 32 code transition. The characteristic 1/4 - 1/2 - 3/4 scale glitches of the IMS G171 are evident on the 700 mV amplitude waveform.

The expanded scale is calibrated to give graticule square areas of 500 pV-sec (100 mV * 5 ns). The mid-scale glitch of the IMS G171 consists of clock feedthrough with an approximate impulse area approaching 120 (12 LSB-ns) pV-sec, while the Bt471 mid-scale glitch area is less than 50 pV-sec. Clock feedthrough produces little visible aberration on the monitor since it represents an equal amount of energy every pixel. However, glitch impulse may be visible when it exceeds 1 LSB/BW monitor, since it occurs only on specific code transitions.

Resolution

The Bt477 and Bt478 offers an upgrade path to 8 bits of resolution in the same pin compatible package as the Bt471, Bt475, and Bt476. Figures 4 and 5 show a comparison between 6 bits and 8 bits of resolution for a 3D solid model.

The gray scale shading is limited and annoying to the eye on the 6-bit rendering, offering only 64 shades.

The 8-bit image offers 256 gray shades and fine shading. The 8-bit photo clearly shows the smooth shading required for 3D modeling or professional slide presentations.

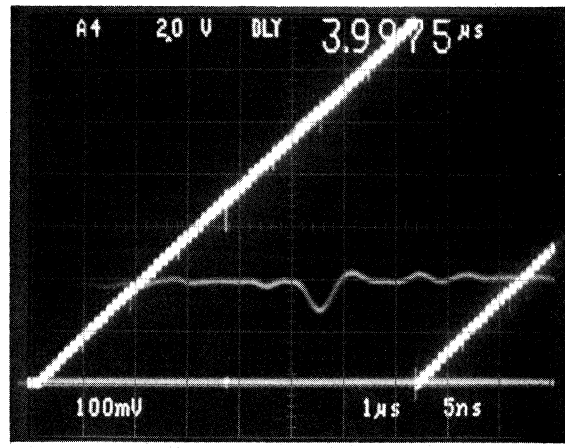

Figure 2. IMSG171 Output Waveform.

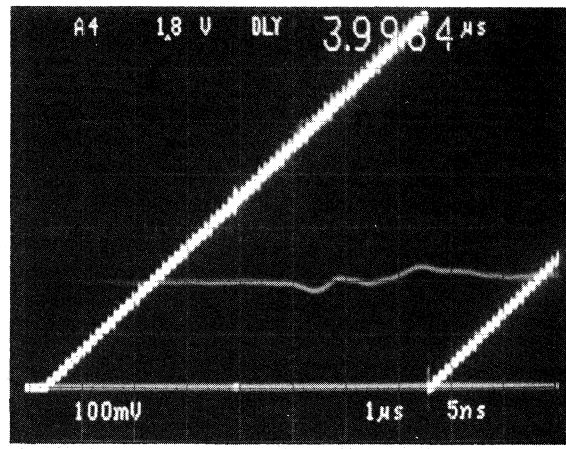

Figure 3. Bt471/478 Output Waveform.

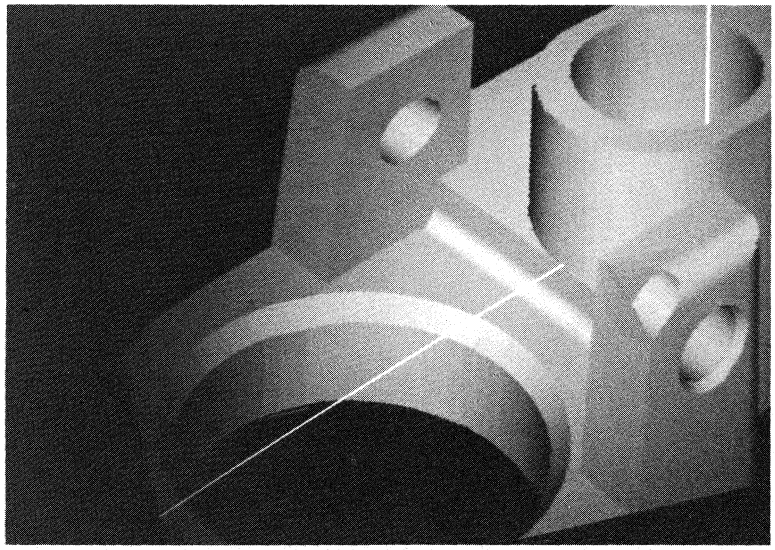

Figure 4. 6-Bit Resolution Example.

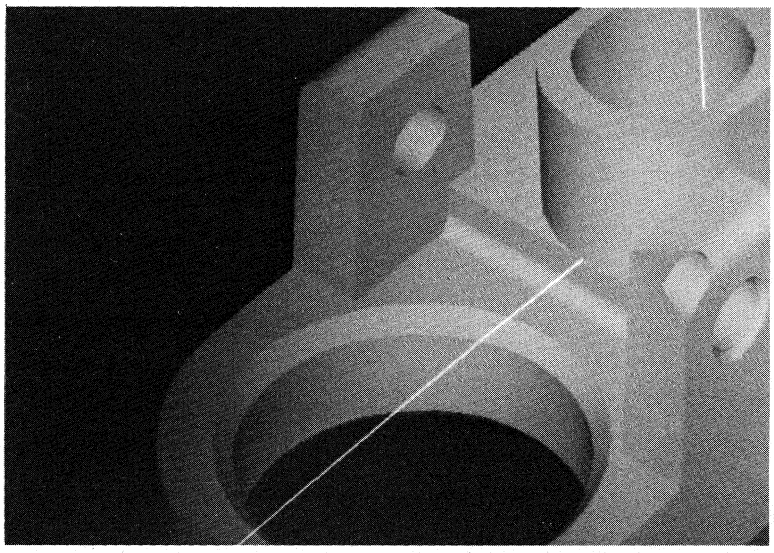

Figure 5. 8-Bit Resolution Eample.

Packaging

The IMS G171 is photographed side by side with the Bt47x in Figure 6. The Bt47x is shown in the ceramic 44-pin package and occupies considerably less area than the IMS G171 in the 28-pin DIP.

Note the internal chip capacitor in the specially-tooled 28-pin DIP package of the IMS G171. The chip capacitor mounted in the cavity serves to compensate for the DIP package inductance. This is less effective in terms of glitch suppression than the inherently lower inductance of the 44-pin PLCC package.

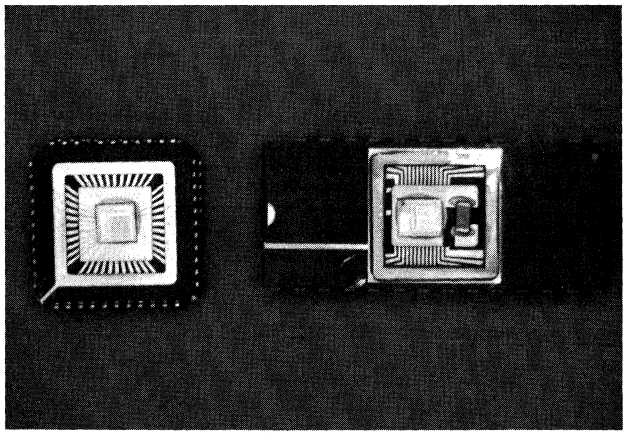

Figure 6. Packaging Comparison.

PC Board Layout Tips

Printed wiring board design considerations for analog output devices can be more critical than for pure digital. Four-or-more layer boards are better for lower power and ground noise as well as for segregating the analog outputs and reference from the digital inputs. This becomes even more important as speed migration from 25 MHz to 75 MHz dictates faster devices which generate more power supply spikes and radiation. Migrating from 6 bits per channel to 8 bit quantization compounds the need for low inductance power and ground returns if true color rendition and low electromagnetic emissions are to be achieved.

The effect of supply and ground noise and digital edges on the palette DAC is to produce image-dependent artifacts on the display which are especially perceptible when images are superimposed. Even the best CMOS DACs couple about 10% of any supply noise to the analog output. Care should be taken to limit supply noise at the DAC (in the bandwidth of the analog channel, typically the pixel rate) to 10 times the amplitude of the least significant bit.

Multiple ground planes make it possible to isolate the DAC current return to the system supply from other digital circuitry while maintaining low plane-to-plane potentials which affect the digital noise margins and contribute to electromagnetic emissions. It is desirable to reduce DAC ground noise to less than 10 mV during the active display line for clean looking 6- and 8-bit displays.

Performance Comparision Chart

	Bt475/471	Bt476	Bt477/478	IMS G171
IBM PS/2 Compatible	YES	YES	YES	YES
Number of Displayable Colors	256 + 15	256	256 + 15	256
Maximum Number of Bit Planes	12 (8 + 4)	8	12 (8 + 4)	8
Total Palette Size	256K	256K	256K or 16M	256K
Frequency (MHz)	35 / 50 / 66 / 80	35 / 50 / 66	35 / 50 / 66 / 80	35 / 50
Palette Read-Back	YES	YES	YES	YES
Sync on Video	YES	NO	YES	NO
Full Scale Reference	Voltage or Current	Voltage or Current	Voltage or Current	Current
Optional Internal Reference	YES	NO	YES	NO
RS-343A and CCIR Standards	YES	YES	YES	NO
Analog Output Comparators	YES	NO	YES	NO
Power Down Capability	YES	NO	YES	NO
Integral Linearity	0.25 LSB (0.4%)	0.5 LSB (1%)	1 LSB (0.4%)	0.5 LSB (1%)
Differential Linearity	0.25 LSB (0.4%)	0.5 LSB (1%)	1 LSB (0.4%)	monotonic
Glitch Impulse	75 pV-sec	75 pV-sec	75 pV-sec	200 pV-sec
Overlay Capability	YES	NO	YES	NO
Rise/Fall Time	3 ns	3 ns	3 ns	8 ns**
Memory Technology	Fully Static	Fully Static	Fully Static	Req. Constant Clock***
Compatible Family	YES	YES	YES	Almost*
Monolithic	YES	YES	YES	On Board Chip Cap
Surface Mountable	YES	YES	YES	YES
Package	44-pin PLCC	44-pin PLCC or 28-pin DIP	44-pin PLCC	28-pin DIP or 32-pin PLCC

*Due to limited number of pins in the INMOS pin-out, trade-offs have been made between products. For example, the pin that allows the color palette to be read in the IMS G171/3/6 is used for SYNC in the IMS G170/2/4 thereby inhibiting the ability to read back the color palette on the later parts. Also, the 6-bit data used in the IMS G170/1/2/3 can not be used directly with the 8-bit IMS G174/6 because the 6 bits are located in the LSBs and would result in an output 1/4 the brightness. Brooktree has a 6/8-bit pin that allows 6-bit code written for either the Bt471/475/476 or the IMS G170/1/2 to run on the 8-bit Bt477/478. Comparisons are based on the Brooktree Bt471/476/478 specification sheet L478001 Rev. L, Bt475/477 specification sheet L477001 Rev. B, and the IMS G171 specification sheet 42-1008-00 dated April 1987.

**Single 75-ohm termination, Bt47x family rated for 75-ohm doubly-terminated loads.
***Pseudo-static RAM cell

Troubleshooting Your Brooktree CMOS VIDEODAC or RAMDAC

Power Supply Considerations

Brooktree devices offer power supply rejection, however, this noise rejection decreases with frequency. Therefore, the noise on the power pins must be kept to a minimum. In particular, about 10% of any frequency components over about 1 MHz will be coupled onto the output. The VREF and COMP pins should be checked to assure noise is minimized. This can be accomplished by keeping PCB and lead lengths to decoupling capacitors short and wide. Decoupling VREF and COMP pins to VAA is vital to reducing switching noise and overshoot on the DAC output.

Another useful technique is to mount a three terminal regulator close to the power supply pins to provide immunity to power supply transients, and use the fact that the regulator will provide excellent power supply ripple rejection. When operating from a switching supply with greater than 100 mV of noise, a two stage VAA decoupling filter is advisable. A CLC pie filter combination ahead of the attenuator bead should have a time constant value much less than the switching frequency to be effective. When using a VAA filter, ensure that VAA power is applied before the inputs to prevent latch-up.

The DAC can have significantly more noise than is seen on the supply bus. Always probe the power supply signals with an oscilloscope probe at the device pins. Probe ground (AC coupled) less than one inch from DAC ground. Measure VREF noise relative to VAA.

Decoupling Capacitors

One of the most common problems is choosing the proper power supply decoupling capacitors and keeping the leads short enough. Refer to recommended capacitor types in individual datasheets. All capacitors exhibit a self-resonant point at which they no longer look like capacitors, but inductors. This resonant point is a function of frequency, capacitor material, lead length, and the PCB trace length of the power and ground traces where the capacitor is soldered. Above self resonance, a capacitor looks like a series resonant inductor (with approximately 1 nH per 0.1 inch of lead length).

For example, a 0.1 µF ceramic radial lead capacitor with 1/4 inch leads generally resonates around 10 MHz. A 0.01 µF ceramic radial lead may resonate around 40 to 60 MHz while a 0.01 µF ceramic chip capacitor may resonant around 400 MHz.

As power supply transient frequencies approach the resonant point, the capacitor offers less effective filtering. At resonance, it is neither a capacitor nor inductor. Past resonance, it becomes an inductor and may exhibit transmission line effects.

To overcome these problems, the parallel connection of a 0.1, 0.01, and 0.001 µF capacitors will generally overcome the most difficult transients. For the lower frequencies, a 10 µF tantalum capacitor is the best choice, mounted near the power and ground pins.

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Attenuator Beads

The purpose of the ferrite attenuator beads is twofold. First, they isolate fast transients (i.e., less than 1 ns) on the regular PCB power plane from the device. They will reduce any fast transients and act as increasing AC resistance with frequency. These frequency vs. impedance characteristics are diagramed in Application Note 1. Therefore, a decoupling capacitor close to the bead and the DAC power pin for long lead length is needed. Second, the ferrite beads also isolate high-frequency noise generated by the VIDEODAC or RAMDAC from being coupled back onto the main PCB power plane.

Experience has found that the ferrite beads are usually not required where the video bandwidth is less than one tenth the time constant of the logic. As an approximation, if the clock rate is less than 10 MHz, beads are usually not necessary but become increasingly important for frequencies above 50 MHz.

Many of Brooktree's devices have signal edges on the order of 2 or 3 ns, which produce harmonic components in the 300 MHz to 500 MHz range. The beads attenuate these components from the PCB supply planes.

When using Surface Mount Technology (SMT) beads, watch the current rating. Bipolar DACs may use ferrite breads on their power pins for stability, while CMOS DACs are for noise rejection. Attenuator beads in the DAC ground return must have tens of ohms of resistance at high frequency to be an effective attenuator. However, this can produce ground potentials of greater than the intrinsic noise margin when DAC currents are greater than 100 mA. Therefore, ground beads are not recommended for DACs with dynamic currents of greater than 100 mA.

Digital Input Considerations

Some of the newer TTL logic families have very fast rise/fall times. It is possible for these fast transients to couple onto the analog outputs, resulting in excessively noisy analog signals.

Possible solutions are to put a 33 to 100 ohm limiting resistor in series with the digital inputs at their source, or use a resistor terminating network (220/330 ohm) at the expense of additional power. A slower logic family, such as ALS, LS, may be used if possible to reduce the input rise/fall times where pixel rates are less than 25 MHz. Noise on three-state lines should be avoided through termination.

ESD and Latchup Considerations

Correct ESD handling procedures are required to prevent damage which can produce symptoms of catastrophic failure or an erratic device behavior with somewhat leaky inputs.

Latch-up can be prevented by assuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5v.

No Video Information

Verify that all power pins have the correct voltage. If a constant DC output is generated, it indicates that the DACs are probably not functioning correctly. The voltage on the VREF pin should be checked first to verify that the external voltage reference (if used) is operational. Decoupling of VREF to VAA near the DAC is vital to reduce switching noise on the DAC output.

The voltage on FS ADJUST should be very close to the VREF voltage. If the device contains an on-chip reference, the measured voltage at the FS ADJUST pin should be approximately equal to the specified internal reference voltage. Offsets of greater than 10 mV may indicate damage to the internal op-amp.

The COMP pin must be coupled to VAA through a ceramic capacitor and the lead lengths kept to an absolute minimum. The voltage on the COMP pin is nominally 3v to 4v. A voltage close to 0v or 5v indicates a bad COMP capacitor, a COMP trace shorted to power or ground, or a bad device. The output traces for video information should be checked for shorts to power and ground supplies.

The control, pixel, overlay input setup and hold times should be verified. To ensure reliable operation over the full temperature and power supply range, the CLOCK input should be buffered by a single dedicated buffer that assures fast edges with glitch free levels.

Incorrect Analog Output Information

If sync and blank information are output, but they are not the correct levels, verify the RSET resistor value, the voltage on VREF and FS ADJUST (they should match), and the output load. When looking at the voltage levels on the video outputs, the oscilloscope probe must have 75-ohm termination, to form the other termination of the doubly-terminated 75-ohm load.

If the sync and blank levels are correct, the analog section of the device is probably operational, and the problem is probably the microprocessor or pixel data interface.

Ensure that all of the control registers and color palette RAM are properly initialized following power-up. The contents of the control registers and RAM may be read back by the MPU to verify their contents. The chip select or chip enable input should always be a logical one, except when the MPU is accessing the device.

Nonlinear Gray Scale Analog Output

If the gray scale video appears to be nonlinear or compressed at one end of the gray scale, the compliance limits of the device are probably being exceeded.

Voltage levels on the analog outputs outside the compliance limits forces the DACs to operate in a nonlinear fashion. The greater the exceeded voltages, the more nonlinear the D/A operation will be. Incorrect output loading, a wrong value for the RSET resistor, or an incorrect reference voltage are the primary causes.

Noisy Analog Output

Excessively noisy analog outputs indicates that either the power supply pins, the COMP pin, or the VREF input have an excessive amount of power supply noise that is not being decoupled, or there is excessive undershoot/overshoot on the digital inputs.

Refer to Application Note 1 or contact the Brooktree technical hotline for further assistance at:

1 (800) VIDEO IC

RAMDAC Initialization

Brooktree RAMDACs need to be initialized through the microprocessor port after power-on. The initialization procedure differs slightly depending on how many control registers the RAMDAC contains. Using the Bt458 as an example, Figure 1 shows the four control registers, pixel port (fast port), MPU port and bus control (slow port), and the DAC outputs. The microprocessor initializes the Bt458 through the MPU port.

Bt458 Initialization Procedure

1. Initialize the control registers:

- Write 0,0 to C1,C0 ; set to write address register
- Put 06H on data bus ; address of command register
- Pull R/W* low ; write mode
- Strobe CE* ; write address to address register
- Write 1,0 to C1,C0 ; set to write command register
- Put 40H on data bus ; data to command register
- R/W* low, Strobe CE* ; write to command register

Note: 40H in the command register configures the device as follows:

- 4:1 mux
- Enable color palette RAM
- Blink rate = 16/48
- Blink disable
- Forces overlay inputs to logical zero

Repeat the control register sequence using the following values to initialize the other command registers. Set R/W* and strobe CE* after every line.

C1,C0	Data Bus	
• 0, 0	04H	; write read mask address
• 1, 0	FFH	; FF hex to read mask register
• 0, 0	05H	; write blink mask address
• 1, 0	00H	; 00 hex to blink mask
• 0, 0	07H	; write test register address
• 1, 0	00H	; 00 hex to test register

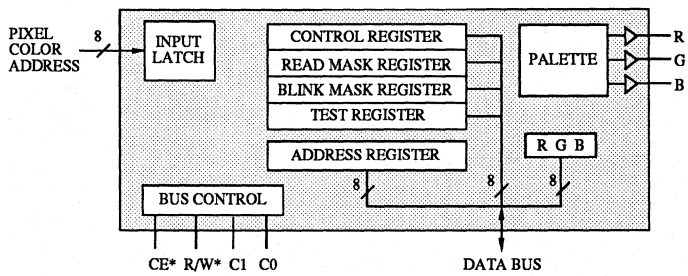

Figure 1. Bt458 Ports.

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2. Write the color palette starting with location 00 hex. Set R/W* and strobe CE* after every line.

C1,C0	Data Bus	
• 0, 0	00H	; write palette address 00H
• 0, 1	rrH	; write red value (hex)
• 0, 1	ggH	; write green value (hex)
• 0, 1	bbH	; write blue value (hex)

Note: At this point, the palette address pointer auto-increments to address 01H. One must rewrite the address pointer to access locations other than 01H.

C1,C0	Data Bus	
• 0, 1	rrH	; write red value (hex)
• 0, 1	ggH	; write green value (hex)
• 0, 1	bbH	; write blue value (hex)

3. To read back the palette or control registers, use the same sequencing but set R/W* high.

4. To write/read the overlay palette; set C1,C0 to 1,1 and continue as in step 2.

This application note explains a basic program flow for initializing a Bt458 RAMDAC. The Brooktree databook contains further information concerning operation of this and other RAMDACs.

Bt458 INITIALIZATION PROGRAMMING SEQUENCE

TABLE OF OPERATIONS

	STEP	CE*	R/W*	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
Command Register	1	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE ADDRESS REGISTER
	2	↑	X	X	X	0	0	0	0	0	1	1	0	DATA 06H INTO ADDRESS REGISTER
	3	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO CONTROL REGISTER
	4	↑	X	X	X	0	1	0	0	0	0	0	0	DATA 40H INTO CONTROL REGISTER
Read Mask	5	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	6	↑	X	X	X	0	0	0	0	0	1	0	0	DATA 04H TO ADDRESS REGISTER
	7	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO READ MASK
	8	↑	X	X	X	1	1	1	1	1	1	1	1	DATA FFH TO READ MASK
Blink Mask	9	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	10	↑	X	X	X	0	0	0	0	0	1	0	1	DATA 05H TO ADDRESS REGISTER
	11	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO BLINK MASK
	12	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO BLINK MASK
Test Register	13	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	14	↑	X	X	X	0	0	0	0	0	1	1	1	DATA 07H TO ADDRESS REGISTER
	15	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO TEST REGISTER
	16	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO TEST REGISTER
Write Color Palette	17	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	18	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO ADDRESS REGISTER
	19	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE RED
	20	↑	X	X	X	RED VALUE								DATA TO RED PALETTE
	21	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE GREEN
	22	↑	X	X	X	GREEN VALUE								DATA TO GREEN PALETTE
	23	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE BLUE
	24	↑	X	X	X	BLUE VALUE								DATA TO BLUE PALETTE
Read OVL0	25	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	26	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO ADDRESS REGISTER
	27	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	28	↑	X	X	X	RED VALUE								RED VALUE AVAILABLE
	29	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	30	↑	X	X	X	GREEN VALUE								GREEN VALUE AVAILABLE
	31	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	32	↑	X	X	X	BLUE VALUE								BLUE VALUE AVAILABLE

2

Building a 4K Look-up Table with the Bt457

Palette Applications

The need for a 4K look-up table for graphics is found in such applications as medical imaging, solids modeling and electronic publishing. A discrete implementation using three Bt457 single channel RAMDACs, twenty-four 4K x 4 static RAMs and miscellaneous MSI circuitry is all that is needed to implement this application.

The circuitry for one of the three channels is shown in Figure 1. This would be duplicated for each of the red, green and blue channels. Each channel interfaces to the twelve plane frame buffer with two F374 devices. Four sets of 12-bit pixels are supplied to the registers from the frame buffer. Since the RGB planes use the same address, these registers can be used for all three channels.

The register's outputs are sent to the address inputs of the 4K x 4 static rams. Eight of these are needed for each of the three channels. The output data is then input into another set of F374 registers. The data has now been reduced to eight bits, which are used as pixel data. Four sets (A-D) of 8-bit pixel data are provided to the pixel inputs of the DACs for color generation. This provides 4:1 multiplexing of the Bt457 input.

Mapping the Bt457 internal LUT RAM allows the pixel data to be used as 8-bit data for the D/A converter, or the Bt457 RAMs can be programmed so that gamma correction, image manipulation or window palette switching can be performed.

MPU Interface

The microprocessor interface to the color palette is provided by a 12-bit address bus and an 8-bit data bus for each of the channels.

The address bus is presented to the RAMs by way of two F244 devices. These provide an output enable such that during a display, the F374s are always enabled and the F244s are disabled. The same address would be provided to each of the look-up tables.

The MPU data interface is a bit different. First, a bidirectional bus is needed so that the data stored in the color palette can be read back by the MPU. For this reason F245 devices are used. Second, each of the RGB channels is provided with its own 8-bit data bus. By using a 32-bit bus the red, green, and blue palettes can be written simultaneously. A counter can be included to generate the addresses so that the 4K addresses can be auto-incremented. The direction of the data bus is determined by the value on the RD* line. Eight bits are also needed for the RAMDAC MPU interface.

If direct color generation is needed, the Bt457 palette wouldn't be used as a look-up table, and the pixel address would be the same as the data. If gamma correction, or any other image transformation is needed, then the RAMDAC would need to be programmed accordingly.

Performance

The limiting factor in building the 4K solution discretely is the overall performance of the video generator. The screen resolution is directly related to the speed of the MSI circuitry and the static RAMs.

The delay of the pipelines is as follows:

F374 Clock to Q	10 ns
Static RAM access(read)	20 ns
F374 Setup Time	2 ns
Interconnect delay	4 ns
Total delay	36 ns

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Because 4:1 multiplexing is used, the time for each pixel generated is 36/4 = 9 ns. This corresponds to a clock frequency of 111 MHz. With this implementation a 1280 x 1024 resolution system (with 60 Hz refresh) can be achieved. To increase the performance of the system, use of faster VRAMs (33 MHz), or a 2:1 multiplexing between the VRAMs and LUT is required.

An 8:1 LUT architecture could also be used. This would require multiplexing the output of the LUT to the Bt457 and also a significant cost increase due to a doubling in the amount of SRAMs. Another approach to increase the resolution of the system is to use faster RAMs as they become available. By using SRAMs with a 15 ns access time, the given architecture can achieve a video rate of 129 MHz.

True Color Application

A true color (36 plane) system can be achieved by multiplexing data from a frame buffer with the LUT output as shown in Figure 1. The F374 outputs would be disabled via True Color Select, and the true color data would be enabled on the red, green and blue channels.

Using the Brooktree Bt457 RAMDAC, a 4K color palette system can be created with the use of standard MSI products and CMOS static RAMs. The 4K palette provides enough simultaneous color for modeling applications and medical imagery. It can be easily implemented using the methods described in this application note.

This information is intended for stimulating design interest and has not been breadboarded. Brooktree accepts no liability for designs contained in this application note. All users are cautioned to verify their own design.

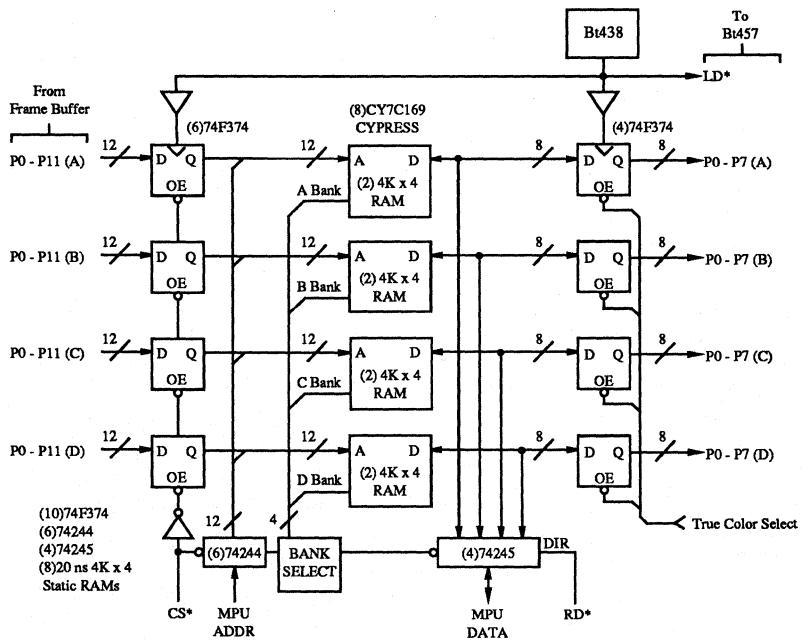


Figure 1. 4K Look-up Table Solution using the Bt457.

Bt471/476/478 Power Saving Features

Various circuit configurations will allow significant savings in power requirements when used with the Bt471/476/478. Laptop computers which support VGA graphics capabilities represent an application that can benefit from utilizing these power saving configurations. Battery-operated portable laptops use liquid crystal displays which do not require the VGA RAMDAC to be active, therefore the Bt471/476/478 power saving modes can be used to reduce supply requirements and extend battery life.

The Bt471/476/478 may be powered down in the following ways:

Power Down Mode	Registers/Memory Accessible
• VREF - shut down the DACs	Yes
• IREF - shut down the DACs	Yes
• Stop the clock	No

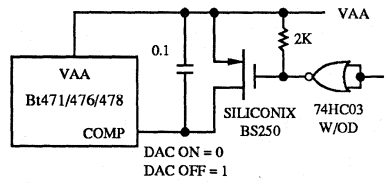
VREF Power Down Mode

The VREF implementation provides an order of magnitude improvement in amplitude stability and noise immunity over an IREF implementation. For this reason, using a voltage reference is recommended over a current reference.

To eliminate the full scale output current and associated supply current to the DACs, open circuit the RSET resistor or pull the COMP pin up to VAA. Figure 1 shows a circuit for pulling the COMP pin to VAA. The 0.1 µF capacitor acts as a bypass capacitor between the VAA and COMP pins. This capacitor should be mounted as close as possible to the RAMDAC, with the leads kept short. The P-channel MOSFET with the source connected to VAA turns on when the gate voltage drops below four volts. The output of the 74HC03 open drain NOR gate pulls up through a 2K-ohm resistor to VAA. A logical one at the input to the NOR gate turns the DACs off.

Shutting down the DACs typically cuts the supply current by forty percent. For the Bt471, each DAC outputs three times the current flowing through the RSET resistor. To get a DAC output current of 21 mA, the current through RSET must be 7 mA (the actual value will be slightly less to achieve the 19.05 mA value specified in the databook). When the DACs are shut off, the total current saved will be 3 x 21 = 63 mA. At nominal supply voltage and room temperature, the Bt471/476/478 typically requires 160 mA. The power down current is therefore 160 - 63 = 97 mA.

Caution: Brooktree guarantees linearity specifications for output voltages up to 1.6 volts and for output currents down to one half of full scale.



Siliconix alternate sources:
Philips #BS250
Topaz #VP106

BS250 Typical Parameters:
IDSS @ VGS = 0v = - 0.5 mA
VGS @ ID = 1 mA = - 2.75v
BVDSS @ VGS = 0v = - 20v

Figure 1. DAC Shutdown Using the COMP Pin.

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IREF Power Down Mode

For systems using a reference current (IREF), shut down the DACs by open circuiting IREF. Like the VREF mode above, the IREF current is proportional to the DAC output current. Figure 2 shows a circuit for supplying a constant current to the IREF pin. Drive the base of the NPN transistor with a low TTL logic signal to turn the DACs off. In the power down mode, the RAMDAC is fully register/memory compatible. Powering down the Bt471/476/478 typically cuts the supply current by forty percent and also saves the IREF current. For the Bt471 as discussed in the previous section the supply current is 160 - 63 - 7 = 90 mA.

Stopping the Clock

This mode is useful in applications where the designer does not need register compatibility or active video. The Bt471/476/478 static RAM does not require clocking to retain memory data. With the DACs on, this power-down mode saves about 10 mA. Shutting off the clocks with the DAC powered down saves 2 to 3 mA. See Figure 3.

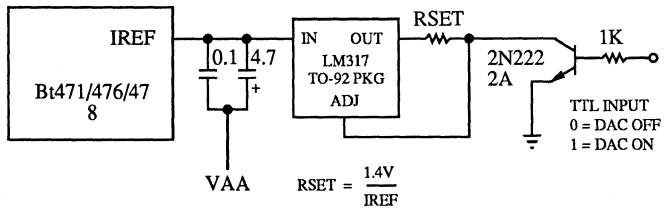

Figure 2. Open Circuit IREF.

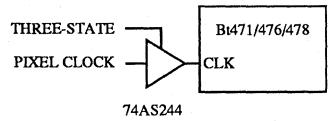

Figure 3. Clock Stopper Circuit.

Summary

This application note shows several methods to reduce power consumption on Brooktree's Bt471/476/478 RAMDACs. Designers will find these power savings useful in laptop computers with VGA graphics capabilities. System designers may use the Bt471/476/478 power-down capabilities to differentiate their products and improve performance.

Bt475/477 Power-Down RAMDAC

Brooktree has developed the Bt475 (6-bit) and Bt477 (8-bit) power-down RAMDACs specifically for laptop applications. The Bt475/477 feature software controlled power-down capabilities, reducing standby supply current to as low as 1 mA with register compatibility. The Bt475 and Bt477 are pin-compatible with the Bt471/476/478 RAMDACs, facilitating drop-in replacement.

Also included on the Bt475/477 are on-chip analog output comparators, on-chip voltage reference, and circuitry to prevent "sparkling" when the MPU accesses the color palette RAM during active video.

Support Components

Brooktree's Technical Hotline has received many requests for assistance in identifying and locating components used with Brooktree products. Brooktree's databook and datasheets recommend components that are not always available in all areas. The following is a list of suggested manufacturers and components that will assure optimum performance of Brooktree products.

Crystal Oscillators

Many of the Brooktree CMOS RAMDACs require a positive ECL differential clock. Common 10K and 100K ECL crystal oscillators powered from +5 volts will provide this positive clock.

The following crystal oscillators come in a 14 pin DIP outline package. Pin 7 is ground, pin 14 is +5V, pin 8 is the clock output, and when a complementary output is available, it is on pin 1.

Manufacturer/ Supplier	Model/Part Number	Description
Monitor Products 502 Via Del Monte Oceanside, CA 92054 (619) 433-4510	970EA 970EA1 970T	• For 10K ECL clocks to 200 MHz, case floating, open emitter output. • For 10K ECL clocks to 200 MHz, case floating, complementary open emitter outputs. • For TTL clocks to 80 MHz.
Vectron Laboratories, Inc. 166 Glover Ave. Norwalk, CT 06850 (203) 853-4433 *In the U.K.:* Lyons Instruments (099-24) 67161	CO-633 CO-450	• For ECL clocks to 200 MHz • For 100K complementary ECL clocks from 5- 400 MHz
Fox Electronics 6225 Presidential Court Fort Myers, FL 33907 (813) 482-7212	F5L F1100	• For 10KH ECL clocks to 200 MHz - Pin 7 (case ground) is an option • For TTL clocks to 80 MHz
Conner-Winfield 1865 Selmarten Road Aurora, IL 60505 (312) 851-4722	ECLA-1 ECLA-2 S15R6 S17R6	• For 10K, 8-150 MHz, case tied to pin 14 • For 100K, 8-150 MHz, case tied to pin 14 • For TTL, 0° to 70° C, 256 KHz-80 MHz • For TTL, 55° to 125° C, 256 KHz-80 MHz

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Ferrite Beads

Decoupling the power to Brooktree's products through a ferrite bead is recommended to prevent power supply noise from being coupled into the video outputs. Use of a ferrite bead is also recommended for suppressing interference caused by the fast switching times of the DACs.

Ferrite beads have a very low impedance at low frequencies which increases at higher frequencies. Refer to **AN-1** for a typical impedance curve. Beads are selected for their impedance at a standard frequency of 100 MHz, typical.

Manufacturer/ Supplier	Model/Part Number	Description
Fair-Rite Products Corporation P.O.Box J Wallkill, NY 12589 (914) 895-2055 *In the U.K.:* Apex Inductive Devices (01) 903-2944	2743001111 2743021446	• Axial lead, 71 ohms @ 100 MHz • Surface mount, 89 ohms @ 100 MHz
TDK Corporation 4711 West Golf Road #300 Skokie, IL 60076 (312) 679-8200	CB30-1210 BF45-4001	• Surface mount, 52 ohms @ 100 MHz • Axial lead, 85 ohms @ 100 MHz
Ferroxcube 5083 Kings Hwy Saugerties, NY 12477 (914) 246-2811 Canada: (416) 561-9311	5659065-3B	• 38 ohms @ 100 MHz

Sockets

For high speed operations and proper heat dissipation, it is generally recommended that Brooktree products be soldered directly to the PC board. However, when prototyping or operating at clock rates less than 50 MHz, or where some degradation of performance is acceptable, sockets can be used. The following is a listing of commonly requested sockets.

Manufacturer/ Supplier	Model/Part Number	Description
AMP Inc. Harrisburg, PA 17105 (717) 564-0100 Canada: (416) 475-6222 U.K.: 44-1-954-2356 W. Germany: 49-6103-7090 Japan: 81-3-404-7171	641444-2 641746-2 641343-2 641747-2 641345-2 641749-2 643151-2 643066-2	• 28 pin, surface mount • 28 pin, solder tail • 44 pin, surface mount • 44 pin, solder tail • 68 pin, surface mount • 68 pin, solder tail • 84 pin, surface mount • 84 pin, solder tail
Burndy Corporation P.O. Box 5200 Richards Ave. Norwalk, CT 06856 (203) 838-4444	QILE28P-410T QILE44P-410T QILE68P-410T QILE84P-410T QILEXT-1	• 28 pin, solder tail • 44 pin, solder tail • 68 pin, solder tail • 84 pin, solder tail • PLCC Removal tool
McKenzie Technology 44370 Old Warm Springs Blvd Fremont, CA 94538 (415) 651-2700	PLCC-28-P-T PLCC-44-P-T PLCC-68-P-T PLCC-84-P-T	• 28 pin • 44 pin • 68 pin • 84 pin

Sockets (continued):

The following sockets are recommended for use with Brooktree's PGA packages.

Manufacturer/ Supplier	Model/Part Number	Description
Augat 33 Perry Ave. Attleboro, MA 02703 (617) 222-2202 U.K.: (0908) 67665 W. Germany: (089) 576085 Japan: (03) 465-8457	PPS069-2A1130-L PPS084-2A1212-L PPS132-2A1414-L PPS145-2A1521-L	• 69 pin PGA, for 68 pin PGA package* • 84 pin PGA* • 132 pin PGA* • 145 pin PGA* *PGA package to PC board standoff distance : 0.166"
Robinson Nugent, Inc. 800 East Eighth St. New Albany, IN 47150 (812) 945-0211 Switzerland: (066) 229822	PGA-068CM3-S-TG PGA-084AM3-S-TG PGA-132AM3-S-TG	• 68 pin PGA* • 84 pin PGA* • 132 pin PGA* *PGA package to PC board standoff distance : 0.175"
Yamaichi U.S. Distributers: Nepenthe 2471 East Bayshore Rd. Suite 520 Palo Alto, CA 94303 (415) 856-9332	IC93-10803-G4	• 84 pin PGA* *PGA package to PC board standoff distance : 0.236"
McKenzie Technology 44370 Old Warm Springs Blvd Fremont, CA 94538 (415) 651-2700	PGA69H003B1-1130T PGA84H003B1-1212T PGA132H003B1-1414T PGA145H003B1-1521T	• 69 pin PGA, for 68 pin PGA package* • 84 pin PGA* • 132 pin PGA* • 145 pin PGA* *PGA package to PC board standoff distance : 0.165"

1.2V Voltage References

To meet RS170/RS343 tolerances, Brooktree DACs require a voltage reference of 1.2V ± 5%. The following devices meet this requirement.

Manufacturer/ Supplier	Model/Part Number	Description
National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051 (408) 721-5000	LM385Z-1.2	
Motorola Semiconductor Products 5005 East McDowell Road Phoenix, AZ 85008 (602) 244-7100 Japan: (03)440-3311 Hong Kong: 0-223111 U.K.: 0296-35252 W. Germany: (089) 92720	LM385Z-1.2	
Maxim Integrated Products 510 North Pastoria Sunnyvale, CA 94086 (408) 737-7600	ICL8069	
Harris Semiconductor 2450 Walsh Ave. Santa Clara, CA 95051 (408) 996-5000	ICL8069	

Video Buffers

Brooktree's DACs are intended to drive transmission line loads, for which most monitors are rated. Transmission line cable lengths greater than 10 meters can attenuate and distort high frequency pulses. Booster buffers can compensate for some cable distortion but must have 6-12 dB voltage gain into the cable load to be effective. Select buffers with ± 30 mA drive, 2 - 4 volt output swing, and full power bandwidth greater than that of the monitor. When selecting a buffer, consider the thermal and supply voltage requirements. Note: Buffers usually require supply voltages greater than 5 volts.

Manufacturer/ Supplier	Model/Part Number	Description
Elantec 1996 Tarob Court Milpitas, CA 95035 (408) 945-1323 U.K.: 0844-68781	EL2003 EL2020 EL2030	• 3dB/50 MHz Unity Gain into 50 Ω • 3dB/50 MHz Gain ≥ 1 into 50 Ω • 120 MHz, Unity Gain
Harris Semiconductor 2401 Palm Bay Road Palm Bay, FL 32905 (305) 724-7418	HA-5033 HA1-2542	• 3dB/50 MHz Unity Gain into 50 Ω • 3dB/50 MHz Gain 2 into 150 Ω
Comlinear Corporation 4800 Wheaton Drive P.O. Box 20600 Fort Collins, CO 80522 (303) 226-0500	CLC400/1	• 3dB/200 MHz Gain 2 into 100 Ω

Other Components

Metal film resistors are recommended for use with Brooktree's products because of low temperature coefficients and low current noise.

For assistance in locating other components, call the Brooktree Technical Hotline at 1 (800) VIDEO IC.

Mixed Signal Layout Considerations

Digital logic PCB design practices that rely on the logic noise margins to assure correct operation are not adequate to obtain the full performance advantage of Brooktree's family of mixed signal products. The coexistence of digital and analog circuitry requires special layout techniques to assure reliable operation and preserve analog signal fidelity.

The goal for a well designed, high-speed mixed-signal PCB layout is to reduce the noise generation sources and isolate the analog circuitry from these sources. This application note will show PC-VGA layout as an example, but these techniques apply to other high-speed designs.

Power Supply Planes

A well designed power distribution network is critical to eliminating logic switching noise that could be coupled into the analog outputs. Since the power system is common to all circuitry, noise reduction and isolation techniques must be used. Common isolation techniques include separate ground and power planes with each plane partitioning the analog and digital circuitry into separate areas.

In mixed signal designs, a multilayered board can use separate planes as shields to isolate the analog traces from the noise sources. Noise sources come from power supply and digital switching. The recommended technique to isolate digital switching noise is to separate the digital and analog signal planes with the ground plane. This also provides a clean analog signal return path from the video output connector to the chassis ground at the edge connector that preserves signal fidelity.

Figure 1a shows a solid ground plane. This technique is usually satisfactory when the DAC can be placed close to the edge connector. This prevents excessive digital currents from inducing noise aberrations in the analog ground.

Figure 1b shows a split ground plane which reduces the digital ground return currents from mixing with the analog ground currents. This technique is recommended by Brooktree to achieve optimum isolation of the analog circuitry. The two sections should connect at the edge connector which is the point of lowest impedance.

Figure 1c is a method used when isolation is needed but the analog components must be placed away from the edge connector. Analog ground current flows out of the isolated analog area and over a portion of the digital ground plane on its way to the edge connector. This localization method reduces the intermixing of digital and analog currents but does not completely isolate them.

Power plane layout techniques are illustrated in Figure 2. Figure 2a shows a solid power plane which can be used when minimal power switching noise exists.

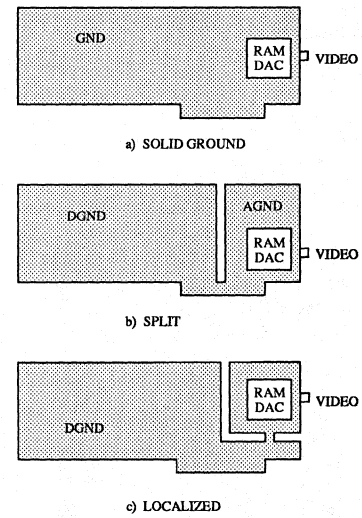

Figure 1. Ground Planes.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

Brooktree®

In Figure 2b, the digital plane feeds the analog plane through a ferrite bead. This technique is recommended to isolate the analog section from digital switching noise of the clocks and memory management circuitry. The ferrite bead isolates the digital switching noise from the analog circuitry. The analog circuitry noise is also isolated from the power supply. The blocking results in a potential difference across the bead when one plane contains large amounts of high frequency current. Typical values are zero to 20 mV for a 25 to 80 MHz frequency range. Do not use an inductor in place of a ferrite bead. Inductors may form a tuned circuit with the RAMDAC and its package parasitic. This can result in a resonance at operating frequencies causing oscillations on the video output. The recommended ferrite bead (Fair-Rite 2743001111) in Brooktree's databook looks similar to a low pass filter with 71 ohms impedance at 100 MHz.

Figure 2c shows an analog plane in the shape of a star or tree. This type of supply plane reduces plane to plane coupling. Use this type of analog supply when the analog plane must overlap digital ground or signal paths. The same is true for digital supply overlapping analog ground or signals. Plane to plane overlap forms a capacitance that acts as a bypass for high frequency signals. The shape of the plane is not as important as reducing the capacitance in the overlap areas with cutouts. The final result may consist of solid plane and cutout areas with traces. Whichever method is used to split the digital and analog area, the desired result is the same: digital noise is isolated from the analog circuitry.

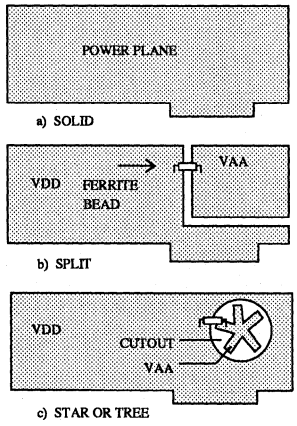

Figure 2. Power Planes.

Power Supply Decoupling

The switching of logic gates and clock drivers that charge and discharge distributed capacitive loads are the major source of switching noise that is coupled into the supply system. The proper technique is to adequately decouple the high current driver devices such as buffers or clock generators. The magnitude of the coupling levels can be determined with Equation 1.

$$I = C_L \, dV/dt \quad \text{where } I = dQ/dt \text{ and } Q = C\,V$$

Equation 1.

A typical clock transition rise time of 2 ns with an output transition of 4v will require a peak transient current of 200 mA from the supply bus. Assume a maximum supply bus drop of 100 mV can be tolerated. Solving Equation 1 for the coupling capacitor yields a value of 0.004 uf. Decoupling capacitors should be placed on all high current high speed devices and placed as close as possible to the power and ground pins.

Transmission Lines

All signal traces should be evaluated to assure adequate termination exists to prevent unwanted signal reflections that are manifested as "ringing". A knowledge of the mechanism that causes signal overshoot and undershoot is required to assure prevention. This general model applies to most signal line cases. Consider the driver in Figure 3 at point A with an output impedance of R_O is driving a line with a characteristic impedance of Z_O. The line length has a delay time T_p that is the time required for the signal at point A to propagate to point B. The load at point B has an impedance of R_L.

Two cases will be considered for this example. In one case the signal edge rate (rise or fall time) is fast compared to the line delay time T_p. The signal arrives at point B after time Tp and electrically has an impedance change from the line Z_O to the load R_L.

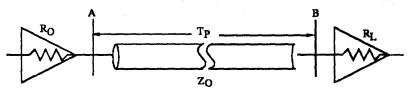

Figure 3. Signal Transmission Line.

This impedance change can be expressed as a reflection coefficient (ρ) at the load point B, and is a function of the line impedance and the load impedance:

$$\rho = (R_L - Z_o) / (R_L + Z_o)$$

Equation 2.

Assuming that R_L equals Z_o and the load impedance matches the line impedance, the reflection coefficient at point B is equal to zero. This condition assures that no portion of the signal is reflected and that the line is matched or terminated. For values of R_L close to Z_o the reflections at point B can be made very small.

Assume that R_L does not equal Z_o and a portion of the signal energy is reflected back to the source point A. Then at time two T_d, the reflected signal energy (determined by Equation 2) arrives at point A. The electrical impedance is again a ratio of the line impedance, Zo, and the driver output impedance, Ro. This impedance change can be expressed as a reflection coefficient (ρ) at the source point A that is a function of the line impedance and the driver output impedance:

$$\rho = (R_o - Z_o) / (R_o + Z_o)$$

Equation 3.

This signal is then reflected from the source to the load and will continue reflections until the coefficients ratio and line resistance slowly degrade the signal strength. This case illustrates that a mismatch or unterminated line leads to overshoot and undershoot of the signal, commonly known as "ringing".

Signal Rise Time

The signal rise time must be evaluated with respect to the line length and propagation line delay time (T_p) to determine if the transmission line effects can be ignored. The propagation delay time is a function of several parameters that are unique for media such as cables, circuit-board trace type, and backplane connections. For PCB traces, the line width, spacing, thickness and dielectric constant all affect the delay time. Equation 4 can be used to calculate the line propagation delay time for a microstrip trace. A microstrip line with a dielectric constant of fiberglass epoxy (E_r = 4.7) would have a propagation delay time of approximately 1.75 ns/ft.

$$T_p = 1.017 \sqrt{(0.475\ E_r + 0.67)}\ \text{ns/ft.}$$

Equation 4.

If the signal rise time T_r is much shorter than the line delay time T_p, and the load reflection coefficient is non-zero, reflections will appear as overshoot and undershoot. The solution is to shorten the line length such that the delay time T_d will allow all the reflected energy to occur within the signal rise time at point A.

Some general guidelines can be used to determine when interconnections are short enough to be treated as lumped. Analog signals are much more sensitive to transmission line effects since preserving signal fidelity and reducing distortion is the goal. For analog signals, a rise time to delay time ratio of 8:1 or greater is necessary before transmission line effects need to be considered. Digital signals are much less sensitive, ratios of 4:1 for threshold sensitive signals such as clocks can be used. Otherwise a 2:1 ratio will give an acceptable signal undershoot. The following table relates the logic family type edge rates to the maximum lumped line length that reflections can be tolerated without termination.

Logic Family	Trise (ns)	Line length(in)
TTL	4	9
AS	1	2.3
F	2	5.5
S	1.6	4
FACT	3	6.5
ALS	6	14

Notes: Trise is defined from 10% to 90% of amplitude. The line length assumes a 4:1 ratio between T_r and T_p.

Table 1. Unterminated Line Lengths vs. Logic Types.

Series Terminated Lines

Overshoot and "ringing" can be controlled by using series dampening or series termination techniques. Series dampening is done by placing a small resistor (10 - 75Ω) in series with the line (see Figure 4).

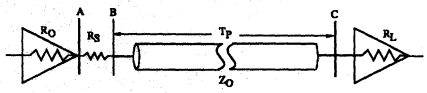

Figure 4. Series Terminated Line.

The resistor should be placed close to the driver output impedance and the value chosen such that the total impedance of R_O and R_S is equal to the line impedance Z_O. The reflection coefficient at point C is large since there is no termination, but the reflection coefficient at point B is zero since $Z_O = R_O + R_S$. Advantages of series termination are less power consumption and only one resistor is required. Disadvantages are the slower propagation delay of the signal with slower edge rates and a resistance load that could limit fan out due to current limiting.

Parallel Terminated Lines

Parallel termination is two resistors placed at the load that form an equivalent Thevenin circuit. The Thevenin resistance is equal to the line impedance, Z_O, and the Thevenin voltage is approximately equal to the load threshold voltage. Figure 5 shows a parallel terminated line. The reflection coefficient at point B is zero since R_1 in parallel with R_2 is equal to the line impedance, Z_O. Advantages of parallel termination are the signal edge rates are not slowed as in the series termination. Sharper signal edges are achieved at the expense of increased power consumption.

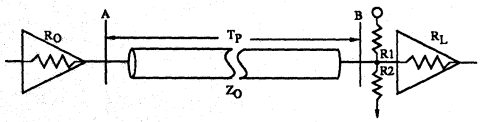

Figure 5. Parallel Terminated Line.

Signal Crosstalk

When signal traces are routed in close parallel, capacitive and inductive coupling between the two lines exists. The amount of signal amplitude that is coupled is determined by several parameters. Figure 6 illustrates an electrical model of two signal traces that are closely coupled.

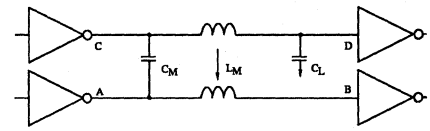

Figure 6. Crosstalk Coupling Model.

The signal on line CD is capacitively coupled into line AB through the mutual capacitance, Cm, and the mutual inductance, Lm. Equation 5 gives an approximation of the crosstalk coupled using the ratio of the line CD load capacitance to the line AC mutual capacitance.

$$dVc = dVs\,(C_M / (C_M + C_L))$$

Equation 5.

For a voltage transition (Vs) of 4V, a load capacitance (C_L) of 100pf and a mutual coupling capacitance (C_M) of 1pf, the approximate coupled voltage due to the capacitive effects would be 40 mV. Clock lines should be routed at a 90 degree angle to signal lines to prevent PCB coupling through these parasitic capacitances and dynamic ground currents.

Clock and Data Feedthrough

Feedthrough noise is any noise that is coupled through the RAMDAC into the analog output and appears as visible aberrations on the screen. The most common sources of this type of noise occur at the pixel data and/or clock inputs. Improper termination of these input signal lines can result in "ringing" noise in the analog output.

Clock feedthrough is a repetitive noise that usually is caused by fast edge rates. Parallel termination can limit the clock excursion about the threshold and reduce the edge rate. Series termination can also be used at the clock source to reduce rise times that cause undershoot.

Data feedthrough is a data dependent phenomena that usually occurs during simultaneous switching of data inputs. These data inputs usually are driven by high speed bipolar logic that often places extreme switching current demand on the RAMDAC input buffers. To reduce the effects of data feedthrough, the power and ground should be adequately bypassed and a robust ground return path to chassis ground provided.

Series termination of the pixel inputs is also a solution. Another method to slow down the edge speed without series terminating every pixel input line is to increase the characteristic impedance of the stripline to the pixel inputs. This has the effect of rounding edges and attenuating high frequency components. If high frequency components cannot be eliminated at the device inputs, sometimes they can be eliminated at the outputs with band limiting techniques.

The CRT is a band limited analog receiver which will reject the high frequency harmonics on the analog output. Since the CRT bandwidth increases with increasing screen resolution, techniques must be employed to control the high-frequency feedthrough noise. Methods for controlling feedthrough are to add passive or active filters to the analog outputs.

The noise in a system not only affects the system and peripherals connected to it, but it can also be transmitted in the form of electromagnetic interference (EMI). Many of the techniques for reducing noise sources will also directly apply to reducing EMI.

EMI

So far this application note has discussed how to separate digital and analog noise and how to reduce digital noise. In today's office or home with many electronic devices, EMI must be below specified limits so neighboring electronic devices will not be disturbed. The FCC has set limits such as class B emissive radiation standards which apply to equipment manufactured for home or office use. CISPR/VDE and MIL-STD 461 are other specifications which define EMI standards.

Any circuit component that transmits a signal on any path other than the intended route is considered a source of EMI. EMI sources come from active or passive components, signal traces, or interconnections.

EMI emissions are dependent on frequency because the signal wavelengths decrease with respect to the size of potential radiating elements on the PCB. This will also increase the radiated EMI power. To get an idea of how higher order harmonics increase with edge rates, consider Figure 7.

The high end of the frequency domain is determined by the signal edge rate. Slowing down edge rates will not only reduce circuit noise, it will reduce the radiated power. The first corner frequency, F1, is determined by the pulse width while the edge rate determines the second corner frequency, F2. The range between F1 and F2 is bounded by an envelope of - 20 dB per decade slope. Beyond F2 the magnitude of the signal power decreases by - 40 dB per decade. For the case of a single pulse, the frequency domain looks the same but the vertical units change from volts for a repetitive pulse, to volt-seconds for a single pulse. In Figure 7, the fundamental frequency, F0, lies between F1 and F2. The integer multiples of F0 are the harmonics reducing in magnitude, but usually contributing more to EMI.

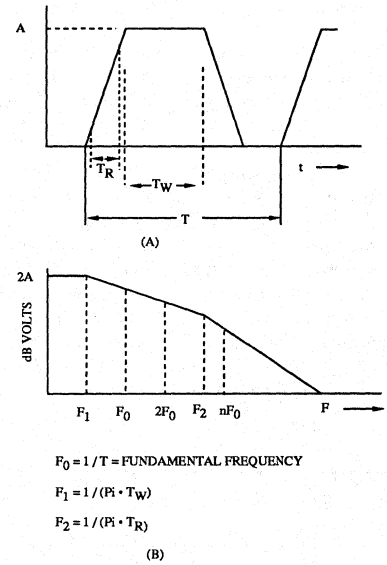

Figure 7.
Time Domain and Corner Frequency

Reducing EMI

Various practices incorporated into the design process will provide a greater possibility of an acceptable EMI profile in the finished product. This saves the trouble of an EMI fix which can be more expensive, time consuming, and less effective than implementing EMI procedures from the beginning of a design.

As mentioned in the previous section, higher frequencies result in greater radiated power. This is because the ratio of wavelength to antenna length determines radiated power for simple dipoles. Other types of antennas and radiation patterns are beyond the scope of this application note and will not be

considered. By reducing the length of interconnections, the wavelength to antenna ratio is changed and radiated power is reduced. For this reason, keep package leads as short as possible. For the same reason, axial lead capacitors are not as good as radial. Any conductive element on the board is a potential antenna.

Bypass capacitors, mentioned earlier for noise reduction, are an effective method of reducing EMI. The purpose of bypass capacitors is to shunt high frequencies to ground. Liberal use should be made of bypass capacitors in any EMI sensitive design.

Signal traces also act as antennas. Long, thin traces are more resistive than wide traces, and thin traces become inductive at higher frequencies. Table 2 shows the impedance of several PCB traces.

At higher frequencies, trace impedance increases. Above about 10 kHz the impedance becomes mainly reactive. This affects EMI in two ways. Increased impedance tends to induce voltage differentials in signal traces. A potential difference may raise a particular point close to a threshold, allowing coupled EMI from another portion of the circuit to cause misoperation. Another effect of a long thin trace is inductive impedance at higher frequencies, acting increasingly like an antenna.

Frequency	w = 1		w = 10	
	l = 30	l = 3	l = 3	l = 30
5 KHz	0.017Ω	0.172Ω	0.001Ω	0.019Ω
50 KHz	0.019Ω	0.215Ω	0.004Ω	0.088Ω
500 KHz	0.087Ω	1.3Ω	0.043Ω	1.21Ω
5 MHz	0.861Ω	12.9Ω	0.438Ω	8.66Ω
50 MHz	8.61Ω	129Ω	4.38Ω	86.6Ω

Table 2. PCB Trace Impedances.

Notes: Widths and Lengths are in mm. Trace thickness is 0.03 mm. Dielectric constant is for epoxy fiberglass.

Containing EMI

Containing the area of EMI requires absorbing or reflecting the radiation already emitted and propagating. Absorbing radiation increases with thickness, conductivity, permeability and frequency. Reflection increases with surface conductivity and wave impedance.

Two ways of containing radiation are EMI fences and boxes. EMI fences surround the radiating components and are usually anchored to the ground plane. For cards plugging side by side into a backplane, this effectively creates a box if all cards have full power and ground planes. EMI fences are used where the frequency is not high enough to pass through the holes in the fence. The fence holes should be less than half the wavelength of the frequency to be blocked. The smaller the hole, the better the block. The circuit enclosure can also be covered with conducting material to create an absorbing, reflecting shield. This is an expensive alternative and should be used as a last resort. Cables and connectors leaving the box must also be considered as possible sources of EMI.

In the case of mixed signal graphics PCB boards, consider the video connector and cable. The line from the DAC output to monitor input is a source of possible EMI radiation. If this link acts like an antenna rather than a transmission line, EMI will result. An important consideration is impedance matching. Match the impedances on the end of the transmission line to reduce reflections that could cause standing waves. Eliminating standing waves reduces the transmission line's ability to act like an antenna.

Figure 8 shows a common RAMDAC output system. The cable should be coaxial so that all magnetic fields cancel. The outer conducting sheath should be connected to the outer conducting shell of the connector. The outer conducting shell should be connected to the analog ground plane of the circuit card. Some difficulties may arise if the system enclosure is isolated from circuit ground. This can be handled by using connectors that will be electrically isolated from the enclosure when mounted.

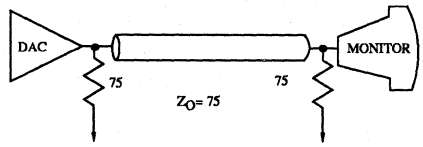

Figure 8. Common Output System.

Conclusion

Mixed signal graphics boards require special layout consideration as dot clocks increase with higher screen resolutions. The added picture sophistication reflects the need for added board sophistication including increased number of layers, use of striplines on the board, and coax off the board. One must design with EMI reduction techniques from the beginning even though the expense might be higher and there may be a learning curve. In the long run there is less risk and frustration, and the product will likely get to market faster.

References

Brooktree Corporation

- Application Note 1 - Getting the Best Performance from Video Digital-to-Analog Convertors
- Application Note 2 - VIDEODAC Essentials
- Application Note 6 - Troubleshooting Your Brooktree CMOS VIDEODAC or RAMDAC
- Motorola MECL System design handbook
- Signetics HCMOS Designers Guide
- "Designer's Guide to Transmission Lines and Interconnections" - (EDN, 6/23/88)
- White, Donald R.J., "EMI Control in the Design of Printed Circuit Boards and Backplanes", Interference Control Technologies, Inc., 1982.
- Mardiguian, Michel, "Interference Control in Computers and Microprocessor-Based Equipment", Don White Consultants, Inc., 1984.
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APPLICATION NOTE 12

Analog Signal Interface Techniques

The interconnection and transmission of high bandwidth analog video requires special consideration to assure preservation of the signal fidelity and compliance with EMI regulations. The high frequency bandwidth of computer generated graphics must be adapted to the limited bandwidth of a display or routing device without severely compromising the crispness of a digitally derived image.

This Application Note will discuss several topics which relate to the preservation of video signal fidelity and will state a specific case to outline the advantages and disadvantages of each method. The following topics will be discussed:

- The frequency limitations of coaxial cable transmission line media.
- Correct techniques and use of analog filtering for noise and emission suppression.
- Common monitor synchronization problems when interfacing with various video signal sync formats.
- Considerations for implementing broadband analog video multiplexing or routing.

The scope of applications will range from PC-VGA signals (35 MHz - 50 MHz) to the Megapixel Workstation class video signals (100 MHz - 200 MHz). The techniques outlined can be scaled down to traditional NTSC-type video or scaled up to super-display (>200 MHz) signal applications.

How far can it be coaxed?

For transmission distances exceeding the quarter-wavelength of the highest frequency component of the signal, a controlled impedance coax medium is required to preserve signal fidelity at the destination (usually a display or distribution amplifier). A typical 30 MHz bandwidth VGA display monitor with a one meter cable (4 - 6 ns propagation time vs. 9 ns quarter wavelength) is vulnerable to pulse aberration (overshoot and reflections) unless cable properties (characteristic impedance and shielding) are controlled to minimize standing waves and radiation (which government agencies discourage in commercial products). While coaxial cable can deliver 90 - 95% of incident low frequency power to a destination several hundred feet away, it is still a dispersive medium which can significantly attenuate high frequency energy. We shall examine how the quality of the coaxial cable and some simple buffer circuits can affect the quality of the computer graphic display.

Coaxial cables and fittings are commonly supplied in characteristic impedances of 50 or 75 ohms, with 75 ohms being preferred for low loss and low cost applications of broadband consumer video systems.

The electrical attenuation characteristics of a coaxial cable for a low frequency signal are a function of the center conductor resistance, which can be minimized with special conductive plating. The high frequency loss is affected by the dielectric loss (which increases linearly with frequency) and "skin effect" losses according with Equation 1.

$$\alpha = (0.434 / Z_o)(1/d + 1/D)\sqrt{\text{freq}}$$

Note: α = Attenuation (db/100ft)

Equation 1.

The coaxial dimension d (outer diameter of the center conductor) and dimension D (inner diameter of the sheath) are maintained at a ratio of about 3.6 for a 75 ohm impedance cable. For smaller values of D in Equation 1, we see that a smaller diameter cable will have a greater high frequency attenuation. This frequency dependent characteristic transforms in the time (or pulse) domain to Equation 2.

$$V_o = V_i (1 - \text{erf}(K \times L / 4R\sqrt{t}))$$

Note: Propagation delay component removed

Equation 2.

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An analysis of the complementary error function (erf) will show a rounded contour such that the response time to 90% of full amplitude is 28.8 times the response time to 50% or mesial point. This is why cables are sometimes rated for 50% rise time, which can be extrapolated to 90% rise time by the 28.8 multiplier. From Equation 2 it can be seen that rise time degrades as the square of the cable length (L), rather than the root-sum-squares model that would apply for a cascade of elements with Gaussian pulse characteristics (e.g. single pole filters, amplifiers and CRT phosphors). This means that fatter cables make for sharper pulses over longer distances. The accuracy of the pulse settling is limited by the high frequency impedance match (5 - 10% if tested for return loss) which also affects the over/under shoot of the dampened pulse.

While there are no prevailing standards for computer graphic transmission systems (such as RS250B for 5 MHz RS170A video), one can arrive at a criteria for acceptable frequency dependent attenuation by reasoning that the cable should not compound the zero-order-hold (also referred to as sinx/x roll-off) attenuation at the Nyquist frequency (half the sample rate) to where the monitor's gamma-dependent phosphor intensity is reduced more than 10%. RS250B tolerates 1 dB roll-off in the luminance bandwidth of 3 MHz corresponding to 320 lines of horizontal resolution (after aspect correction), which extrapolates to 48 MHz for a 1280 line, non-interlaced display requiring at least a 96 MSPS DAC clock (more typically 107 MSPS due to monitor retrace time requirements). Typical display monitors in this class have small signal (<100 mV) bandwidth of 100 MHz and slew-rate-limited 10%/90% rise times of 5 ns. The energy delivered to the screen phosphor at the 50 MHz Nyquist frequency is less than one fourth that delivered at much lower frequencies (assuming the monitor roll-off rejects higher-order harmonics). The convolution of a 5 ns monitor rise time with the sinx/x function produces a half-power frequency of about 25 MHz, so by the square-root-of-frequency cable attenuation characteristic one can relate a 10% (1 dB) attenuation at 25 MHz to a 2 dB loss at 100 MHz. Applying the acceptable criteria of 2 dB cable loss at a 100 MSPS pixel clock frequency, one arrives at acceptable lengths of cable for the various generic types listed in Table 1. Other bandwidth requirements can be determined by scaling according to the square root of the pixel frequency.

Cable Type	Diameter	@100 MHz	-2 dB Reach
RG179	0.100"	9 dB/100'	22 feet
RG59	0.242"	3 dB/100'	67 feet
RG6	0.275"	2 dB/100'	100 feet
RG11	0.405"	1.5 dB/100'	133 feet

Table 1. Cable type vs. loss / length

Some cable manufacturers may offer special versions with better loss ratings, but they should be tested for impedance match better than 20% (or return loss exceeding 20 dB). The use of smaller 50 ohm coax (such as RG58 or RG174) runs the risk of 20% of the signal bouncing off the 75 ohm monitor, producing ghosts (see Equation 3) and potentially greater radiation due to standing waves.

$$\rho = (R_L - Z_o) / (R_L + Z_o)$$

Equation 3. Reflected Voltage.

When considering different transmission media for very long runs (such as fiber-optics), a similar analysis can be applied assuming the transducers have Gaussian characteristics which can be convolved approximately by root-sum-squaring the individual rise-times and limiting power loss to 10% at a quarter of the pixel clock frequency. For non-Gaussian components or stronger gamma effects, the calculation of delivered pulse power would be appropriate using analytical representation or non-linear simulation tools. Note that systems with excess dynamic range (such as 1.4 V compliance with an MSB to spare) can compensate for all these frequency dependent effects given the higher order computational power to predict intensity frequency and pre-compensate the data to the DAC.

Preserving the Fidelity

Techniques to compensate for coax cable attenuations include signal compensation by pre-emphasizing the pulses with peaking buffers before transmission. While precise compensation for cable attenuation is best implemented in passive RLC networks, amplifiers with up to 6 dB of gain peaking at the high frequency limit (.35/<monitor rise time> is practical) can approximately compensate for cable losses. Such peaking produces overshoot on the analog edges but also serves to compensate for the sin x/x (zero-order hold function) attenuation effect for spectral components near the Nyquist frequency limit (half the sample clock rate).

One simplistic implementation of a peaking buffer (Figure 1.) for a CMOS palette DAC is just a common base PNP stage between the DAC output and the load resistor. The drawback of this circuit is that the Hfe linearity of the MRF536 dominates the overall integral linearity, with the net integral linearity being 1 - 3%. Fortunately the non-linearity is hidden in the black region and is alleviated by the 7.5 IRE set-up pedestal bias. The DAC output node may be outside its rated compliance range (usually 1.2 - 1.5 V) without limiting the overall linearity. The rise/fall times of 1.0 - 1.5 ns are slightly better than that of commercial boxed distribution amplifiers with peaking (such as the INLINE 2085) which exhibit about 3 ns transition times with a minimum gain of 2 at 150 MHz. The linearity and pulse fidelity parameters must be convolved with the monitor amplifier characteristics (which may include some gamma correction) to arrive at an overall channel fidelity figure. If linearity better than 1% is required, then consider using monolithic or hybrid operational amplifiers from Comlinear, National, Harris Semiconductor, or Burr-Brown which usually require dual supplies, and have full-power (>1Vpp) bandwidth at least half the pixel frequency (to preserve information in the Nyquist Bandwidth). Peaking for cable compensation is achieved by introducing a pole in the feedback network. This must be limited and checked to assure stability margin with possible mis-termination, such as cable faults or capacitive monitor loading.

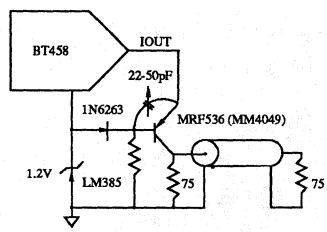

Figure 1. Peaking Buffer.

The effects of cable attenuation are illustrated in Figure 2. Staggered traces depict the 1.2 ns rise time from a Bt458 being rounded to 1.5 ns after 60 feet of RG6 cable; to 8 ns after 100 feet; and to 13 ns after 200 feet. The DC component is down 15% after 200 feet, which is the nominal amplitude tolerance of RS330/343 video. The INLINE 2085 RGB amplifier can restore the pulse rise time to 3.7 ns (OK for 100 MSPS) after 70 feet of RG6 (Figure 3). The common base stage delivers sub-four nanosecond edges after 200 feet of RG6 (where 20 - 40pF of emitter-base capacitance reduces the edge speed 1.0 - 2 ns) as shown in Figure 4.

Filter with Care

Where cables can be considered constant group delay filters, with low shape factors to pass a wide spectrum of frequencies, the display monitor amplifier generally constitutes a multi-pole pulse filter, with a slew rate limited rise time for full scale transitions and a slightly higher 3 dB bandwidth for small (<10%) signals. Constant group delay filters (or Bessel) are desirable for passing pulses to preserve reasonable overshoot with their large harmonic content. However, they have shape factors which rolloff gradually with frequency and are less effective at reducing undesirable high frequency noise. In raster graphics applications, noise arises from the digital signals getting on the analog channel to produce data related foreshadows (generally within 10 pixels of sharp picture transitions), bleed-through with overlaid images, or signals beyond the monitor's bandwidth which aren't visible yet radiate under FCC restriction. Frequency selective pulse filtering can be used to limit the video transmitted to the important spectral content, while maintaining perceived horizontal resolution and picture intensity within government agency restrictions.

Figure 5 depicts four different filter pulse responses using simple pi filter topologies, as driven by a 1.5 ns palette edge. The first is a 3-pole Bessel filter using discrete LC components optimized for 100 MHz/ 3 dB attenuation (about 12 dB @ 200 MHz), which exhibits a 3.8 ns rise time with about 10% peak-peak ring. The other three responses correspond to ferrite bead filters with successively greater impedance (60 - 100 ohms) at 100 MHz, and corresponding 8 - 16 ns rise times (the slowest representing a monolithic chip with distributed LC characteristics). While any of the ferrite beads would provide acceptable fidelity on a 25 MSPS VGA graphics channel, even the smallest bead would induce significant intensity dimming on a 65 MSPS pulse. The discrete 3 pole Bessel filter shown in Figure 6 (115 nH followed by 47 pF for 100 MHz), passes the full power in the Nyquist spectrum (50 MHz) while reducing by half any energy at the harmonics of the palette's TTL drivers above the sample clock frequency. By reducing the pulse edge rate from 1.5 to 3.8 ns, the Bessel filter further diminishes the effect of reflections off the monitor since their input impedance is largely reactive above the rated bandwidth. These reflections can produce "ghosts" whose after-shadow is dependent on the cable length.

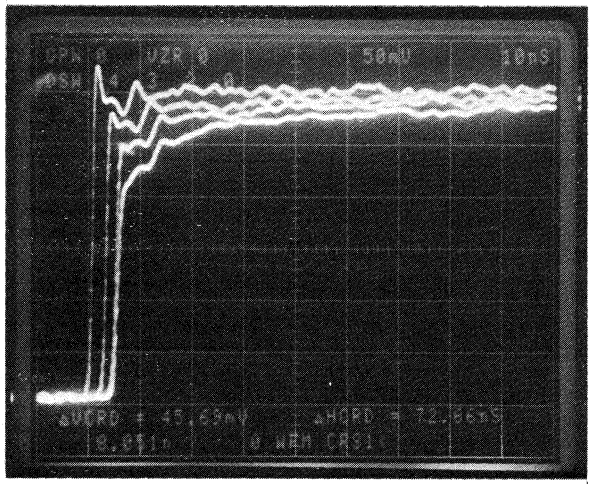

Figure 2. Cable Attenuation

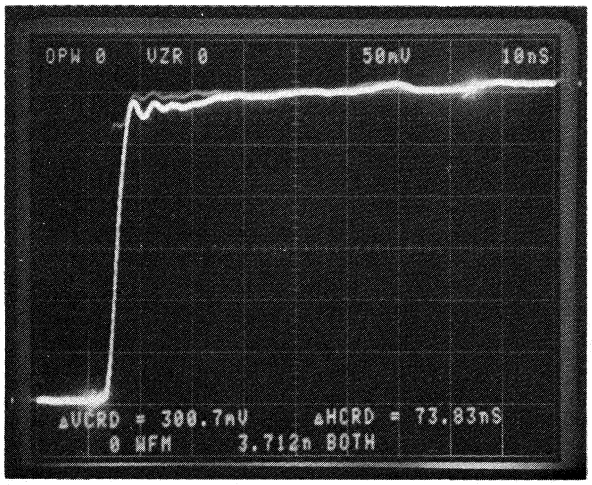

Figure 3. Sub-four Nanosecond Edges

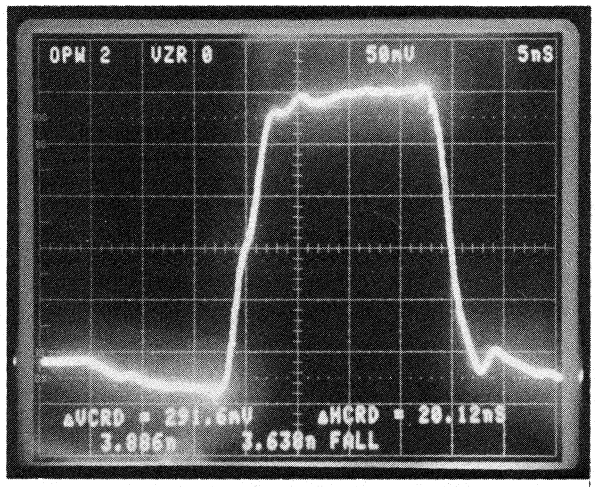

Figure 4. Rise Time Restoration.

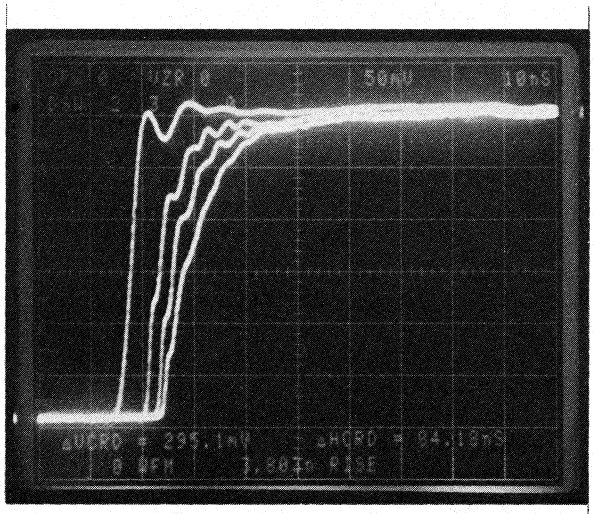

Figure 5. Filter Pulse Response.

Keeping the Video in Sync

Modern multi-raster monitors can be tolerant of diverse scanning frequencies yet be sensitive to parameters such as separate sync channels, sync polarities, and some of the more elaborate analog synchronization signals employed in HDTV equipment. Normal RS343A analog video prescribes composite sync on the green channel, which is usually generated by the palette DAC with the same propagation time and level accuracy as the active pixel video. The display device is usually internally AC coupled and must detect the synchronization pulse to correctly perform internal DC restoration by clamping its amplifiers to a specific level when the video waveform is at a prescribed level in the retrace interval (usually the back porch interval following the sync tip). DACs which generate composite sync on the Red, Green, and Blue channels (to serve multiple displays or to provide channel gain reference levels for AGC processing) can confuse some monitors which get separate sync timing, giving rise to color imbalance or poor black level stability. Sync signal polarities which vary with the generator's display format (such as VGA) usually affect the display size and degree of overscan, but can create havoc with monitor requirements for clean porches for clamping. The following discussion will cover situations where the sync generated by the palette DAC must work in concert with other channels to achieve stable raster display.

While traditional RS170/343 video camera formats are quite specific about horizontal and vertical synchronization pulse polarity, due in part to the delicacy of interlaced timing, the newer non-interlaced computer formats take advantage of separate synchronization channels with independent polarities to tailor the display presentation to a multitude of screen resolutions. The IBM VGA/8514 standard, while maintaining a raster frequency of 31 - 35 kHz, prescribes four possible combinations of H/V sync polarities depending upon the screen display mode (EGA/Text/Gfx/HiRes). For maximum compatibility with VGA monitors and self-test conditions, there should be no composite sync or offsets on the analog channels since the monitors will give precedence to the TTL sync signals when present. With VGA controllers, where all the raster timing parameters and signal polarities are programmed, care must be taken to compensate in software for time skews between the buffered sync channels and the pipelined palette channels, which can affect horizontal screen placement by several pixels. When interfacing to monitors prone to give precedence to composite sync information on the analog channels, it may be best to inhibit any separate sync channel signals. It is furthermore prudent to maintain wide back porches (Blank period after Sync) in the horizontal retrace since most monitors clamp their amplifiers in that interval.

The newer HDTV production formats rely on more elaborate composite synchronization signals known as Tri-Level Sync. In this scheme the sync detector threshold is dynamically set near the Blank level, such that sync pulses swing +/-300 mV around the Blank level. DACs tailored for RS343 composite sync do not have explicit input controls to generate sync levels above Blank, so adapting these DACs to the SMPTE 240M standard requires mapping sync into the data range or current summing a switched 8 mA sync source into the 37.5 ohm load. With a palette DAC, one CLUT location can be defined as the positive-going sync pulse, but for conventional DACs the circuit shown in Figure 7 is a solution. The Sync Hi control should be registered or pipelined to match the DAC's internal register propagation time within 10 ns to reduce glitches near the sync trigger level. This adds about 12 mA to the DAC supply current, of which 8 mA is switched between ground and the video termination. The sync rise time is less than 50 ns or four clock cycles (75 MSPS).

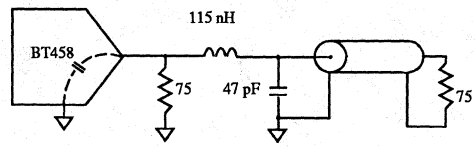

Figure 6. 100 MHz Bessel Filter.

Sharing the Medium

It is common to multiplex other analog signals into the video channel as an analog overlay technique or where multiple palettes must share the same monitor. Analog overlays require multiplexing at the pixel clock rate, while analog sharing is done during graphic mode switching (like from VGA resolution to very high resolution). The two situations call for different component technologies whose cost is strongly dependent on the multiplexing rate, and driving low impedance transmission lines with minimal loss yet full channel bandwidth. The nature of current output DACs as fast current switches makes them easy to tie outputs together with the caveat that the resultant higher parasitic capacitance can produce some aberrations on fast pulse edges.

Situations arise where it may be cost effective to use a relatively slower palette DAC for lower resolution modes, with common connections to a high performance palette sharing a multi-frequency monitor. The inactive DAC can be virtually shut off by asserting Sync/Blank inputs, but the slower DAC presents an extra 15 - 20 pF of parasitic capacitance load which can degrade the rise time of the high performance palette when it is active. Placing low barrier Schottky diodes (such as HP 1N6263) in series with the DAC's slower outputs (see Figure 8), isolates its loading when it is inactive. The one disadvantage is that its fall time degrades to about 4 ns (useable to about 65 MSPS). This approach can be used to combine high speed CMOS DAC outputs to achieve greater resolution, but the DAC's compliance range must accommodate the extra diode drop as well as any offset current in the shared terminator. Combining multiple DACs usually entails significant switching glitches which should be counteracted by drop-shadow masking (software) or precise clock timing compensation. Note also that varying pixel pipeline delays through the palette(s) may produce horizontal position offsets, where monitor sync signals are provided through separate digital channels.

Solid-state multiplexors fabricated in CMOS or DMOS technologies generally have an RDS-Coff time constant of about 200 picoseconds, which for 75 ohm applications connotes 3 dB of insertion loss with worse than 60 dB isolation above 10 MHz. A Siliconix Si2400 (representative of DMOS FETs of requisite size) switches in less than 10 ns but requires negative channel bias. The best power FET or optoFet will have 12 - 30 ohms of on-resistance with 8 - 20 pF of associated drain capacitance. When placed in series with a CMOS DAC output, this will satisfy compliance requirements but will effectively double the DAC's output capacitance and transition times.

GaAs switches and diode bridges are inherently faster at greater expense and with special interface considerations. The Mini-Circuits KSW series of GaAs switches are rated for 1 dB of 50 ohm insertion loss with 50 dB of isolation at 200 MHz and less than

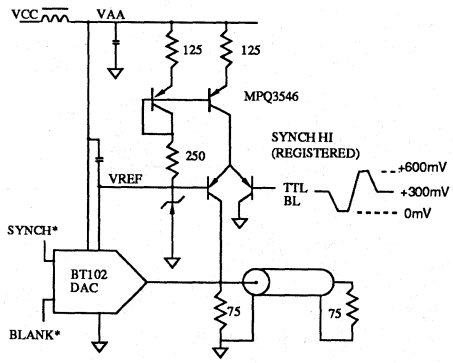

Figure 7. Tri-level Sync

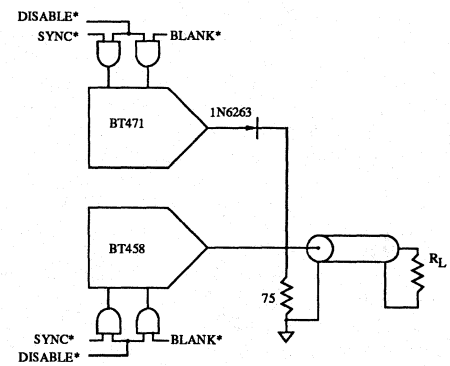

Figure 8. Sync Solution

5 ns switching driven by 0/-8 V controls. In the diode arena, the HP5918/38/58 series and Metelics MSS-30/40/50/60 series of beam-lead devices must be driven by fast complimentary current sources/sinks to achieve fast switching, but they have a channel time constant of under 10 picoseconds. Special ratings for diode on resistance at >10 mA may be necessary for direct coax interface, or a modified bridge which substitutes complimentary emitter followers for the output diode pair can provide high-current voltage drive in much the same fashion as LH002-type buffers (from National, Harris, Precision Monolithics, and Elantec). The Harris/RCA CA3019 diode array is an inexpensive alternative, useable for signals up to 100 MHz with 2.6 dB loss. (See references)

Special Situations

Particular palette DACs may have unique characteristics which deserve special attention. For instance, DACs with compliance ranges substantially greater than the required video amplitude can readily interface to inexpensive distribution amplifiers to drive multiple monitors simultaneously. Other DACs may have RS170A-type Blank-Black setup pedestals which create problems for PAL or Component Analog Video equipment. Some simple examples will illustrate how subtle modification to the DAC signal can extend its utility without severely compromising its fidelity.

In limited bandwidth (e.g. VGA resolution) applications where the cable propagation time (usually 1.5 ns/foot) is less than a quarter of the pixel interval and about equal to the DAC rise time, several monitors can be driven by a simple emitter-follower distribution amplifier which uses just +5 V and modest back-termination in each feed to maintain load isolation. Figure 9 illustrates how the 1.5 V compliance range of the Bt478 palette is enough to accommodate the 600 mV emitter-base drop through a 2N2222 buffer with 22 ohm resistor in each output. The 25 ohm source impedance represents a better standing wave ratio (2.25) than most VGA boards, which mimic the IBM 150 ohm source termination (3:1 VSWR). Linearity of the buffer is improved with higher transistor beta, the use of Setup and Sync pedestals, or multiple loads (up to the thermal limitations of the transistor) which reduce the emitter-base source impedance variation with current.

Note the DAC output must swing more positive than in typical VGA applications, to overcome the 25% signal loss through the buffer. Transition times will be slowed (10 ns) slightly and any circuitry which detects output levels must take the diode offset into account.

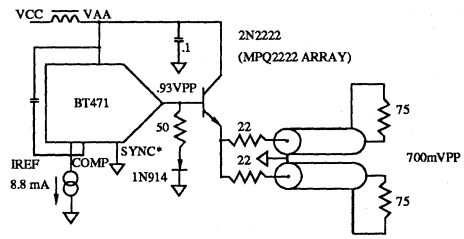

Figure 9. VGA Distribution Amplifier.

DACs with RS170/343A Blank-Black setup levels generally cannot drive PAL or CAV video equipment which require Black at Blank level. For these DACs the easiest solution is to mask the setup current into the sync tip (a 7% tip boost, still within specs) by placing a latch with a Clear function (such as 74273) in the data path. By asserting Blank via the latches Clear pin, rather than through the DAC, and by tying the DAC's Blank* and Sync* inputs together (asserted by composite Sync), the 7.5 IRE setup pedestal will appear on the Sync tip rather than in the grey scale range.

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- Motorola Small Signal Data Book (MPQ3546)
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Bt208 Evaluation Module Operation and Measurements

Introduction

The Bt208EVM is a two layer printed circuit board for the evaluation of the Bt208. The EVM features a socketed Bt208, an SMA input connector, and a 48-pin DIN connector.

In combination with a customer-designed driver board, the EVM board can be used to evaluate the Bt208, or for testing at incoming inspection.

Driver Boards

The driver board is a user configured custom designed circuit that connects to the Bt208EVM by a 48 pin DIN input connector. The driver board should provide all clock and control signals to the Bt208, as well as the ability to receive the digitized outputs. All input signals should conform to the Bt208 datasheet specifications.

Operation

To operate the Bt208EVM, video and control signals must be supplied by the customer. If a video signal of known configuration (i.e. a wedge, or ramp signal) is supplied to the Bt208EVM, the digitized output can be reconstructed using a DAC and compared to the input signal to determine correct operation.

The Bt208EVM will digitize a standard RS-170A, RS-343, or PAL video signal whose range is 1.2 volts peak-to-peak or less. If the input signal contains a chroma subcarrier, a chroma trap should be inserted in front of the digitizer to remove any chroma information. To AC couple the video signal, remove the jumper at U2 and replace it with a 0.1 µF capacitor. Also, jumper the level pin on the Bt208 to either ground or Vin.

The internal voltage reference of the Bt208 is fed back to the positive reference input, giving a VREF+ of 1.2 volts. A 200 ohm resistor is connected from VREF to ground to provide a resistive load as specified in the Bt208 datasheet.

The Bt208EVM allows the user to make modifications in the circuit to suit individual needs. The positive reference voltage circuitry can be modified to provide for an externally controlled, variable voltage reference. To use the internal 1.2 volt voltage reference to provide a variable REF+, remove jumper C and install a jumper in location D. Also, R7 should be replaced by a 300 ohm resistor, and a 100 ohm trimpot should be installed in location R6. In this configuration REF+ can be varied from 1.2V to 0.9V.

The Bt208EVM also has empty locations on the printed circuit board for buffers and amplifiers. These locations are intended for manufacturing test only, and are not required.

With the Bt208EVM, the user can make a variety of measurements and compare these against the datasheet specifications. Parameters such as Signal to Noise Ratio, Output Delay, Integral Linearity and Differential Linearity may be measured and verified.

AC Measurements

SNR

Signal to Noise Ratio is defined as the ratio of the amplitude of a desired signal at any point to the amplitude of noise signals at that same point. SNR in digitizers can also be described as the amount of noise and distortion introduced by the digitization process.

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There are many methods that can be used to evaluate the SNR of a flash converter, or digitizer. One method that is well suited for use with the Bt208EVM is the Best Fit Sine Wave method.

The Best Fit Sine Wave method uses a sine wave of known amplitude and frequency as the signal to be digitized. An input clock is chosen such that the sample points on the sine wave will not repeat until a given number of samples later. In the configuration to be outlined, 4096 samples will be taken before the same point is reached on the sine wave.

These 4096 samples are then used to reconstruct one period of a sine wave. Since the 4096 samples are never repeated, they can be used to construct a sine wave with greater resolution than a simple reconstruction at the clock frequency. This reconstructed sine wave is then compared against the ideal sine wave that was input into the Bt208. Any errors in the reconstructed sine wave will be due to distortion and noise, and may be used to determine the Signal to Noise Ratio of the Bt208.

Data Output Delay

Data output delay in the Bt208 is the time from the rising edge of the sample clock to valid data on the pixel outputs. The Bt208 has a maximum output delay of 25 ns. This delay may be seen on an oscilloscope by triggering the oscilloscope on the rising edge of the pixel clock, and determining the time required for the pixel outputs to change.

DC Measurements

Linearity

Linearity can be broken down into two measurements: Integral Linearity and Differential Linearity.

Integral Linearity is the maximum deviation from a straight line that has been best fit to the data points of the input-output transfer function. Linearity is normally expressed as a fraction of an LSB or as a percentage of full scale. The Bt208 has a typical value of ± 1/2 LSB, with a maximum value of ± 1 LSB. One LSB is approximately 0.4 % of full scale.

Differential Linearity is the maximum deviation of any bit size from its theoretical value 1 LSB over the full conversion range. For example, a Differential Linearity of ± 1/2 LSB demands that each step be 1 LSB ± 1/2 LSB. A Differential Linearity of < 1 LSB is the maximum allowed for monotonic operation. The Bt208 has a typical value of ± 1/4 LSB Differential Linearity with a maximum value of ± 1 LSB.

Performance Measurements

This section will illustrate measurement examples of Signal to Noise Ratio and Linearity. The signal to noise measurements require that a driver board be built which will facilitate the storage of 4096 samples of digitized data. This data can then be fed to a program which can calculate the SNR from the sampled data (Equation 1).

To measure and plot the Integral and Differential Linearity of the Bt208, the driver board must contain circuitry similar to that of Figure 1. This figure shows a closed loop system that can be used to measure voltage and step values. These values can then be used in Equation 2 and Equation 3 to plot the Integral and Differential Linearity, respectively.

AC Characterization

Signal to Noise Ratio can be measured in a variety of ways. Many of the methods require expensive equipment and precision waveforms. The method we will be showing is very simple to implement, and will give an accurate SNR value.

As mentioned earlier, the Best Fit Sine Wave method will be used. This involves sampling a known sine wave at a frequency such that no two of the 4096 samples taken will be on the same point of the sine wave.

Once the data has been sampled and stored it may be fed to a series of software functions. The first function must be one to reorder the samples to make one period of a sine wave. This function must know the frequency of the sampled sine wave, the frequency of the sample clock, the number of samples and the starting point of the input array. With this information, the software can take the input array and restructure it to appear as a single cycle of a sine wave. Once this has been accomplished, the output array can be passed to the next section of software.

Once the data has been reordered, a sine wave must be fit to these data points. An algorithm to fit a sine wave to a set of data points is discussed in the IEEE Standard for Waveform Recorders (1057-1988). *Section 4.1.3.1 An algorithm for three parameter (known frequency) least squared fit to sin wave data* presents an algorithm to fit a sine wave to a set of data

points, given the number of samples and the frequency. A series of sums are computed which will yield a set of values that give the amplitude of the reconstructed sine wave, and the RMS error of the data from the ideal sine wave.

With the amplitude and RMS error, the SNR of the Bt208 can be calculated. Equation 1 gives the formula for computing the SNR given amplitude and RMS error.

$$SNR = 20\ LOG_{10}((Amplitude * SQR(2))/(2*E_{RMS}))$$

Equation 1.

DC Characterization

The Integral and Differential Linearity of the Bt208 may be measured quite easily with the Bt208EVM. The circuit shown in Figure 1 uses a closed loop system to obtain data points which can be plotted to measure the Integral and Differential Linearity of the Bt208.

The Threshold Select lines, I0 through I7, are used to set the desired output of the Bt208. These lines may be driven with a simple DIP switch arrangement. The chosen threshold value is presented to the two 4-bit comparators, which measures it against the digitized output of the Bt208. The comparators will then raise or lower the analog input voltage until the digitized value out of the Bt208 is equal to the selected threshold value. A simple DVM can then be used to measure the output of the integrator to obtain the analog voltage required to generate the specified digital output.

The voltages corresponding to each threshold value from 0 to 254 should be recorded to be used in computing and plotting the Integral and Differential Linearity of the Bt208.

Plot Integral Linearity as:

For I = 1 to 253:

$$IL(I) = 100*\left(\frac{I}{254} - \frac{VOLT(I) - VOLT(0)}{VOLT(254) - VOLT(0)}\right)$$

Equation 2.

Plot Differential Linearity as :

For I = 1 to 254:

$$DL(I) = 100*\left(\frac{VOLT(I) - VOLT(I-1)}{VOLT(254) - VOLT(0)} - \frac{1}{254}\right)$$

Equation 3.

Typical plots for Integral Linearity and Differential Linearity are shown in Figures 2 and 3. IL and DL are expressed as a percentage of full scale in these plots.

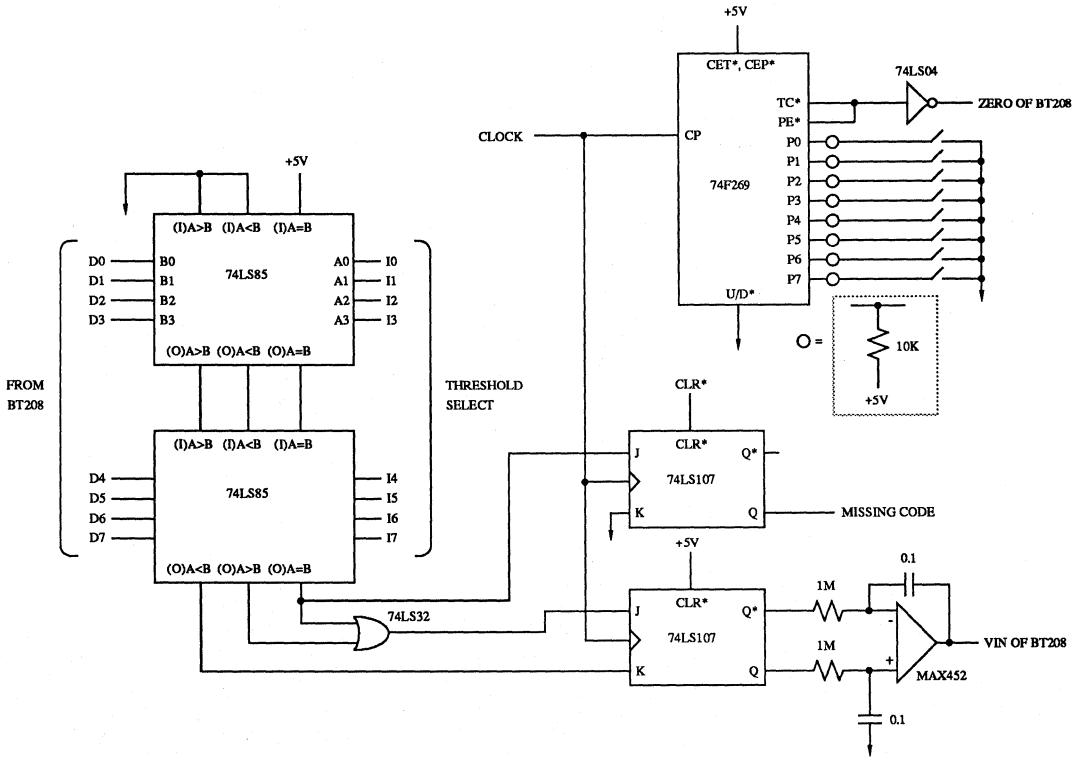

Figure 1. Bt208 Test Circuit.

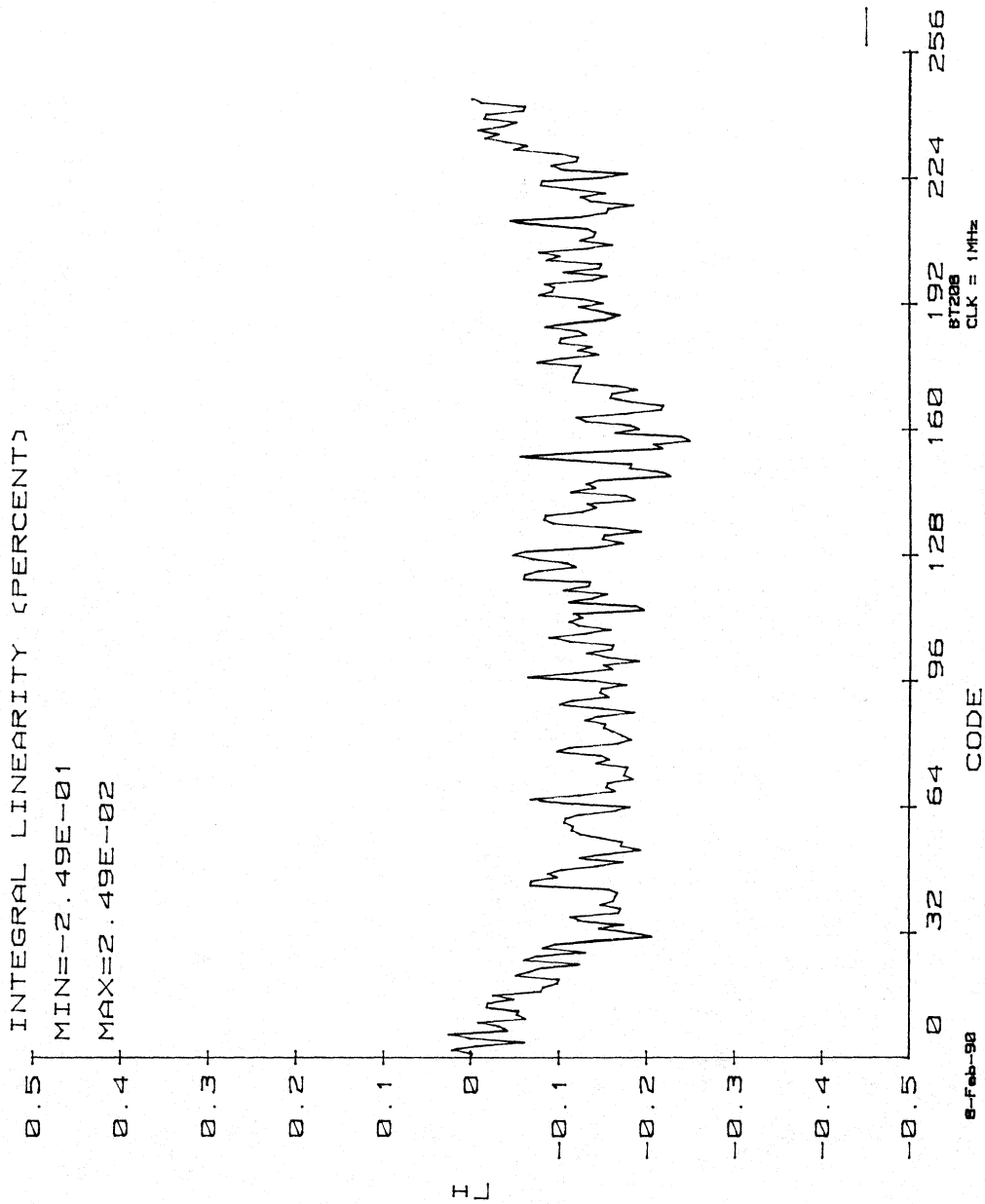

Figure 2. Typical IL Plot.

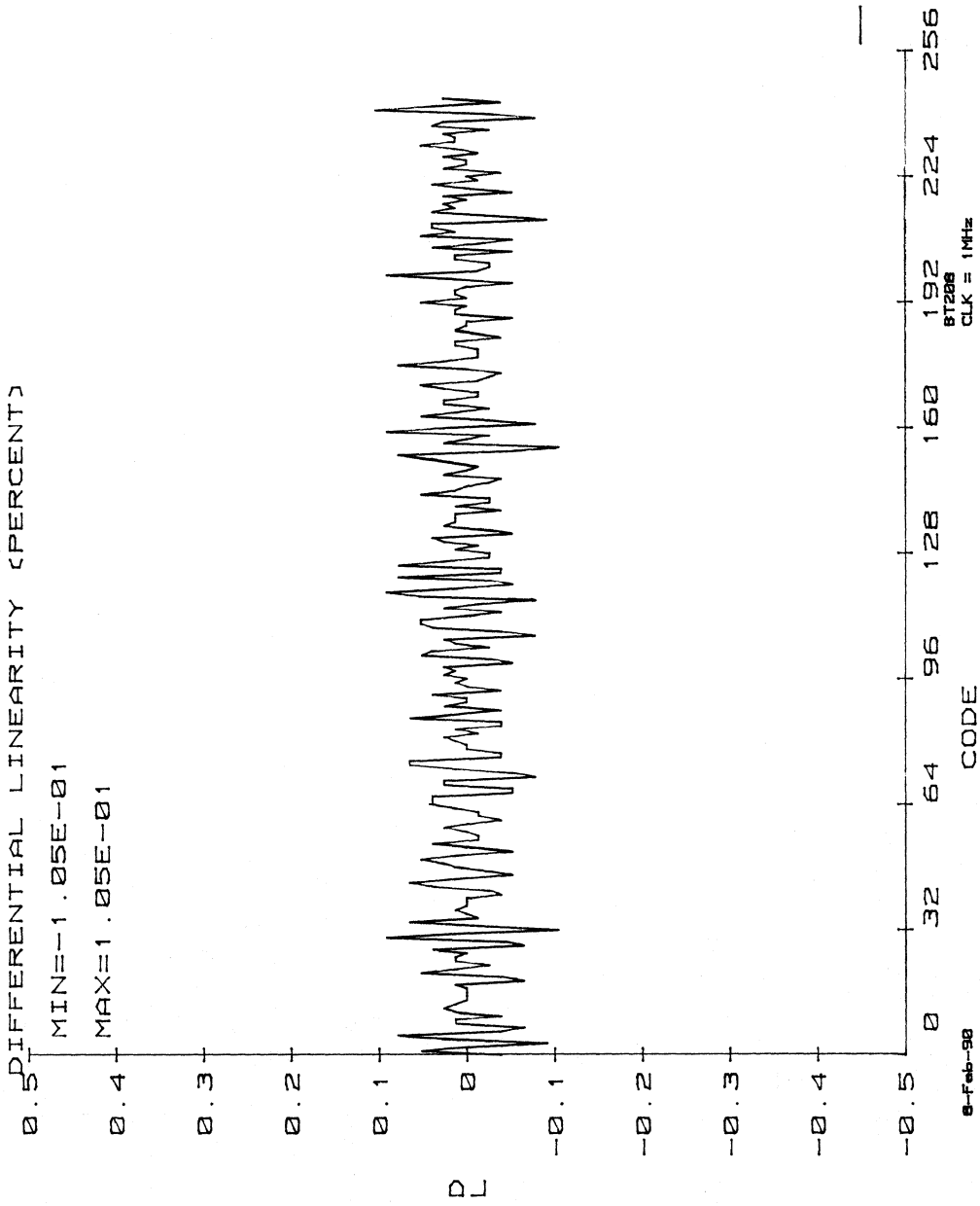

Figure 3. Typical DL Plot.

PCB Construction

The Bt208EVM board is an epoxy fiberglass board constructed with two copper layers for VAA, signal, and ground.

The PCB artwork is provided for evaluation purposes only. These layouts should not be considered ideal and have not been tested for FCC compliance.

The following descriptions highlight critical component placement and considerations for modification of this information to your application environment.

Schematic Diagram (Figure 4)

Jumper U2 can be removed and replaced with a capacitor to provide AC coupling of the input video signal.

Assembly (Figures 5 and 6)

Figure 5 shows all areas of customer interest on the Bt208EVM. A complete silkscreen is provided in Figure 6.

Solder Side (Figure 7)

To provide proper decoupling to the Bt208, the decoupling capacitors should be as close to the device as possible, with the shortest lead lengths possible. The Bt208EVM uses chip capacitors surface mounted directly next to the Bt208. In addition, 10 microfarad capacitors are used in parallel with the .01 microfarad chip caps for maximum decoupling over a wide bandwidth.

Component Side (Figure 8)

Since the Bt208EVM is only two layers, power and ground distribution is not ideal. When designing a multilayer board, ensure that analog power does not overlap digital ground, and analog ground does not overlap digital power.

J1					
1A	D7	1B	D6	1C	D5
2A	D4	2B	D3	2C	D2
3A	D1	3B	D0	3C	SPARE
4A	SPARE	4B	SPARE	4C	SPARE
5A	SPARE	5B	SPARE	5C	SPARE
6A	SPARE	6B	SPARE	6C	SPARE
7A	SPARE	7B	SPARE	7C	SPARE
8A	SPARE	8B	SPARE	8C	SPARE
9A	OE	9B	SPARE	9C	SPARE
10A	SPARE	10B	ZERO	10C	STROBE
11A	−8V	11B	−8V	11C	−8V
12A	+8V	12B	+8V	12C	+8V
13A	$+5V_D$	13B	$+5V_D$	13C	$+5V_D$
14A	$+5V_D$	14B	$+5V_D$	14C	$+5V_D$
15A	DGND	15B	DGND	15C	DGND
16A	DGND	16B	DGND	16C	DGND

JUMPER	
B	INTERNAL REF
C	INTERNAL REF

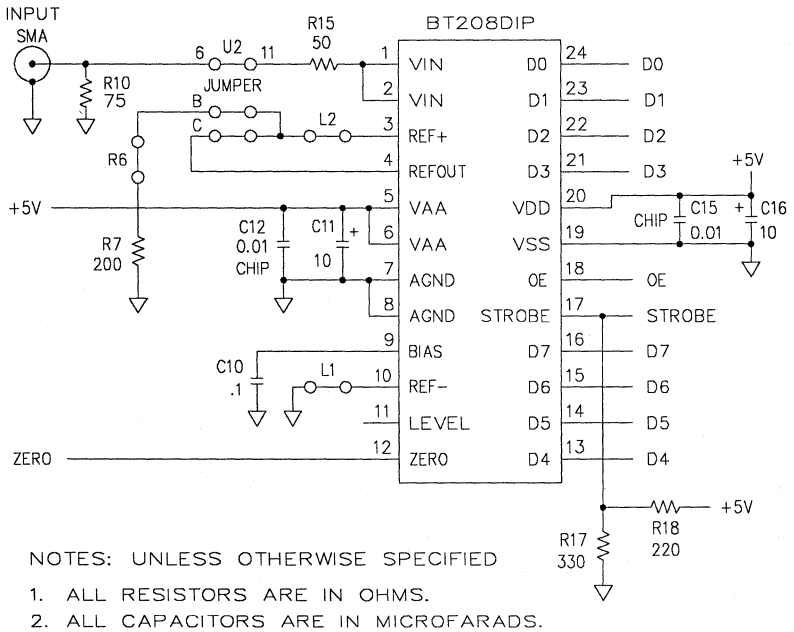

Figure 4. Schematic Diagram.

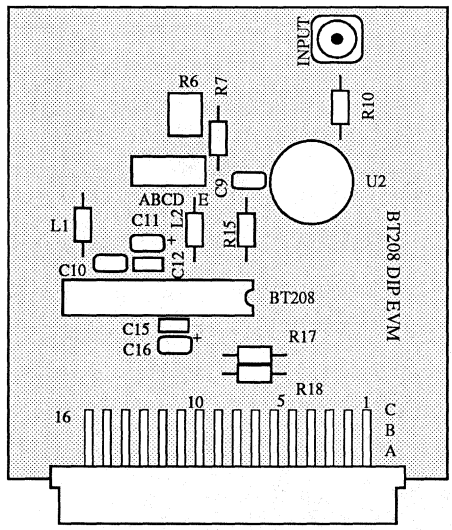

Figure 5. Assembly Diagram.

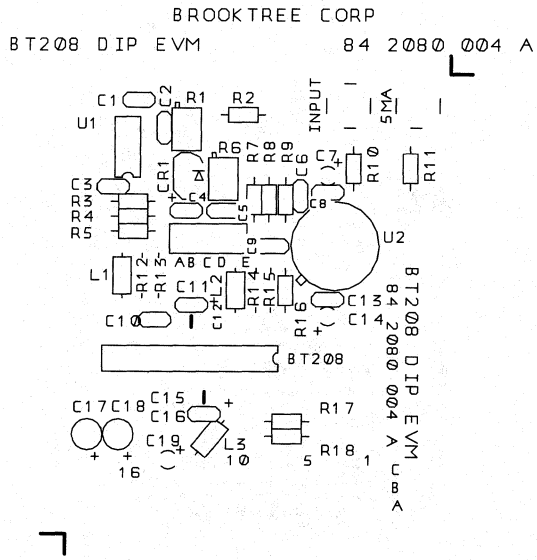

Figure 6. Silkscreen Layer.

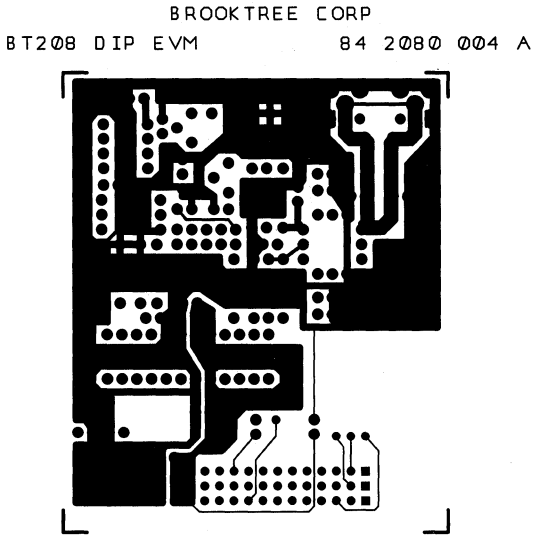

Figure 8. Solder Side.

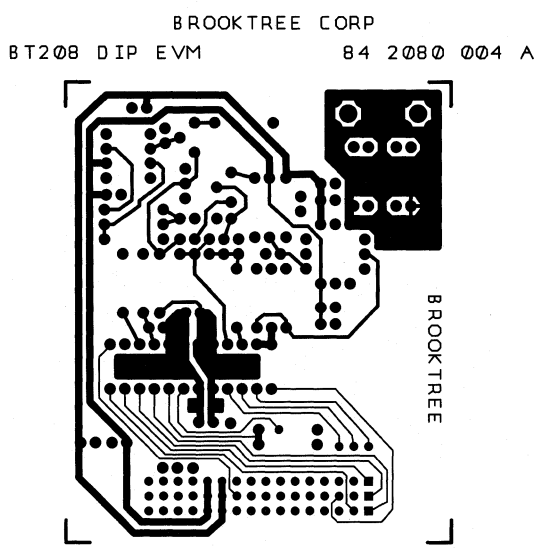

Figure 9. Component Side.

Bt251 Evaluation Module Operation and Measurements

Introduction

The Bt251EVM Board is a multi-layer printed circuit board that includes a socketed Bt251, two SMA input connectors, circuitry to support software configurable reference levels and two 48-pin DIN connectors.

In combination with a customer-designed driver board, this EVM board can be used to evaluate the Bt251, or for testing at incoming inspection.

Driver Boards

The driver board is a user configured custom-designed circuit that connects to the Bt251EVM by a 48-pin DIN input connector. The driver board should provide all clock and control signals to the Bt251, as well as the ability to receive the digitized outputs. All input signals should conform to the Bt251 datasheet specifications.

Operation

The Bt251EVM provides SMA connectors for two video inputs. VID0 is configured as an AC coupled input, while VID2 is configured as a DC coupled input. It is important to note that RS-170 permits a 2V, 2mA offset in the video signal. This should be taken into account when attempting to digitize an RS-170 signal that is DC coupled. By providing both styles of coupling, the user is able to test the Bt251 in both configurations. If the VID0 input is to be used, the level pin of the Bt251 should be jumpered to ground. This will allow the incoming signal to be DC restored.

The selection of the video signal to be digitized is controlled via software. The command register of the Bt251 contains two bits, D7 and D6, which specify which analog video source is to be digitized. A two step process must be followed to program the command register of the Bt251. First, the address register must be loaded with the address of the command register. The two LSBs of the address register must be loaded with zeros, the remaining 6 bits can be loaded to any value. When accessing the address register, the A1 and A0 lines on the Bt251 must be logic zeros at the falling edge of the RD* or WR* control lines. Once the address register is loaded the command register can be programmed. The A1 line should be a logic one and the A0 line should be a logic zero to properly access the command register. Data is latched into the register on the rising edge of WR*. The selected input source is output onto VOUT. Video inputs VID1 and VID3 are not connected on the Bt251EVM and should not be programmed as sources for digitization.

The command register also controls the source for the sync detection circuitry, data bits D5 and D4, as well as the sync level detect, data bits D3 and D2. The MPU selects one of four levels of sync threshold by selecting how many millivolts above the sync tip to use for sync detection. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero. A value of 125 mV, setting D3 and D2 both equal to one, is a good value to start with.

The Bt251, in addition to digitizing the incoming signal, provides a 256 X 8 LUT, enabling real-time manipulation of the image. Therefore, if the Bt251 is to provide accurate data, the LUT must be loaded with valid data. If desired, the LUT can be effectively bypassed by loading the RAM array with a data equals address, or ramp, pattern.

The Bt251EVM may be configured for MPU adjustable references, or in the case of REF+, externally controlled. The Bt251EVM is shipped configured for

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MPU controlled references. The IOUT data registers are not initialized at power-up, and should be programmed before use.

A jumper is provided on the Bt251EVM board between the VIDOUT pin and the VIDIN pin. By removing this jumper, which is located at P3 pins 17 to 18, the user may inset an analog filter before the video signal is digitized. A low pass filter rolling off at 6 MHz would provide suppression of high frequency noise in the video signal. If an active filter is used, a resistor and capacitor may have to be added after the output stage of the filter. See the Bt251 datasheet for details.

If the jumper from pins 1 to 2 in jumper block P4 is removed, and a jumper from pins 3 to 4 is installed, REF+ will be controlled by the trimpot R19. If the jumper from pins 9 to 10 is removed, and a jumper is installed from pins 11 to 12, REF- will be connected to ground. When R19 is used to control the level of REF+, the reference will be allowed to vary over a range of .8V, from 1.2V to .4V.

AC Measurements

SNR

Signal to Noise Ratio is defined as the ratio of the amplitude of a desired signal at any point to the amplitude of noise signals at that same point. SNR in digitizers can also be described as the amount of noise introduced by the digitization process.

There are many methods that can be used to evaluate the SNR of a flash converter, or digitizer. One method that is well suited for use with the EVM is the Best Fit Sine Wave method.

The Best Fit Sine Wave method uses a sine wave of known amplitude and frequency as the signal to be digitized. An input clock is chosen such that the sample points on the sine wave will not repeat until a given number of samples later. In the configuration to be outlined, 4096 samples will be taken before the same point is reached on the sine wave.

These 4096 samples are then used to reconstruct one period of a sine wave. Since the 4096 samples are never repeated, they can be used to construct a sine wave with greater resolution than a simple reconstruction at the clock frequency. This reconstructed sine wave is then compared against the ideal sine wave that was input into the Bt251. Any errors in the reconstructed sine wave will be due to noise, and may be used to determine the Signal to Noise Ratio of the Bt251.

Data Output Delay

Data output delay in the Bt251 is the time from the rising edge of the sample clock to valid data on the pixel outputs. The Bt251 has a maximum output delay of 25 ns. This delay may be seen on an oscilloscope by triggering the oscilloscope on the rising edge of the pixel clock and determining the time required for the pixel outputs to change.

DC Measurements

Linearity

Linearity can be broken down into two measurements: Integral Linearity and Differential Linearity.

Integral Linearity is the maximum deviation from a straight line that has been best fit to the data points of the input-output transfer function. Linearity is normally expressed as a fraction of an LSB or as a percentage of full scale. The Bt251 has a typical value of ± 1/2 LSB, with a maximum value of ± 1 LSB.

Differential Linearity is the maximum deviation of any bit size from its theoretical value 1 LSB over the full conversion range. For example, a Differential Linearity of ±1/2 LSB demands that each step be 1 LSB ± 1/2 LSB. A Differential Linearity of < 1 LSB is the maximum allowed for monotonic operation. The Bt251 has a typical value of ± 1/4 LSB Differential Linearity with a maximum value of ± 1 LSB.

Performance Measurements

This section will illustrate measurement examples of Signal to Noise Ratio and Linearity. The signal to noise measurements require that a driver board be built which will facilitate the storage of 4096 samples of digitized data. This data can then be fed to a program which can calculate the SNR from the sampled data (Equation 1).

To measure and plot the Integral and Differential Linearity of the Bt251, the driver board must contain circuitry similiar to that of Figure 1. This figure shows a closed loop system that can be used to measure voltage and step values. These values can then be used in Equation 2 and Equation 3 to plot the Integral and Differential Linearity, respectively.

AC Characterization

Signal to Noise Ratio can be measured a variety of ways. Many of the methods require expensive equipment and precision waveforms. The method shown is very simple to implement and will give an accurate SNR value.

As was mentioned earlier, we will be using the Best Fit Sine Wave method. This involves sampling a known sine wave at a frequency such that no two of the 4096 samples will be on the same point of the sine wave.

Once the data has been sampled and stored it may be fed to a series of software functions. The first function must reorder the samples to make one period of a sine wave. This function must know the frequency of the sampled sine wave, the frequency of the sample clock, the number of samples, and the starting point of the input array. With this information, the software can take the input array and restructure it to appear as a single cycle of a sine wave. Once this has been accomplished, the output array can be passed to the next section of software.

Once the data has been reordered, a sine wave must be fit to these data points. An algorithm to fit a sine wave to a set of data points is discussed in the IEEE Standard for Waveform Recorders (1057-1988). *Section 4.1.3.1 An algorithm for three parameter (known frequency) least squared fit to sin wave data* presents an algorithm to fit a sine wave to a set of data points, given the number of samples and the frequency. A series of sums are computed to yield a set of values that give the amplitude of the reconstructed sine wave, and the RMS error of the data from the ideal sine wave.

With the amplitude and RMS error, the SNR of the Bt251 can be calculated. Equation 1 gives the formula for computing the SNR, given amplitude and RMS error.

$$SNR = 20\ LOG_{10}((Amplitude * SQR(2))/(2*E_{RMS}))$$

Equation 1.

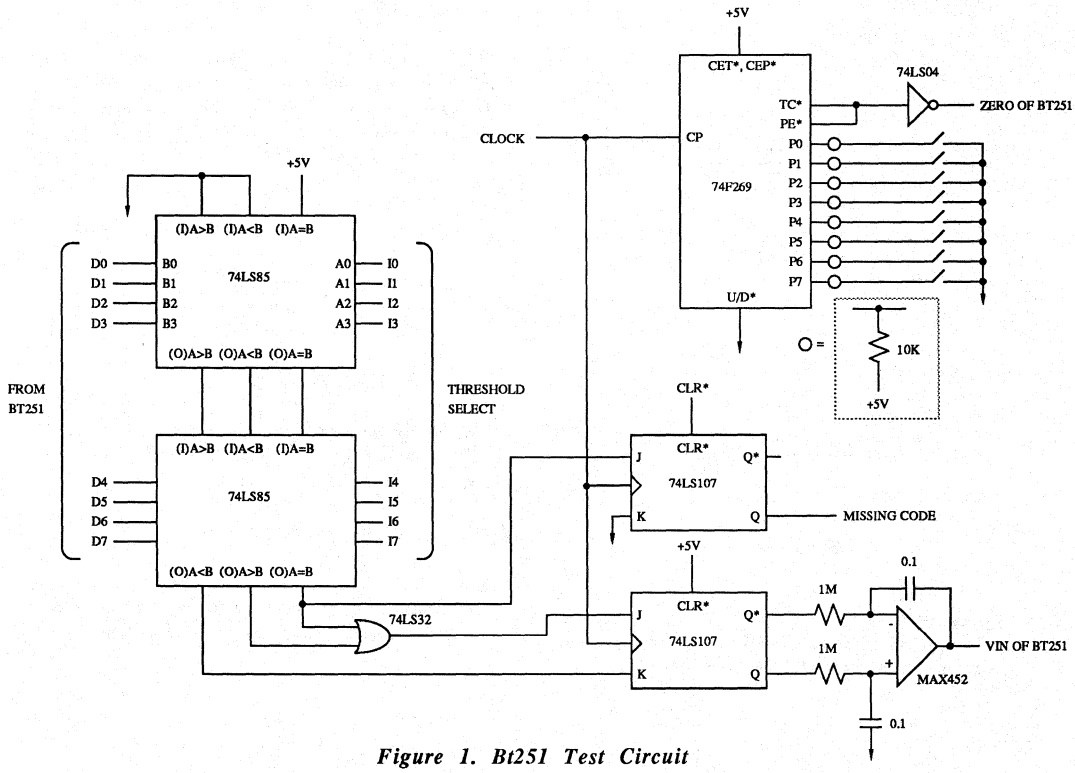

Figure 1. Bt251 Test Circuit

DC Characterization

The Integral and Differential Linearity of the Bt251 may be measured quite easily with the Bt251EVM. The circuit shown in Figure 1 uses a closed loop system to obtain data points which can be plotted to measure the Integral and Differential Linearity of the Bt251.

The Threshold Select lines, I0 through I7, represent the desired output of the Bt251. These lines may be driven with a simple DIP switch arrangement. The chosen threshold value is presented to the two 4-bit comparators, which measure it against the digitized output of the Bt251. The comparators will then raise or lower the analog input voltage until the digitized value out of the Bt251 is equal to the selected threshold value. A simple DVM can then be used to measure the output of the integrator to obtain the analog voltage required to generate the specified digital output.

The voltages corresponding to each threshold value from 0 to 254 should be recorded to be used in computing and plotting the Integral and Differential Linearity of the Bt251.

Plot Integral Linearity as:

For I = 1 to 253:

$$IL(I) = 100*\left(\frac{I}{254} - \frac{VOLT(I) - VOLT(0)}{VOLT(254) - VOLT(0)}\right)$$

Equation 2.

Plot Differential Linearity as :

For I = 1 to 254:

$$DL(I) = 100*\left(\frac{VOLT(I) - VOLT(I-1)}{VOLT(254) - VOLT(0)} - \frac{1}{254}\right)$$

Equation 3.

Typical plots for Integral and Differential Linearity are shown in Figures 2 and 3. IL and DL are expressed as a percentage of full scale in these plots.

PCB Construction

The Bt251EVM board is an epoxy fiberglass board constructed with four copper layers: VAA, two signal planes, and ground.

The PCB artwork is provided for evaluation purposes only. These layouts should not be considered ideal, and have not been tested for FCC compliance.

The following descriptions highlight critical component placement and considerations for modification of this information to your application environment.

Schematic Diagram (Figure 4)

The Bt251 Evaluation Module schematic shows the pixel outputs of the Bt251 connected directly to the inputs of a 74F373. By only driving one TTL load with each output, less ringing is present on the digital outputs. This will help the Bt251 keep noise down to a minimum.

Assembly (Figures 5 & 6)

Figure 5 shows the Bt251EVM as it is shipped to the customer. The silkscreen layer is shown in Figure 6. This provides a more detailed view of the board. Note should be taken of the proximity of the decoupling capacitor to the Bt251. Chip capacitor C8 is located beneath the Bt251.

Signal Interconnect Plane (Figures 7 & 8)

The digital traces are separated from the analog area as much as possible to prevent coupling. The analog signals are kept in the analog area to reduce noise.

Power Plane (Figure 9)

The analog and digital power planes are combined at a point with a ferrite bead (L1). The analog power area underlays the analog signals to reduce noise.

Ground Plane (Figure 10)

The analog and digital ground areas are separated using tub isolation. They are connected as close as possible to the power and ground connector to reduce noise.

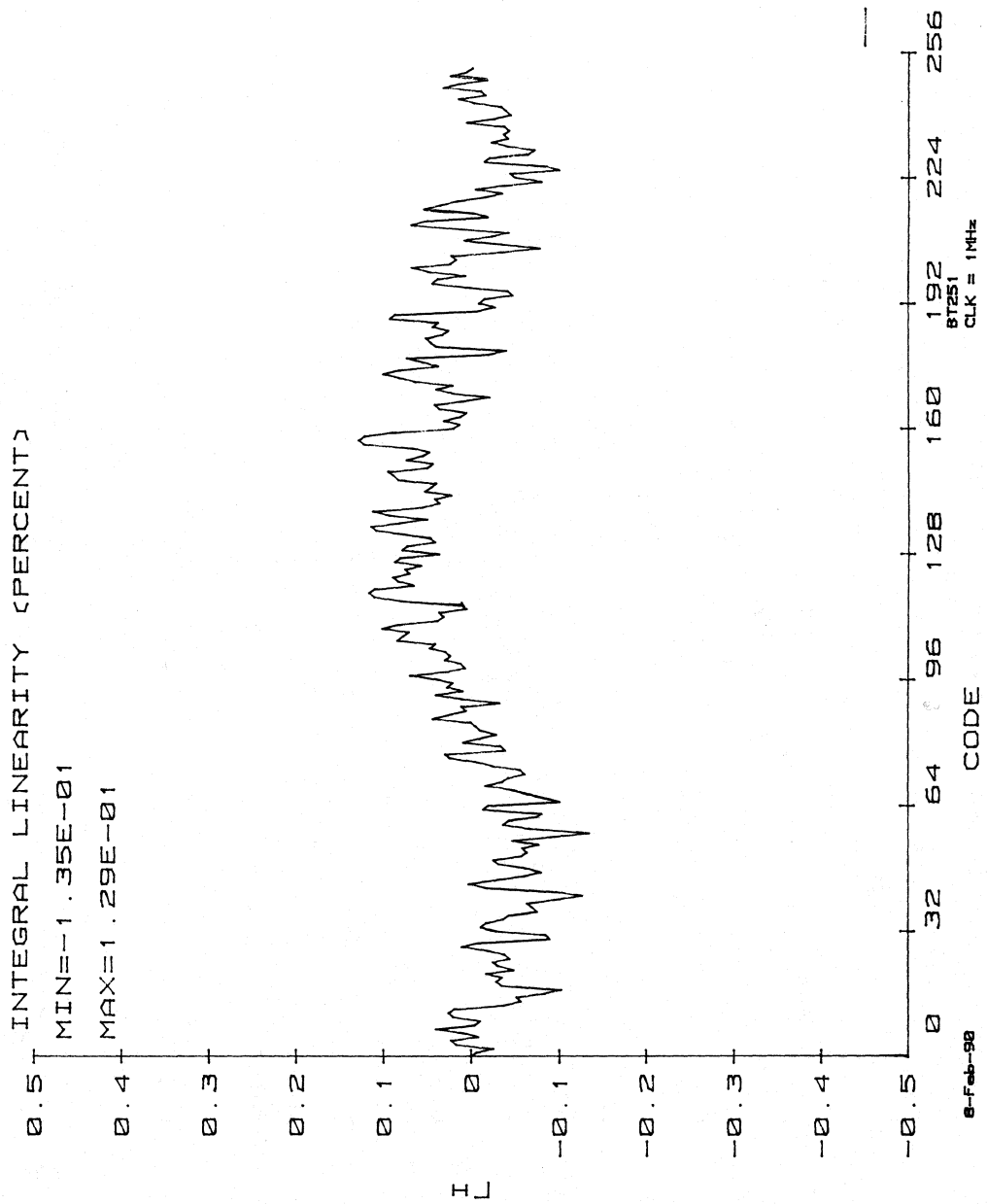

Figure 2. Typical IL Plot.

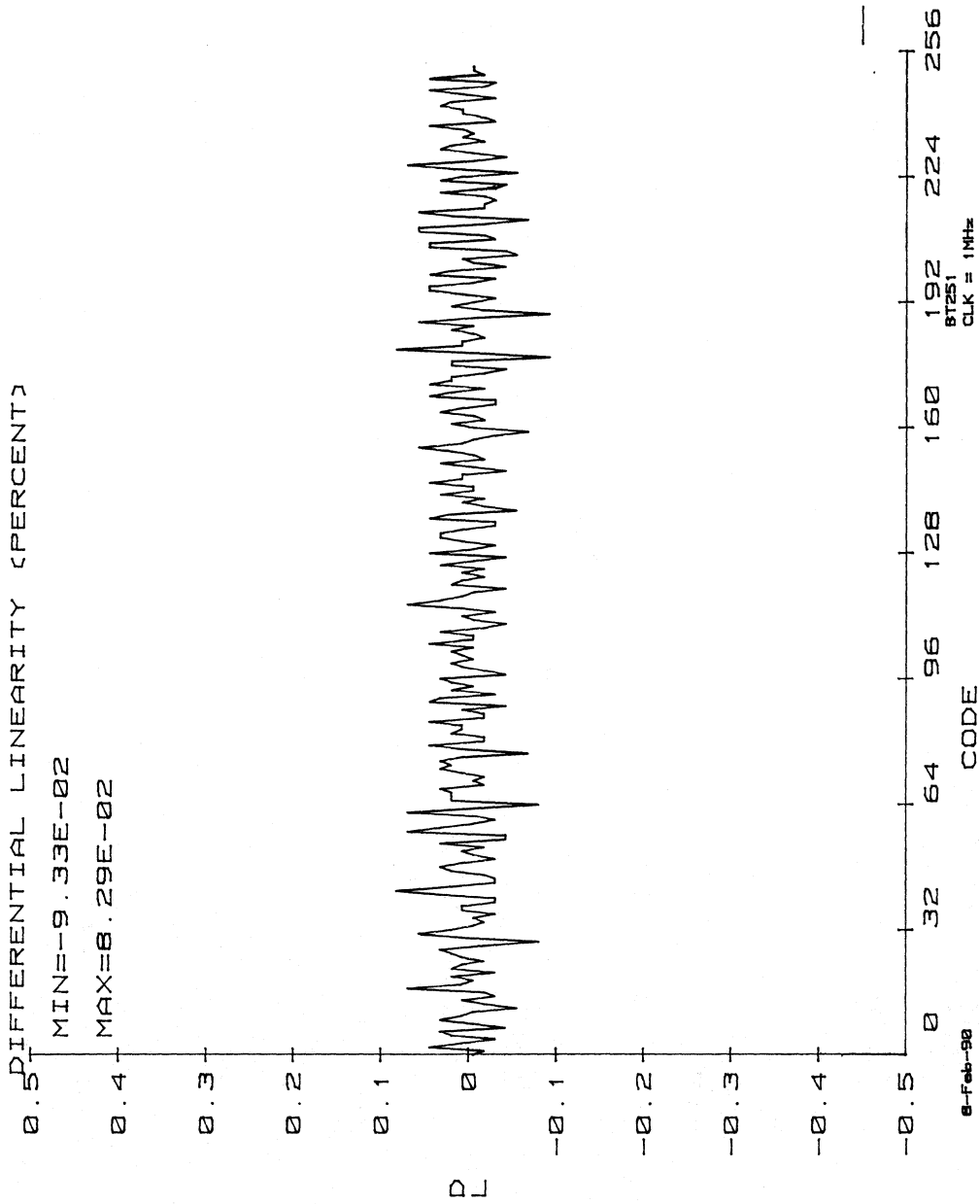

Figure 3. Typical DL Plot.

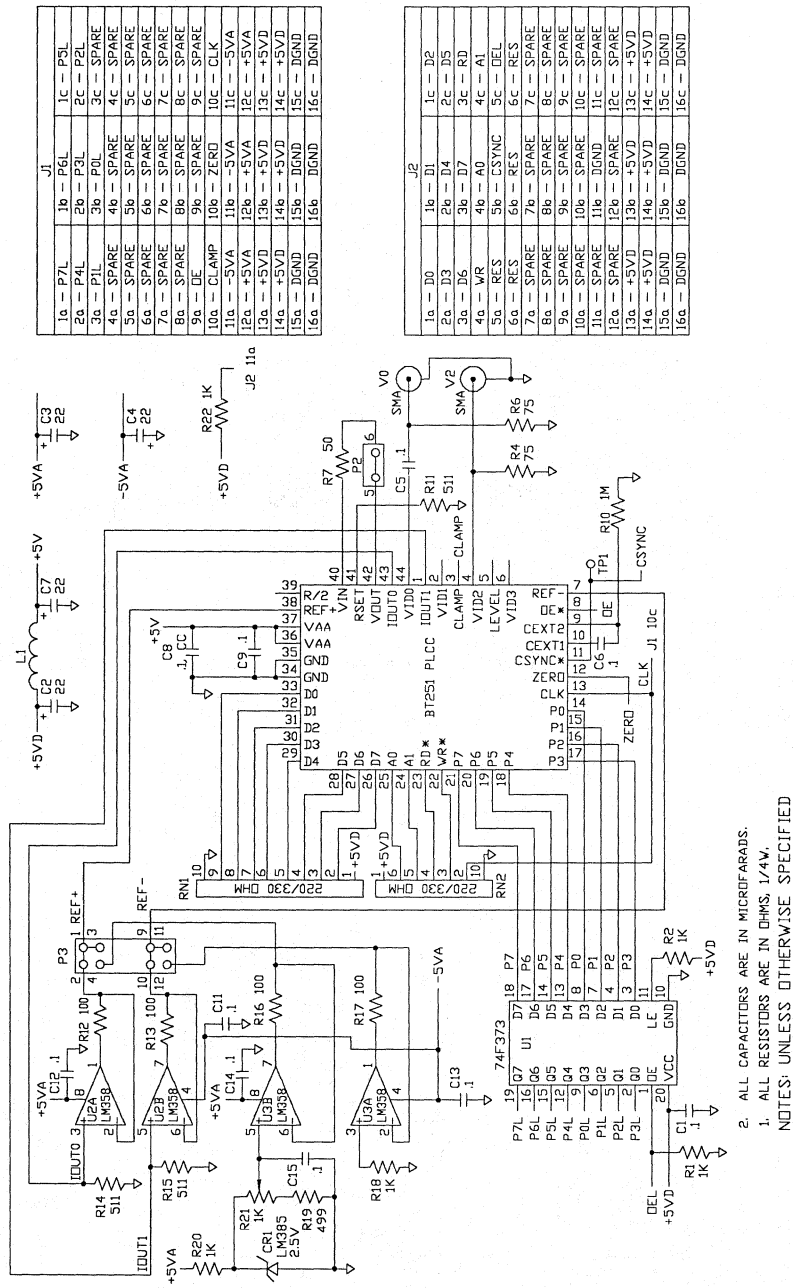

Figure 4. Schematic Diagram.

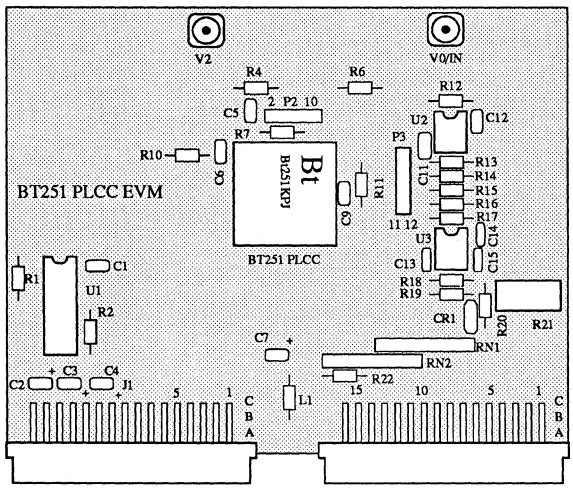

Figure 5. Assembly Diagram.

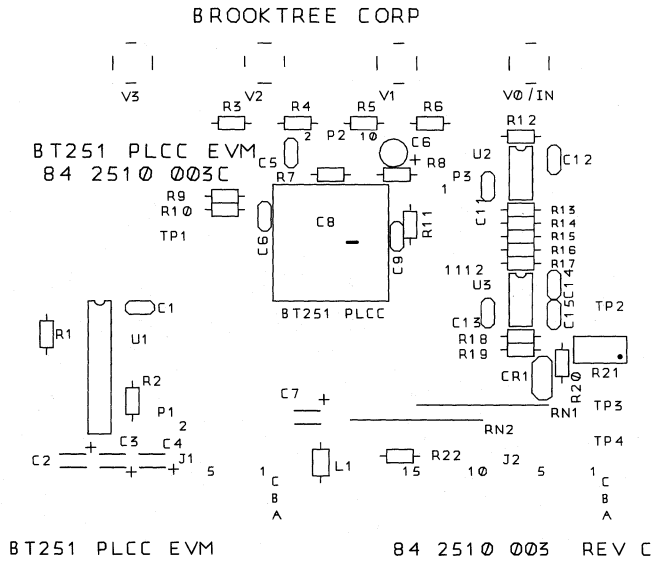

Figure 6. Silkscreen Layer.

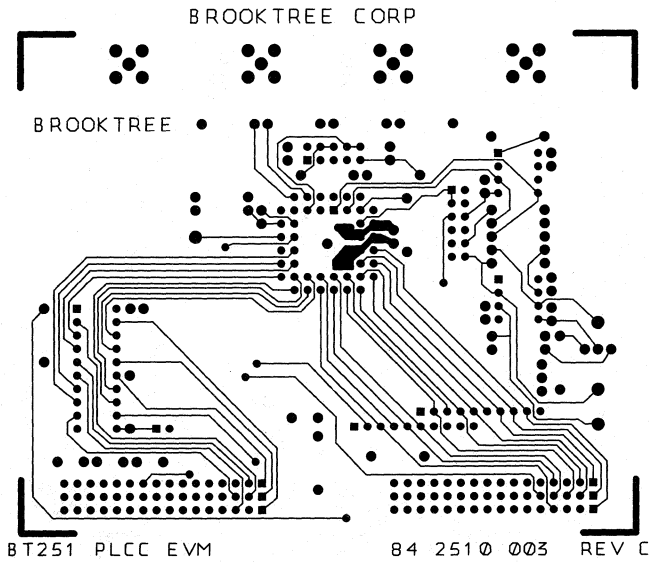

Figure 7. Signal Interconnect Plane.

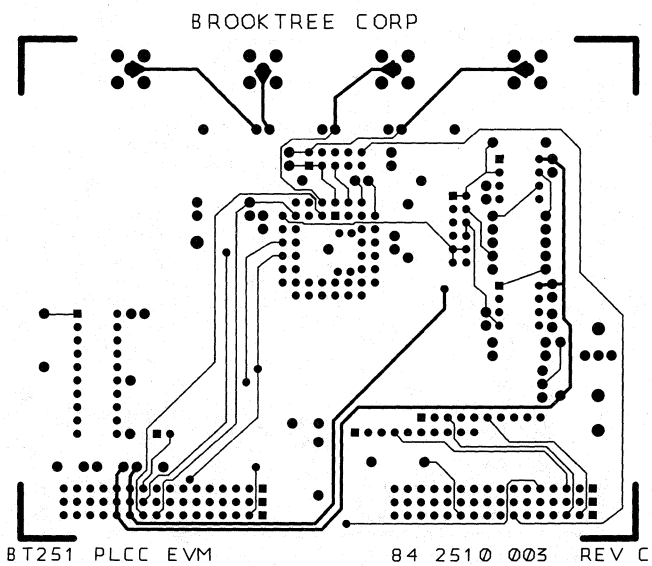

Figure 8. Signal Interconnect Plane.

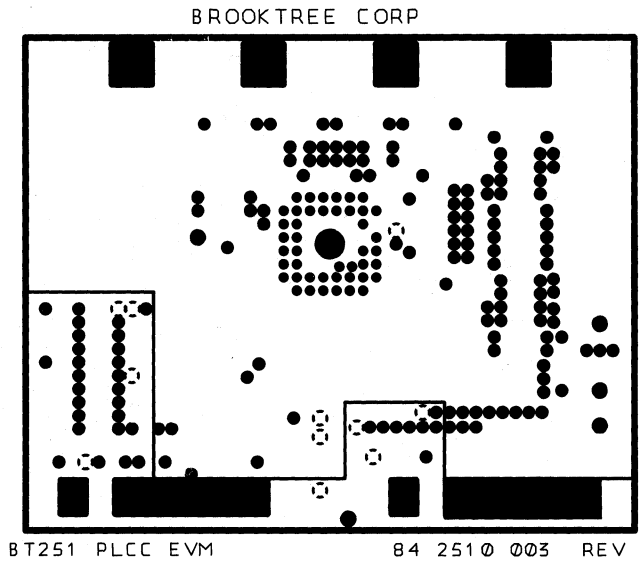

Figure 9. Power Plane.

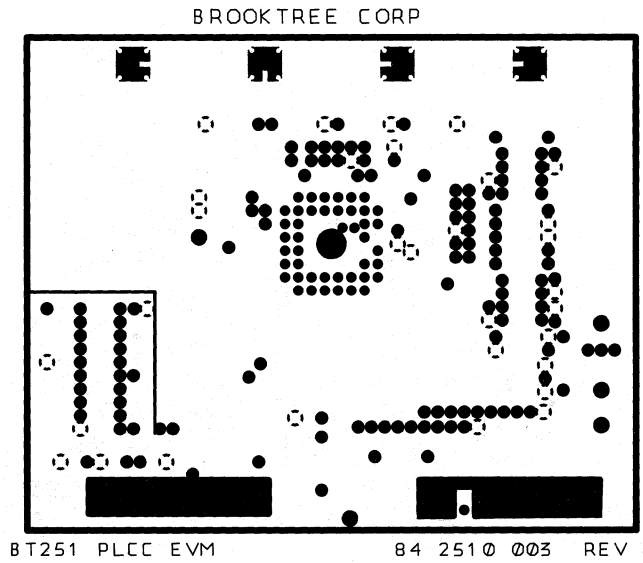

Figure 10. Ground Plane.

Bt253 Evaluation Module Operation and Measurements

Introduction

The Bt253EVM is a multi-layer printed circuit board that contains three SMA connectors (RGB inputs), circuitry for software controllable reference levels for each color, and two 48-pin DIN connectors.

In combination with a customer-designed driver board, this EVM board can be used to evaluate the Bt253, or for testing at incoming inspection.

Driver Boards

The driver board is a user configured custom designed circuit that connects to the Bt253EVM by a 48-pin DIN input connector. The driver board should provide all clock and control signals to the Bt253, as well as the ability to receive the digitized outputs. All input signals should conform to the Bt253 datasheet specifications.

Operation

The Bt253EVM provides SMA connectors for the Red, Green, and Blue video input signals. The video input signals are DC coupled to the Bt253. In this configuration the level inputs for each of the three colors should be left floating. It should be noted that RS-170 signals have the potential to be offset as much as 2V from ground. This should be taken into consideration when attempting to digitize an RS-170 video signal. Since the Bt253 allows for the connection of two video sources per color, the control register must be programmed to digitize the VID0 video signal. In addition, the Bt253 allows for multiple sync sources, sync0, sync1, and all video channels. The Bt253EVM must therefore be programmed to detect sync on one of the VID0 video sources. In most applications sync will be present on the green channel, but that is not required.

To program the Bt253, the A0 - A2 lines are used to specify which register is being accessed. These control lines are latched into the Bt253 on the falling edge of RD* or WR*. During a read cycle data is valid 40 ns after RD* is asserted. During a write cycle the WR* line must be asserted for a minimum of 50 ns, with data valid 10 ns before the rising edge of WR*. Data is latched into the Bt253 on the rising edge of WR*. MPU operations are asynchronous to the pixel clock.

The Bt253 control register must be programmed for the appropriate digitization mode. Four modes are supported: 8 bit pseudo color, 8 bit true color, 15 bit true color, and 24 bit true color. See Table 1 for output configuration.

Once the Bt253EVM is programmed for its environment, video can be sampled and digitized. The reference voltages used in the digitization process are under the control of DACs in the Bt253. The reference voltages can be varied by changing the values in the IOUT data registers of the Bt253. These registers may be written to or read from at any time, and are not initialized.

The IOUT registers specify the output current on the IOUT0 through IOUT5 output pins. The six MSBs of data are used to drive the DACs. D0 and D1 (the two LSBs) must be programmed to be a logical zero.

To ensure linearity, the Bt253 must be periodically zeroed. Asserting ZERO during each horizontal retrace period is convenient, and will keep the linearity of the Bt253 in spec. It should be noted that the Bt253

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should have ZERO asserted for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of scan lines that will have occurred before using the Bt253.

The video signal is sampled on the falling edge of the sample clock, with an aperture delay of 10 ns. The data is valid 40 ns after the rising edge of the sample clock. The data is then fed to a transparent latch before reaching the DIN connector. The user should determine when the data will be valid out of the transparent latch for the clock frequency being tested.

AC Measurements

SNR

Signal to Noise Ratio is defined as the ratio of the amplitude of a desired signal at any point to the amplitude of noise signals at that same point. SNR in digitizers can also be described as the amount of noise introduced by the digitization process.

There are many methods that can be used to evaluate the SNR of a flash converter, or digitizer. One method that is well suited for use with the EVM is the Best Fit Sine Wave method.

	24-Bit True Color	15-Bit True Color	8-Bit True Color	8-Bit Pseudo Color
Output Pins	Mode (00)	Mode (01)	Mode (10)	Mode (11)
R7	R7	0	R7	G7
R6	R6	R7	R6	G6
R5	R5	R6	R5	G5
R4	R4	R5	G7	G4
R3	R3	R4	G6	G3
R2	R2	R3	G5	G2
R1	R1	G7	B7	G1
R0	R0	G6	B6	G0
G7	G7	G5	R7	G7
G6	G6	G4	R6	G6
G5	G5	G3	R5	G5
G4	G4	B7	G7	G4
G3	G3	B6	G6	G3
G2	G2	B5	G5	G2
G1	G1	B4	B7	G1
G0	G0	B3	B6	G0
B7	B7	0	R7	G7
B6	B6	0	R6	G6
B5	B5	0	R5	G5
B4	B4	0	G7	G4
B3	B3	0	G6	G3
B2	B2	0	G5	G2
B1	B1	0	B7	G1
B0	B0	0	B6	G0

Table 1. Color Output Configurations.

With the Best Fit Sine Wave method, a sine wave of known amplitude and frequency is used as the signal to be digitized. An input clock is chosen such that the sample points on the sine wave will not repeat until a given number of samples later. In the configuration to be outlined, 4096 samples will be taken before the same point is reached on the sine wave.

These 4096 samples are then used to reconstruct one period of a sine wave. Since the 4096 samples are never repeated, they can be used to construct a sine wave with greater resolution than a simple reconstruction at the clock frequency. This reconstructed sine wave is then compared against the ideal sine wave that was input into the Bt253. Any errors in the reconstructed sine wave will be due to noise, and may be used to determine the Signal to Noise Ratio of the Bt253.

Data Output Delay

Data output delay in the Bt208 is the time from the rising edge of the sample clock to valid data on the pixel outputs. The Bt208 has a maximum output delay of 25 ns. This delay may be seen on an oscilloscope by triggering the oscilloscope on the rising edge of the pixel clock and determining the time required for the pixel outputs to change.

DC Measurements

Linearity

Linearity can be broken down into two measurements. Integral Linearity and Differential Linearity.

Integral Linearity is the maximum deviation from a straight line that has been best fit to the data points of the input-output transfer function. Linearity is normally expressed as a fraction of an LSB or as a percentage of full scale. The Bt253 has a typical value of ± 1/2 LSB, with a maximum value of ± 1 LSB.

Differential Linearity is the maximum deviation of any bit size from its theoretical value 1 LSB over the full conversion range. For example, a Differential Linearity of ± 1/2 LSB demands that each step be 1 LSB ± 1/2 LSB. A Differential Linearity of < 1 LSB is the maximum allowed for monotonic operation. The Bt253 has a typical value of ± 1/4 LSB Differential Linearity with a maximum value of ± 1 LSB. One LSB is approximately 0.4% of full scale.

Performance Measurements

This section will illustrate measurement examples of Signal to Noise Ratio and Linearity. The signal to noise measurements require that a driver board be built which will facilitate the storage of 4096 samples of digitized data. This data can then be fed to a program which can calculate the SNR from the sampled data (Equation 1).

To measure and plot the Integral and Differential Linearity of the Bt253, the driver board must contain circuitry similar to that of Figure 1. This figure shows a closed loop system that can be used to measure voltage and step values. These values can then be used in Equation 2 and Equation 3 to plot the Integral and Differential Linearity, respectively.

AC Characterization

Signal to Noise Ratio can be measured in a variety of ways. Many of the methods require expensive equipment and precision waveforms. The method we will be showing is very simple to implement, and will give an accurate SNR value.

As mentioned earlier, the Best Fit Sine Wave method will be used. This involves sampling a known sine wave at a frequency such that no two of the 4096 samples taken will be on the same point of the sine wave.

Once the data has been sampled and stored it may be fed to a series of software functions. The first function must reorder the samples to make one period of a sine wave. This function must know the frequency of the sampled sine wave, the frequency of the sample clock, the number of samples, and the starting point of the input array. With these pieces of information, the software can take the input array and restructure it to appear as a single cycle of a sine wave. Once this has been accomplished, the output array can be passed to the next section of software.

Once the data has been reordered, a sine wave must be fit to these data points. An algorithm to fit a sine wave to a set of data points is discussed in the IEEE Standard for Waveform Recorders (1057-1988). *Section 4.1.3.1 An algorithm for three parameter (known frequency) least squared fit to sin wave data* presents an algorithm to fit a sine wave to a set of data points, given the number of samples and the frequency. A series of sums are computed which will

yield a set of values that give the amplitude of the reconstructed sine wave, and the RMS error of the data from the ideal sine wave.

With the amplitude and RMS error, the SNR of the Bt253 can be calculated. Equation 1 gives the formula for computing the SNR, given amplitude and RMS error.

$$SNR = 20\ LOG_{10}((Amplitude * SQR(2))/(2*E_{RMS}))$$

Equation 1.

DC Characterization

The Integral and Differential Linearity of the Bt253 may be measured quite easily with the Bt253EVM. The circuit shown in Figure 1 uses a closed loop system to obtain data points which can be plotted to measure the Integral and Differential Linearity of the Bt253.

The Threshold Select lines, I0 through I7, represent the desired output of the Bt253. These lines may be driven with a simple DIP switch arrangement. The chosen threshold value is presented to the two 4-bit comparators, which measures it against the digitized output of the Bt253. The comparators will then raise or lower the analog input voltage until the digitized value out of the Bt253 is equal to the selected threshold value. A simple DVM can then be used to measure the output of the integrator to obtain the analog voltage required to generate the specified digital output.

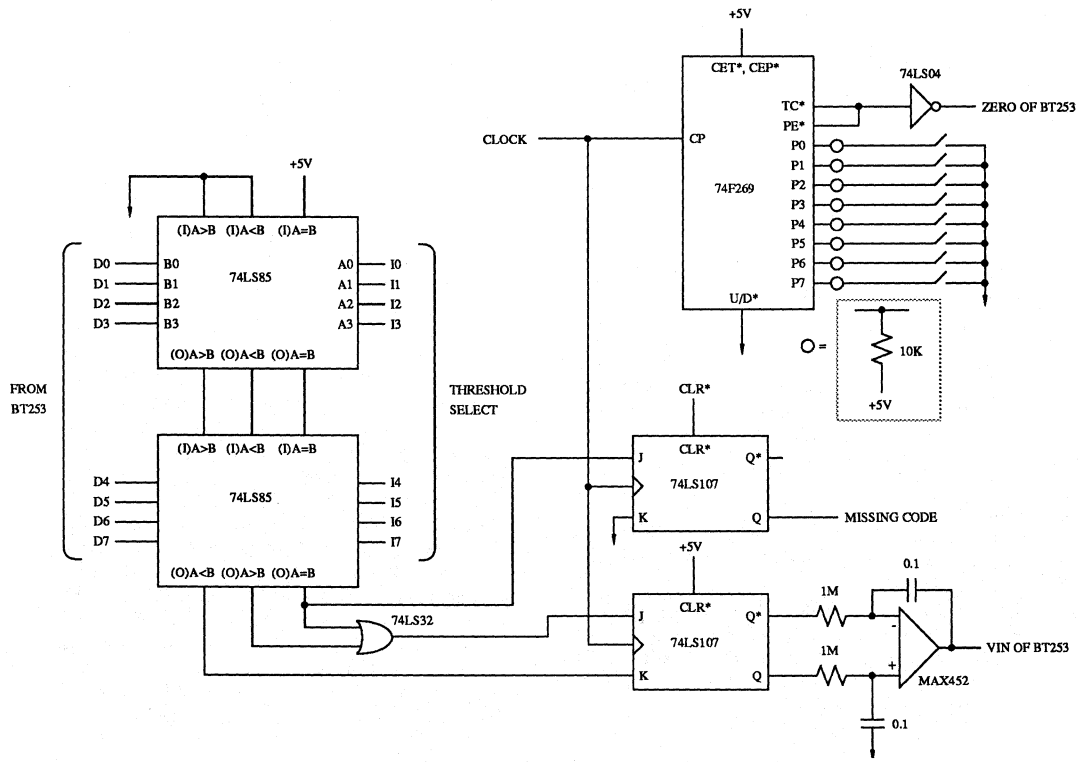


Figure 1. Integral and Differential Linearity Measurement Circuit

The voltages corresponding to each threshold value from 0 to 254 should be recorded to use in computing and plotting the Integral and Differential Linearity of the Bt253.

Plot Integral Linearity as:

For I = 1 to 253:

$$IL(I) = 100*\left(\frac{I}{254} - \frac{VOLT(I) - VOLT(0)}{VOLT(254) - VOLT(0)}\right)$$

Equation 2.

Plot Differential Linearity as :

For I = 1 to 254:

$$DL(I) = 100*\left(\frac{VOLT(I) - VOLT(I-1)}{VOLT(254) - VOLT(0)} - \frac{1}{254}\right)$$

Equation 3.

Typical plots for Integral and Differential Linearity are shown in Figures 2 and 3. IL and DL are expressed as a percentage of full scale in these plots.

PCB Construction

The Bt253EVM board is an epoxy fiberglass board constructed with four 1 oz copper layers: VAA, 2 signal planes, and ground. The Bt253EVM design is outlined with a schematic diagram giving the component values and the DIN I/O connections, the assembly diagram of component placement, and the PCB artwork film.

The PCB artwork is provided for evaluation purposes only. These layouts should not be considered ideal, and have not been tested for FCC compliance. The following descriptions highlight critical component placement and considerations.

Schematic Diagram (Figures 4 & 5)

The Bt253 Evaluation Module schematic shows the pixel outputs of the Bt253 connected directly to the inputs of a 74F373. By only driving one TTL load with each output, less ringing is present on the digital outputs. This will help the Bt253 keep noise down to a minimum.

Assembly (Figures 6 & 7)

Figure 6 shows the Bt253EVM as it is shipped to the customer. The silkscreen layer is shown in Figure 7. This provides a more detailed view of the board. Note should be taken of the proximity of the decoupling capacitors to the Bt253.

Signal Interconnect Plane (Figures 8 & 9)

The digital traces are separated from the analog area as much as possible to prevent coupling. The analog signals are kept in the analog area to reduce noise.

Power Plane (Figure 10)

The analog and digital power planes are combined at a point with a ferrite bead (L1). The analog power area underlays the analog signals to reduce noise.

Ground Plane (Figure 11)

The analog and digital ground areas are separated using tub isolation. They are connected as close as possible to the power and ground connector to reduce noise.

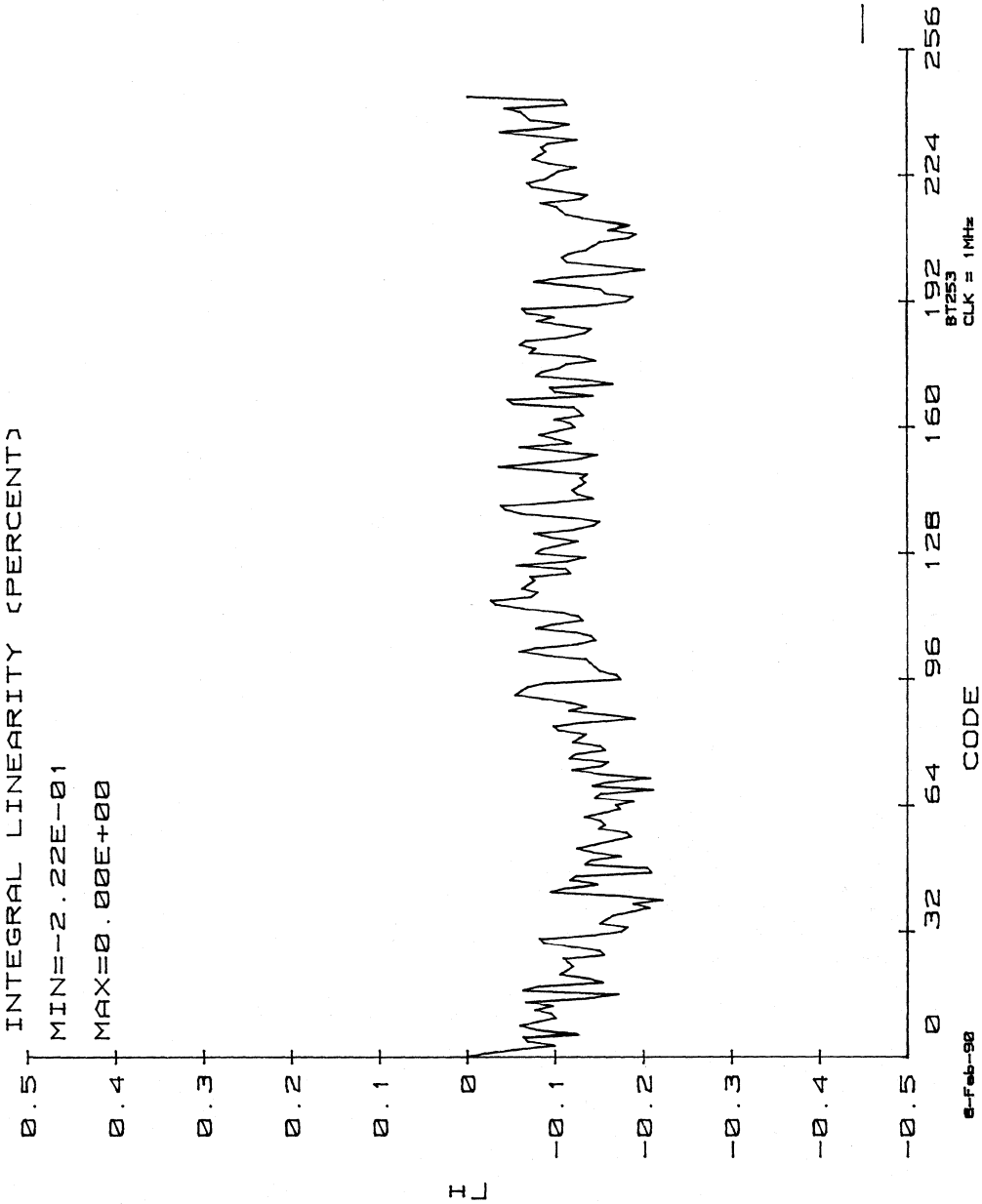


Figure 2. Typical IL Plot.

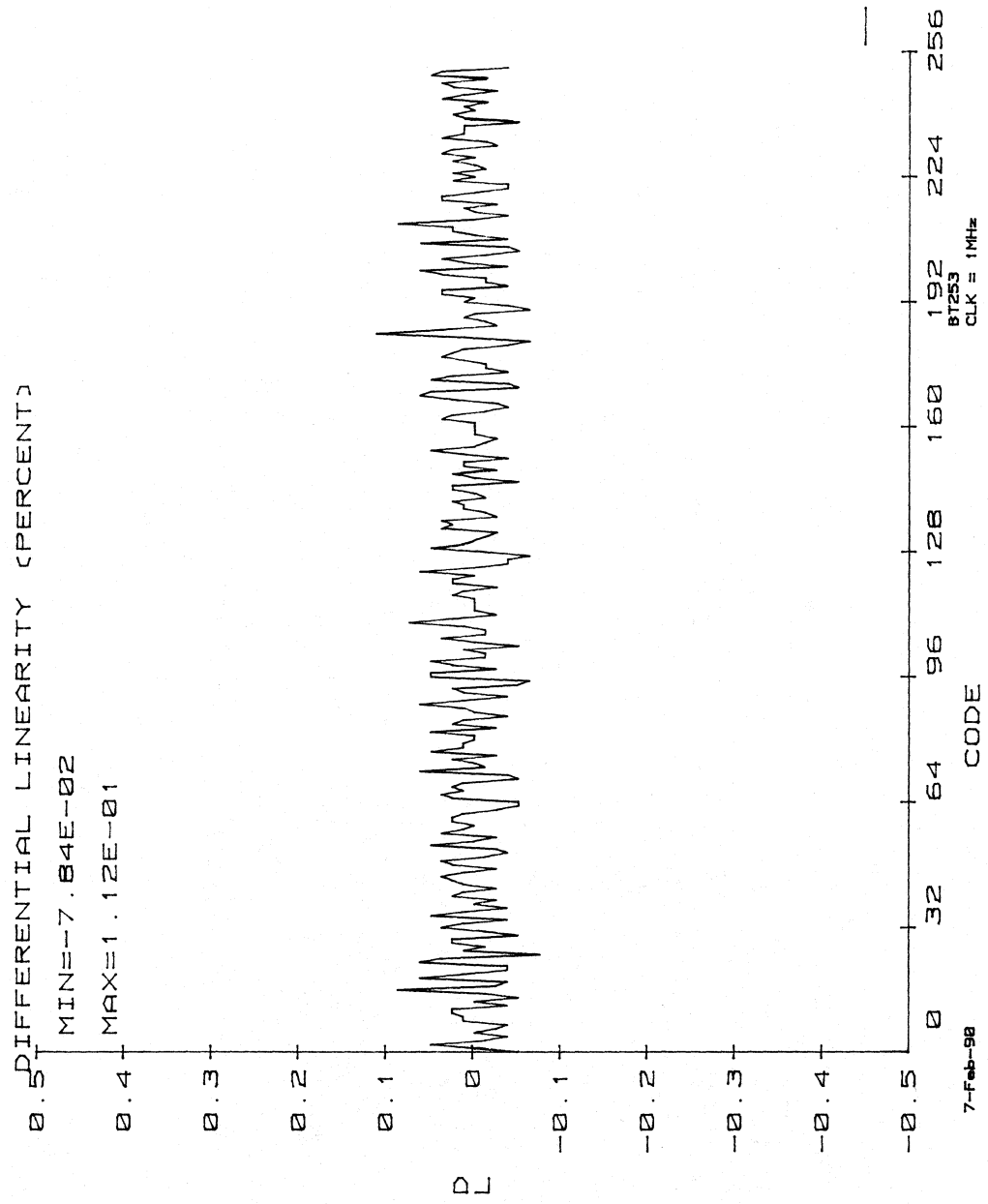


Figure 3. Typical DL Plot.

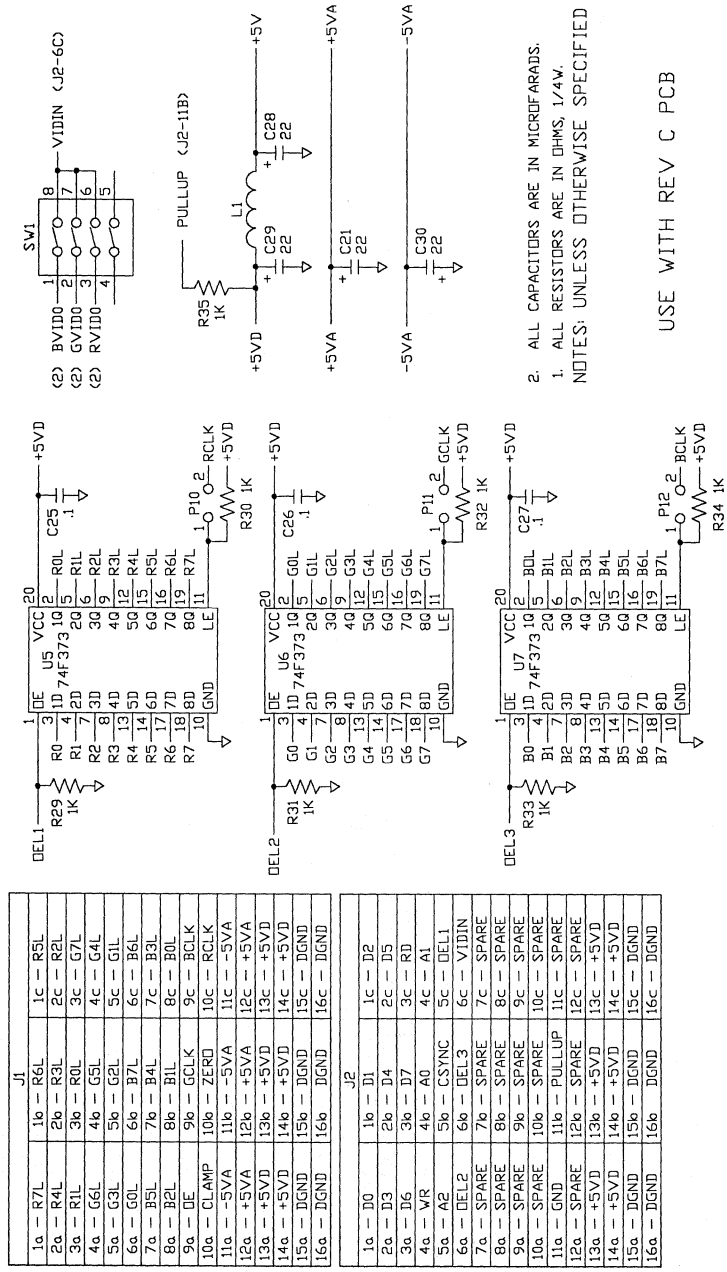


Figure 4. Schematic Diagram.

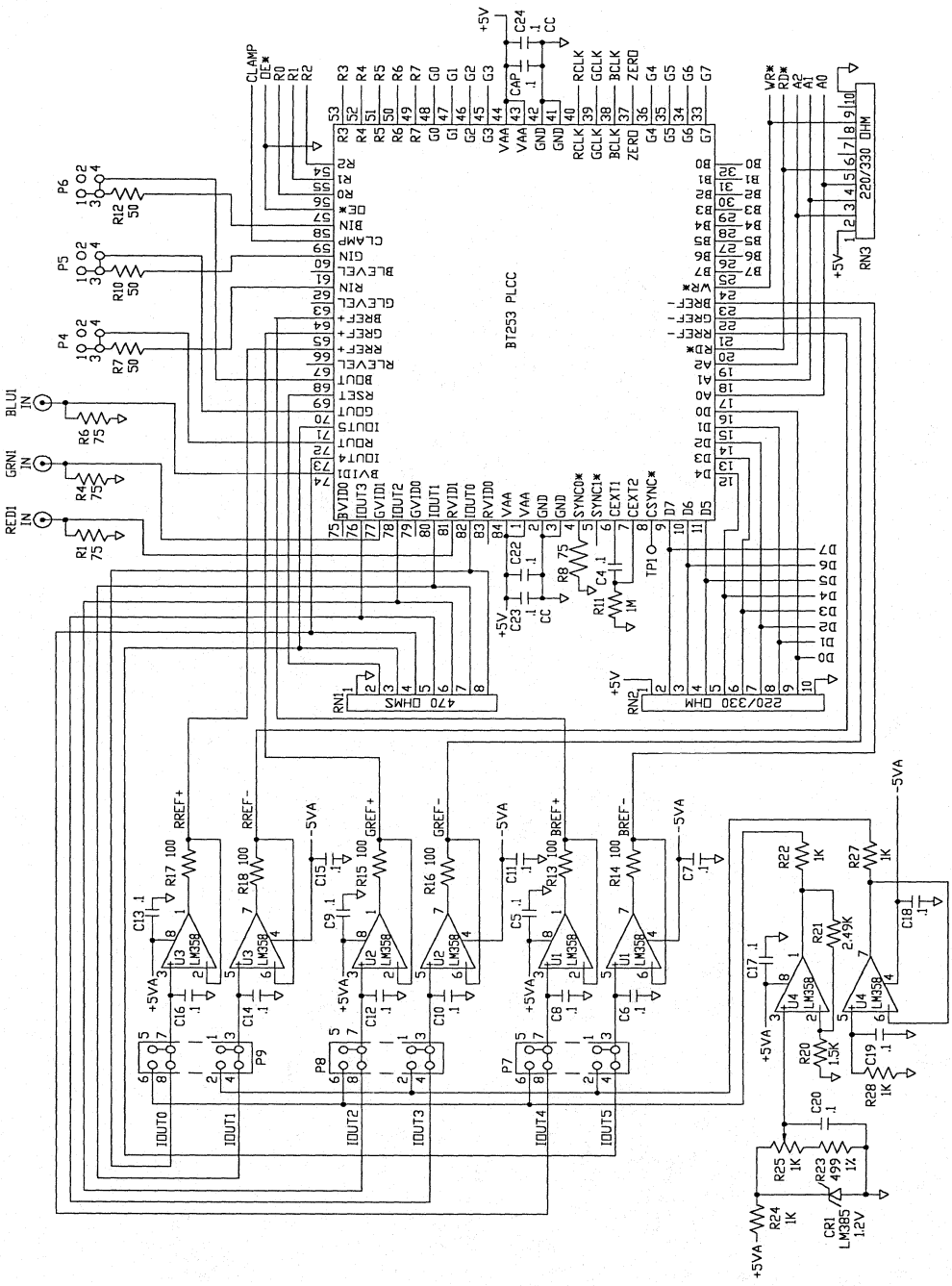


Figure 5. Schematic Diagram (continued)

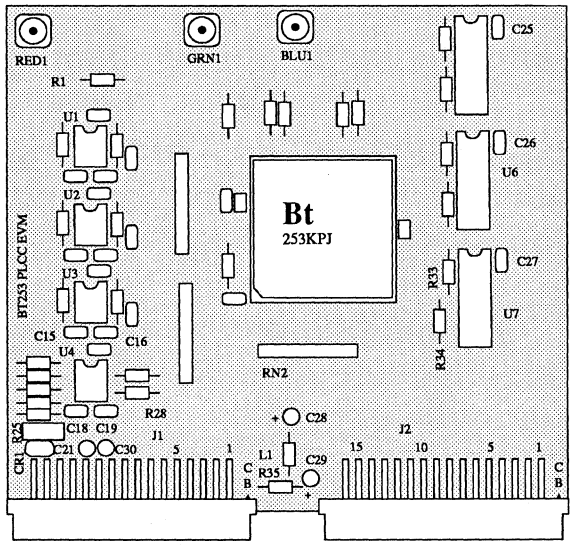


Figure 6. Assembly Diagram.

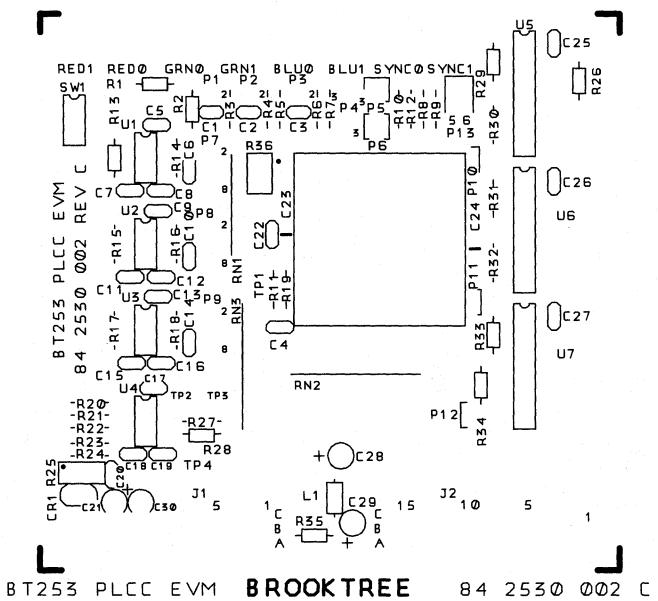


Figure 7. Silkscreen.

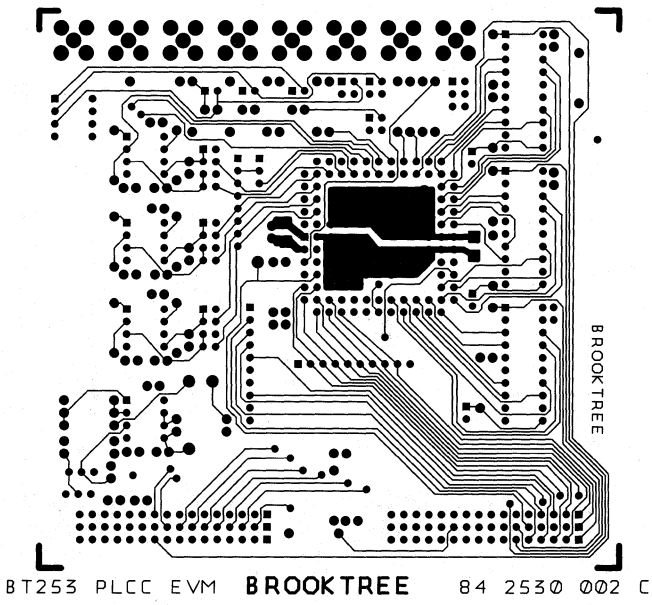


Figure 8. Signal Interconnect Plane.

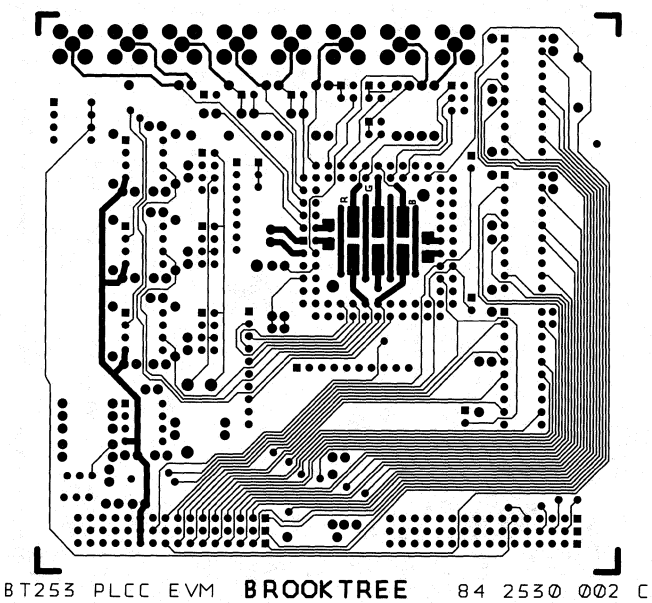


Figure 9. Signal Interconnect Plane.

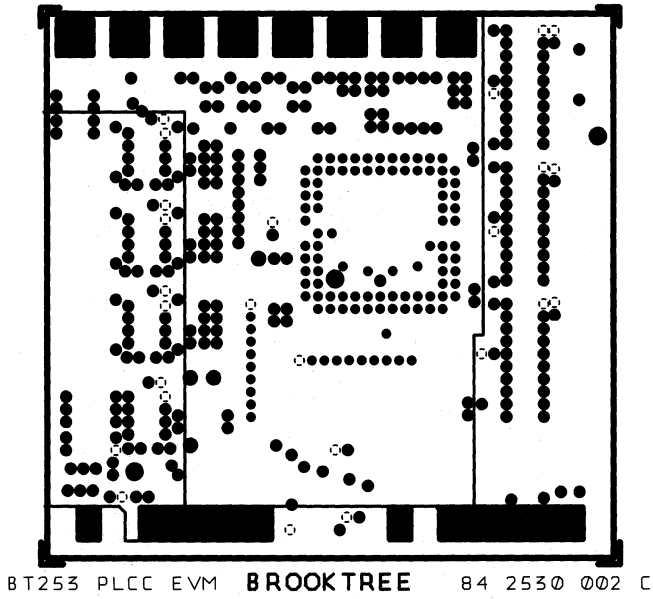


Figure 10. Power Plane.

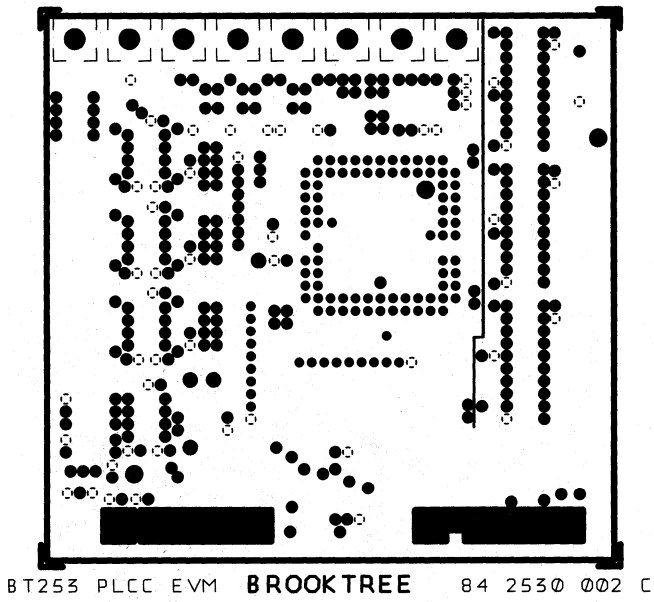


Figure 11. Ground Plane.

Bt451/457/458 Evaluation Module Operation and Measurements

Introduction

The Bt451EVM is an evaluation circuit board for the Bt451, Bt457, and Bt458 pin/software compatible RAMDACs. The EVM features an 84-pin PGA socket, voltage reference circuitry, SMA output connectors and a 96-pin DIN input connector.

In combination with a customer-designed driver board, this EVM can be used to evaluate the RAMDACs, or test at incoming inspection.

Features

The Bt451EVM can be used to exercise all of the functionality of the respective RAMDACs. The on chip features include programmable blink rates, bit plane masking and blinking, and selectable pixel multiplexing. Each of these features are controlled by a driver board supplied by the user.

The RAMDACs also include a 256 location dual port color palette RAM, and 4 dual ported overlay registers. The word length of the color palette, overlay registers, and output structure are different for each of the RAMDACs.

Bt451

The color palette RAM and overlay registers of the Bt451 are 12 bits wide, and drive three 4-bit VIDEODACs. This structure allows for pseudo-color applications with 256 displayable colors out of a palette of 4096.

Bt457

The Bt457 is a single channel version of the Bt458. It has a 256 X 8 color palette, and four 8-bit overlay registers. The Bt457 is aimed at 24 bit true color applications where three Bt457s would be used. When installed in the EVM the Bt457 can only be used to evaluate gray scale applications. It can not be connected to other Bt457EVM boards to provide 24 bit true color.

Bt458

The Bt458 overlay registers and color palette RAM outputs are 24 bits wide and drive three 8-bit VIDEODACs. This allows the Bt458 to be used in pseudo-color applications where a larger addressable palette address is required. In this case the palette is 16 million colors.

Driver Board

The driver board is a user-configured custom-designed circuit that connects to the 96-pin DIN input connector of the EVM and provides stimulus to the RAMDAC. The input signals drive and timing specifications should conform to the Bt451/7/8 datasheet.

Driver board designs vary a great deal, dependent upon the measurement and accuracy required. Designs can provide an interface with existing test equipment or a custom design to facilitate multiple parameter characterization.

Designing a driver board for the multiplexed pixel/overlay inputs requires a multiplexer interface so that pixels are presented to the RAMDAC at the load clock rate. Composite video sync and blank timing generation can be accomplished with a PAL device.

The block diagram of a general purpose driver board is shown in Figure 1. The microprocessor interface port can be used to upload the palette and overlay RAMs, and address the RAMDAC internal registers.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

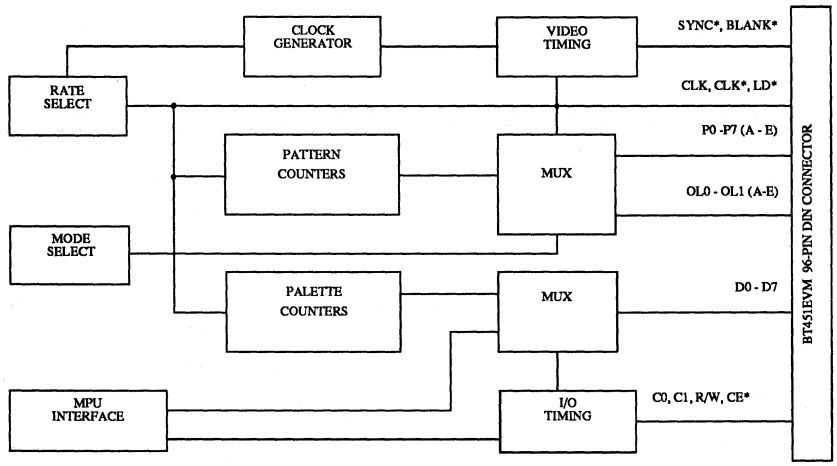


Figure 1. Driver Board Block Diagram

Operation

The EVM board contains a 100 ohm trimpot in series with a 470 ohm resistor to provide a variable RSET value. RSET is used to set the full scale output current, and thus the full scale output voltage, of the DAC. The relationship between RSET and the full scale output current on IOG or IOUT for the Bt457 is:

RSET (ohms) = 11,294 * VREF(v) / IOG (mA).

The full scale current on IOR and IOB for the Bt451 and Bt458 is:

IOR, IOB (mA) = 8,067 * VREF (v) / RSET (ohms)

With the trimpot all the way off, the RSET value is 470 ohms, giving a full scale IOG of 29.31 mA, typical. Full scale IOR and IOB would be equal to 20.94 mA, typical. With the trimpot fully on, the RSET value would increase to 570 ohms, giving a full scale IOG of 24.17 mA and a full scale IOR/IOB of 17.26 mA.

The FS ADJUST pin on the RAMDAC should be equal to the voltage on the VREF pin. VREF should be equal to approximately 1.235V, the nominal output voltage of an LM385BZ-1.2 voltage reference. The COMP pin should have a voltage equal to approximately 3V.

Since the EVM board may be used to test the Bt451, the Bt457, and the Bt458, the user may wish to evaluate more than one part. To remove the RAMDAC without damaging it or the EVM board, a PGA extraction tool, such as the Augat TX8136, should be used. To prevent latch-up when inserting a device into the EVM, power must be off to assure that no inputs will exceed the VAA by greater than + 0.5V. Note: Signals to the EVM should be at a logical low level until power to the EVM has stabilized.

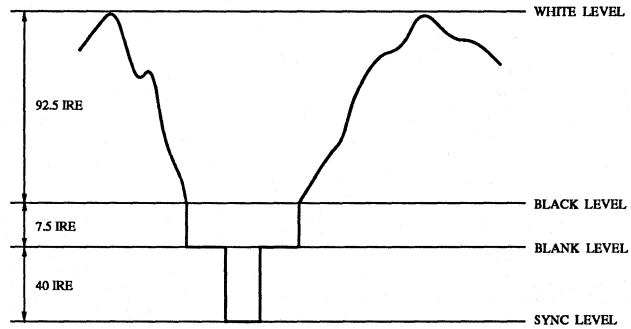
The Bt451EVM has been optimized for analog fidelity and thus can be used to measure a variety of DC and AC parameters from the Bt451/7/8 datasheet specifications. Parameters such as Video output levels, Pixel Rise, Fall and Settling times, Glitch, Feedthrough, Prop Delay, PSRR and others can be measured and verified. The measurement equipment accuracy and proper measurement technique must be considered for each parameter setup to assure consistent and accurate results.

DC Measurements

RS343 Levels

A video ouptut waveform that conforms to RS343 compatible levels has the green channel output voltage set to + 1.0V with the sync and blank pins enabled. This is done by adjusting the RSET trimpot. For a 75-ohm doubly-terminated load the total RSET value is 523 ohms. Using a Vref of 1.234V and a total

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 523 ohms, VREF = 1.235v. RS343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform

load impedance of 37.5 ohms, Figure 2 shows the typical output current and voltage values for a RS343A composite video signal.

The measured video signal output peak-to-peak amplitude for the green channel will be 1.0v ± 0.05 volts. The red and blue video signal will have a peak-to-peak amplitude of 0.714v ± 0.1 volts. The measured sync level should be 0.286v ± 0.05 volts and a measured blank level of 0.054 ± 0.018 volts. The intensity or grey scale range is the difference in output from blank to white. These values should measure 0.660 ± 0.018 volts on all channels.

Linearity

Integral Linearity Error is the maximum deviation of the output from a straight line passing through the end points. This value is expressed in LSBs or percent of the grey scale range. If the code into the RAMDAC is at any value (N), the output voltage should be N / 255 of the full-scale output. The maximum deviation from that output value to the straight line value is the Integral Linearity Error.

Differential Linearity Error is the maximum difference between the actual step size and an ideal step size. The ideal step size is from an ideal converter with the same end points as the devices tested. If the code for an ideal RAMDAC is changed by 1 count, the output should change by 1/255 (full-scale output - zero-scale output). A deviation of this step size is a Differential Linearity Error.

AC Measurements

Rise, Fall and Settling Time

The RAMDAC output signal rise and fall times are measured from the 10% to 90% points of the transition output waveform. Settling time is a measure of how fast the RAMDAC output settles from the 50% point to within a ± 1/2 LSB value. These Rise, Fall and Settling time waveform measurement points are defined in Figure 3.

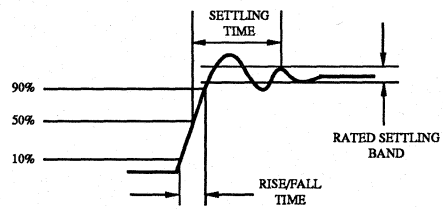


Figure 3. Rise/Fall and Settling Time.

Performance Measurements

This section will illustrate measurement examples of linearity and pixel rise/fall and settling times. The Linearity measurements can be made with a ramp output that will provide a step change equal to the LSB value. The ramp output signal is generated by providing 256 discrete input code changes to the pixel inputs. The pixel rise/fall time measurements are performed with an output signal that exercises the pixels on and off. This output signal is generated by providing input code values that change by single or multiple bits and repeats.

These measurements were made with a 1 GHz Sampler BW oscilloscope using a 75-ohm doubly-terminated coaxial cable connection. The driver board is clocked at a pixel rate of 100 MHz.

DC Characterization

Integral Linearity Error is measured with an input code that increments by the LSB value and is applied to the pixel inputs. The output is measured for each discrete input code step and recorded. The output values measured for each input code step are then put into Equation 1 for a calculation of the worst case error value in LSBs.

Integral Linearity = ((Vout (code) - Vout (0)) - Ideal (code)) * 255 / (Vout (256) - Vout(1))

Grey Scale Range = difference in output from black to white

LSB = Grey Scale Range / (2**n - 1)

Units are LSBs

Equation 1.

The RAMDAC output ramp signal is shown in Photo 1 with the sync and blank enabled. The input codes are counting at an LSB code step from 0 to 255 and repeating. The total grey scale range is 0.66 ± 0.018 volts. The LSB value for a 0.66 volts grey scale range that has 256 discrete levels is approximately 2.5 mV.

For the data shown in Table 1, the value measured for code 255 is 0.716205V. The value measured for code 0 (Black level), is 0.053952V. This value includes the setup, or blank pedestal, for the RED channel of the Bt451/7/8.

Differential Linearity is measured with an input code that increments by the LSB value and is applied to the pixel inputs. The output is measured for each discrete input code step and recorded. The output values measured for each input code step are then put into Equation 2 for a calculation of the worst case error value in LSBs.

Differential Linearity = (((Vout (code) - Vout (code-1)) * 255) / (Vout (256) - Vout (1))) - 1

Units are LSBs

Equation 2.

AC Characterization

Output rise/fall time measurements can be taken when a single or multiple input code change pattern is repeatedly applied to the pixel inputs. This burst or multi-burst pixel pattern is used to exercise the RAMDAC output switching transition. The pixel burst code pattern is shown in Photo 2 with the sync and blank enabled.

The output pixel burst signal that is shown in Photo 3 is enlarged such that calibrated measurements can be made on the pixel switching characteristics. The DAC rise time value is 2 ns and the fall time value is 3 ns. These values indicate a good response time for a 20 ns pixel width.

Step	Measured	IL Error	DL Error
0	0.053952	0	0
1	0.056544	-0.00195	-0.00195
2	0.059054	-0.03547	-0.03352
3	0.061645	-0.03781	-0.00233
4	0.064240	-0.03861	-0.00079
5	0.066824	-0.04364	-0.00503
6	0.069336	-0.07640	-0.03275
7	0.071926	-0.07912	-0.00272
8	0.074344	-0.14807	-0.06895
9	0.076935	-0.15041	-0.00233
10	0.079445	-0.18394	-0.03352
11	0.082035	-0.18666	-0.00272
12	0.084621	-0.19092	-0.00426
13	0.087211	-0.19364	-0.00272
14	0.089725	-0.22563	-0.03198
15	0.092316	-0.22797	-0.00233
16	0.095618	0.04346	0.27143

Table 1.

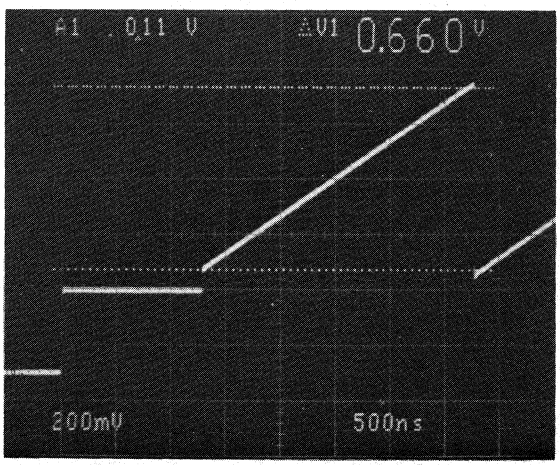


Photo 1. RAMDAC Output Ramp.

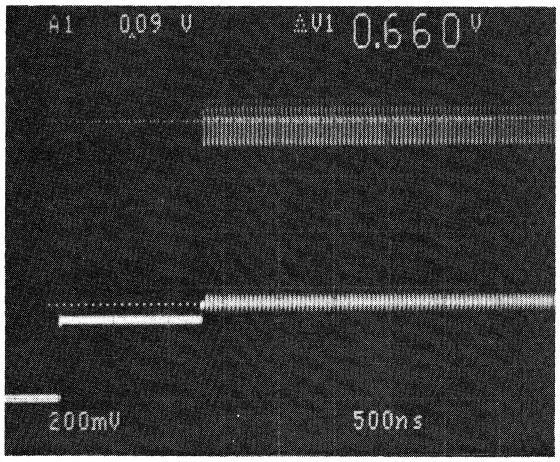


Photo 2. Pixel Burst Code Pattern.

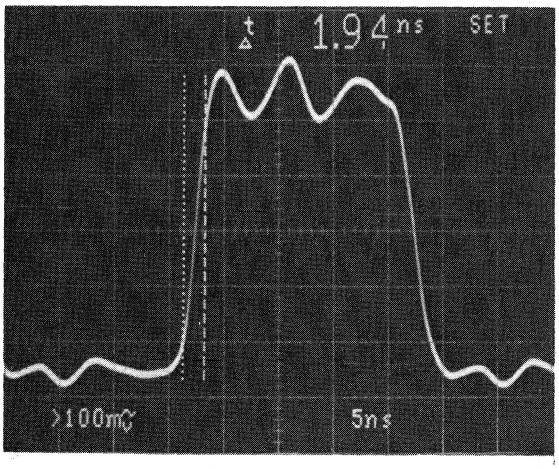


Photo 3. Rise/Fall Time.

PCB Construction

The Bt451EVM board is an epoxy fiberglass board with four copper planes for power, ground, and signal interconnects.

The following descriptions highlight critical component placement and considerations for modification of this information to your application environment.

Schematic Diagram (Figure 4)

Parallel termination (R1/R2) is used on CE* to reduce noise sensitivity. The clock lines use a balanced termination (R9) to reduce the common mode noise. Jumper (J2) is shorted.

Assembly (Figure 5 & 6)

The board silkscreen is also provided in Figure 6. Pixel parallel termination (RN1-RN8) sockets are provided to reduce data feedthrough.

Signal Interconnect Plane (Figure 7)

Digital traces are separated from the analog area to prevent coupling. The analog signals overlay the analog ground area to reduce noise.

Ground Plane (Figure 8)

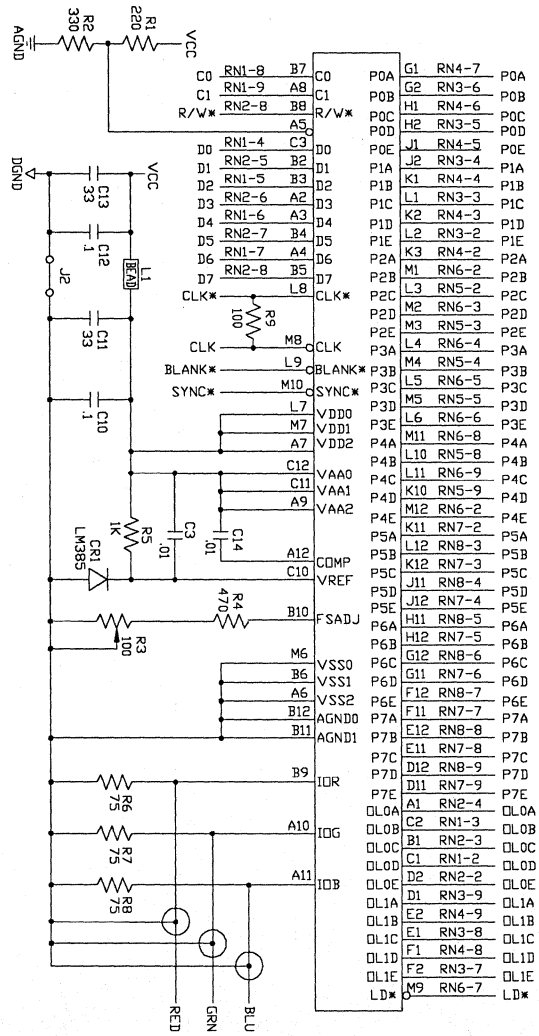
The analog and digital ground areas are shorted together at Jumper (J2). The analog areas (signal, power or ground) do not overlay any of the digital areas (signal, power or ground) to reduce signal and power coupling noise.

Power Plane (Figure 9)

The analog and digital power areas are combined at a point with ferrite bead (L1). The analog power area underlays (Figure 10) the analog signals to reduce noise.

Signal Interconnect Plane (Figure 10)

Comp chip capacitor (C14) is used for reduced lead inductance and to allow close placement to the Comp pin. The RGB output traces are short and of equal length to reduced noise pickup and signal reflections.



1a - GND	1b - GND	1c - GND
2a - GND	2b - GND	2c - GND
3a - GND	3b - GND	3c - GND
4a - VCC	4b - VCC	4c - VCC
5a - VCC	5b - VCC	5c - VCC
6a - VCC	6b - VCC	6c - VCC
7a - SPARE	7b - SPARE	7c - SPARE
8a - SPARE	8b - SPARE	8c - SPARE
9a - SPARE	9b - SPARE	9c - SPARE
10a - P7D	10b - P7E	10c - SPARE
11a - P7A	11b - P7B	11c - P7C
12a - P6C	12b - P6D	12c - P6E
13a - P5E	13b - P6A	13c - P6B
14a - P5B	14b - P5C	14c - P5D
15a - P4D	15b - P4E	15c - P5A
16a - P4A	16b - P4B	16c - P4C
17a - CLK*	17b - LD*	17c - SYNC*
18a - CLK	18b - BLANK*	18c - SPARE
19a - P3C	19b - P3D	19c - P3E
20a - P2E	20b - P3A	20c - P3B
21a - P2B	21b - P2C	21c - P2D
22a - P1D	22b - P1E	22c - P2A
23a - P1A	23b - P1B	23c - P1C
24a - P0C	24b - P0D	24c - P0E
25a - OL1E	25b - P0A	25c - P0B
26a - OL1B	26b - OL1C	26c - OL1D
27a - OL0D	27b - OL0E	27c - OL1A
28a - OL0A	28b - OL0B	28c - OL0C
29a - D2	29b - D1	29c - D0
30a - D5	30b - D4	30c - D3
31a - CE*	31b - D7	31c - D6
32a - C1	32b - R/W*	32c - C0

5. ON RN1-RN8 THERE IS A .01 CAP TO PWR AND GND.
4. RN1-RN8 PIN 10 TO VCC.
   RN1-RN8 PIN 1 TO GND.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. R6-R9 ARE SURFACE MOUNT CHIP RESISTORS.
1. ALL RESISTOR VALUES ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 4. Schematic Diagram.

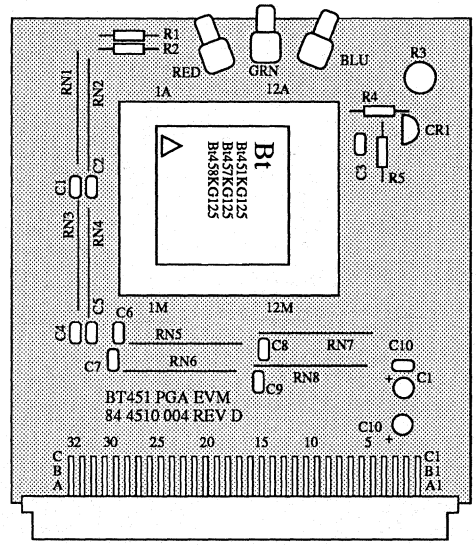


Figure 5. Assembly Diagram.

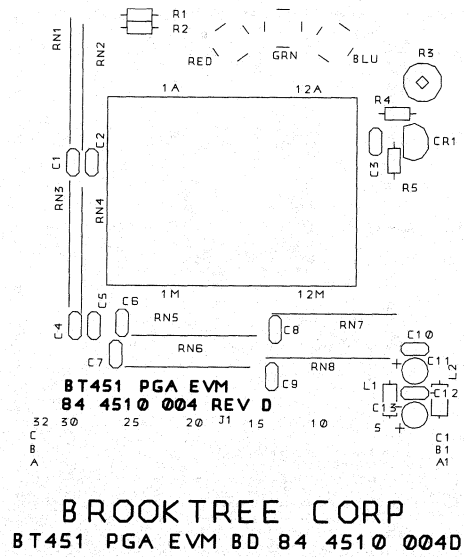


Figure 6. Silkscreen Plane.

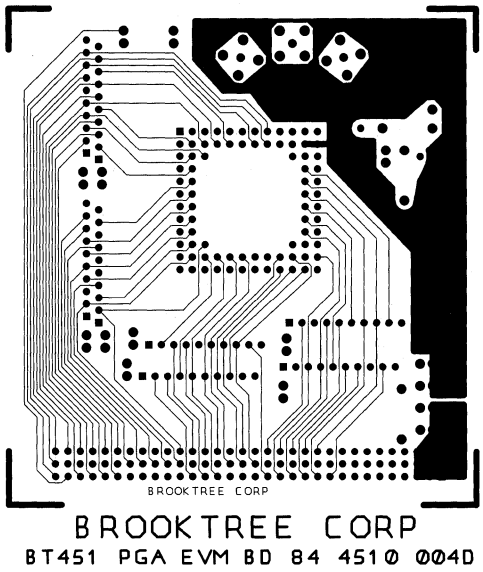


Figure 7. Signal Interconnect Plane.

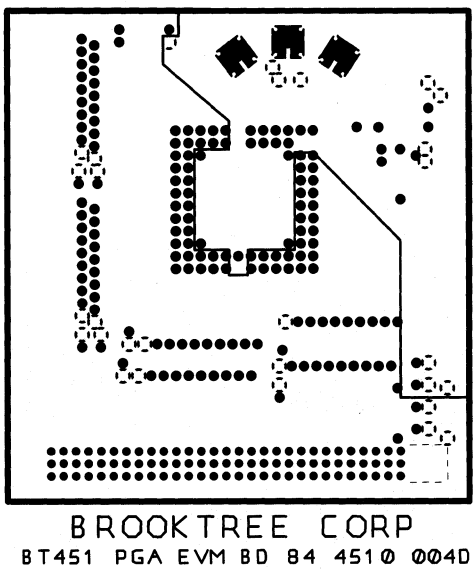


Figure 8. Ground Plane.

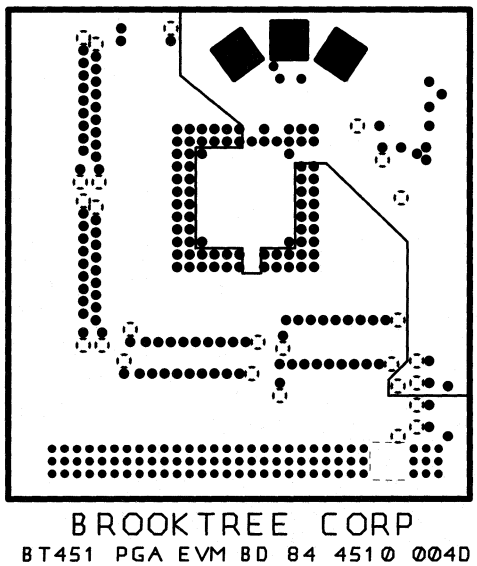


Figure 9. Power Plane.

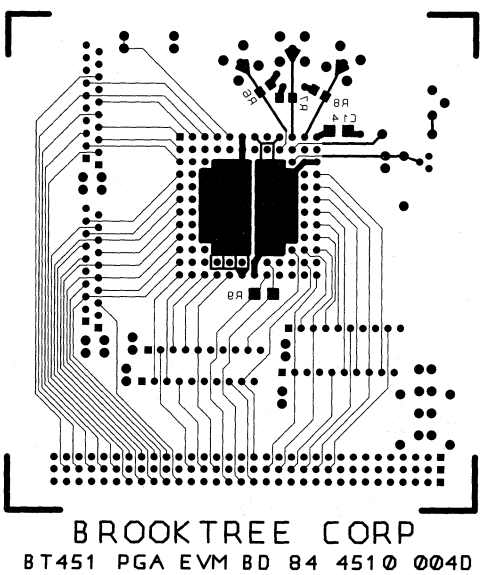


Figure 10. Signal Interconnect Plane.

Bt604/605/606 Evaluation Module Operation and Measurements

Introduction

Placing edges accurately in time has been the domain of analog specialists. With the advent of mixed-signal high-performance devices, this function has evolved from analog biasing of transistors for variable control over timing functions, to digital control with precise steps and programmed response.

Accurate edge placement using digital control depends on the accuracy of the components, the layout of the board, and interconnections between components. Driving these changes are Brooktree's line of timing verniers, or programmable delay lines. The following discussion centers around the operation of the Bt604 and how to use the evaluation board to make meaningful measurements.

Description

The Bt604EVM is an evaluation circuit board for the dynamically programmed timing edge vernier. The board contains circuitry to exercise the delay span range under internal or external control.

The PCB is designed as a low noise 50 ohm environment. The signals are 10KH logic compatible and are terminated into a -2V load. All input trigger and output signals are differential ECL to minimize crossover error. The basic circuitry consists of the Bt604, two MC10H136 4-bit binary counters, and the circuitry associated with current sink transistors Q1 and Q2.

Operation

The EVM requires a single -5.2 volt power supply and ground which should be input to connector J1 at the VEE and GND points respectively. The -2 volts shown on connector J1 is the output of voltage regulator VR3.

SW1 and SW2 (Figure 5) set the counters to count up, count down, load, or hold. If external control of the counters is desired, then the counter data and the counter control pins SW1 and SW2 may be input through connector J1.

Trig, Trig* and Tout, Tout* are accessed through 50 ohm SMA connectors. Under normal operation it is recommended that a true differential signal be applied to the Trig and Trig* inputs. The Trig and Trig* input lines are terminated with a 50 ohm resistor to -2 volts on the board. There is a position for ground termination which requires removing and resoldering R5 and R6.

The clock for the 10H136 counters can either be input through connector J1 or through the supplied SMA connector. This input line is not terminated, but may be terminated with a 50 ohm resistor to -2 volts on the EVM board, or on a separate control board connected to J1.

The circuitry associated with Q1 and Q2 enables the user to connect Tout and Tout* directly to either 50 ohms to ground (oscilloscope termination), or 50 ohms to -2 volts (ECL termination). For oscilloscope termination, switch SW4 should be in the ON position, thus turning on current sinks Q1 and Q2. For ECL termination, SW4 should be in the OFF position. The control of SW4 is also available at connector J1, if external control is desired.

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Additional controls for the Bt604 include the adjustment of Tspan using trimpot R8. Adjusting the trimpot allows the user to set Tspan from 3.9 to 40 ns. Figure 1 shows the span adjustment in relation to the minimum output (propagation) delay and the fixed width output pulse. Input CE* is controlled through switch SW3 and/or connector J1.

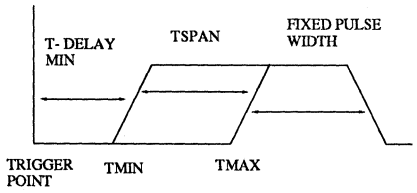


Figure 1. Pulse Timing

Performance Measurements

This section will illustrate measurement examples of linearity, the primary parameter indicating the performance of the part. The Bt604EVM board may also be used to measure propagation delay, pulse width, setup and hold times, and all DC current and voltage measurements.

Static vs. Dynamic Operation

In order to understand the important performance criteria of the Bt604, it is best to separate the specifications into two categories: Static Operation and Dynamic Operation. In static operation, the vernier input data changes less frequently than the input trigger rate. In dynamic operation, the vernier data changes at the same rate as the input trigger (timing on-the-fly).

Static Operation

Linearity

The vernier should be specified in terms of how linear the delay is as a function of input data code. Integral Linearity Error (ILE) and Differential Linearity Error (DLE) will have the same definition as in data converters, but applied to the time domain. ILE is defined as the worst case deviation over all data codes of programmed delay, as compared to the ideal end-point to end-point straight line of delay. DLE is the worst case deviation of LSB increments of delay compared to the ideal LSB increment of delay. Both are specified in terms of LSBs of error.

Linearity for the timing vernier can be a multi-dimensional problem, where linearity vs. Tspan and Trigger rate are important. Adding another dimension to the error specification is the sensitivity of delay changes to changes in trigger rate, given a specific Tspan setting. Ideally, the timing vernier delay should be independent of input trigger rate at any code, but this is never the case. In reality the delay will vary slightly as the input trigger frequency is swept. The characteristic can be described by specifying the range of trigger rate, under a specific Tspan where the output delay changes less than some number of LSBs of delay. To make testability economically feasible, the Bt604 linearity is tested under a specific Tspan and Trigger rate. However, it is characterized under many combinations of Tspan and Trigger rate.

Figure 2a is a plot of the linearity of the Bt604 at frequencies of 20 to 100 MHz. The delay span of the device under test is 5.0 ns. Each linearity curve is normalized to its own endpoints for each particular frequency. Each curve is a plot of delay integral linearity for all codes, code 0 on the left, 255 on the right. The values present on the plot for each frequency are worst case deviations from the endpoint determined straight line, in picoseconds.

Examining this type of plot yields information about how frequency affects the linearity of the ramp, ramp reset times and DAC settling times. Because the fixture hardware is stable with frequency, one can also determine what effects are present for absolute time over frequency. Figure 2a has each linearity curve normalized to its own endpoints so variations in Tspan and absolute time are not evident.

Figure 2b plots the same linearity curves as Figure 2a, with all curves referenced to the endpoints of the 20 MHz measurements. The values that appear at the ends of the linearity curves are the variations from the 20 MHz endpoints, expressed in picoseconds. The points furthest from the horizontal line are the worst case deviation from ideal linearity, based on normalization to the 20 MHz plot. Linearity, time offsets, and span variations over frequency for all codes can be seen, making this a valuable tool for testing and characterizing programmable delay elements.

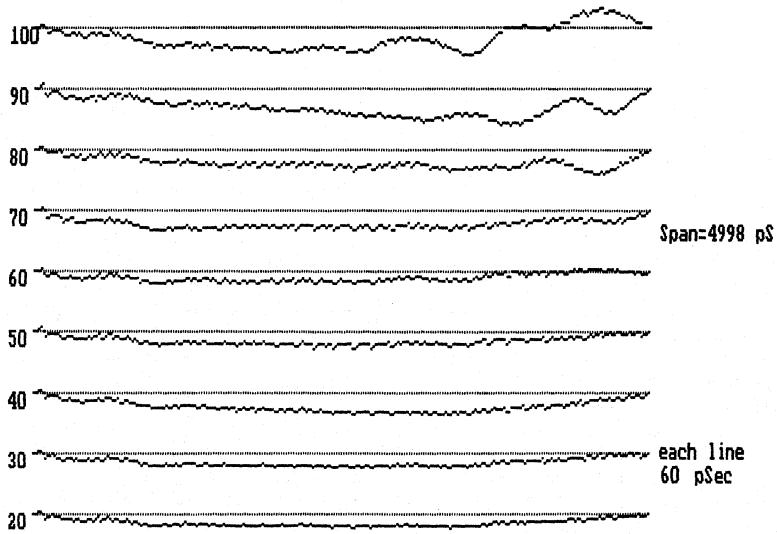


Figure 2a. Endpoint Linearities.

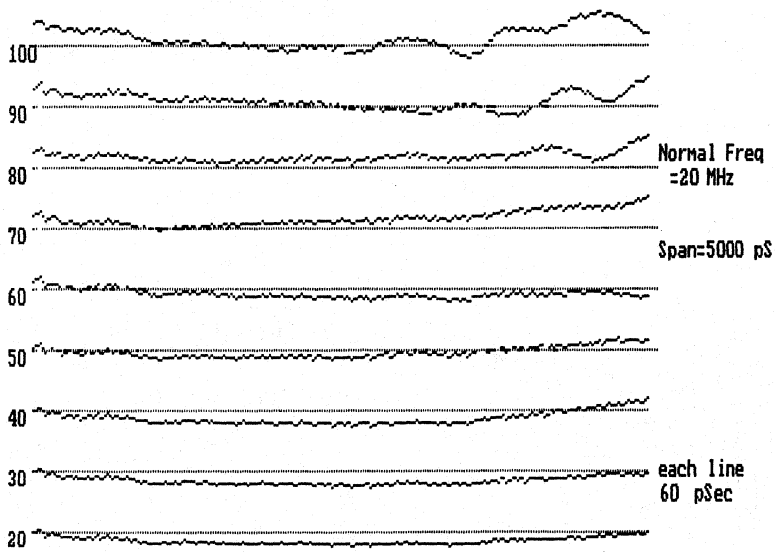


Figure 2b. All Data Normalized to 20 MHz Endpoints.

Static Linearity Over Frequency

Dynamic Characterization

Once the linearity of the device has been determined, one can test for dynamic performance. The test involves two steps. First the device is set to a specific Tspan and forced to count down the four MSB bits. The counter is clocked at the trigger rate to ensure on-the-fly timing. The output of the device is connected to a high speed digital oscilloscope such as the HP54120T, required to observe picosecond resolutions. With the persistence on the scope turned up to infinity, one can view the 16 individual output pulses as the counter is clocked through its states (on-the-fly). Next, by incrementing the counter slowly, one can observe the same 16 output pulses, which are overlaid on the pulses generated under the previous on-the-fly condition. Figure 3a is a printout of a Bt604 clocked at 100 MHz with the four MSBs decrementing on-the-fly. Figure 3b is a printout of the same device, this time incrementing all codes at 100 MHz. The prior linearity experiment shows how linear the device is under static conditions, so any difference observed between the overlaid pulses is the error attributed to the dynamic performance of the device. This simple, yet effective, experiment yields extremely valuable data.

Measuring Dynamic Performance

Best dynamic performance (data changing each clock cycle) is obtained with an input trigger pulse width of 2 ns to 3 ns and a data setup time of 5 ns to 6 ns. When SW1 and/or SW2 are set to count down (DEC), maximum trigger rate with 5 ns Tspan is 100 MHz (10 ns clock period). With 4 ns Tspan the maximum trigger rate is 111.11 MHz (9 ns clock period).

When SW1 and/or SW2 are set to count up (INC), to avoid violating the specification for output pulse spacing (when the counters wrap around maximum delay to minimum delay) the maximum trigger rate with 5 ns Tspan is 71.42 MHz (14 ns clock period) and with 4 ns Tspan the maximum trigger rate is 76.92 MHz (13 ns clock period).

When the Bt604 data input pins are driven from an external source (via connector J1) with the counters in pre-set (LOAD) mode, ensure that changing delay from a higher to lower value does not violate the output pulse spacing specification.

Figure 4 illustrates a suitable evaluation test setup. The 8 ns delay on Trig and Trig*, in conjunction with the typical 3 ns propagation delay through the counters, results in a setup time of 5 ns. Setup time may be adjusted by choosing appropriate cable lengths for clock, Trig and Trig*.

A small cooling fan is recommended.

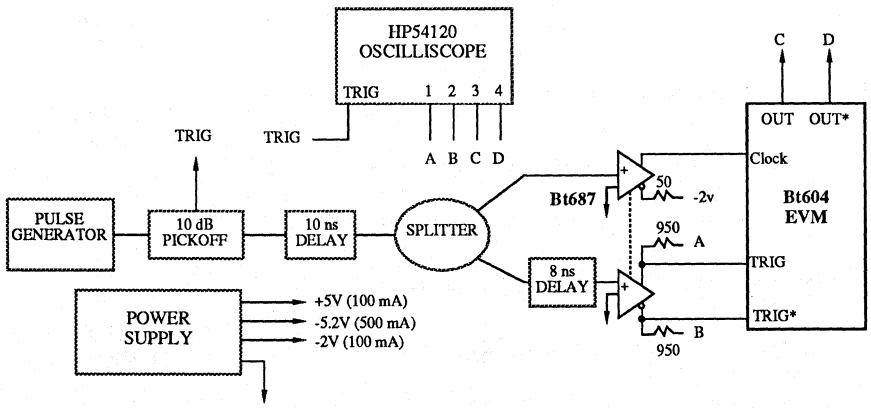
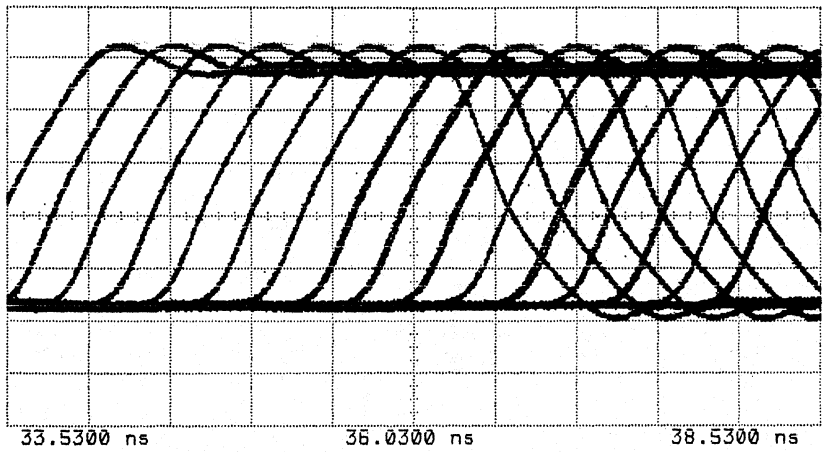


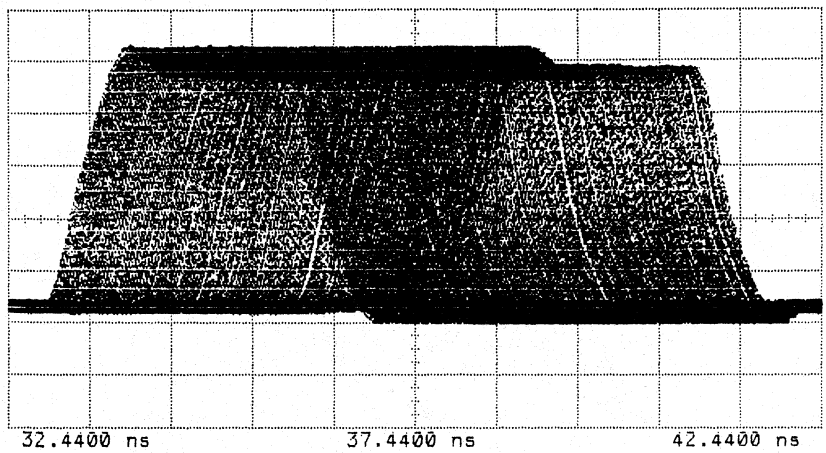
Figure 4. Dynamic Measurement Setup



Ch. 2 = 200.0 mVolts/div Offset = -1.500 Volts
Timebase = 500 ps/div Delay = 36.0300 ns

100MHz DECREMENTING 4MSBs OVERLAYED WITH STATIC MSBs

Figure 3a.



Ch. 2 = 200.0 mVolts/div Offset = -1.500 Volts
Timebase = 1.00 ns/div Delay = 37.4400 ns

Figure 3b.

Dynamic Linearity

PCB Construction

The Bt604EVM board is an epoxy fiberglass board with five 1 oz. copper planes for power, ground, termination and signal interconnects. The Bt604EVM design is outlined with a schematic diagram giving the component values and the DIN I/O connections, the assembly diagram of component placement, and the PCB artwork film. The PCB artwork is provided for evaluation purposes only. These layouts should not be considered ideal, and have not been tested for FCC compliance. The following descriptions of the figures highlight critical component placement and considerations.

Schematic Diagram (Figure 5)

The component schematic diagram shows terminations for D0 - D7 signals from the 40-pin DIN connector. All interconnecting signal lines on the board are 50 ohm terminated into -2V.

Assembly (Figure 6 & 7)

Figure 6 shows the Bt604EVM as it is shipped to the customer. The silkscreen layer is shown in Figure 7. This provides a more detailed view of the board.

Signal Interconnect Plane (Figure 8 & 12)

The digital traces are 50 ohm transmission lines for all signal interconnects. DC signal traces may not be 50 ohms.

Power and Ground Planes (Figure 9, 10 & 11)

The board uses solid power and ground planes. The -2V plane is split with a subplane for -5.2V. The -5.2V plane is the larger plane in Figure 10.

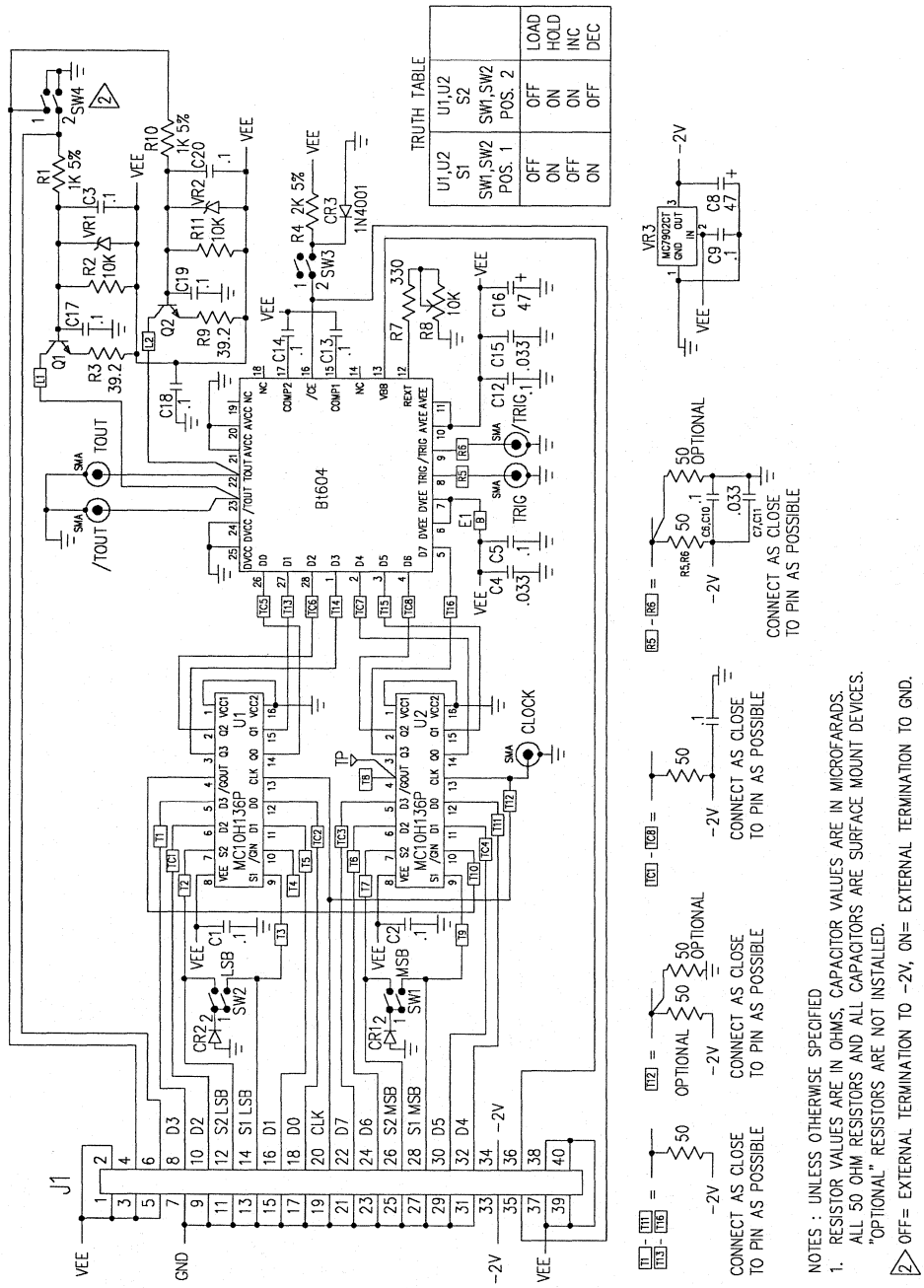


Figure 5. Schematic Diagram.

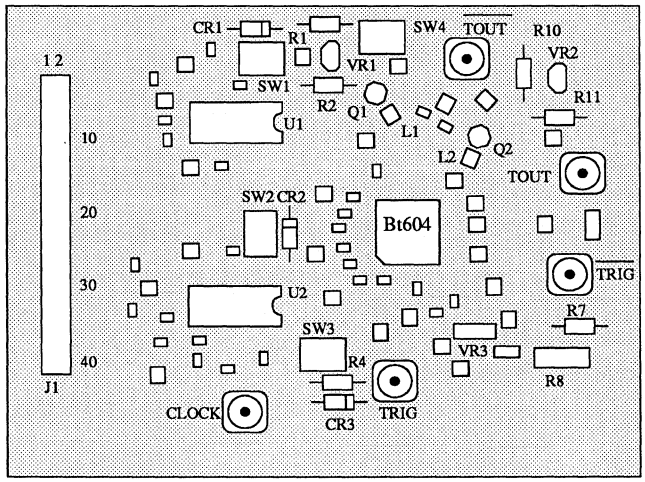


Figure 6. Assembly Diagram.

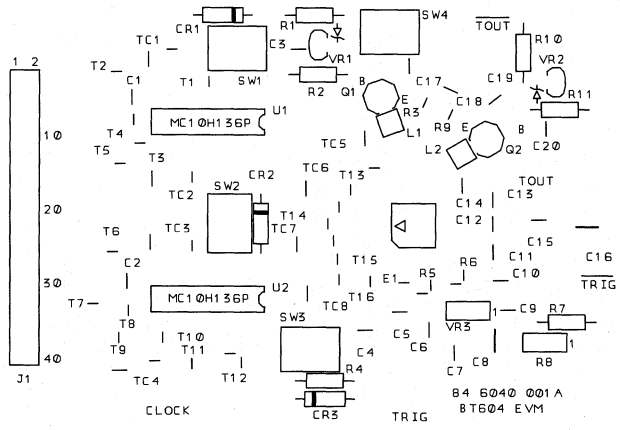


Figure 7. Silkscreen.

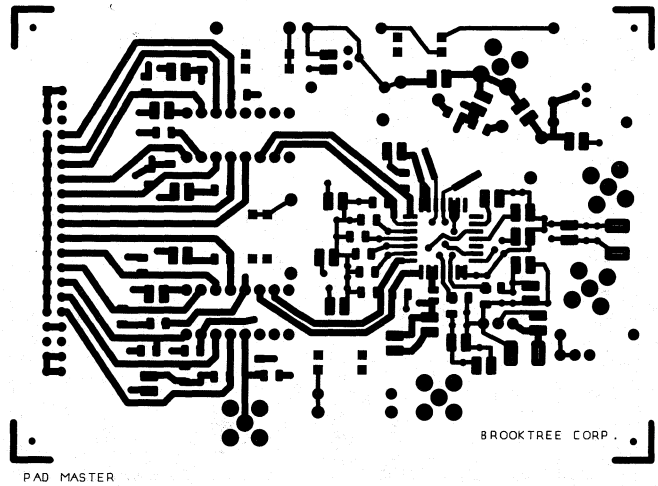


Figure 8. Signal Interconnect.

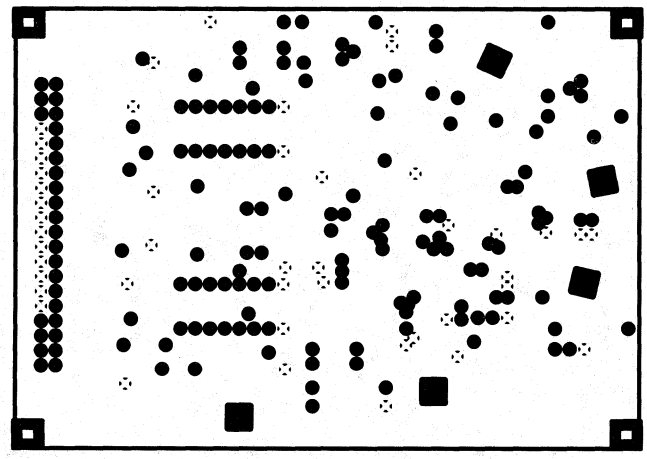


Figure 9. Ground Plane.

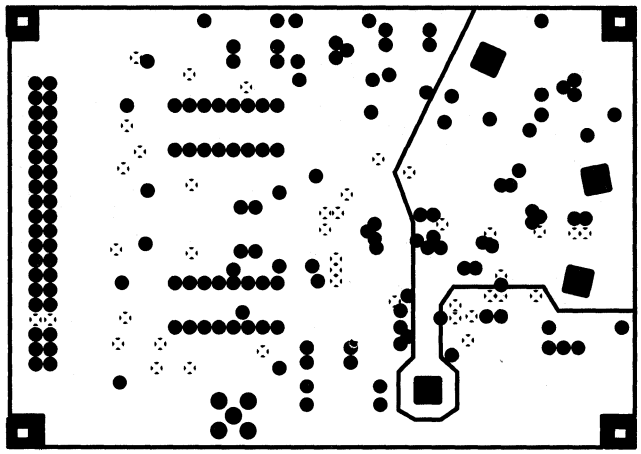


Figure 10. Termination Plane (-2 Volts).

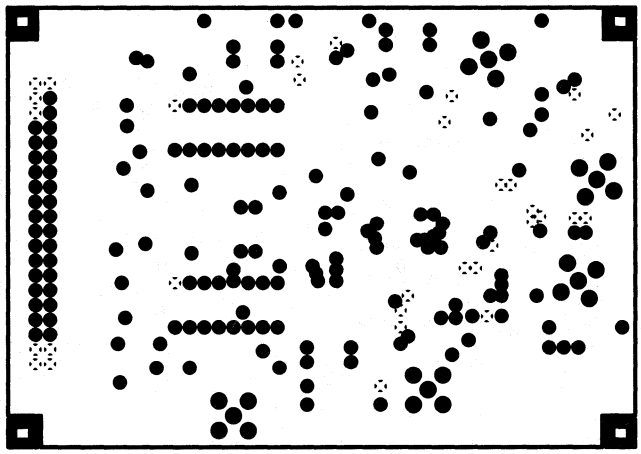


Figure 11. Power Plane (VEE = -5.2 Volts).

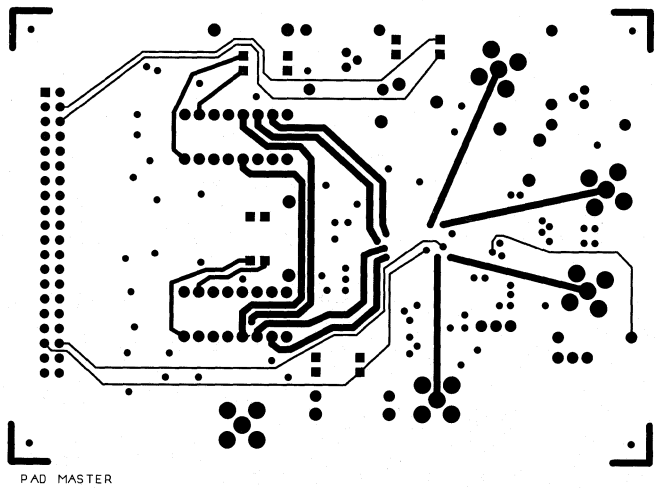


Figure 12. Signal Interconnect.

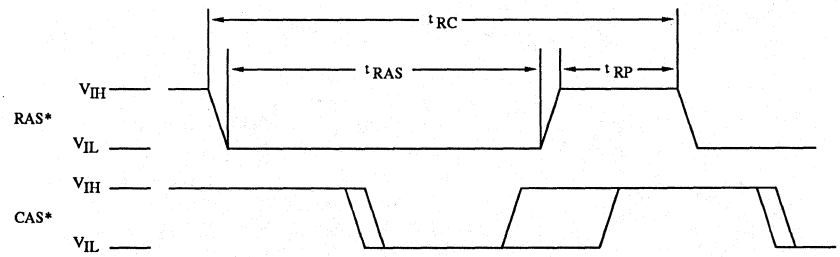
Pixel Interleaving Benefits of the Bt459

As the speed of microprocessors increases, a greater percentage of operating time is spent waiting for memory based transactions. This is becoming increasingly obvious in video applications.

As more designers incorporate dedicated, high speed processors and busses for frame buffer control and manipulation, the demand for faster memories increases. Current memory technology has brought the access time of VRAM down to 100 ns. While this is fast compared to memories of only a few years ago, it presents a problem to the memory or frame buffer designer. This problem is due entirely to the difference between Access time and Cycle time. Access time is the time required from the falling edge of RAS* to valid data, and is typically 100 ns. Cycle time is the time required from the falling edge of RAS* to the next falling edge of RAS*, and is much greater. In a typical 256K X 4 VRAM, the cycle time for a 100 ns part is 190 ns (Figure 1).

The added 90 ns are due to precharge. When back-to-back accesses are made to the same memory chip, the designer must allow 80 ns of precharge from the rising edge of RAS* to the next falling edge of RAS*, which would start the next memory cycle. If many repeated accesses are made to the same device, a large time penalty in the form of precharge would have to be paid. In frame buffer applications where many vector operations are to be performed, this situation can impact system performance.

In many frame buffer applications, pixels are stored sequentially in memory. That is, pixel 0 of line 0 is stored in address 0, pixel 1 of line 0 is stored in address 1, and so on. If the frame buffer uses four banks of VRAM to multiplex the pixels, as would be the case in a 1024 X 1024 frame buffer using the Bt459, every fourth pixel would be stored in the same bank of VRAM. This arrangement causes the pixels to line up vertically in memory (Figure 2). In this



t_{RC} - Read or Write cycle time = 190 nS
t_{RAS} - RAS pulse width = 100 ns
t_{RP} - RAS precharge time = 80 nS

Figure 1. VRAM Cycle Timing.

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Figure 2. 4:1 Multiplexed Frame Buffer.

configuration, pixel 0 of line 0 is stored in the same chip as pixel 0 of line 1, pixel 0 of line 2, pixel 0 of line 3 and so on. As this memory arrangement uses four banks of pixels, this situation repeats itself every four pixels.

This type of memory arrangement can cause problems in vector operations. In a vector operation, the processor operates on the memory from point a to point b. For example, to draw a line from one point to another, memory is accessed on a pixel-by-pixel basis. When one pixel is accessed, the next pixel accessed will most likely be one of eight adjacent pixels (Figure 3). This means that as frame buffers are usually configured, a precharge penalty will be incurred in 25% of the cases, as the next pixel addressed will be in the same chip in two out of eight cases. In the worst case, a vertical line drawn from one point to another, precharge would be incurred between every cycle. The designer then faces a problem: increasing the speed of the frame buffer when current memory technology forces a large time penalty in vector based operations.

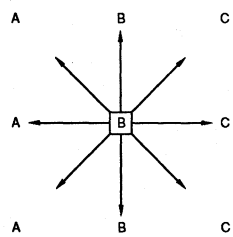

Figure 3. Pixel Alignment.

The solution lies in memory architecture. By reorganizing the memory, the need for precharge can be greatly reduced. By taking advantage of pixel interleaving, the designer can arrange memory so that no two adjacent pixels are stored in the same memory chip. One method of interleaving pixels is shown in Figure 4.

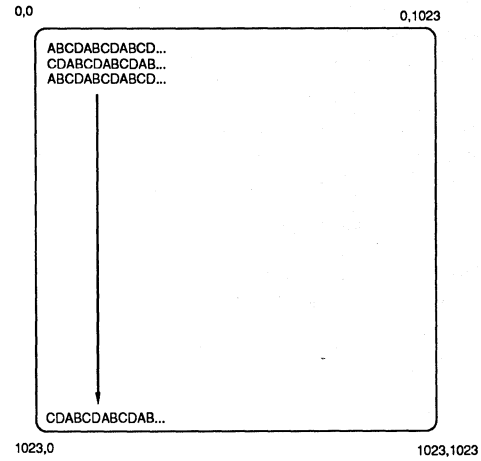

Figure 4. Pixel Interleaved Frame Buffer.

If the method of interleaving shown in Figure 4 is implemented, a vector operation would never encounter a situation where a precharge penalty would be incurred for accessing an adjacent pixel. In the worst case scenario (a vertical line), considerable time is saved. A vertical line of 10 pixels would, under normal frame buffer architecture, have 720 ns of precharge penalty when using a 100 ns VRAM. When pixel interleaving is implemented, the same vertical line would not require any precharge. This would mean a time savings of over 40%, and a corresponding system performance improvement.

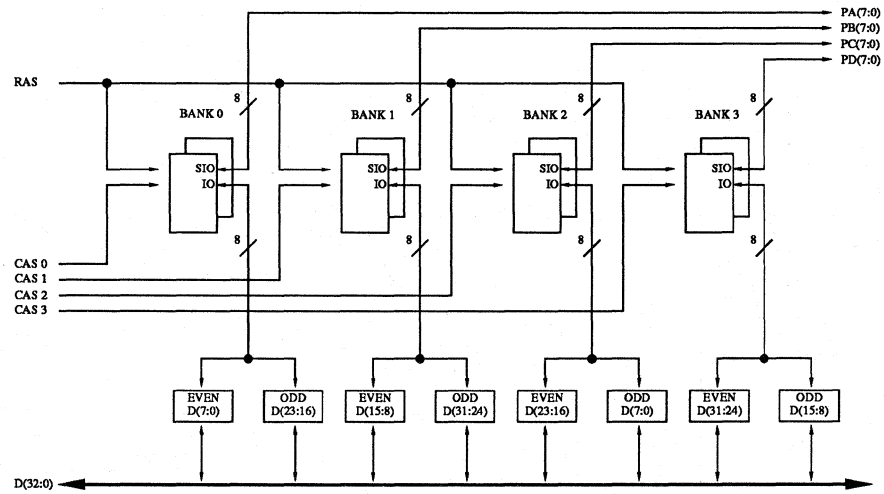

Figure 5. 1024 X 1024 X 8 Frame Buffer Block Diagram.

Interleaving the frame buffer presents some issues, however. Frame memory is no longer sequential. Pixels are stored out of sequence. Raster based operations now need to track the image to sort out the interleaved pixels, unless some method can be devised to make the interleaving transparent.

Since the pattern of the interleaving is regular, and in this method repeats every two lines, it is very easy to sort in hardware. The frame buffer can be made to appear sequential to software. Pixel interleaving can be added to current systems with no software impact.

The drawback to this is the requirement for extra hardware. For a frame buffer in a 32 bit host system, eight data transceivers would be required to interface the frame buffer to the host system. An additional transceiver would be needed for each bank of VRAM. While the number of transceivers has been doubled, this cost in hardware is offset by the increased system speed.

As is shown in Figure 5, to implement a 1024 X 1024 X 8 bit frame buffer using this interleave scheme, eight 256K X 4 VRAMs are required. The frame buffer pixels are stored in four banks, labeled 0 through 3. This means that while the frame display is organized as 1024 pixels by 1024 lines, the actual organization of the memory is 2048 pixels by 512 lines. This means that new data is shifted into the VRAM shift registers every *two* lines.

The two LSBs of the address, AD0 and AD1, are not driven on the host bus. Rather, BHE (Byte High Enable) lines, are decoded from AD0 and AD1 and driven to signify which bytes are active on the bus. There are four BHE lines, BHE0 through BHE3. BHE0 controls data lines D0 through D7, BHE1 controls D8 through D15, and so on.

The address to the memory is composed of a pixel address, and a line address. The frame buffer address of 1024 pixels by 1024 lines is converted to 2048 pixels by 512 lines for use as RAS and CAS addresses to the VRAM.

To make the interleaving transparent to the software, the data must be routed to the appropriate VRAM. AD10 determines the frame buffer line. AD10 is low for even, or non interleaved lines, and high for odd lines, which have pixel interleaving. AD10, in conjunction with the BHE lines, can be decoded to enable the appropriate transceivers, and can be used to drive the appropriate CAS lines to the VRAM.

The Bt459 has the ability to decode interleaved pixels in the frame buffer for added system performance. The pixel data may be latched into the Bt459 according to any one of four available interleaving formats, and be displayed in the proper order. The Bt459 may also be programmed to accept various forms of pixel interleaving, as well as different pixel multiplexing formats.

To specify the method of interleaving, the interleave register of the Bt459 must be programmed. The interleave register fields CR30 - CR37 specify the format of the interleave, the first pixel to be displayed on a line that is panned, overlay interleave enable, and underlay interleave enable. See Table 2 for the Bt459 interleave register specifications.

In addition to pixel interleaving, the Bt459 supports block mode operation in 4:1 and 5:1 pixel multiplexing. Block mode operation allows the Bt459 to latch pixels of various bit depths. In block mode, the Bt459 will latch pixels of 8 bits per pixel, 4 bits per pixel, 2 bits per pixel, and 1 bit per pixel. Table 1 shows the order in which pixels are displayed when in block mode. The combination of pixel interleaving and block mode operation make the Bt459 ideally suited for high resolution CAD/CAM applications, as well as scientific workstation applications.

1 Bit per Pixel (RA1 - RA7 = 0) RA0 =	2 Bits per Pixel (RA2 - RA7 = 0) RA1, RA0 =	4 Bits per Pixel (RA4 - RA7 = 0) RA3 - RA0 =	8 Bits per Pixel RA7 - RA0 =
P7A	P7A, P6A	P7A, P6A, P5A, P4A	P7A, P6A, P5A, P4A, P3A, P2A, P1A, P0A
P6A	P5A, P4A	P3A, P2A, P1A, P0A	P7B, P6B, P5B, P4B, P3B, P2B, P1B, P0B (4:1)
:	P3A, P2A	P7B, P6B, P5B, P4B (4:1)	P7C, P6C, P5C, P4C, P3C, P2C, P1C, P0C (4:1)
P0A	P1A, P0A	P3B, P2B, P1B, P0B (4:1)	P7D, P6D, P5D, P4D, P3D, P2D, P1D, P0D (4:1)
P7B (4:1)	P7B, P6B (4:1)	P7C, P6C, P5C, P4C (4:1)	P7E, P6E, P5E, P4E, P3E, P2E, P1E, P0E (5:1)
P6B (4:1)	P5B, P4B (4:1)	P3C, P2C, P1C, P0C (4:1)	
:	P3B, P2B (4:1)	P7D, P6D, P5D, P4D (4:1)	
P0B (4:1)	P1B, P0B (4:1)	P3D, P2D, P1D, P0D (4:1)	
P7C (4:1)	P7C, P6C (4:1)	P7E, P6E, P5E, P4E (5:1)	
P6C (4:1)	P5C, P4C (4:1)	P3E, P2E, P1E, P0E (5:1)	
:	P3C, P2C (4:1)		
P0C (4:1)	P1C, P0C (4:1)		
P7D (4:1)	P7D, P6D (4:1)		
P6D (4:1)	P5D, P4D (4:1)		
:	P3D, P2D (4:1)		
P0D (4:1)	P1D, P0D (4:1)		
P7E (5:1)	P7E, P6E (5:1)		
P6E (5:1)	P5E, P4E (5:1)		
:	P3E, P2E (5:1)		
P0E (5:1)	P1E, P0E (5:1)		

Note: Each line represents one pixel clock cycle. A column represents one LD* cycle loading new P0 - P7 data. All entries with "4:1" descriptor are also valid for 5:1 mode.

Table 1. Block Mode Operation (RA = Color Palette RAM Address).

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to data bus bit D0. The interleave register is for support of frame buffer systems configured for interleave operation.

CR37 - CR35	Interleave select (000) 0 pixels (001) 1 pixel (010) 2 pixels (011) 3 pixels (100) 4 pixels (101) reserved (110) reserved (111) reserved	These bits specify the order in which the pixels are to be output, as shown in Table 3. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line. The phrase "repeats every x" in Table 3 means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1 pixel interleave select, ABCD would be repeated every 4th scan line. In the 1:1 input multiplex mode, a value of 0 pixels (000) must be specified.
CR34 - CR32	First pixel select (000) pixel {A} (001) pixel {B} (010) pixel {C} (011) pixel {D} (100) pixel {E} (101) reserved (110) reserved (111) reserved	These bits are used to support panning in the Y direction with an interleaved frame buffer. Due to the interleave capability, it is necessary to specify the value of the first pixel on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode. These bits are ignored in the 1:1 multiplex mode.
CR31	Overlay interleave enable (0) interleaving disabled (1) interleave enabled	This bit specifies whether or not OL0 - OL3 and OLE are to be interleaved or not. If interleaving is enabled, the interleave factor and first pixel selection are the same as for P0 - P7. If interleaving is disabled, pixel {A} is always output first and no interleaving occurs.
CR30	Underlay enable (0) underlay disabled (1) underlay enabled	If command bit CR22 is a logical zero, this bit is used to enable or disable the underlay from being displayed. If CR22 is a logical one, this bit is ignored. If the underlay is enabled (and CR22 is a logical zero), the OLE inputs function as follows: If OLE = 0, P0 - P7 data is displayed. If OLE = 1, the underlay is displayed if P0 - P7 = 0, if P0 - P7 ≠ 0 then normal pixel data is displayed. The underlay uses overlay color 0 to provide underlay color information.

Table 2. Interleave Register Field Definitions.

	5:1 multiplexing		4:1 multiplexing	
interleave select	output sequence	scan line number	output sequence	scan line number
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Table 3. Interleave Operation (First Pixel Select = Pixel A).

Bt281 Real-Time Color Space Converter and Corrector

Introduction

A color space is a mathematical representation of a set of colors from which a specific color may be selected. Different applications may require different color spaces. The choice of color space depends on the source of the image, the operations to be performed on the image once it is acquired, and the type of output device the image will be displayed on.

The RGB Color Space

The red, green, and blue (RGB) color space is widely used throughout graphics and imaging. Red, green and blue are the three primary additive colors and are represented by a three dimensional, Cartesian coordinate system (see Figure 1). With additive color primaries, equal values of all three components must be added to a black surface to create white.

The RGB color space is the most prevalent choice for frame buffers because a color CRT uses red, green and blue guns to create the desired color. The red, green and blue planes of the frame buffer can each drive their own DAC, which in turn directly drives the RGB inputs of the color monitor. Therefore, the choice of the RGB color space for a frame buffer simplifies the architecture and the design and building of the buffer interface to the display DAC.

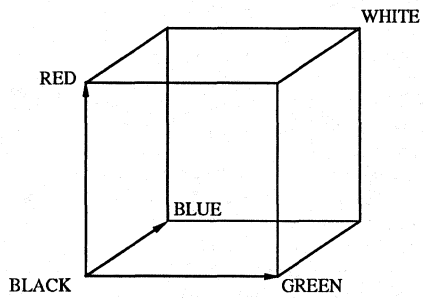

Figure 1. The RGB Color Space

Another reason for the popularity of RGB is due to the considerable amount of research and experimentation that has been performed to characterize the human visual system using this color space. If RGB is chosen as the color space, this research can be utilized when designing other aspects of the imaging system.

The NTSC Color Space

The National Television Standards Committee (NTSC) developed a technique to broadcast color images in the same bandwidth occupied by a black and white image, without obsoleting the black and white television receiver. The result was a color space that defined intensity and color separately.

The intensity, or luminance (Y) component, was defined as the black and white portion of the image. The intensity component of the color space allows color transmissions to be displayed on a black and white receiver with minimal loss of detail, thereby meeting one of the goals of the NTSC.

The color portion of the image is divided into two components, I and Q, which could then be used to Quadrature Amplitude Modulate (QAM) an RF carrier. Essentially, I and Q are two orthogonal vectors which specify a point of color, as shown in Figure 2. Values of I and Q represent a vector which can also be represented by the magnitude (vector magnitude R in Figure 2) and theta (vector angle ø in Figure 2). The magnitude is also referred to as the saturation of a color, and the angle is the hue or tint of a color. With

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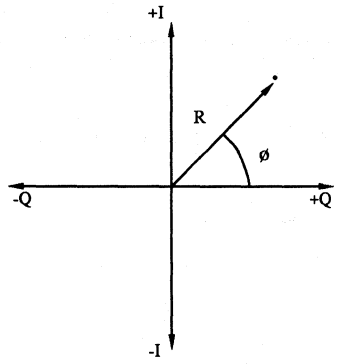

Figure 2. The NTSC, I and Q Color Space

the color carrier frequency at 3.579545 MHz, this combined signal could then fit within the existing broadcast television bandwidth.

The equations to convert between RGB and NTSC are:

Y = 0.30(RED) + 0.59(GREEN) + 0.11(BLUE)

I = 0.60(RED) - 0.28(GREEN) - 0.32(BLUE)

Q = - 0.21(RED) - 0.52(GREEN) + 0.31(BLUE)

and to convert from YIQ to RGB are:

RED = Y + 0.96(I) + 0.62(Q)

GREEN = Y - 0.272(I) - 0.647(Q)

BLUE = Y - 1.108(I) + 1.705(Q)

One should notice from the equations for I and Q that I and Q can be represented by negative numbers. This is of no consequence when mathematically converting from one space to the other, but may pose a problem for the designer. The system software that must be provided and the video backend of the imaging system must allow negative numbers to exist.

One result of the NTSC specifications is that the two chrominance components be bandwidth limited to 1.5 MHz for R-Y and 500 KHz for B-Y. This can be accomplished with no perceived loss of image detail because the eye is less sensitive to color than it is to black and white. Since the bandwidth of the chrominance components is reduced, the sampling rate of I and Q can also be reduced thereby resulting in a reduction of the amount of storage required over the full bandwidth RGB components. For real world images, an NTSC buffer can be less expensive and require less board area than a comparable RGB buffer.

Selecting the Color Space

The RGB color space is not the most efficient when dealing with real world images. All three components need to be of equal bandwidth to represent all of the colors contained in the space defined by the cube (see Figure 1) since any point within the cube has the same probability of occurring as the next. The result of this is an image buffer that has the same resolution and pixel depth for each color. Selecting RGB as the color space may also be a drawback if the image will be operated on after acquisition. It is more efficient to filter an image in the YIQ space once, than to apply the same filter three separate times, one for each color in the RGB space. To determine the "color" of a certain pixel, it would be necessary to read all three components out of the buffer and process them to obtain the desired answer.

The NTSC color space is more efficient than RGB at representing real world images for two primary reasons. First, luminance and chrominance of an image exist separately. This facilitates quick and efficient image processing algorithms. Second, due to the fact that the chrominance bandwidth is reduced, the size of the image buffer can be reduced in resolution and pixel depth.

A system that is designed using RGB can take advantage of a large number of existing software routines since the RGB color space is the prevalent choice for frame buffers. The backend of the image buffer (DACs and other circuitry) may be easier to implement than NTSC, especially when driving an RGB monitor.

An NTSC image buffer may be the choice if the application requires manipulation of the image. Since the luminance component of the image explicitly exists, operations such as filtering are more efficient since the luminance value does not need to be calculated by the CPU.

Most of the inexpensive image sources that exist today are NTSC, which implies that the front end of an NTSC buffer would be simpler to design than a front end to an RGB buffer for an NTSC source. Supporting both color spaces gives the best of both worlds, since the image can be represented to optimize CPU processing.

The solution to the correct selection of a color space is provided with the Bt281 Color Space Converter and Corrector. The Bt281 allows an imaging system to optimize a particular color space for a particular application. The input to the Bt281 is a set of three color primaries from any color space, such as RGB, NTSC, YUV, YCrCb and others, with the result being a set of three color primaries in the desired color space.

Conversion and Correction

The Bt281 can be used to implement a completely flexible color space imaging system. As shown in Figure 3, the input to the system can be any color space provided by the imaging source. The video data is digitized by the Bt253 Triple Digitizer and is then converted by the first Bt281 to the required color space required for CPU processing. For display, the image in the frame buffer is routed through the second Bt281 and is converted to RGB so that it can be displayed easily with a Bt473 True-Color RAMDAC.

The Bt281 Color Space Converter and Corrector can accept inputs at a clock rate of 36 MHz, making the part ideal for real-time applications. Three 256 x 8 look-up tables are provided in the input path before matrix conversion. This allows the input data to be modified prior to color conversion. Performing the look-up transformation before the color space conversion is a requirement for gamma correction of the source image data.

To support image buffers that utilize the reduced chrominance bandwidth, the Bt281 contains linear interpolation filters. These filters can be used on the bandwidth-limited chrominance channels to reconstruct the missing values and provide full bandwidth inputs to the conversion matrix. This is important if the chrominance inputs to the Bt281 are utilizing the bandwidth reduction allowed by the NTSC specifications, and the output of the Bt281 is required to be full bandwidth RGB.

The Bt281 coefficients for the 3 x 3 matrix multiplier are programmable over a range of -4.00 < = X < = 3.996. The designer is not hindered by being limited to only RGB to NTSC conversions. An imaging system can be programmed to use any color space that meets the input/output requirements, and a completely different color space for storage and manipulation. Since coefficients are programmable and are not fixed to any particular color standard, the Bt281 can also be used for sophisticated color correction algorithms and image enhancement in real-time.

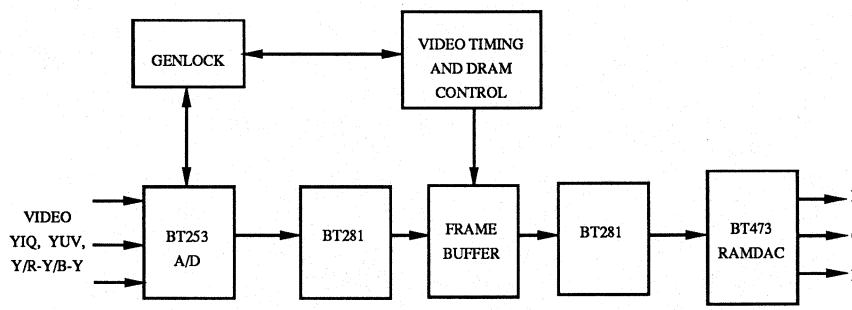

Figure 3. Typical color space convertor system

Summary

Imaging systems need to be designed so that they are flexible enough to support different color spaces. This is becoming a requirement because no one color space is optimum for satisfying the requirements of image processing, reduced image storage, graphics and interfacing with input/output devices. The Bt281 Color Space Converter and Corrector gives an image system the flexibility to use any color space, in real-time, that is optimum for the application.

GRAPHICS

AND IMAGING PRODUCTS

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NEWSFRONT

Trailblazing architecture creates 8-bit video DAC that clips along at 75 MHz

Pipelined logic, segmented current sources, and an innovative TTL-to-CMOS buffer are the building blocks in a video converter.

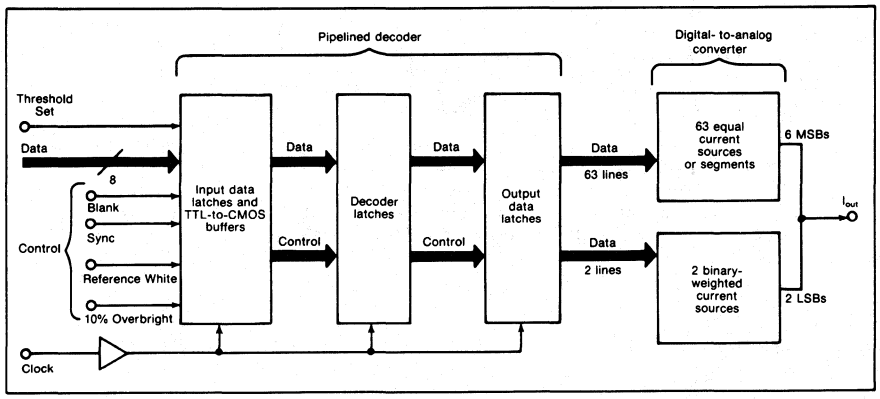
True 8-bit resolution at 75 MHz can now be had in a CMOS digital-to-analog converter. The formula for this unprecedented achievement is a pair of architectural innovations combined with two new circuit designs.

Pipelined decoding logic and almost completely segmented conversion stages are the architectural elements. They team up with two circuit designs: a single MOS-transistor current source and a buffer that shifts rapidly from TTL to CMOS levels. Together, these ingredients make possible the higher resolution called for by the next generation of color CRTs.

Moreover, the converter, developed by Brooktree Corp. (San Diego, Calif.), requires neither ratio-matched passive or active devices nor any form of trimming. Until now, digital-to-analog converters, regardless of their speed, fabrication process, or the number of chips, have used some combination of ratio-matched resistors, capacitors, or transistors, as well as some form of trimming.

The first CMOS video converter arrived only a year ago. However, its 24-MHz update rate, 7-bit accuracy (8-bit resolution), and glitch energy of 300 pV-s cannot compete with this chip's 75-MHz update or its true 8-bit resolution for use in many of the high-end engineering workstations.

With this chip, input data can be pipelined at the front end of the converter, because the few nanoseconds of delay are inconsequential to the user—the display changes seem instantaneous. The typical gate delay with



1. In Brooktree's video digital-to-analog converter, pipelining and segmentation yield 75-MHz word rates with 8-bit resolution and an accuracy of ± ¼ LSB.

the 3-μm process is 3 ns; in fact, to achieve the settling time of under 12 ns, no more than four gate delays are allowed in series in the 8-to-65-line decoder (Fig. 1).

The three sets of pipelined, synchronous decoding latches (registers) employ over 130 D-type flip-flops. Yet the process lets the chip fit into a 0.3-in.-wide DIP of 24 pins (ELECTRONIC DESIGN, June 13, p. 177).

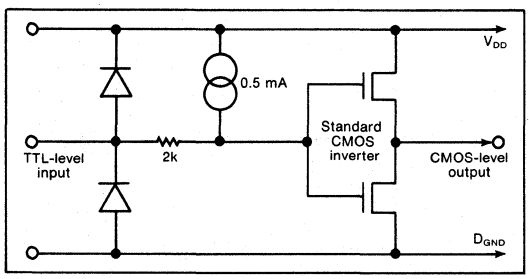
Most switch sequentially

The decoder furnishes 65 control lines for the high-speed CMOS current switches, which connect the single-transistor current sources to the analog output. As the binary code to the input increases, 63 of these lines sequentially switch in the 63 equal current sources, or segments.

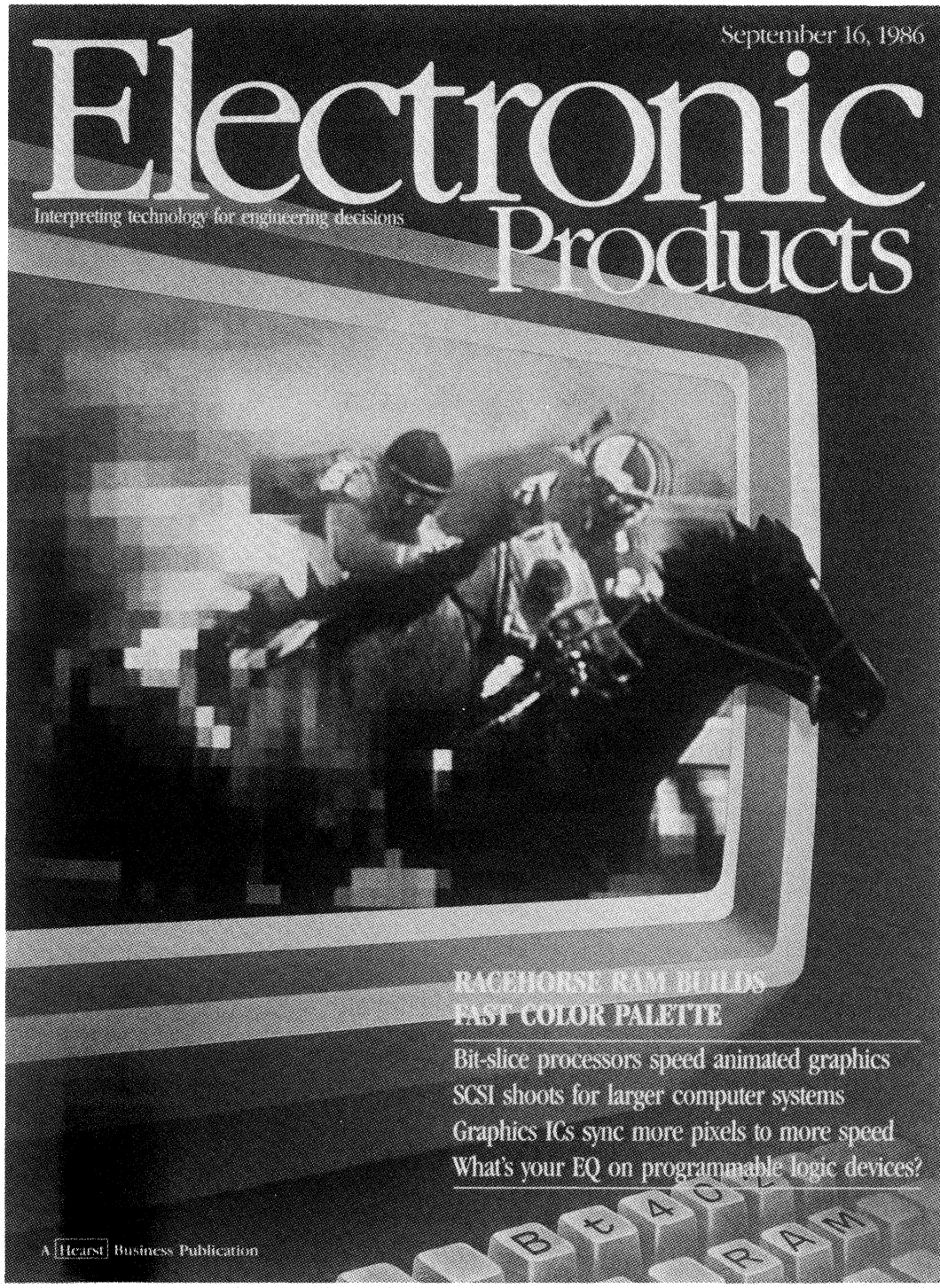
Those, in turn, combine to form the 6 MSBs. The two additional lines from the decoder switch in a pair of binary-weighted current sources (½I and ¼I) to form the 2 LSBs.

Typically, circuits converting TTL input levels into CMOS logic levels (on a CMOS chip) incorporate an input inverter buffer with a strong n-channel transistor and a weak p-channel device. Although that approach turns in fast fall times, it comes in with poor rise times and cannot handle 75-MHz signals. Therefore Brooktree developed a buffer that level-shifts 2.5 to ., using only a 2-kΩ resistor and a 0.5-mA tracking current source (Fig. 2).

The technique also compensates for the effects of temperature change. What's more, it permits transistors in the buffer circuit to be identical with the rest of the transistors on the chip. *Frank Goodenough*



2. At 75 MHz, the converter needs only a resistor and a current source to change TTL levels into CMOS levels.


September 16, 1986
Electronic Products
Interpreting technology for engineering decisions
RACEHORSE RAM BUILDS FAST COLOR PALETTE
Bit-slice processors speed animated graphics
SCSI shoots for larger computer systems
Graphics ICs sync more pixels to more speed
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A Hearst Business Publication

3

Racehorse RAM spurs sharper color graphics

Fastest-ever color-palette RAM IC uses ECL and pipelining to bring new economies to high-resolution display

Jeff Teza, Director of Product Marketing, and Wylie Plummer, Sr. Design Engineer, Brooktree Corp., San Diego, CA

Speed is the most outstanding characteristic of Brooktree's newest pipelined static RAM, the 256 x 8-bit Bt402. At 4 ns, its cycle time is the shortest in the industry. That kind of performance is crucial to the memory's intended use as a color palette in superhigh-resolution color graphics systems; for superhigh resolution these days means around 3 million pixels, which have to be scanned at a speed of 250 MHz.

In this application it also helps that the Bt402 is cascadable, includes 3 x 8 bits of RAM (dubbed Sidecar) for graphics overlays, and is fully compatible with the Bt108 and the (new) Bt109 8-bit video D/A converters. Furthermore, its advanced ECL circuitry makes it directly compatible with 100K ECL. A 10K version, the Bt401, is also available.

The video RAM does, however, have one notable limitation: it does not write as quickly as it reads. Its applications are therefore limited to those in which the read cycle time sets the speed criterion. This is true of—but not limited to—graphics systems.

Applications galore

For example, *automatic test equipment* (ATE) needs fast pattern-generation RAM to send short, fast bursts of data to the device under test. Another case in point is microcode storage in CPUs. In "soft systems," microcode is typically loaded when the system is booted and then accessed at fairly high rates. In most CPU (and especially mainframe) architectures, the microcode can be pipelined out from static RAM storage. Still other examples are telecommunications and general digital signal-processing jobs like high-speed waveform synthesis, in which data is written slowly but read in high-speed bursts.

But the video graphics arena, with its need for fast color palette RAMs, is definitely the hottest application for the Bt402 (see *box,* "The quest for speed in computer graphics"). The RAM's 4-ns cycle time qualifies it for use in graphics systems that operate at update rates of up to 250 MHz. In fact, an interleaved pair can through a latched multiplexer handle 360 MHz, which is necessary for 2 x 2-Kbit resolution, or 4 million pixels. And, the 3 x 8-bit Sidecar RAM comes in handy for such overlay displays as cursors, grids, and other graphic elements. (For non-graphics applications, another version of the Bt402 comes without the Sidecar RAM.)

Because its output buffers can be tri-stated, the Bt402 can be cascaded in depth. So, two Bt402s can be employed to build a 512 x 8-bit color palette, four for a 1,024 x 8-bit palette and so on. Sixteen of the devices can build a 4,096 x 8-bit palette before serious speed degradation occurs in the cycle time.

With its inputs and outputs

latched on chip, the Bt402 cascades without the delays imposed by external latches (see *Fig. 1*). Two additional control signals, DX and QX, are used to synchronize the output data with the rest of the control signals, such as sync and blank. The DX input is latched on the rising edge of the clock and appears on the QX output three clock cycles later.

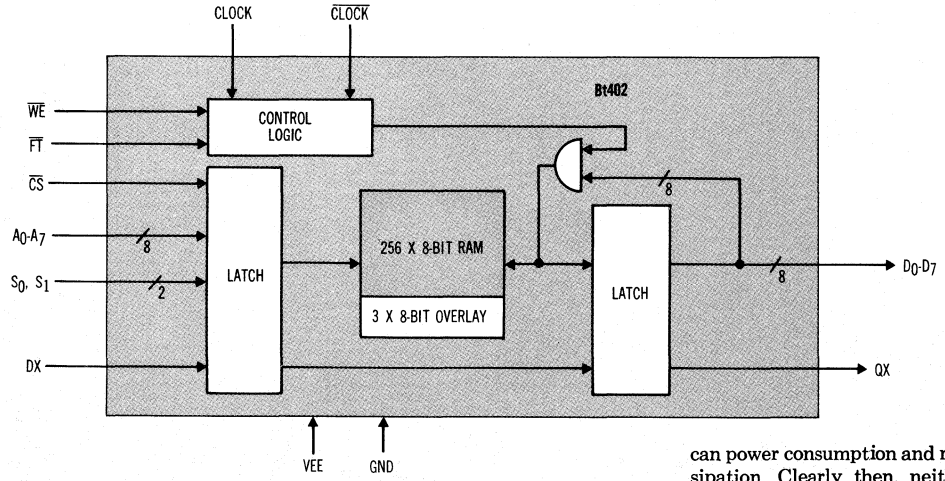

Fig. 1. The pipelined Bt402 color palette RAM includes DX and QX control signals that maintain synchronization between data and control signals. The feedthrough (FT) pin enables the user to select either pipelined or nonpipelined operation, depending on system speed requirements.

In speed and cascadability, the Bt402 far outruns that old workhorse of the video scene, the 100422. This 256 x 4-bit RAM has given dependable performance in color palette applications. But, it is grossly inefficient at implementing the 150 to 360-MHz graphics designs of tomorrow.

For one thing, the 100422 is only 4 bits wide. But in an RGB color system, an 8-bit-wide color palette is essential to the smooth shading of 3-d solids. (The human eye can perceive about 9 bits of green, 7 or 8 bits of red, and 7 or 8 bits of blue.)

For another, the 100422, like most other static RAMs but unlike the Bt402, relies on external latches. These add 2 to 3 ns to its cycle time —and 3 ns is about the entire cycle time allowed a color palette at the high end of the video speed spectrum.

And third, the 100422 starts out with a cycle time of 7 ns. Of course, with a lot of additional circuitry, including interleaving, 100422s or the newer 4-ns 100474s can be rigged for fast cycle times. But this approach gets complicated.

For instance, a 1,536 x 1,280-pixel system with a 4,096-color palette and speed of 165 MHz would require no fewer than 192 of the 100422s, not to mention the attendant glue logic. With a 256-color palette and 250-MHz updating, such a system still requires the use of four 100422s per channel—two to get up to speed and two more to achieve 8 bits of brightness. And to the dozen 100422s must be added the nontrivial circuitry needed for interleaving (see *Fig. 2*).

Another level required

Worse yet, in a 360-MHz system implemented with 100422s, another level of interleaving would be required: eight RAM chips per channel. The faster 100474 would still require interleaving to allow adequate setup and propagation delays in a latched (pipelined) system.

Such system complexity is especially to be avoided at speeds of 150 MHz and more because it complicates pc-board design. Frequently, the controlled-impedance techniques of stripline board design must be used. For this complex, expensive approach, a proliferation of chips must be avoided to reduce the number of traces. But, because so many 100422s are needed to achieve 250-MHz performance, the real estate becomes very tight and more stringent production tolerances must be maintained. Down the line, board yield can become an issue, and so can power consumption and rent dissipation. Clearly then, neither the 100422 nor the 100474 offers the most elegant design solutions for high-resolution systems.

All of the features of the Bt402 combine to reduce the chip counts of color palette designs. In a three-channel color graphics system, three Bt402s per channel can replace the dozen 100422s. The new RAM's 4-ns cycle time makes a speed of 250 MHz practical by eliminating the interleaving (see *Fig. 3*). A 360-MHz system does, however, involve interleaving two Bt402s, but if 100422s are used instead, the design would once again take on the appearance of a bird's nest of RAMs.

By offering a 4:1 reduction in chip count, the Bt402 now makes high-resolution, high-speed display applications far easier to design and much less costly. Moreover, the glue logic needed is negligible, power supply costs are cut, less heat is generated, and pc-board design is simplified.

To achieve additional design economies, a high-performance static RAM like the Bt402 should be used

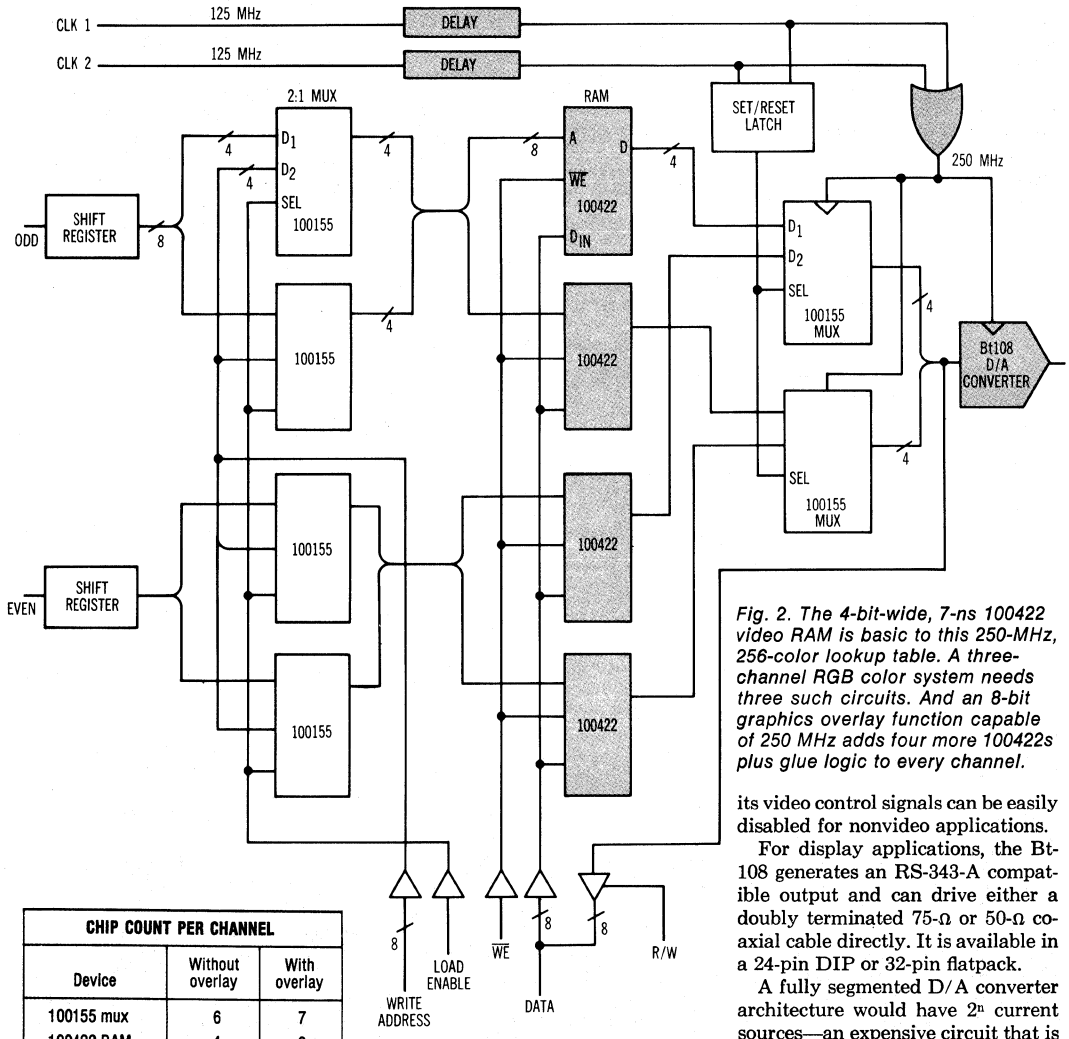

Fig. 2. The 4-bit-wide, 7-ns 100422 video RAM is basic to this 250-MHz, 256-color lookup table. A three-channel RGB color system needs three such circuits. And an 8-bit graphics overlay function capable of 250 MHz adds four more 100422s plus glue logic to every channel.

CHIP COUNT PER CHANNEL		
Device	Without overlay	With overlay
100155 mux	6	7
100422 RAM	4	8
Set/reset latch	1	1
ECL/TTL level-translators	8	9
Glue logic	2	3
Total	21	28

with complementary, high-performance D/A converters—like the 200-MHz, 300-MHz, and faster Bt-108s. Interleaved Bt402s linked with top-end Bt108s can provide a 360-MHz pipelined channel—the fastest track yet to 2,048 x 2,048 pixels.

The Bt108 is an 8-bit, multifunction video D/A converter designed primarily for high-performance, high-resolution color graphics applications up to 400 MHz. (The Bt108-300 is for 300-MHz operation, the Bt108-200 for 200 MHz, and still faster Bt108s are being selected by the factory for special customers.) Implemented in bipolar technology, its unique bias circuitry enables operation with either of the standard 100K or 10K ECL power supplies (respectively −4.5 and 5.2 V). And, although it is a video D/A converter, its video control signals can be easily disabled for nonvideo applications.

For display applications, the Bt-108 generates an RS-343-A compatible output and can drive either a doubly terminated 75-Ω or 50-Ω coaxial cable directly. It is available in a 24-pin DIP or 32-pin flatpack.

A fully segmented D/A converter architecture would have 2^n current sources—an expensive circuit that is rarely justified. The Bt108 instead employs a partially segmented architecture incorporating proprietary Brooktree techniques. It therefore operates with low glitch energy, so that maximum differential and linearity errors are only ±½ LSB over the range of −25° to +85°C.

The partially segmented architecture employs a sophisticated decoding scheme for routing bit currents to the output. Precision component ratios are eliminated, and so are the switching transients that arise when sources are turned on and off.

Integrated Circuits

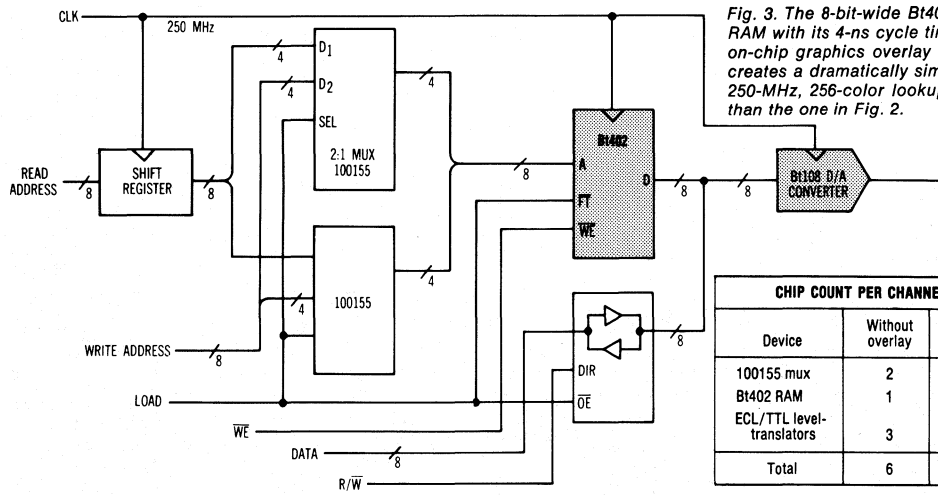

Fig. 3. The 8-bit-wide Bt402 video RAM with its 4-ns cycle time and on-chip graphics overlay RAM creates a dramatically simpler 250-MHz, 256-color lookup table than the one in Fig. 2.

CHIP COUNT PER CHANNEL		
Device	Without overlay	With overlay
100155 mux	2	3
Bt402 RAM	1	1
ECL/TTL level-translators	3	3
Total	6	7

Another sensible video RAM and D/A converter combination is the Bt402 plus Bt109. The new Bt109 triple 8-bit video D/A chip is an ECL version of its pioneering Bt101 CMOS predecessor. It is rated up to 200 MHz and so can handle resolutions of up to 1,536 x 1,280 pixels. Thus, it is ideally suited to mid-range graphics display applications like the current generation of CAD/CAM systems. These today employ 1,280 x 1,024-pixel resolutions and typically use 125-MHz D/As.

The Bt109, like the Bt108, offers pipelined operation to ensure synchronization of the sync, blank, and reference white inputs with the digital input data. It also uses a partially segmented architecture to achieve the same maximum differential and linearity errors and is compatible with 10K ECL logic. It generates an RS-343-A compatible output and can drive doubly terminated 75-Ω coax directly. □

The quest for speed in computer graphics

The ultimate goal in video graphics is a display with the quality of a 35-mm photograph. Such quality entails a screen resolution of 4,096 x 4,096-bit pixels and requires an update rate of 600 MHz—way beyond the reach of currently available CRTs, RAMs or video D/A converters. Instead, the state of the art now has designers grappling with 2,048 x 2,048 resolutions and a 360-MHz update rate.

This level of display clarity must become affordable for critical applications. Air traffic control systems, for instance, could benefit from easier-to-interpret high-resolution displays. In military systems, large sets of data should be displayed very clearly so as not to fatigue the eyes and give rise to human error. In high-performance workstations, only high-resolution displays can do justice to the detail of intricate drawings.

As always, the success of such systems hinges on the price-performance ratios of their constituent ICs and CRTs. A 2,048 x 1,500-pixel or 2,048 x 2,048-pixel color graphics display typically involves some type of static RAM for the color lookup table, coupled with video D/A converters, all running at speeds ranging from 250 to 360 MHz. Today, the only technology that can provide these speeds at all economically is ECL.

Even so, ECL components generally sell for twice to three times as much as equivalent TTL functions. Clearly then, improved and lower-cost components are essential for the next generation of high-performance displays and other pipelined data systems.

That's where the two new Brooktree ECL chips come in—the Bt402 video RAM with its maximum cycle time of 4 ns and 256 x 8-bit density and the compatible Bt109 triple 8-bit D/A.

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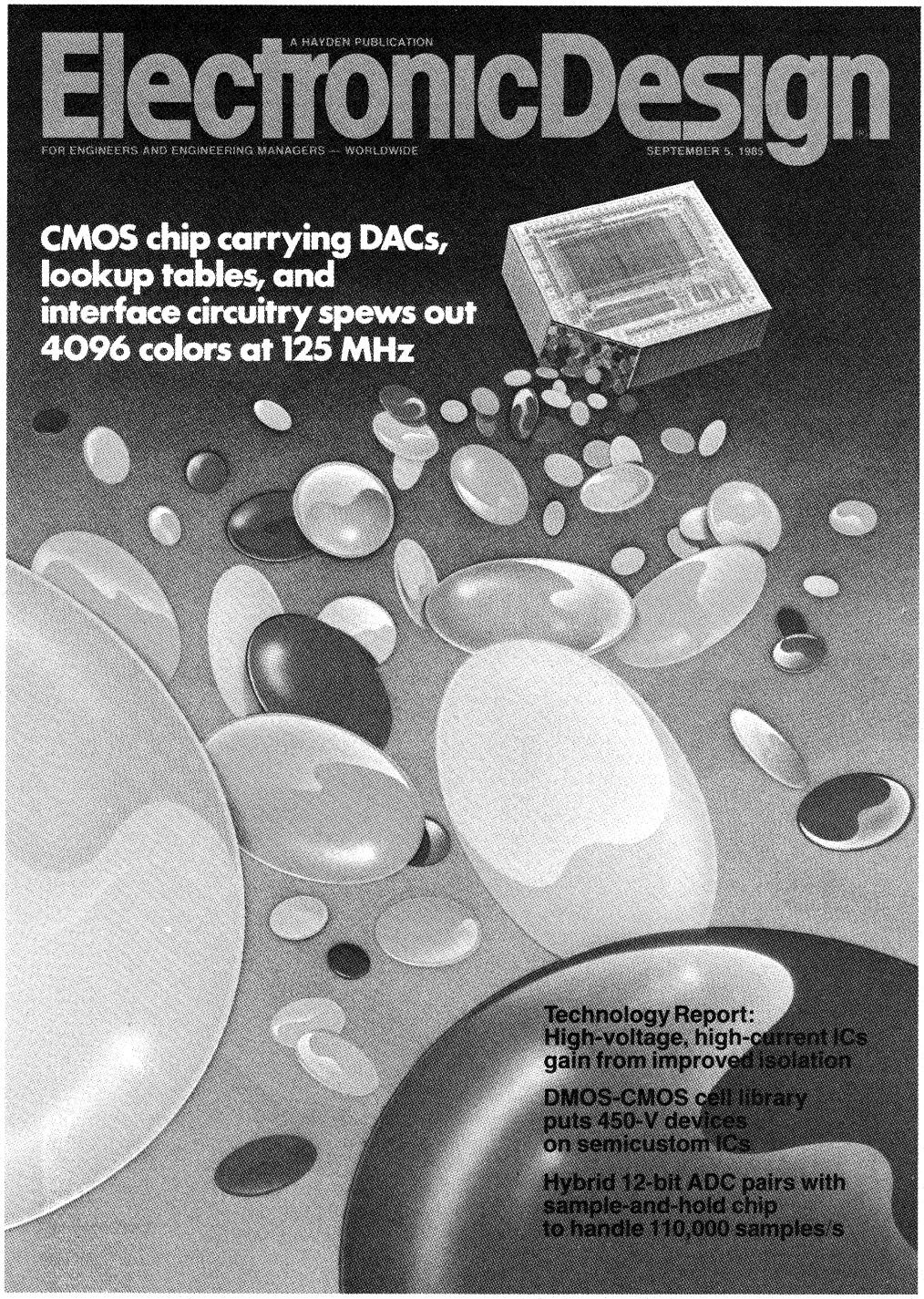
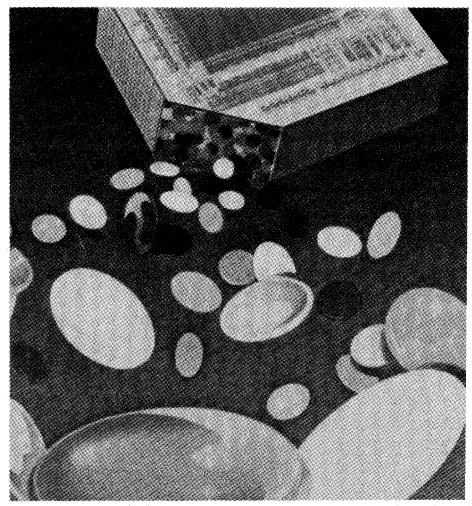

A HAYDEN PUBLICATION
ElectronicDesign
FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE
SEPTEMBER 5, 1985
CMOS chip carrying DACs, lookup tables, and interface circuitry spews out 4096 colors at 125 MHz
Technology Report: High-voltage, high-current ICs gain from improved isolation
DMOS-CMOS cell library puts 450-V devices on semicustom ICs
Hybrid 12-bit ADC pairs with sample-and-hold chip to handle 110,000 samples/s

DESIGN ENTRY

125-MHz CMOS IC supplants numerous ECL parts, drives million-pixel color CRTs

A graphics subsystem on a chip cures high-speed headaches by packing three 4-bit d-a converters, two palettes, two interfaces, and more.

The high-resolution images and rainbow of colors displayed by today's most advanced graphics systems represent a difficult and complex job of engineering. As definition and number of shades soar, so does the data rate, and with it climb the problems of designing with discrete ECL components. Although several integrated circuits have simplified laying out and assembling graphics systems, none has explicitly aimed at eliminating the intrinsic troubles of working with power-hungry ECL circuitry.



Stepping into the picture with just that purpose is the first member of a graphics IC family: the Bt451 RAMDAC. The CMOS chip operates at 125 MHz and consolidates the functions of most, if not all, the ECL components typically found in a high-performance graphics system. It replaces 20 to 30 mostly ECL parts and eliminates the board layout, power supply, and dissipation problems inextricably linked to that high-speed technology. It also solves the interface problem of ECL-to-TTL translation that plagues graphics (see "In Pursuit of the Perfect Picture," p. 134).

Specifically intended to form the core of a high-performance display (1280 by 1024 pixels) for a graphics workstation, the chip contains a 256-color dual-port palette (look-up table), an overlay palette, and a trio of 4-bit digital-to-analog converters that are noteworthy for their low glitch energy and high linearity (ELECTRONIC DESIGN, June 27, p. 37). In addition, it carries logic for masking bit planes and blinking colors, plus a microprocessor interface.

Because the chip's high-speed circuitry has multi-

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As an applications engineer at Brooktree, Keith Jack does product planning and works with customers. He holds a BSEE from Tri-State University in Indiana.

Dale Roark is a product manager for computer graphics chips, and plans long-term strategy. He earned a BS in computer science from the University of Utah.

DESIGN ENTRY

Cover: 125-MHz graphics chip

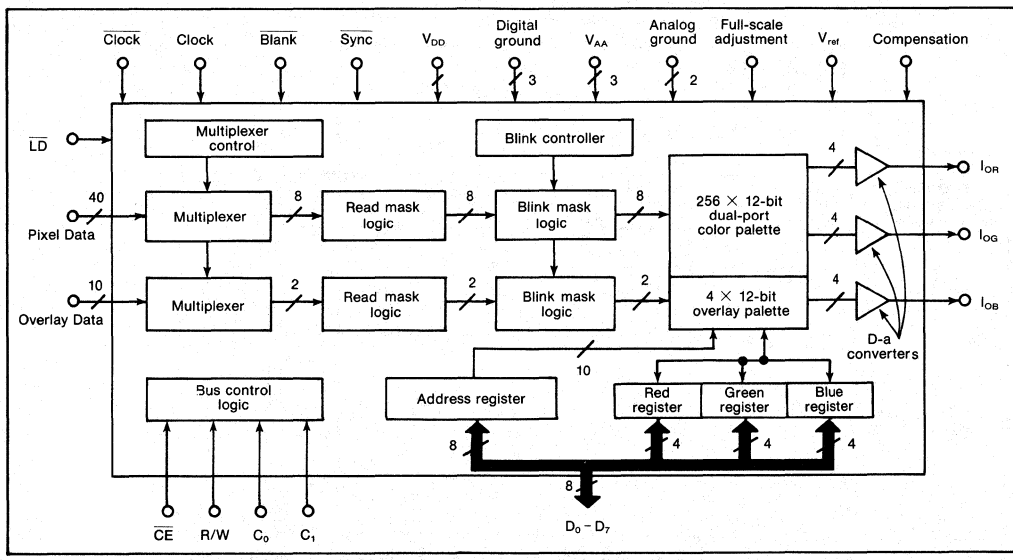
plexed inputs, all but two of its I/O signals can function at 25-MHz TTL levels. Only its differential clock input must meet the 125-MHz requirement for high resolution, and even that signal is powered from a TTL supply. As an added benefit, the chip is highly testable, with critical sections available to the system bus. Finally, the 84-pin (pin-grid array) device runs on a single dc supply of 5 V and consumes no more than 1.5 W.

Blossoming graphics

As computer graphics and imaging systems have evolved from medium-resolution displays of 512 by 512 pixels to high-resolution screens that resolve 1280 by 1024 pixels, data rates have jumped more than an order of magnitude, from 10 MHz to over 100. At the same time, color capability has blossomed from simple schemes that delivered 8 hues and called for 3 bit planes to complex designs that furnish 256 shades, employ 8 bit planes, and incorporate color palettes and 125-MHz d-a converters.

At the latter level of performance, designers have had to reach for expensive and difficult-to-use ECL devices to build much of a system's display-refresh and special-effects circuitry. TTL-compatible memories and d-a converters are simply too slow. Even though ECL may add up to only a small part of the overall system, it requires a separate −5.2-V dc power supply and TTL-to-ECL level-shifting components. Also, special layout rules must be followed and steps must be taken to dissipate heat. And despite their speed, ECL RAMs must be doubled up and multiplexed to match the fastest output rates. Because they are not dual-ported, image updating and refreshing must be carefully juggled to avoid clashes.

To solve these problems, the CMOS graphics chip supplies the high-speed functions that are typically reserved for ECL components (Fig. 1). Its multiplexed TTL-level ports simultaneously accept either four or five pixels, each comprising eight bits of color and two of overlay data. Consequently, the chip's dual-port color palette of 256 by 12 bits paints frames of up to 256 colors from 4096 possible hues. The 4-by-12-bit overlay palette, also dual-ported, offers four options for supplementing the original image with messages and cursors. In addition, read- and



1. Included among the major functional blocks of the Bt451 RAMDAC are three 4-bit d-a converters, TTL-compatible pixel input latches and multiplexers, and read- and blink-mask logic. On-chip pipelining ensures operation at 125 MHz and CMOS technology guarantees dissipation of 1.5 W.

blink-mask registers give designers the ability to control the pixel data on a plane-by-plane basis. On the output, three 4-bit segmented d-a converters supply a signal compatible with RS-343-A specifications to directly drive a monitor through doubly terminated 75-Ω coaxial cable.

By reading the information for several pixels at a time and multiplexing it internally, the chip cuts the 125-MHz data rate of the frame buffer to an input rate of 25 MHz or less. Within the chip, the signals are pipelined at each stage. If an 8-ns pipelined throughput within a particular stage is not possible with conventional techniques, then extra measures are taken. In the palette, for example, these measures include high-speed sense amplifiers and individually dual-ported RAM cells. Consequently, the chip sustains the 125-MHz pixel output rate needed for high resolution.

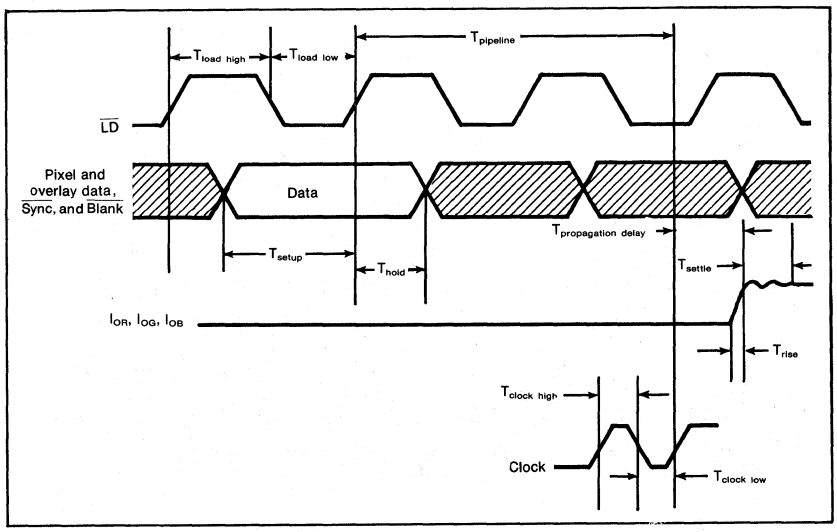
The internal multiplexers can be programmed to operate at either 5:1 or 4:1. As a result, the Load Control signal ($\overline{LD}$), which latches all video data on its rising edge, runs at 1/5 or 1/4 of the pixel clock rate (Fig. 2).

Video data consists of color, overlay, blank, and sync inputs, which all run at 25 MHz. The clock input is the only external signal that runs at the full pixel data rate of 125 MHz. It consists of the complementary ECL signals, Clock and $\overline{Clock}$. The phase relationship between the two clock signals and $\overline{LD}$ is automatically adjusted by the chip so that the setup and hold times of the video data can with confidence be made relative to Load Control only.

Minimized with multiplexers

The chip's programmable multiplexers let designers build a frame buffer with the minimum number of memory chips. When 5:1 multiplexing is picked, the external video frame for a display of 1280 by 1024 pixels can be assembled from just five dynamic RAMs (256k by 1 bit apiece) for each bit plane. Alternatively, the 4:1 setting creates a 1024-by-1024-pixel display from four such RAMs. Static column and dual-ported video dynamic RAMs are both suitable candidates for a frame buffer, provided that they meet the 25-MHz data rate.

Once the pixel data is latched into the chip, subse-



2. In the video I/O timing, pixel and overlay data, as well as the Sync and Blank signals are loaded by the rising edge of the 25-MHz $\overline{LD}$ input. Internally, the pixel data is multiplexed and processed at 125 MHz. Palette pixel data generates the analog outputs for red, green, and blue (I_{OR}, I_{OG}, and I_{OB}).

DESIGN ENTRY

Cover: 125-MHz graphics chip

quent clock cycles move it first to the read-mask logic and then to the blink-mask logic on its way to addressing the color palette. In the read-mask logic, a register's contents is ANDed with bit-plane data to determine if a particular plane will address the color palette. In that way, logical layers can be selectively turned on and off. Such control is useful in applications in which particular logical layers are associated with physical bit planes, as in circuit and IC design. Similarly, the blink-mask register specifies which planes will blink at one of four rates selected by a command register. An internal counter, which is incremented by the video blanking signal, determines the base frequency from which the blinking rate is calculated.

A color palette is an essential part of a high-performance graphics system, enabling all pixels of one color to be changed to another without updating the bit map. In the graphics chip, the aforementioned eight color bits and two overlay bits respectively address one of 256 12-bit options in the color palette and one of 4 12-bit options in the overlay palettes. The 12 bits of color information selected from 1 of the 2 palettes are then pipelined to the three 4-bit d-a converters.

Two modes exist for selecting the four overlay addresses. The first includes the color palette as a possible choice; the second does not.

In the first arrangement, the initial overlay address is ignored, and the two Overlay Control bits

In pursuit of the perfect picture

A range of challenges, most having to do with high data rates, confronts designers of high-resolution bit-mapped graphics systems. For instance, the output data path of a 1280-by-1024-pixel color display demands a searing 125-MHz clock rate. The requisite high-speed circuitry, which mixes ECL and TTL components, makes board layout critical, since care must be taken to prevent clock noise and hold down propagation delays.

High-speed parallel-to-serial conversion is a must if the 8-ns a pixel video-data rate demanded by high resolution is to be met. The frame buffer for a bit-mapped system is typically implemented with dynamic RAMs because it needs so much memory. Conventional dynamic RAMs, however, have relatively slow cycle and access times. Consequently, video data must be read from the frame buffer in parallel and serialized by ECL components. That need to serialize data has given rise to the video RAM, essentially a dynamic RAM with an on-chip shift register. All the same, to achieve a 125-MHz pixel rate still requires ECL multiplexers, TTL-to-ECL interface logic, and control circuitry.

Although only a small portion of the video-timing logic may need to operate at the pixel clock rate, it still needs fast circuits to control the CRT monitor and to refresh the display and the frame buffer's dynamic RAMs. Typically, the logic must also arbitrate accesses to the frame buffer by the system microprocessor and various memory refresh operations. Depending on how the frame buffer's memory is configured, logic may be needed to translate the address and data signals as well.

Creating cursors and overlays is another troublesome task in bit-mapped graphics that frequently necessitates ECL interface components. There are several ways to add cursor and overlay information to the video data, but whatever the approach the end result must modify the displayed colors pixel by pixel. Software solutions, additional bit planes, and dedicated hardware are three possibilities. Also, cursor and overlay information can be merged with the video data at the input to a color palette RAM by addressing additional memory or dedicated locations within the palette. Alternatively, that data can be added at the output of a palette by forcing the d-a converters to a specific color.

Since it must operate at the pixel-data rate, the color palette itself is a natural for ECL and ECL-to-TTL translation logic. Even if multiple palettes are multiplexed to avoid working with such logic, ECL-to-TTL translation is still required at the color palette's interfaces to the d-a converters and to the system microprocessor.

The output of the color palette is fed to three high-speed d-a converters, one each for driving the CRT's red, blue, and green color guns. Depending on the system, a pixel has four, six, or eight bits dedicated to each d-a converter, and therefore to each color. Operating at up to 125 MHz, the converters need an ECL interface as well as other high-speed circuitry to drive terminated coaxial cable. Moreover, each converter must generate signals that are compatible with RS-343-A, exhibit low glitch energy, and produce low differential and integral linearity errors.

(OL_1 and OL_2) select the second, third, and fourth overlay addresses. When the overlay bits are set at 00, a pixel's color is picked by the eight bits addressing the color palette; when the overlay bits are set at 01, 10, or 11, the pixel color data is ignored and the color comes from overlay location one, two, or three, respectively. In addition, the timing of the overlay control bits matches that of the pixel data. Thus the source of the control bits can be either extra planes in the frame buffer or cursor- and character-generation circuits.

Attention getter

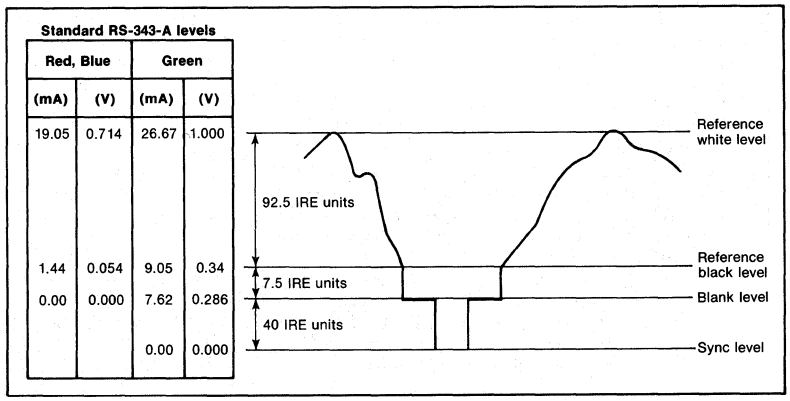
The second mode ignores pixel port data altogether and accesses only the overlay palette. Specifically, any existing image is removed and the first overlay address becomes the source of the background color. The mode is invoked by setting a command-register bit. It is useful when messages that need immediate attention must be flashed to the screen, such as the panic messages displayed before a system shuts down. It also is handy for developing graphics software. In the latter case, the graphics source code for an image can overlay the image itself. To do so, an external character-generator chip set is attached to the overlay port and accessed directly by the system microprocessor.

Regardless of the source of the four bits each of red, green, and blue color data, their target (once every clock cycle) is the same: three 4-bit d-a converters. Each converter has a segmented architecture, in which a sophisticated decoding scheme routes current either to an analog output or to a return line. The architecture eliminates transients that typically result from switching current sources on and off.

Steering identical current sources in that way guarantees monotonicity and low glitch energy. Further, temperature and power supply variations are stabilized by an internal op amp. Differential and integral linearity errors are guaranteed to be less than $\pm 1/16$ LSB and $\pm 1/8$ LSB, respectively, over a temperature range of $-25°$ to $+85°C$.

The chip's video timing signals, $\overline{\text{Blank}}$ and $\overline{\text{Sync}}$, also control the converters' current sources and are TTL-compatible. Asserting $\overline{\text{Blank}}$ overrides the converters' inputs and forces their outputs to the blanking level (Fig. 3). $\overline{\text{Sync}}$, which switches off the current of the green converter only, does not override any data inputs and so should be asserted only during the blanking period. If $\overline{\text{Blank}}$ and $\overline{\text{Sync}}$ are not used, they should be connected to V_{CC} through pull-up resistors.

On the system side, the chip's microprocessor interface eliminates the need for external address and data multiplexers. Eight data bits carry information



3. The graphics chip conforms to the RS-343-A video standard, and is able to drive doubly terminated 75-Ω coaxial cable directly. The d-a converters, which feature a fully segmented architecture, produce the video output waveforms by sourcing current into an external load.

DESIGN ENTRY

Cover: 125-MHz graphics chip

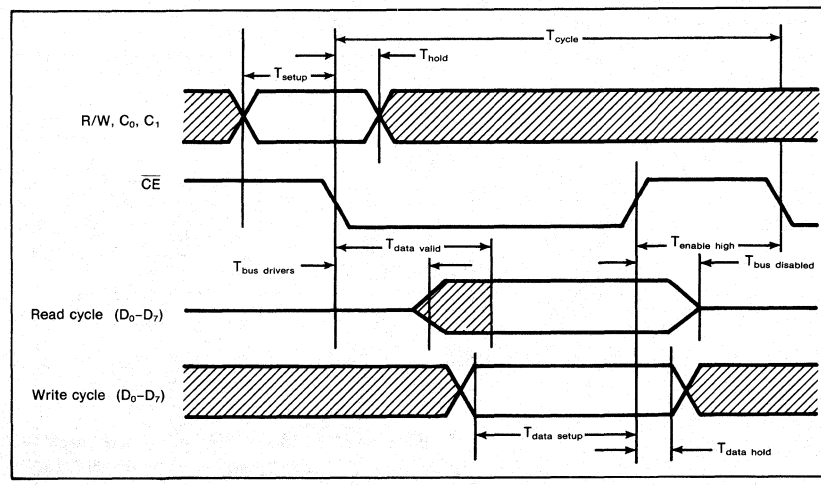
between the graphics chip and a processor, and control inputs C_0, C_1, and $\overline{CE}$ specify the interaction. Among the possible interactions are reading or writing to a palette, and accessing control registers (Fig. 4).

When the microprocessor is reading or writing to a palette, the chip's address counter holds the address of the specific palette entry and selects whether it is red, green, or blue. The counter's 8 MSBs use binary values and choose the specific entry. The 2 LSBs work in modulo three to access one of three color registers. For example, when a new color is being written to the palette, its red and green values are temporarily stored in two of the registers, so that during the write cycle for its blue value, all 12 bits of color information can be written to the palette at once. Conversely, when the microprocessor is reading the color values, it accesses a palette location and the red, blue, and green data is put onto the 8-bit data bus 4 bits at a time.

Not only is the chip dual-ported by virtue of its separate pixel and microprocessor ports, but every RAM cell of a palette is dual-ported as well. Therefore, if a palette location is updated (through the microprocessor port) at the same time that it is being read by the pixel port, the maximum disturbance is held to a single pixel. Subsequent reads are guaranteed to produce the updated information. That feature eliminates the color streaks that frequently occur when a palette entry is updated asynchronously to the display-refresh timing. It also does away with the circuits needed to restrict updating operations to the retrace time.

Instant access

Another valuable feature obviates the need for extra test circuits to verify that the chip and its surrounding system are operating as intended. Usually, the high speed of the video output, compared with that of the system microprocessor, requires an intervening layer of multiplexers to diagnose any probems between the bit plane and the output converters. In contrast, all of the chip's internal test registers, as well as the palettes, are accessible at all times through the microprocessor port. By writing to one of several test registers, the processor can in-



4. The graphics chip is designed to appear like a typical peripheral device to a microprocessor, which can read to or write from all internal registers and RAM locations at any time. The dual-ported color palette lets the processor access and modify color information without significantly disturbing the displayed image.

dividually read each output converter's input.

Applications typically call for a minimum of interface logic. As mentioned, the chip requires five dynamic RAMs for each plane of a display comprising 1280 by 1024 pixels; four dynamic RAMs for 1024 by 1024 pixels. Up to 10 planes are possible: eight for color and two for overlay information. The RAM outputs drive the chip directly (Fig. 5).

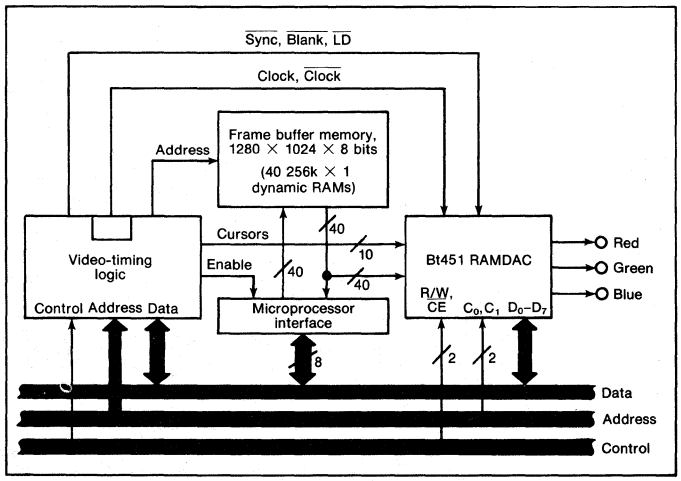
The same outputs also drive the data bus, letting the microprocessor read the buffer memory. If 25-MHz dual-ported video RAMs are used, the processor should be able to access the frame buffer about 98% of the time. If static column RAMs are employed, however, the processor should access the frame buffer only during the retrace interval to avoid disturbing the display. Alternatively, double-buffered bit planes can be used.

The advantage of using static-column RAMs for each bit plane is that the memory row refresh cycles occur only during the display's horizontal retrace intervals. Consequently, during the display time, video data can be read from the frame buffer as fast as the RAM can supply it. As long as the memory has a maximum static-column access time of 40 ns or less, no external multiplexers or shift registers are needed to read the frame buffer.

The video timing logic is responsible for generating the differential clock signal, $\overline{LD}$, $\overline{Sync}$, and $\overline{Blank}$. It must also arbitrate access to the frame buffer and refresh the dynamic RAMs, if they are used. Finally, it must generate the cursor if one or two additional frame buffers are not allocated for that purpose. As noted, only a small portion of the video logic must run at 125 MHz.

The logic can send out up to five consecutive cursor pixels at 25 MHz and can then connect directly to the graphics chip's TTL inputs. To do that takes only two ECL devices: a 125-MHz oscillator and a 3-bit counter, which divides the oscillator's frequency by 5.

Such a small number of ECL chips can be connected to the system's 5-V dc supply, instead of a separate −5.2 V dc source. The graphics chip is designed to accept differential clocks generated that way.□



5. In a typical system built around the graphics chip, most of the high-speed ECL components are eliminated. The frame buffer and video-timing logic connect across 25-MHz TTL interfaces. Only the clock line and the chip's internal circuitry (highlighted) run at the 125-MHz pixel rate.

DESIGN ENTRY

ELECTRONIC DESIGN EXCLUSIVE

Octal DAC chip's interface meets processor bus directly

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Eight DACs arranged in four symmetrical pairs get instructions straight from a microprocessor, simplifying designs with programmed signals.

Cutting the number of components in a system down to the absolute minimum is the goal of every design engineer. As chips have evolved from discrete units, through small- and medium-scale integration to the present large- and very large-scale circuits, the number of parts needed in any system has fallen sharply. Integration of components also lets computers control analog outputs through multiple digital-to-analog converters.

Applications of this useful arrangement include the generation of programmable dc reference levels and waveforms for electronic test equipment; waveform generation for multichannel control systems; and provision of multiple waveforms for music synthesizers and pattern generators.

Such hardware applications have until now been handled by dual or quad 8- and 12-bit d-a converters—the highest density commercially available in that kind of chip. However, these dual and quad circuits did not always interface easily with microprocessors to generate programmable signals. Integration has now moved forward again, however, in the development of the industry's first monolithic octal 8-bit d-a converter chip. Fabricated in CMOS, the Bt110 is TTL-compatible and connects through a normal bus directly to standard microprocessors, without any peripheral interface circuitry—which greatly simplifies system design.

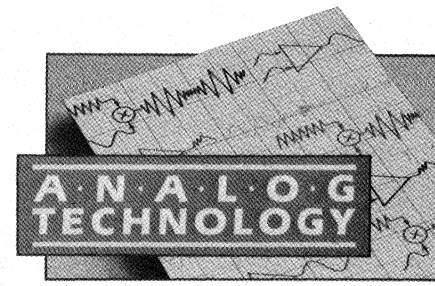
The new chip includes an on-board voltage reference, and needs only a few passive components to decouple and set up its full-scale output. (The designer has the option of using an external reference voltage.) The chip's eight converters are set out in pairs for tracking and thermal symmetry. The members of each pair track each other closely, which makes possible the construction of d-a converters with more than eight bits of resolution.

The chip's usefulness derives from its unusual internal architecture (Fig. 1). Eight bits are routed through an address-controlled multiplexer into one of the latches on the rising edge of the Write control input, $\overline{WR}$. The latches in turn statically feed the selected converter's decoder. Each converter has 63 major on-chip current cells and three minor current cells (Fig. 2). The major cells connect with the most-significant 6-bit decoder, the minor cells with the least-significant 2-bit decoder. With a 4:1 current ratio, the cells' outputs add up to the total current output for any given state.

INTERNAL ARCHITECTURE

Each pair of converters lies symmetrically on either side of the chip's axis, one being the mirror image of its partner. This arrangement enhances tracking and matching as a function of variations in the manufacturing process—any variation affects each one of a pair in exactly the same way. The chip's design and architecture trades off the size of the chip against differential and integral nonlinearities.

Monotonicity is crucial to the operation of any d-a converter. If a converter chip is truly monotonic, its analog output signal increases with any increase in the input binary code. The Bt110 main-



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ANALOG TECHNOLOGY

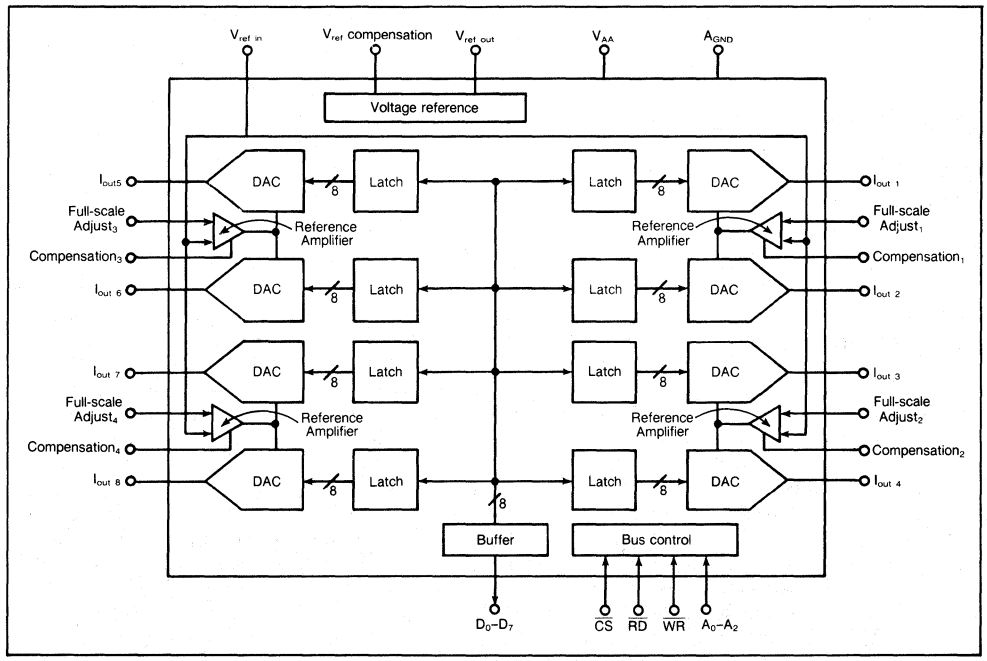
tains its monotonicity and low glitch energy through identical current sources and by current-steering their outputs. While ladder-type converter designs depend for their monotonicity on precision resistors with ratios held to tight tolerances, the segmented architecture of the Bt110's eight converters does away with any need for such precision. The converters route their bit currents to either I_{out} or A_{GND} through proprietary decoding networks, which perform a "thermometer" type of decoding and increase the converter's output by one LSB as its input increments in binary.

The Bt110's on-chip voltage reference is a conventional bandgap design supplying a 1.2-V output with a typical 50-ppm drift as temperature varies. The low-offset internal amplifiers that set up the full-scale output are similar to those used for precision op amps. The amplifiers are unconditionally stable and their low output impedance provides a stable reference voltage to drive each pair of converters.

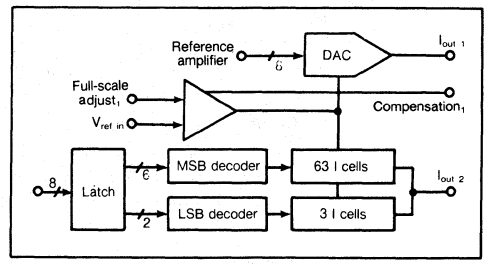
Each of the Bt110's eight converters offers ± 1-LSB differential and integral non-linearity at temperatures from 0° to 70°C. Power dissipation is typically 150 mW at a 10-MHz update rate, far less than for bipolar and hybrid d-a converters. The chip features typical full-scale converter-to-converter matching of 2% between all eight converters, and 5-ppm tracking between any two pairs.

OUTPUT LOADING

The output current source of each converter is designed to drive a virtual ground and provides a maximum load capacitance of 20 pF. The output impedance has a relatively flat characteristic from 0 to 10 MHz for driving op amps. When feeding into a 50-Ω resistive load with 10-pF capacitance, the 10-ns maximum output rise/fall time is



1. The Bt110's eight d-a converters are arranged in four pairs for close tracking and thermal symmetry. The converters connect directly to a standard microprocessor bus without any need for external peripheral interface circuitry.



2. Each d-a converter in the Bt110 uses a current source scheme for decoding, with 63 major current cells connected to the most-significant 6-bit decoder and three minor current cells connected to the least-significant 2-bit decoder.

faster than that for many commercial op amps. Converter-to-converter crosstalk, important when the Bt110 generates several independent precision voltages, is typically −46 dB at a 200-kHz update.

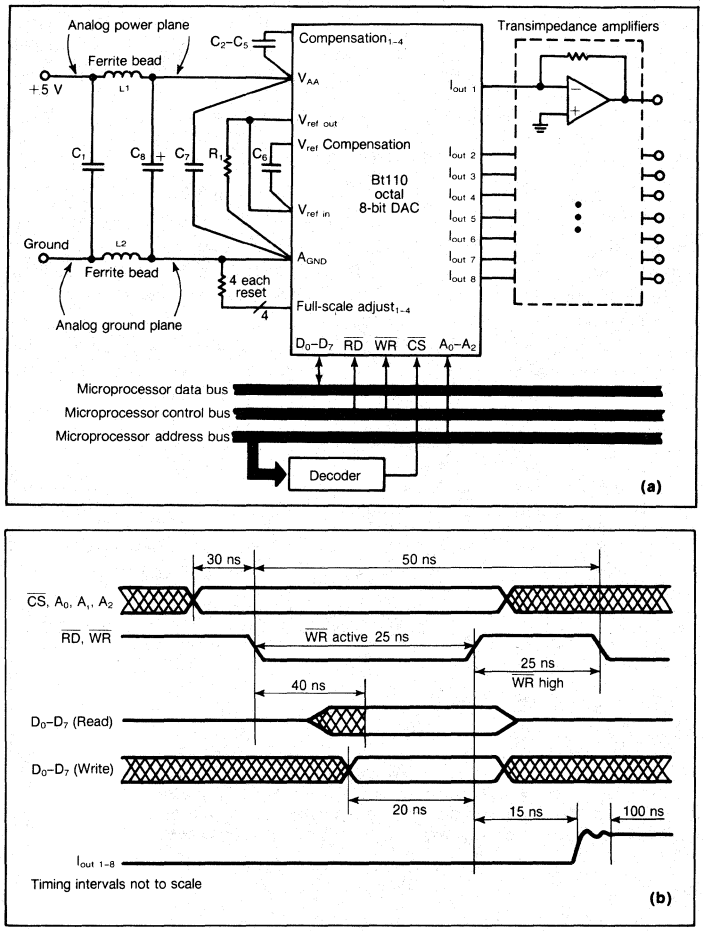
The chip addresses any of its eight converters by incorporating a TTL-compatible microprocessor interface with a bidirectional 8-bit data bus (D_0–D_7), Chip Select input ($\overline{CS}$), Read input ($\overline{RD}$), Write input ($\overline{WR}$), and three bits of address data (A_0–A_2). Hitching the chip to an Intel or Motorola microprocessor is easy; the microprocessor addresses the converters directly, as though the chip were a memory-mapped device (Fig. 3a).

When loading data into any one of the converters, the microprocessor operates just as though it addressed a memory location and wrote a data byte to it. Each converter has its own address and can be loaded independently, allowing the microprocessor to manage up to eight analog channels at once, and to change the status of all the converters with only eight writes.

The microprocessor can also read back the input to the converters, and thus need not store copies of those inputs in its memory. The chip can be loaded in 80 ns—made up of 30 ns address setup, 25 ns $\overline{WR}$ active, and 25 ns $\overline{WR}$ high (Fig. 3b). Settling time for the converters is 100 ns.

ANALOG INTERFACING

The eight converter outputs ($I_{out\ 1-8}$) are high impedance current sources providing up to 1 mA with an output compliance of −1.0 to +1.2 V. An external op amp can be connected to the chip's outputs to provide any higher voltages and limit output speed. A faster op amp can create problems, since the user then needs experience in high-frequency design in order to avoid parasitic oscillations in the circuit, along with problems caused by poor



3. A microprocessor addressing the Bt110 treats it like a memory location. Each d-a converter has its own address and can be loaded with data independently (a). Loading can be accomplished in 80 ns, the limiting cycle consisting of 30 ns address setup, 25 ns $\overline{WR}$ active, and 25 ns $\overline{WR}$ high (b).

3

DESIGN ENTRY ■ Octal IC DAC
ANALOG TECHNOLOGY

layout of the components and the wiring.

Among op amps that perform well with the Bt110 are the HA-2539 and HA-5033 for fast settling time and wide bandwidth, the 1435 for medium performance, and the LM318 for a good compromise between speed and bandwidth at less than 1 MHz. Most op amps with acceptable offset drift and stability are suitable for dc applications. Output to a maximum of about ± 1 V can also be achieved by terminating the Bt110 with a resistor.

ON-BOARD REFERENCE

The on-chip voltage reference ($V_{ref\ out}$) can supply a stable voltage to the $V_{ref\ in}$ input over a specified temperature range. This reference, along with a resistor to ground on the Full-scale Adjust pin, sets the full-scale output of each pair of converters. The resistor value is determined as follows:

$$R_{set} = 1000\frac{(V_{ref\ in})}{(I_{out})}$$

where R_{set} is in ohms, V_{ref} is in volts, I_{out} is in milliamperes.

If more than one Bt110 is used, the $V_{ref\ out}$ of one can drive up to three $V_{ref\ in}$ inputs of the others. Although the Bt110's on-chip reference is adequate for most applications, an external 1.2-V reference such as the LM385Z-1.2, with a drift of no more than 50 ppm, will improve stability across variations in temperature.

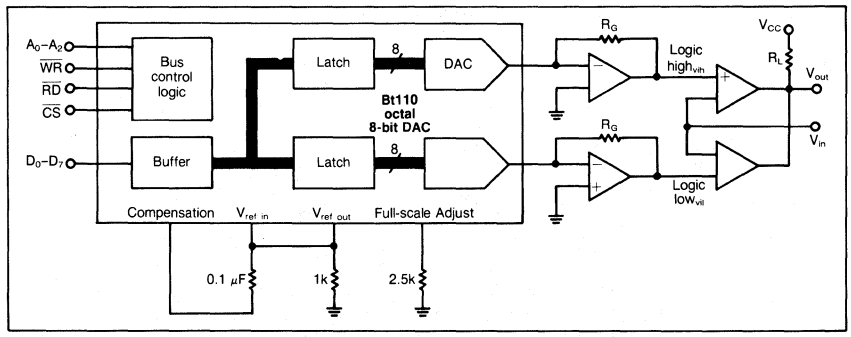
Each pair of converters shares a reference amplifier (Full-scale adjust 1–4) that controls their output current. Because of the close tracking within each pair of converters the chip can be configured for a range of requirements. The close tracking is especially important when a pair of converters is to function as one high-resolution unit, or is used as an a-d converter with a successive-approximation register.

The Bt110's speed and high level of integration make it ideal for multi-DAC applications. Because the chip can be updated to 10-MHz, disk-drive testing—which requires millisecond or microsecond timing waveforms—is a natural application. A disk-drive tester with a Bt110 can generate such analog waveforms as stepper pulses and multifrequency-modulated data signals, and can simulate the necessary timing signals.

MULTI-DAC DESIGNS

An engineer designing an analog I/O board for data acquisition or control will also find the Bt110 useful. The chip economically adds eight analog outputs to a printed circuit board. It takes up little space on the board, and its built-in microprocessor interface connects handily with the board's bus.

In the design of programmable function generators, the chip can produce the necessary sinewaves, squarewaves, and nonlinear functions. Greater than 8-bit resolution is



4. Two DACs on the Bt110 can serve as a window comparator and provide high-low threshold voltages. Output is high inside the window and low above the high limit or below the low limit. One practical application for this circuit is as part of a pin receiver card in automatic test equipment, where a matched pair of converters determines the threshold limits.

often needed in such cases, and can be achieved by adding the outputs of two pairs of converters. The scheme has the added advantage of reducing the even-ordered harmonic content of any sine or cosine wave generated by the chip—similar to the harmonic reduction from analog push-pull amplifiers.

A digital potentiometer based on the Bt110 will also show significant improvement in performance over mechanical devices, since the dirt, wear, and other problems affecting mechanical potentiometers is eliminated. Substitution of d-a circuits makes calibration of voltmeters, oscilloscopes, signal generators, and similar equipment fully programmable.

Where, for example, a potentiometer is used as a voltage divider, an 8-bit converter can provide a linear 255:1 voltage-control range—enough to be a fine adjustment for many linear functions. Using the Bt110, any adjustment takes place entirely under the control of the microprocessor. Although a d-a converter is more expensive than a potentiometer, the extra cost is made up in increased system reliability, simplified operation, and lower assembly costs.

AUTOMATIC TESTING

Generating multiple dc voltage levels and/or analog waveforms for automatic test equipment (ATE) is something the Bt110 does well. The close tracking and matching between the chip's individual converters make it possible to program high-low-level limit comparators in ATE, with repeatability over time and variations in temperature (Fig. 4).

Using the chip to build four 12-bit reference d-a converters gives the system designer important economies in integration. In the testing of ICs or printed-circuit boards, dc reference levels (logic-high and logic-low) must be generated to test the device's input. In this type of automatic test equipment application, 12 digital bits are often needed to obtain 6-mV resolution over a ±12-V range.

During a power-up check of hardware for automatic test equipment, the Bt110 can be tweaked as necessary to calibrate hundreds of circuits against a single a-d reference circuit. When resolution drifts away from the reference level, adjustment of the converter input involved will yield the correct 12-bit value through direct writes from a microprocessor.

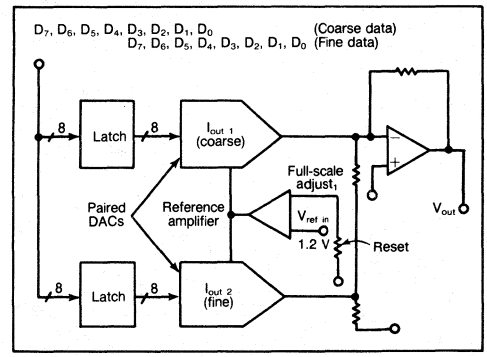
One Bt110 can also provide four calibrated 12-bit references (Fig. 5). The coarse d-a converter creates 256 major steps, all filled by the fine converter (fine d-a current is resistively split by the ratio of two resistors tied to the op amp's negative input). The resistor ratio forming the current divider should be chosen to bleed current into the op amp's negative input.

This current level is directly related to the amount of data overlap between the coarse and fine converters. Additional circuitry may be needed to null any offsets, but the fine converter can be loaded with binary values in order to trim the voltage output and achieve 12-bit accuracy during calibration cycles. The Bt110's paired d-a converters make possible a stable 12-bit converter over a range of temperatures. □

Jeff Teza is Brooktree's director of product marketing. A cofounder of the company, he was its first design engineer. He holds a BEE from State University of New York at Stony Brook, Long Island, and recently graduated from the University of California, San Diego, executive program for scientists and engineers.

Keith Jack joined Brooktree a year ago as an applications engineer after experience designing microcomputer systems and VLSI with Burroughs and Rockwell International. He holds a BSEE degree from Tri-State University, Angola, Ind.

Chuck Stanley is Brooktree's applications engineering manager. With 14 years experience in integrated circuit and hardware design, both digital and analog, he holds a BEE from Georgia Institute of Technology, Atlanta.



5. When the Bt110's matched pairs of d-a converters are teamed up, each pair can serve as a 12-bit reference converter, sharing four overlapping bits. The eight LSBs contribute to the fine adjust and the eight MSBs to the coarse adjust. One chip can thus provide four calibrated references.


FOR PROJECT MANAGERS AND DESIGN ENGINEERS—WORLDWIDE
AUGUST 20, 1987
ELECTRONIC DESIGN
A HAYDEN/VNU PUBLICATION
DESIGN INNOVATION
Build custom bus interfaces with function-specific PLDs
ELECTRONIC DESIGN REPORT
Advanced connectors break the bottlenecks in backplane speed
DESIGN APPLICATION
Hassle-free designs for T1-to-PBX links
Display 1024 colors plus a 256-color window with dual-palette DACs

3

DESIGN INNOVATION

Video palette raises color ante to 1024 separate hues

Thanks to a CMOS RAM d-a converter, a palette of 1024 colors alternates with one supplying 256 colors to yield true color at 135-MHz speeds.

NICOLAS MOKHOFF

Imagine having 1024 different colors to choose from to paint a computer-generated object on your screen. Now visualize another object within a window of that display—defined by a separate 256-color palette. To top it off, consider the image quality when you operate the two palettes at 135 MHz. That is what you can expect in the first of Brooktree's new crop of CMOS RAM digital-to-analog converters (RAMDACs).

With the Bt461 converter, the company's designers have considerably improved on the previous part, the 84-pin Bt458 (ELECTRONIC DESIGN, June 26, 1986, p. 131). In comparison, the Bt461 converter, housed in a 132-pin grid array, has two more address inputs that expand the addressability of the primary color palette to 1024 by 8 bits; five new address inputs for the alternative palette of 256 by 8 bits; and another five new address inputs for a larger (32 by 8) overlay palette (Fig. 1).

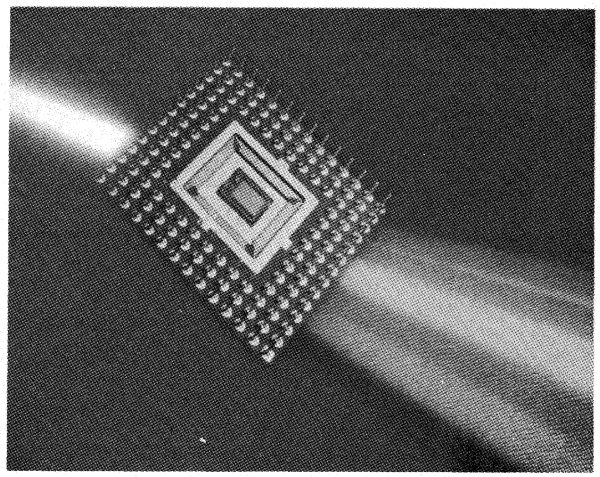
This expansion carries a sacrifice, however. While the earlier part had three 8-bit d-a converters at the output stage, the Bt461 unit accommodates but one 8-bit converter. As a result, when the 461 converter goes to work as a single-chip in a monochrome system, only 256 shades of gray are possible. In a color system built with three Bt461s and 10 planes, though, 1024 colors can be displayed out of a possible 16.8 million. And Brooktree has pumped up the top clock speed to 135 MHz to ensure a comfortable screen refresh rate.

Future members of the converter family will house three d-a converters to accommodate single-converter color systems. "The 132-pin grid package was chosen to allow for future compatible RAMDACs," says product manager Lauren Schlicht. "Our current CMOS process uses 1.5-μm design rules, but future RAMDACs will be designed using 1.2-μm rules, and later, 1-μm rules. Those parts will be able to address color palettes of up to 4096 by 8 and incorporate three 8-bit converters in the same 132-pin package."

Meanwhile, the new converter's features make possible sophisticated graphics in 1280-by-1024-pixel images. Besides giving the user control over alternative palettes, the 8-bit d-a converter also supplies a third palette—a 32-by-8 color overlay. Thus, the designer can run EGA graphics through the overlays without interference from main workstation graphics.

"We have found that users want to design their graphics to best suit their needs without worrying about EGA," says Schlicht. "The 32-word overlay color palette accommodates the full 4 bits of EGA and still has 1 bit left over for something like the cursor display."

Often the graphics application software chiefly generates and manipulates images in the frame buffer. The system software is usually reponsible for cursor movement, menu insertion and deletion, and user messages, with minimal con-



DESIGN INNOVATION ■ Cover: RAM d-a converter

cern about the graphics image.

Using three to five additional bit planes for overlays enables the system software to control user interface graphics independently of the graphics image. Using 32 overlay words (32 by 8 bits) gives the designer maximum flexibility for deciding what should run through the overlays. Multiple-color cursors, text, grids, and windows can be run through the overlay ports and kept separate from the main frame buffer.

The multiple pixel ports and internal programmable multiplexers (3:1, 4:1, or 5:1) enable TTL-compatible interfacing with incoming data lines up to 45 MHz to the frame buffer, while maintaining the 135-MHz video data rate. The programmable multiplexers allow designers to build a frame buffer with the fewest possible memory chips.

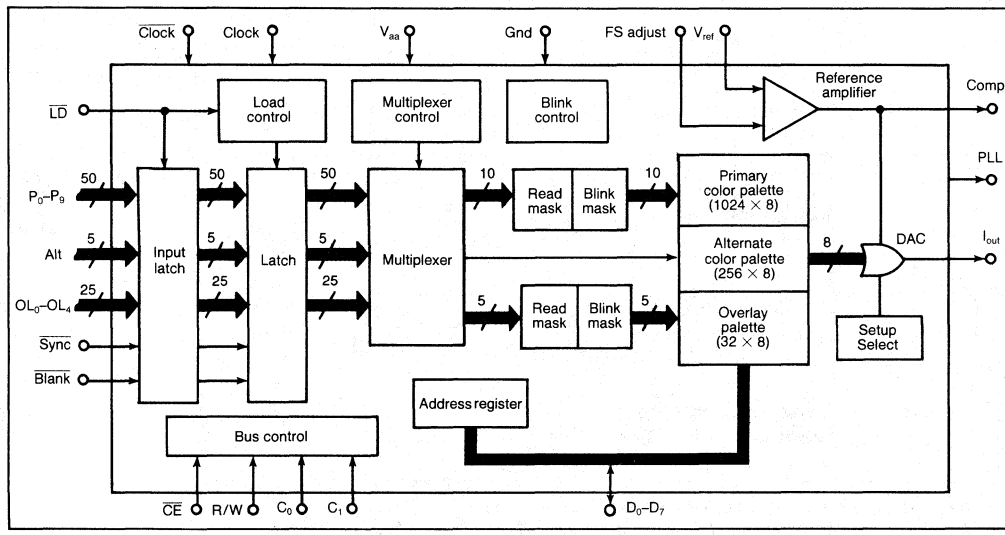
After considering user needs, designers came up with Bt461's two switchable palettes, which are aimed at the high-resolution graphics becoming more and more common in personal computers and workstations. With two separate palettes that can be switched on a per-pixel basis, the designer can control multiple windows with completely different color palettes (Fig. 2). In addition, true color (8-bit) windows within a complete graphics environment are possible.

PIXEL BY PIXEL

The 256-color palette can be used for lookup table bypass by sending data directly to the d-a converters or can be used to correct the gamma strength of a true-color input. Thus, true-color input from a CD ROM or another external source can be displayed in a window. Or users can switch color graphics from the frame buffer and CD ROM input pixel by pixel. Alternatively, the 256-color palette can be used as 256 words of overlay as long as data is multiplexed with regular pixel input lines.

Another sought-after feature, pixel panning, allows the user to shift the data being displayed on the screen. As the data is being output from the frame buffer, the user wants to display the subsequent pixels as if they were the first pixel out of the buffer, thereby panning the display. Using a multiplexed RAM-DAC, where the Sync and Blank information is loaded every four or five pixels, panning is difficult.

The Bt461, however, can be programmed to "slide" the Sync and Blank signals. This information is latched in the cycle before it is needed. Then the Sync and Blank signals can occur after any one of the four or five pixels is loaded in the following cycle. This feature allows the user to load Sync and Blank signals

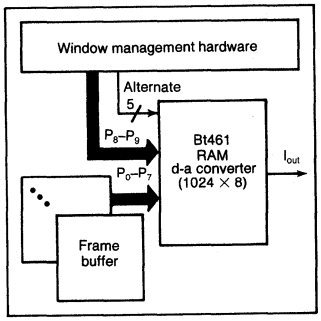


1. Brooktree's single-channel RAM d-a converter contains three different color palettes from which a designer can extract 1024 colors from up to 16.8 million possible shades. A PLL output synchronizes multiple Bt461 converters with sub-pixel resolution.

DESIGN INNOVATION ■ Cover: RAM d-a converter

at any pixel—without operating the inputs at pixel speeds.

Built into the Bt461 converter is compensation for output skews from the d-a converters, which could cause inferior-looking graphics on the display. Most converter manufacturers leave the skew problems to the system designer to solve. The Bt461 supplies a phase-lock loop (PLL) output, which is a positive-going current that can be programmed to be active during Sync or Blank. This signal can then genlock or synchronize clock signals between chips or to an external sync source, without having to strip the Sync or Blank out of the Composite Video out signal. This saves on extra hardware and ensures a distortion-free analog output.



2. In a system, window-management hardware would use the higher order pixel address bits (P9 and P8) and the five alternate palette select inputs to choose between five unique 256 by 8 color palettes without reloading the color palette RAM.

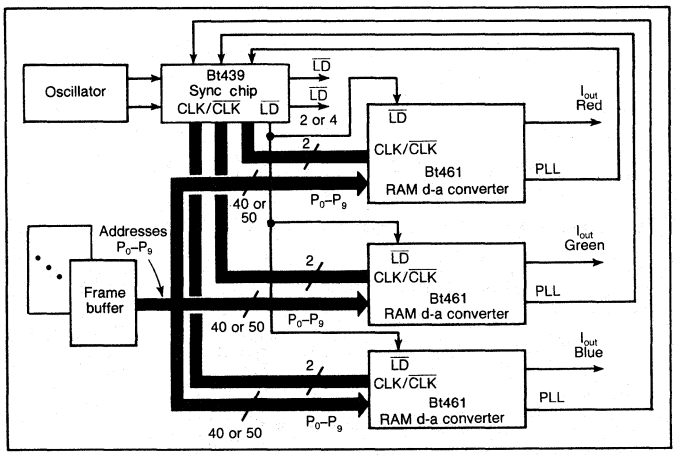
Brooktree is developing a separate clock-generator chip (Bt439) to allow three PLL signals as inputs and move the clock inputs to the RAMDAC (Fig. 3). It will support the 3:1, 4:1, and 5:1 input multiplexing of the 461 converter, synchronize them to sub-pixel resolution, and will optionallly set the pipeline delay of the converter to eight clock cycles. This synchronization chip then, with the Bt461 converter, synchronizes the three-channel processors within one-quarter-pixel time (about 1 ns at 135 MHz).

Sub-pixel synchronization is suppported through the PLL output. Essentially, PLL gives a signal to show the converter's amount of analog output delay, relative to the clock signal. The CMOS process and the analog output delay variation from device to device makes this necessary. The Bt439 compares the phase of PLL signals generated by up to four Bt461s and adjusts the phase of clock signals to each 461 to minimize PLL phase difference.

Because the 461 is the first in a family of software and pin-to-pin compatible converters, Brooktree designers have incorporated an identification register on board that allows each part to identify itself. This helps accommodate future designs and software, which can utilize any member of the family. In each system, the microprocessor driving the 461 converter discern the size of the palette and whether the part is a single-channel or multiple-channel one. The ID register lets the microprocessor determine the type of RAMDAC in use.

Just as with the company's other RAMDACs, the 461 supports a standard microprocessor bus interface, giving the microprocessor direct access to the internal control registers and color palettes. Users have two ways to write and read color data to and from the device. In the normal mode, color data is loaded in each write cycle and is output each read cycle. In the RGB mode, color data is loaded during red, green and blue write cycles and output using corresponding read cycles.

At the output video stage, a programmable setup of either 0 or 7.5 IRE (video output signal ratio) opens the part up for European applications since the zero setup is required by the European PAL video standard. The Bt461 generates a RS-343A compatible video signal, used by high-end workstations and most PCs, and can directly drive a doubly terminated 75-Ω coaxial line, without requiring external buffering.□



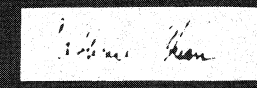
3. In a color system built around three Bt461 converters, 16.8 million shades of color are possible. With 10 planes (10 bits per color) 1024 colors can be displayed simultaneously by having the pixel data inputs (P_0–P_9) tied to the three devices. A new sync chip (Bt439) is expected to synchronize the d-a converter outputs to within a 1-ns skew.

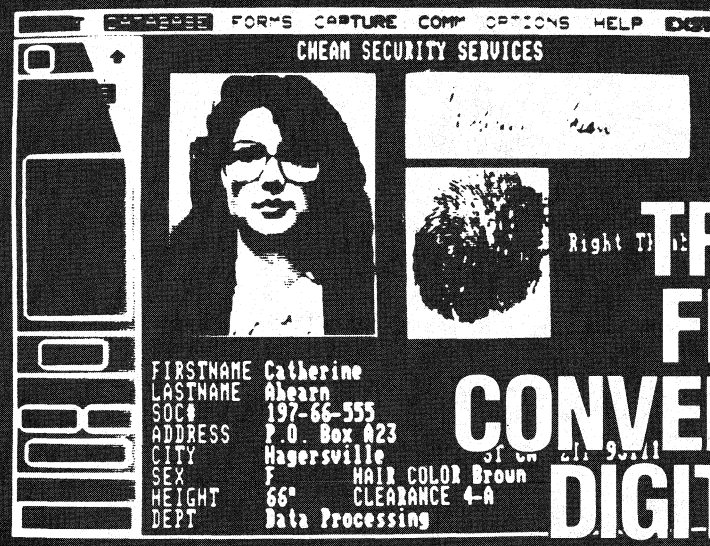
STRETCHING THE LIMITS OF COMPUTER BUSES
PARALLEL RISC BRINGS 40 MIPS TO VMEBUS

ELECTRONIC DESIGN

A VNU BUSINESS PUBLICATION IN U.S. $5.00

FEBRUARY 9, 1989





TRIPLE FLASH CONVERTER DIGITIZES TV IMAGES

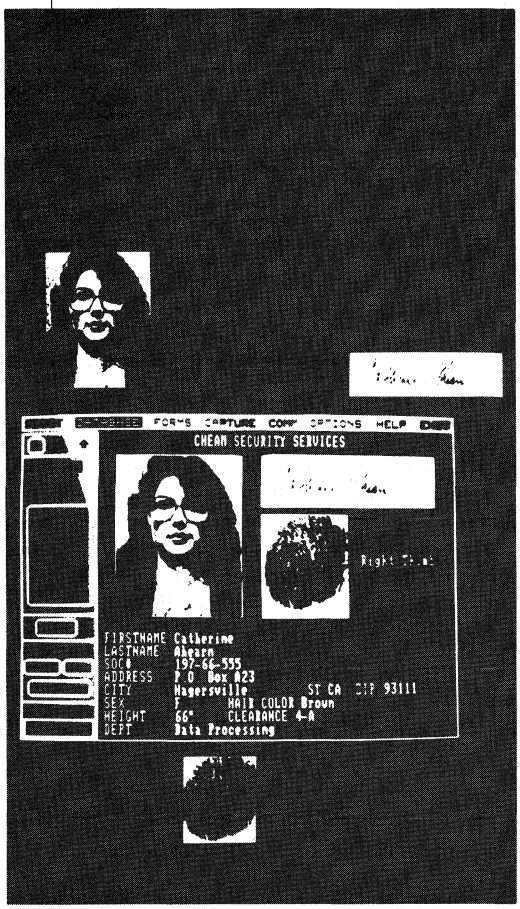
• SPECIAL REPORT: NEW DESIGNS WRING SPEED FROM SMALL PLDs
• USING RISC FOR VMEBUS CONTROL • DESIGNING WITH PLDs

3

COVER FEATURE

THE FIRST TRIPLE FLASH ANALOG-TO-DIGITAL CONVERTER—AND THE FIRST WITH A LOOKUP TABLE—JETS 8-BIT IMAGES AT 15 MHZ.

IMAGING CHIP HOLDS THREE 15-MHZ 8-BIT ADCS



FRANK GOODENOUGH

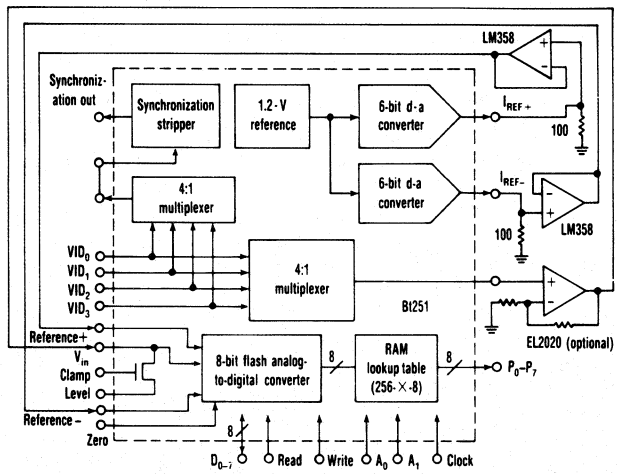
Most systems designed to digitally capture video TV images, be they for PCs or for TV studio special-effects equipment, contain RAM lookup tables between their flash analog-to-digital converters and their digital signal processor. These RAMs perform real-time data manipulation prior to storing the data for processing or analysis. Such manipulation includes inverse gamma correction, contrast enhancement such as thresholding, data inversion, and creation of a nonlinear transfer function for the a-d converter. In addition, most of these systems employ not one but three converters, one each for the red, green, and blue signals. And many systems must be capable of handling multiple video and/or synchronization inputs.

If you're designing such systems, Brooktree, creator of the first triple-color-palette digital-to-analog converter, or RAMDAC, has just made your job easier. They've come up with two host-controllable a-d converter systems on a chip. Dubbed "image digitizers" by Brooktree, the CMOS Bt251 and Bt253 are true firsts. The 251 is intended for black-and-white applications; its cohort for color.

At the core of the Bt251 lie two circuits: an 8-bit flash a-d converter ca-

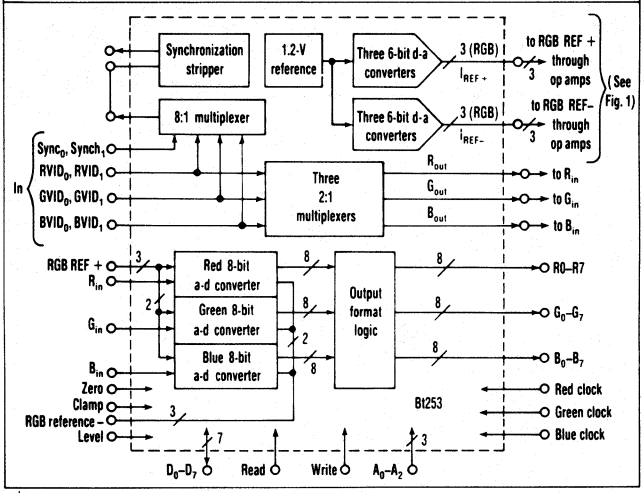
COVER: 8-BIT, 15-MHZ IMAGE DIGITIZERS

8-BIT, 15-MHz ADC WITH LOOKUP TABLE



1. BROOKTREE'S Bt251 IMAGE DIGITIZING 8-BIT flash converter sports an on-chip lookup table, a four-channel video input multiplexer, a dc reference, and a sync stripper, all under control of a host microprocessor.

TRIPLE 8-BIT, 15-MHz FLASH ADC



2. THE Bt253 COLOR IMAGE DIGITIZER from Brooktree has three 8-bit, 15-MHz flash analog-to-digital converters. Output format, input multiplexer, sync stripper, and six digital-to-analog converters are under host-microprocessor control.

pable of sampling video signals beyond 6 MHz at more than 15 megasamples per second (MSPS) and a 256-×-8-bit RAM lookup table *(Fig. 1)*.

The Bt253, on the other hand, can boast of having not one but three 8-bit flash converters *(Fig. 2)*. With this chip you can grab red, green, and blue video signals simultaneously. The flash trio is followed by output-format logic that lets you select (through the host) 24-, 15-, or 8-bit true-color or 8-bit pseudo-color data formats.

A 24-bit true-color format uses all 8 bits from the three converters; 15-bit true-color uses each converter's 5 most-significant bits (MSBs); 8-bit true-color uses the 3 MSBs. In an 8-bit pseudo-color format, an 8-bit gray scale is produced by one converter and the colors are added by the CPU.

Both of these chips hold enough pc-board-size-slashing, power-cutting, design-time-trimming bells and whistles to build a carousel—calliope and all. The chips include such functions as input multiplexers, synchronization strippers, dc-restoration circuits, and an on-chip reference which, with associated circuits, provides variable gain and offset. All these features, like the lookup table on the Bt251 and the formatting logic on the Bt253, are under host-processor control.

According to Brooktree, these chips were designed for imaging applications. However, many engineers designing multichannel, high-speed data-acquisition systems (especially for DSP applications) would jump at the opportunity to get three flash converters for $17.33 each; especially if the converters need less than 200 mW each and together take up less than 1.2 by 1.2 in. of pc-board space. And at $39 each (a price that includes the multiplexer and reference), the Bt251 flash converter should find some general-purpose applications too.

Performance figures for the two chips are eye openers *(see the table)*. Let's start with the input multiplexers. The Bt251 gives you four one-line inputs (VID_0–VID_3); the Bt253 a

3

COVER: 8-BIT, 15-MHZ IMAGE DIGITIZERS

pair of three-line (RGB) inputs ($RVID_0$, $RVID_1$, $GVID_0$, $GVID_1$, $BVID_0$, and $BVID_1$). You externally connect the multiplexer outputs to the flash converter inputs (V_{in} for the 251, R_{in}, G_{in}, and B_{in} for the 253). The input impedance of the converters is 1 MΩ shunted by about 15 pF, leading Brooktree to recommend insertion of buffer amplifiers—such as the EL2020 from Elantec of Milpitas, Calif.—between multiplexer outputs and flash inputs. The amplifiers can also be used to adjust video gain if required.

Because most standard TV video signals are ac-coupled and must be dc-restored with a clamp before digitizing, on-chip clamp circuits are provided for both devices. The Clamp signal, a logical one, restores the video to the voltage on the Level pin, which is nominally at ground. If the video is dc-coupled, you can either float the Level pin or connect it to the video input; or you can wire the Clamp signal to a permanent logical-zero point.

Six DACs In A Row

If you've been examining the block diagram of these chips, you're surely wondering what a flash a-d converter is doing with a flock of on-board 6-bit d-a converters (only two on the Bt251). Silicon costs money. You'll notice that each d-a converter takes an input from the chip's 1.2-V bandgap reference, and that the d-a converters' outputs are tied to the Reference+ and Reference– pins of the converters through external op amps. These inputs drive, respectively, the top and bottom of their reference-divider resistance strings. Having variable, rather than fixed, references allows the converters to perform both gain and offset adjustments.

Full-scale current from the d-a converters is 10 mA. Thus a voltage from 0 to 1 V is developed across the op amp followers' 100-Ω input resistors. Resolution is 15 mV per least-significant bit. Most standard video signals run from about 700 mV to 1 V. For maximum accuracy, the d-a converter driving the top of the divider circuit should be programmed to the value of the maximum expected input voltage, but no more than 1.2 V.

The second d-a converter trims the offset voltage at the bottom of the divider. The top of the ladder should be operated between 0.7 and 1.2 V; the bottom between 0 and 0.5 V. The minimum input video signal for 8-bit resolution is 0.7 V. By modifying the circuits between the output stage of the d-a converters and the reference divider, resolution may be increased or decreased. For example, decreasing the value of the resistor between a converter's output stage and ground increases resolution. In many applications, changing the reference voltage precludes the need for a variable-gain amplifier for the video signal.

For all practical purposes, the CMOS flash converters' comparator offset voltage must be repeatedly zeroed. With the exception of these Brooktree converters, comparator zeroing is automatically performed every clock cycle. But with a proprietary Brooktree architecture, zeroing need only be performed when required. For example, when digitizing TV or any other kind of raster-scan signals, comparator offset-voltage zeroing can be done during the retrace time of each line.

Flashy Strippers

For those working with one of the standard TV video formats (RS-170, RS-170A, RS-343A, RS-330, PAL or SECAM), these chips provide synchronization strippers. Any one of the input lines to either chip can be selected through multiplexers to be fed into the synchronization stripper circuit. Additionally, either of two

BT251 AND BT253 SPECIFICATIONS

Conditions: REF+ = 1 V, REF– = 0, REF– ≤ V_{in} ≤ REF+, T = 0° to 70°C, V_S = 4.75 to 5.25 V

Parameter	Units	Minimum	Typical	Maximum	Conditions
Video input signal	V	0.7	1	1.2	
Voltage on reference inputs					
REF+ (top)	V	0.7	1	1.2	
REF– (bottom)	V	0	0	0.5	
Resolution	Bits	8	8	8	
Integral linearity error	LSBs			±1	
Differential linearity error	LSBs			±1	
Input resistance	MΩ	10			Clamp = Logic 1
Input capacitance	pF		15		Clamp = Logic 1
Input resistance	Ω		50		Clamp = Logic 0
Reference divider resistance	Ω		1000		
Differential gain error	%		2		
Differential phase error	Degrees		1		
Conversion rate	MHz			15	
Multiplexer switching time	ns		100		
Full-power input bandwidth	MHz	6			
Rms signal-to-noise ratio					
F_{in} = 4.2 MHz	dB	43			Sampling rate = 10.7 MHz
F_{in} = 4.2 MHz	dB	42			Sampling rate = 14.32 MHz
F_{in} = 2.75 MHz	dB	44			Sampling rate = 6.75 MHz
F_{in} = 2.75 MHz	dB	41			Sampling rate = 13.5 MHz
Supply voltage	V	4.75	5	5.25	
Supply current	mA		120		

COVER: 8-BIT, 15-MHZ IMAGE DIGITIZERS

separate synchronization inputs ($Sync_0$ and $Sync_1$) can be selected by the Bt253's host. Thus synchronization information can be recovered from one signal while a second signal is being digitized—which is useful for systems with red, green, blue, and synchronization video interfaces.

The Synchronization signal from the multiplexer circuit to the stripper circuit is ac-coupled through a 0.1-μF capacitor. An internal clamp circuit ensures that the tip of the synchronization signal is at 1 V, regardless of the amplitude or dc offset of the video signal. In this circuit, the video is compared to 1.1 V—100 mV above the desired sync-tip level. As long as the input signal to the stripper is less than 1.1 V, its output will be a logical zero.

The two flash converter chips support a standard digital microprocessor interface (D_0-D_7, RD, WR, A_0 and A_1, plus A_2 for the Bt253 flash converter). In the Bt251 flash converter, an internal 8-bit address register, in conjunction with A_0 and A_1, specifies which control register or RAM location the microprocessor is accessing. All registers and RAM locations may be written to or read by the microprocessor at any time. The address register increments after each write cycle, facilitating read-modify-write operations.□

IMAGING AND GRAPHICS

How to Drive 4-Mpixel Displays

by Dana Wilcox, Wyle Plummer, and Dennis Galloway,
Brooktree Corp.,
San Diego, CA

Designers can now build 2K × 2K (4 Mpixels) color graphics display controllers with off-the-shelf ICs. Fast 1-Mbit VRAMs, multibit shift registers, and DACs can be used to rapidly implement the back ends of such controllers.

Aviation, medical instruments, and imaging beg for color graphics displays with greater size and resolution than what is offered by 19″ 1280 × 1024 display subsystems. Although the graphics controllers and monitors that support 4-Mpixel displays cost as much as $100,000, this price is expected to drop. Sony, Hitachi, and Mitsubishi have demonstrated 26″ to 30″ color monitors capable of 2K × 2K resolution. In fact, Sony is already shipping its 30″ monitor for $40,000; in 18 months the price of that monitor will likely fall to just $10,000.

The impetus behind this decreased price and increased availability is the fact that designers can now build controllers—for just $10,000—using off-the-shelf ECL and VRAMs. The use of these standard parts removes the cost-prohibitive burden of using semicustom ICs in low-volume applications.

Controllers Head for the Sun

Many 2K × 2K display controllers to be introduced this year will be based around the Sun-3/4 CPUs. These 9U-based VME controllers can display full 2K × 2K images with a number of different bit-planes. Controller specifications dictate design characteristics. Both VLSI ICs and CMOS 1-Mbit VRAMs must be used to fit on a 9U board. To meet the $10,000 price constraint, the controller must utilize off-the shelf ICs.

Such graphics subsystems can be partitioned into four functional blocks: a front-end graphics processor, a frame buffer, the back-end display circuitry, and the monitor. **Figure 1** shows the functional blocks of a graphics subsystem and the bandwidth associated with each partition. Color and monochrome display subsystems include the same basic blocks. In color systems, however, more planes of memory are included in the frame buffer and three DACs are needed to drive the RGB guns of the CRT.

In operation, an on-board graphics processor accepts commands from the host CPU, processes the commands, and controls the frame buffer and back-end circuits. The graphics processor is used to write image data into the display frame buffer.

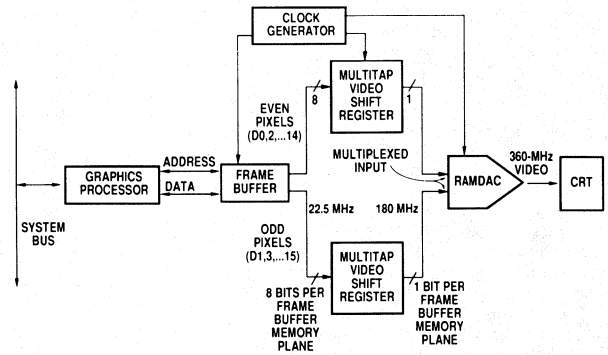


Figure 1: Build your own 2K × 2K graphics controller. Shown here are the functional partitions of a graphics system as well as the bandwidth associated with each partition.

Adding Value to 2K × 2K Controller Designs

by Julius Perl, Univision Technologies, Burlington, MA

To meet the needs of the next decade, board-level graphics designers increasingly will focus on higher resolution. Today, the maximum attainable resolution for a color monitor is 2K × 2K. In medical, military, and seismic applications, such monitors let the user view 4 Mpixels on-screen. To drive these monitors at their full 360-MHz bandwidth, designers can utilize high-speed off-the-shelf ICs. Companies such as Brooktree, AMD, IDT, and Motorola are now producing DACs, shift registers, and high-speed logic to rapidly implement designs.

Specific applications require greater effort to add more functionality to off-the-shelf designs. For instance, in medical image processing, scanned X-ray images may require 12-bit data. Designers cannot turn to off-the-shelf parts to view such images. Instead, custom LUTs must be developed in 12-bit in/8-bit out configurations, enabling the complete 12-bit image to be windowed and leveled.

In desktop publishing as well as medical imaging applications, the need for fast pixel replicated hardware zooms must also be addressed. By using sophisticated clocking methods with off-the-shelf parts, board-level controllers can be developed to meet these needs.

Univision chose to use off-the-shelf VLSI ICs where possible in the development of its UDC-3412, a VME-based 9U graphics controller for Sun-3 workstations (**Figure 2**). To accommodate both hardware zoom and 12-bit images, high-speed clocking and 12-bit LUTs were incorporated into the 2K × 2K design. The board features 2K- × 2K- × 12-bit memory in a double-buffered configuration. Due to real estate constraints, 96 1-Mbit VRAMs were used—48 for each memory buffer.

Output from the 12-bit memory plane divides into even and odd pixels, which are fed into multiplexers 16 pixels at a time. The design uses four Brooktree Bt424s and two AMD 8177 multiplexers. Each Bt424 can be thought of as five 16:1 multiplexers that multiply the 22.5-MHz clock frequency from memory to the 180 MHz needed to drive the DACs. Both even and odd pixels are output—12 bits at a time—from the mux section. These bits, describing odd and even pixel values within the image, drive a 12-bit in/8-bit out LUT. In operation, this LUT allows 256 intensity levels in the frame buffer of the image to be displayed from the total of 12 bit-planes. In addition, the LUT can be programmed to allow 8-bit images plus four overlay bit-frame buffer organization.

The two proprietary LUTs were designed around high-speed static RAMs. Like the shift register section, partitioning was used within the LUT, reducing the clock speed needed to access the static RAMs. The output from the LUTs results in two series of odd and even 8-bit pixels. These are both fed to the input section of three Brooktree Bt492 palette DACs. At the input of the DAC, an 8-bit in/8-bit out LUT allows pseudocoloring of the 8-bit data. Finally, a 2:1 multiplexer in the DAC increases the 180-MHz bandwidth from the LUT stage to the 360 MHz needed to switch the DAC.

An important design consideration of the UDC-3412 was the clocking needed to provide the hardware image zoom function. In essence, hardware zoom is accomplished in two stages for both horizontal and vertical directions. To zoom the image in the horizontal direction, the 180-MHz clock speed feeding the Bt424s and LUTs is halved to 90 MHz, and the clock speed of the DACs reduced to 180 MHz. This results in a widening of the clock period and associated pixel values, providing a 2× zoom.

At the same time, the vertical image direction must be zoomed by duplicating every other image line on the screen. An on-board Intel 82786 graphics chip is used to load every data line twice into the VRAM's video shift registers. Thus, although the picture is the same size, the information has been reduced by a factor of two, resulting in the vertical zoom.

The advent of high-speed VLSI graphics ICs has eased the design burden of single-board 2K × 2K controllers. And, while it is unlikely that display resolutions larger than 2K × 2K will soon proliferate, such designs will help both IC vendors and board manufacturers. Very likely, IC manufacturers will offer wide high-speed monolithic LUTs within the next decade as well as more specialized high-speed DACs. And future board designers will find such designs commonplace.

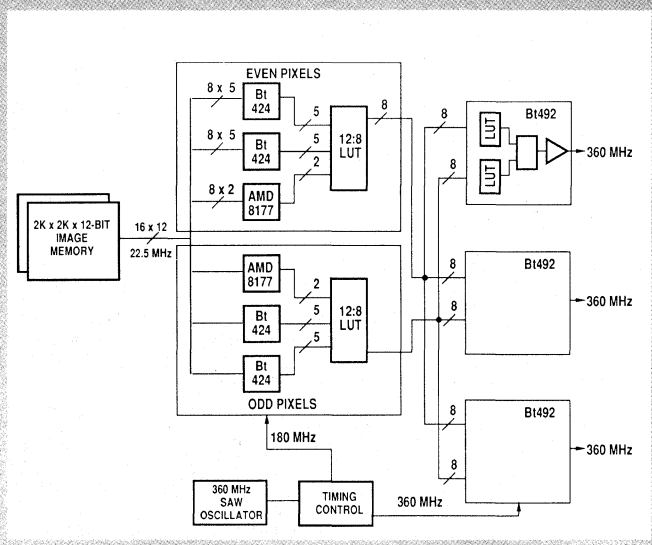


Figure 2: Univision's UDC-3412 is a double-buffered 2K- × 2K- × 12-bit display controller based on a Sun-3 9U format. The design uses off-the-shelf Bt424 multiplexers, Bt492 RAMDACs, and 1M VRAMs. In order to clock the board at 3-nsec/pixel frequencies, a 360-MHz SAW oscillator is used.

IMAGING AND GRAPHICS

Four 256K × 4-bit VRAMs comprise each plane of the buffer in a 4-Mpixel display subsystem. Single bit-per-plane monochrome displays require a single plane. **Figure 3** shows a single plane of memory and the frame-buffer organization. Monochrome displays with gray-scale as well as color displays require a frame buffer with multiple planes. Every plane of memory includes 1 bit of information pertaining to each pixel.

Each plane of a frame buffer outputs a 16-bit word (representing 16 pixels) on every clock cycle. Here, shift registers on-board the 256K × 4 VRAMs are used to output the data. A typical 1-Mbit VRAM can shift data at speeds up to 33 MHz. In a 4-Mpixel display, a 22.5-MHz clock provides the output bandwidth—multiplied by 16, the clock ultimately provides the 360-MHz bandwidth required to drive a 4-Mpixel monitor. One way to achieve this 16× multiplication involves splitting the frame-buffer output into even and odd channels. Bit 0 (of each word) represents an even pixel, bit 1 represents an odd pixel, and so on. Figure 1 shows the data flow split into two 8-bit streams and input into two separate multitap video shift registers. The shift registers accept an 8-bit parallel input and shift the data out 1 bit at a time. The 8:1 ratio provides an 8× speed increase to 100 MHz in both the even and odd output channels.

The multiplexed input to a Brooktree RAMDAC provides the final 2× speed increase. The RAMDAC combines both even and odd pixel data streams and generates the 360-MHz signal. Shift registers, color LUTs, and DACs make up the back-end circuitry.

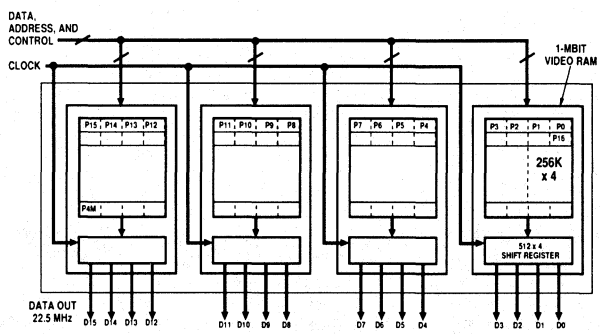


Figure 3: A single plane of memory in a planar frame-buffer organization. Color display controllers require such frame buffers to be designed with multiple planes. Each plane will output a 16-bit word for every clock cycle.

Designing the Board

In 2K × 2K display controllers, the final system application will dictate both the choice of graphics processor and the frame buffer design. In this example, the frame buffer consists of a planar organization with 8 bits/pixel and single buffering. This type of design also includes four planes of overlay image memory. The overlay buffer provides a method of adding a color cursor or selectively masking parts of an image for X Windows applications.

Four 1-Mbit VRAM chips define a single plane; the 12-plane system requires a total of 48 memory chips. Each plane produces 16 bits of data per clock cycle. Thus, the frame buffer produces a total of 192 bits (12 words). Typically, the shift register clock input to the VRAM will be around 22.5 MHz. Output from each memory plane is split into even and odd pixel data streams. **Figure 4** shows how a single plane connects to a shift register to generate a 180-MHz data stream. Because the frame buffer employs a planar architecture, each word of data from a plane contains a single bit (plane) of 16 different pixels output from the frame buffer.

Sixteen (8 for even pixels, 8 for odd pixels) 8-bit shift registers are required to accept the eight individual words from the eight image planes. These shift the data out so that the combined dual 8-bit outputs of the shift registers represent all eight planes of single odd and even pixels. The shift-register operation orders the data and provides an 8:1 bandwidth increase to 180 MHz. Likewise, four pairs of 8-bit shift registers handle even and odd pixel inputs from the four frame-buffer planes dedicated to the overlay image.

Off-the-Shelf IC Solutions

Figure 5 shows a back-end 2K × 2K graphics controller design implemented with two off-the-shelf VLSI ICs from Brooktree—Bt424 and Bt492. In the Bt424 design, a 40-bit multitap shift register is used to shift video data. The part can accept 40 inputs and provide five outputs. It can also be programmed to operate as a single shift register of up to 40 bits, two 16- or 20-bit shift registers, five 8-bit shift registers, or four 10-bit shift registers.

Five Bt424 shift registers are required to handle the 12 words of data available on each memory cycle. Working in parallel, these ICs implement 24 8-bit shift registers and output dual 180-MHz data streams. These dual data streams represent even and odd pixel data. Overlay data streams are wired in a logical-OR to the

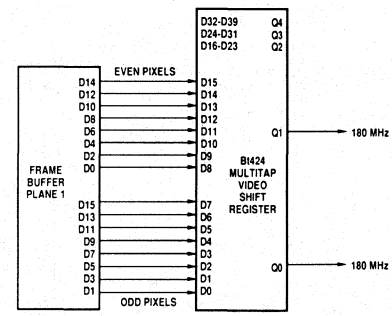


Figure 4: Connecting image planes to shift registers. In this diagram, a single image plane is connected to a multitap video register to produce a 180-MHz data stream.

IMAGING AND GRAPHICS

Putting Four Million Pixels On-Screen

by Sarah Macdonald and Michael Laurie, Matrox Electronic Systems Ltd., Dorval, Quebec, Canada

Until recently, 2K x 2K color display processors were only available as a series of add-in boards or complete systems. A single-board solution that can be integrated into existing computer systems eliminates external boxes which, in turn, reduces costs. Power consumption and physical size are also decreased, making it possible to integrate such display subsystems into a variety of application areas.

Matrox's decision to design a 2K x 2K controller was prompted largely by customer interest. At present, the $100,000 cost of integrating a 2K x 2K system is prohibitive for all but a few applications. Air traffic control is virtually the only area where the price is now feasible. Here, 2K x 2K raster-based systems act as a replacement for vector-based systems. Unlike vector-based systems, however, moving to a raster allows for greater interactivity and networking.

Introduced at last year's Siggraph '88 conference in Atlanta, GA, the Matrox VG-2048 single-board 2K x 2K display processor occupies one slot of a Sun-3 or Sun-4 system. The VG-2048 was designed around TI's TMS34010 graphics processor. It also contains a 2K- x 2K- x 8-bit frame buffer and 1.5 Mbytes of display list RAM. The 34010 can serve as the interface between the board's resources and the VMEbus. The GSP's host port allows access to its various registers, frame buffer, and display list RAM.

Building a 2K x 2K color graphics subsystem at the microcomputer board level presented several challenges. Designing the graphics board was relatively straightforward. The board's graphics processing section is similar to that of Matrox's current graphics boards but with a larger frame buffer. The major design challenge was fabricating a back end capable of driving a monitor at 360 MHz.

One of the first and most important questions was where to place the video output section. At first, the video output was to be implemented on a single pc board. But due to the high frequency required for the VG-2048, the timing requirements could not be met, and a single pc board was regarded as too risky.

The video output section of the VG-2048 was built around three Bt107 DACs from Brooktree. Since these DACs output video data at a rate of 357 MHz, the board's frame buffer could not interface directly with the DACs. Therefore, two stages were required to funnel the low-speed data stream coming from the frame buffer to the high-speed data stream entering each DAC. A Bt424 serializer first converts the parallel video data to a high-speed serial stream. Two of these streams are then fed to a register interfacing to the DACs. The initial design of the VG-2048 does not include LUTs, but they are being incorporated into the final product.

Video output supports the Sony DDM-2801C color monitor with a 60-Hz vertical frequency and a 127-kHz horizontal fre-

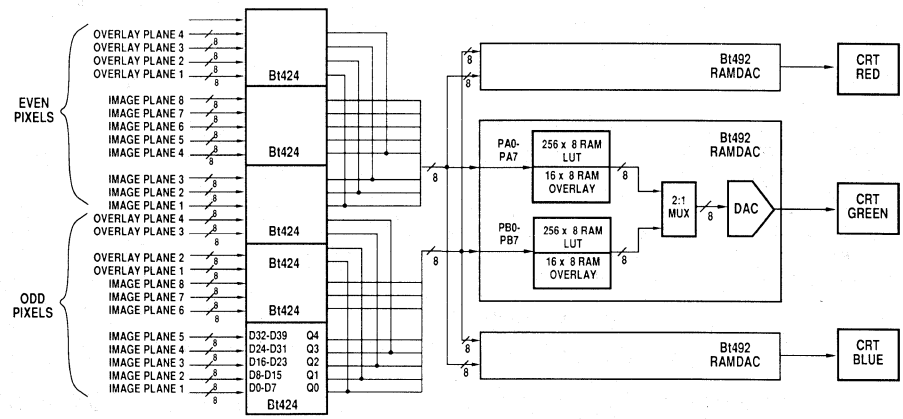


Figure 5: Completing the design. Combining fast 1-Mbit VRAMs with four Brooktree Bt424 shift registers and three Bt492 RAMDACs allows designers to build 2K- x 2K- x 12-bit display controllers with off-the-shelf parts.

quency. There are five output connectors for red, green, blue, horizontal, and vertical synchronization.

A second and very important consideration was the 360-MHz frequency needed to drive the DACs at full speed. With the system operating at such a high frequency, the propagation delay between points (often one-foot intervals) was equal to one clock cycle. This became too large for reliable operation. There were basically two ways to reduce propagation delay, only one of which was acceptable. Reducing the physical space between the chips would have solved the problem but there were too many chips on-board to make this solution feasible. Also, such high-frequency chips must occupy specific positions on the board and cannot be moved closer together simply to eliminate delays. The only other possible solution was to change the type of pc-board material.

Instead of epoxy, which is often used, the VG-2048 was made out of a combination of materials, with a far better dielectric constant than epoxy. This change in material improved the propagation delay between points.

Moving to 2K × 2K represents a major jump in high-end graphics processors, but the trend to ever higher resolution and performance will undoubtedly continue. Matrox's 2K × 2K controller was designed to meet specific needs for a high-end product. It will only be a matter of time before this technology becomes the new resolution standard.

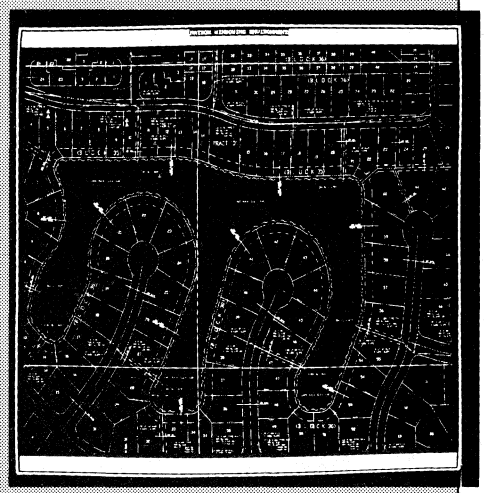


Figure 6: Taken directly from Sony's Corp.'s DDM-2801C 2K × 2K monitor, this image was displayed using Matrox's VG-2048 9U graphics board. Capable of displaying four million pixels simultaneously, the TMS34010-based controller features a 2K- × 2K- × 8-bit frame buffer and 1.5 Mbytes of display list memory.

four lower-order bits of each pixel. Therefore, an overlay enable signal can override the normal image.

RAMDAC Role

Both the even and odd pixel data streams feed three Bt492 RAMDACs. Each RAMDAC accepts the dual data stream into separate color LUTs. Outputs of the dual LUTs are then combined by a 2:1 on-board multiplexer. This multiplexer outputs an 8-bit 360-MHz stream of data to the on-chip DAC driving the CRT. The RAMDAC also accepts an overlay input associated with each byte received. Dual on-chip 16 × 8 overlay memory overrides the normal color LUT when the overlay input is active. The lower 4 bits of the pixel data input provide the index into the overlay-memory LUT.

Eight planes of image memory can be used to display 256 colors. However, the 256 × 8 LUTs offer a palette of 16.8M. Thus, the Bt424 and Bt492 can be used to implement true-color display systems. For example, a design that includes eight planes of memory per color in the frame buffer can display 16.8M colors out of a palette of 16.8M.

Using eight planes per color also requires a set of shift registers dedicated to each color, with each set of shift registers feeding separate RAMDACs. Such designs therefore require triple the number of VRAM and shift register ICs compared to the example here. Interconnections of the frame buffer, shift registers, and RAMDACs, however, will remain the same.

VLSI ECL ICs offer several advantages. In the example shown, five shift-register ICs were used. Other available ECL shift registers only handle 8 bits. Therefore, similar designs would require 36 shift-register ICs. Using the Brooktree Bt424 results in lower parts cost, more board space, and a simpler layout. Brooktree's Bt492 RAMDAC features dual 180-MHz inputs, an on-board multiplexer to increase bandwidth to 350 MHz, the 180-MHz dual-color LUTs, and a 350-MHz DAC.

Implementing the controller with the Bt424 and Bt492 provides a clear cost advantage over controllers implemented with semicustom ICs. Functional features key to 2K × 2K display systems include support for a 16-color overlay function used to implement X Windows and TTL interfacing. Furthermore, both ICs can be used in nongraphics applications. Brooktree's Bt424 can serve as a general-purpose fast ECL shift register while the Bt492 can be used as a 512- × 8-bit transcendental DAC for synthesizing sinusoids. **ESD:**

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GRAPHICS

AND IMAGING PRODUCTS

APPLICATIONS HANDBOOK 1990

Brooktree®

This collection of international standards provides concise descriptions of some common video and image transmission formats. Each document contains the essential signal and coding parameters necessary for the designer who must interface to transmission protocols.

The Electronic Industry Association (EIA) publishes bulletins, recommendations and standards applicable to broadcast television and display systems. The RS-170 monochrome standard, which was updated to the composite chrominance subcarrier "A" version, describes the common video interface for NTSC format television. The RS-330 and RS-343 standards describe camera interfaces for raster scan formats ranging from 525 lines to 1024 lines; the parameters are also widely applied to component RGB computer graphics interfaces.

The International Telecommunications Union (ITU) is the governing body of several committees, including the Consultative Committee of International Radio (CCIR). The recommendation CCIR 601-1 defines the digital encoding standards for television signals, report CCIR 624-3 lists the electrical specifications for worldwide broadcast television signals.

Component Analog equipment usually has individual hardware requirements and has not been widely adopted by standards agencies, although manufacturers usually provide specific parameters in their literature. The newest HDTV production standards (such as SMPTE 240M) present some unique interface requirements (like Tri-Level Sync), but are not yet universally accepted and, hence, not included. For the international equipment designers, the CCIR 624 report summarizes the fourteen television formats to be found worldwide.

With the advent of digital video transmission, the problems of conflicting video formats came together in the CCIR 601 recommendation, which also described desirable filtering limits. This was the basis for the D1 (SMPTE) Digital Component Video Tape Recorder interface, which has evolved into the lower cost Composite Digital Video Tape Recorder interface D2 (SMPTE 244M). The serial transmission of CCIR 601 protocol digital video has been covered in CCIR 656, but adoption of uniform coding schemes for DC noise tolerance has not resulted in wide standardization.

Other agencies that publish relevant standards are the European Broadcast Union (EBU), the Society of Motion Picture and Television Engineers (SMPTE), and the Institute of Electronic and Electrical Engineers (IEEE). An address reference list of these agencies is provided at the end of this section.

T A B L E O F C O N T E N T S

ELECTRICAL PERFORMANCE STANDARDS FOR HIGH RESOLUTION MONOCHROME CLOSED CIRCUIT TELEVISION CAMERA

(From EIA Standard RS-343 and Standards Proposal No. 1025 formulated under the cognizance of EIA Committee TR-17 on Closed Circuit Television.)

1. INTRODUCTION

The Electrical Performance Standards for High Resolution Monochrome Closed Circuit Television Equipment given here represent, it is believed, the best agreement between the members of the Closed Circuit Television Committee, who drafted these Standards, consistent with the rapidly developing state-of-the-art.

The Standards consist of (1) Definitions, (2) Minimum Standards, and (3) Methods of Measurement, for those parameters believed to be of importance.

These Standards are intended to apply only to locally generated signals; that is, signals generated in the camera itself or at a nearby point where control can be exercised over picture quality.

This Standard is written to encompass equipment which operates in the range from 675 to1023 scanning lines with a field rate of 60 hz, interlaced 2:1. It is understood that special requirements may require different line numbers. It is recommended that one of the following be considered to satisfy particular requirements: 675, 729, 875, 945, or 1023 lines.

The tolerance on any line number in this specification shall be ± 1%.

2. CAMERA OUTPUT - VIDEO

Definition - The camera output terminals are defined as the junction between the camera or switching facilities and the line feeding either a transmission system or a visual display. The camera output signal is that signal which appears across the camera output terminals.

In this document any reference to camera output refers to the output of the camera channel whether it is a single unit or a multi-unit system.

The standard signal which will be discussed below is the signal which appears across the output terminals of the camera when they are connected to the standard load impedance.

The signal which appears across the line feeding either a transmission system or a visual display may be different from the standard signal. This is because the circuit may be equalized on an overall transmission basis and not with a view to keeping the input impedance of the line a specified value.

Under these conditions monitoring measurements made at the output terminals of the camera must be properly interpreted.

2.1 Impedance

Definition - The complex ratio of voltage to current in a two terminal network, expressed in ohms.

Minimum Standard - The standard load impedance of the camera output shall have a value of 75 ohms ± 5% over the frequency range of 0 to 10 MHz and shall be connected for single-ended operation.

Method of Measurement - It is recomennded that the load impedance for the camera be measured by means of impedance bridges capable of an accuracy of ± 1% in the vicinity of 75 ohms.

2.2 Direct Current in Output

Minimum Standard - The open-circuit DC voltage of the camera output shall not exceed 2 volts. The short-circuit DC current shall not exceed 2 milliamperes. These DC values are presumed to be independent of the output signal.

Method of Measurement - The open-circuit DC voltage should be measured with a voltmeter of at least 20,000 ohms per volt. The short-circuit DC current should be measured with a milliammeter of, at most, 10 ohms internal resistance.

2.3 Polarity

Definition - The sense of the potential of a portion of the signal representing a dark area of a scene relative to the potential of a portion of the signal representing a light area. Polarity is stated as "black-negative" or "black-positive".

Standard - The standard polarity of the output of the camera shall be black-negative.

Method of Measurement - It is recommended that signal polarity be measured by means of an oscilloscope of known deflection polarity.

2.4 Composite Picture Signal*

Definitions:

Picture Signal - The signal resulting from the scanning process.

Sync Signal - The signal employed for the synchronization of scanning.

Sync Level - The level of the peaks of the sync signal.

Blanking Level - That level of a composite picture signal which separates the range containing picture information from the range containing synchronizing information. (This term should be used for controls performing this function.)

Black Peak - A peak excursion of the picture signal in the black direction.

White Peak - A peak excursion of the picture signal in the white direction.

Reference White Level - The picture signal level corresponding to a specified maximum limit for white peaks.

Reference Black Level - The picture signal level corresponding to a specified maximum limit for black peaks.

Setup - In television, the ratio between reference black level and reference white level both measured from blanking level. It is usually expressed in percent. (This is equivalent to the difference in level between reference black level and blanking level, expressed in IRE units).

*Measurement of signal levels shall be made in accordance with 58 IRE 23.S1, IRE Standards on Television: Measurement of Luminance Signal Levels, 1958 or latest revision thereof. This standard defines the levels of a Television signal in terms of IRE units. Reference white level is + 100 IRE units; blanking level is 0 IRE units; sync level is - 40 IRE units. Thus the peak-to-peak level of a signal extending from reference white to sync tip is 140 IRE units.

Composite Picture Signal - The signal which results from combining a blanked picture signal with the sync signal.

Blanked Picture Signal - The signal resulting from blanking a picture signal. (This signal may or may not contain setup. (A blanked picture signal with setup is commonly called a non-composite signal.)

Level (in television)

Signal amplitude measured in accordance with specified techniques.

A specified position on an amplitude scale applied to a signal waveform.

Standard - It shall be standard that the blanked picture signal with setup (non-composite), as measured from blanking level to reference white level across the standard load impedance of the camera, be 0.714 ± 0.1 volt (100 IRE units).

It shall be standard that the synchronizing signal as measured across the standard load impedance of the camera be 0.286 ± 0.05 volts (nominally 40 + IRE units).

It shall be standard that the setup be 7.5 ± 5 IRE units (2.5% to 12.5% of the blanked picture signal).

Method of Measurement - It is recommended that the signal voltage output of the camera be measured by means of an oscilloscope capable of measuring such a signal with an accuracy of ± 2% of the actual value over the voltage range of 0.2 to 1.5 volts. The oscilloscope should incorporate a linear scale having a zero line which can be alligned with blanking level and divisions extending to at least 100 in the white direction and to at least 50 in the black direction. Some means of calibration should be provided so that signal level measurements can be made in volts as well as in IRE units.

HIGH RESOLUTION TV SYSTEM PARAMETERS

Lines/ Frame	(1) Active Lines	(2) Ver. Res R_V	(3) f_h KHz	(4) t_h µsecs	(5) t_{ha} µsecs	Fundamental Generated Frequency (MHz) (8)							
						R_hMhz (6)		$R_h = R_V$ (9)		R_h = 800 lines		R_h = 1000 lines	
						4:3(7)	1:1	4:3	1:1	4:3	1:1	4:3	1:1
675	624	425	20.25	49.38	42.38	63.6	84.8	6.69	5.01	12.6	9.44	15.7	11.8
729	674	475	21.87	45.72	38.72	58.1	77.4	8.18	6.13	13.8	10.3	17.2	12.9
875	809	575	26.25	38.09	31.09	46.6	62.2	12.3	9.25	17.2	12.9	21.4	16.1
945	874	600	28.35	35.27	28.27	42.4	56.5	14.1	10.6	18.9	14.1	23.6	17.7
1023	946	650	30.69	32.58	25.58	38.4	51.2	16.9	12.7	20.8	15.6	26.1	19.5

Vertical Blanking = 1250 µsecs nominal.
Horizontal Blanking = 7 µsecs nominal.

NOTES:

1. Active Lines = Lines / Frame less those occurring during vertical blanking.
2. Vertical Resolution = Active Lines times Kell Factor (0.7). Vertical Resolution rounded to nearest 25 lines.
3. f_h = Horizontal scanning frequency.
4. t_h = Total horizontal line time.
5. t_{ha} = Total active horizontal line time (t_h - 7 µsecs.)
6. R_h/MHz = Lines of horizontal resolution per MHz of bandwidth.
7. Aspect Ratio.
8. Fundamental generated frequency required to provide indicated resolution in lines per picture height.
9. Fundamental generated frequency required to provide horizontal resolution equal to vertical resolution.

COMPOSITE VIDEO WAVEFORM
HIGH RESOLUTION MONOCHROME TELEVISION CAMERA

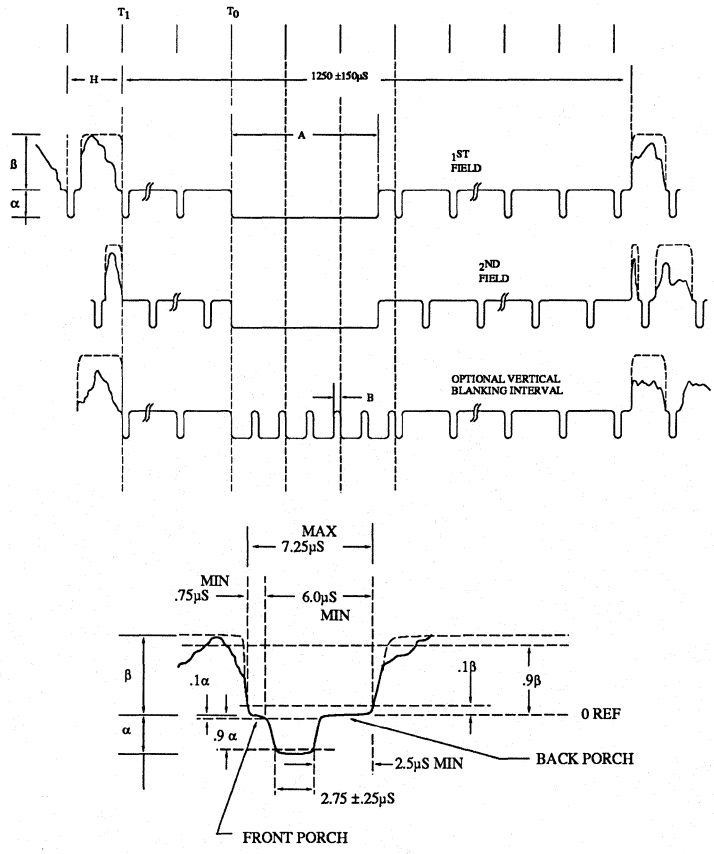


FIGURE 1

NOTES:

1. ß = 0.714 ± 0.1 volt (100 IRE Units)
2. α = 0.286 (40 IRE Units) nominal.
3. Sync to total signal ratio (α/(ß + α)) = 28.6 ± 5%
4. Blanking = 7.5 ± 5 IRE Units (2.5% to 12.5% of ß)
5. Horizontal Rise Times measured from 10% to 90% amplitudes shall be less than 0.1µ/s.
6. Overshoot on horizontal blanking signal shall not exceed 0.02ß at beginning of front porch and 0.05ß at end of back porch.
7. Overshoot on sync signal shall not exceed 0.05ß.
8. T_0 = start of vertical sync pulse.
9. T_1 = start of vertical blanking.
10. $T_1 = T_0 \begin{matrix} +0 \\ -250\,\mu s \end{matrix}$
11. A - vertical sync pulse = 125 ± 50µ/s measured between 90% amplitude points.
12. Rise and fall times of vertical blanking and vertical sync pulse, measured from 10% to 90% amplitudes, shall be less than 5µ/s.
13. Tilt on vertical sync pulse shall be less than 0.1a.
14. If horizontal information is provided during the vertical sync pulse it must be at 2H frequency and as shown in the optional vertical blanking interval waveform.
15. B - vertical serration = 2 ± .5µ/s measured between the 90% amplitude points. Rise time measured from 10% to 90% amplitudes shall be less than 0.1µ/s.
16. If equalizing pulses are used in the vertical blanking interval waveforms they shall be 6 in number preceding and following the vertical sync pulse, be at 2H frequency and 1/2 the width of H sync pulse.
17. It is recommended that for proper interlace the time duration between the leading edge of vertical sync and the leading edge of horizontal sync be a multiple of H/2.

ELECTRICAL PERFORMANCE STANDARDS FOR CLOSED CIRCUIT TELEVISION CAMERA 525/60 INTERLACED 2:1

(From Standards Proposal No. 900 Formulated under the cognizance of EIA Committee TR-17 on Closed Circuit Television.)

1. Introduction

The Electrical Performance Standards for Closed Circuit Television Camera given here represent, it is believed, the best agreement between the members of the Closed Circuit Television Committee, who drafted these Standards, consistent with the rapidly developing state-of-the-art.

(The term "camera" as used in this document may include a single or multiple unit camera chain.)

The Standards consist of (1) Definitions, (2) Standards, and (3) Methods of Measurement, for those parameters believed to be of importance.

These Standards are intended to apply only to locally generated signals; that is, signals generated in the camera itself or at a nearby point where control can be exercised over picture quality. They are not intended to apply to equipment described by EIA Standard, RS-170, Electrical Performance Standards - Monochrome Television Studio Facilities, November 1957, or revision thereof.

2. CAMERA OUTPUT - VIDEO

Definition - The camera output terminals are defined as the junction between the camera or switching facilities and the line feeding either a transmission system or a visual display. The camera output signal is that signal which appears across the camera output terminals.

The standard signal which will be discussed below is the signal which appears across the output terminals of the camera when they are connected to the standard load impedance.

The signal which appears across the line feeding either a transmission system or a visual display may be different from the standard signal. This is because the circuit may be equalized on an overall transmission basis and not with a view to keeping the input impedance of the line a specified value.

Under these conditions, monitoring measurements made at the output terminals of the camera must be properly interpreted.

2.1 Load Impedance

Definition - The complex ratio of voltage to current in a two terminal network, expressed in ohms.

Standard - The standard load impedance of the camera output shall have a value of 75 ohms ± 5% over the frequency range of the camera and shall be connected for single-ended operation.

Method of Measurement - It is recommended that the load impedance for the camera be measured by means of impedance bridges capable of an accuracy of ± 1% in the vicinity of 75 ohms.

2.2 Direct Current in Output

Standard - The open-circuit DC voltage of the camera output shall not exceed ± 2 volts. The short-circuit DC current shall not exceed 2 milliamperes. These DC values are presumed to be independent of the output signal. (These values chosen are to facilitate interconnection of various pieces of equipment in the system.)

Method of Measurement - The open-circuit DC voltage should be measured with a voltmeter of at least 20,000 ohms per volt. The short-circuit DC current should be measured with a milliammeter of, at most, 10 ohms internal resistance.

2.3 Polarity

Definition - The sense of the potential of a portion of the signal representing a dark area of a scene relative to the potential of a portion of the signal representing a light area. Polarity is stated as "black-negative" or "black-positive".

Standard - The standard polarity of the output of the camera shall be black-negative.

Method of Measurement - It is recommended that signal polarity be measured by means of an oscilloscope of known deflection polarity.

2.4 Composite Picture Signal*

Definitions:

Picture Signal - The signal resulting from the scanning process.

Sync Signal - The signal employed for the synchronization of scanning.

Sync Level - The level of the peaks of the sync signal.

Blanking Level - That level of a composite picture signal which separates the range containing picture information from the range containing synchronizing information. (This term should be used for controls performing this function.)

Black Peak - A peak excursion of the picture signal in the black direction.

White Peak - A peak excursion of the picture signal in the white direction.

Reference White Level - The picture signal level corresponding to a specified maximum limit for white peaks.

Reference Black Level - The picture signal level corresponding to a specified maximum limit for black peaks.

Setup - In television, the ratio between reference black level and reference white level both measured from blanking level. It is usually expressed in percent. (This is equivalent to the difference in level between reference black level and blanking level, expressed in IRE units).

Composite Picture Signal - The signal which results from combining a blanked picture signal with the sync signal.

Blanked Picture Signal - The signal resulting from blanking a picture signal. (This signal may or may not contain setup. A blanked picture signal with setup is commonly called a non-composite signal.)

Level (in television) - Signal amplitude measured in accordance with specified techniques.
A specified position on an amplitude scale applied to a signal waveform.

Standard - It shall be standard that the blanked picture signal with setup (non-composite), as measured from blanking level to reference white level across the standard load impedance of the camera, be 0.714 $\pm$ 0.1 volt (100 IRE units).

It shall be standard that the synchronizing signal as measured across the standard load impedance of the camera be 0.286 $\pm$ 0.05 volts (nominally 40 + IRE units).

*Measurement of signal levels shall be made in accordance with 58 IRE 23.S1, IRE Standards on Television: Measurement of Luminance Signal Levels, 1958 or latest revision thereof. This standard defines the levels of a television signal in terms of IRE units. Reference white level is + 100 IRE units; blanking level is 0 IRE units; sync level is - 40 IRE units. Thus the peak-to-peak level of a signal extending from reference white to sync tip is 140 IRE units.

It shall be standard that the setup be 7.5 ± 5 IRE units (2.5% to 12.5% of the blanked picture signal).

Method of Measurement - It is recommended that the signal voltage output of the camera be measured by means of an oscilloscope capable of measuring such a signal with an accuracy of ± 2% of the actual value over the voltage range of 0.2 to 1.5 volts. The oscilloscope should incorporate a linear scale having a zero line which can be aligned with blanking level and divisions extending to at least 100 in the white direction and to at least 50 in the black direction. Some means of calibration should be provided so that signal level measurements can be made in volts as well as in IRE units.

SECTION 2.5 PICTURE FIDELITY - DELETED

2.6 SYNC SIGNAL TOLERANCE

Definition - It shall be standard that the synchronizing signal waveform at the output of the picture line amplifier conform with the drawing, Figure #1, Composite Video Waveform, 525/60 Interlaced 2:1.

Standard - It shall be standard that the time of occurrence of the leading edge of any horizontal pulse "N" of any group of twenty horizontal pulses not differ from "NH" by more than 0.001H where "H" is the average interval between the leading edges of horizontal pulses as determined by an averaging process carried out over a period of not less than 20 or more than 100 lines.

It shall be standard that the frequency of horizontal and vertical scanning pulses not vary from the values established by the standards of frame frequency and number of scanning lines by more than ± 1% regardless of variations in frequency of the power source supplying the camera.

Method of Measurement - It is recommended that pulse amplitudes be measured in peak-to-peak volts. This can be done satisfactorily with an oscilloscope and a calibrated comparison signal. Accuracy of measurement should be at least ± 2%. The time of rise is the time required for changing from 10 percent to 90 percent of normal amplitude. The time of decay is the time required for changing from 90 percent to 10 percent amplitude. Peak pulse width shall be the width measured at 90 percent amplitude. Base pulse width shall be the width measured at 10 percent amplitude. Pulse interval measurements shall be made between corresponding 10% points on the pulses. The width of the vertical pulse, as well as the phase relationship between this pulse and the other blanking and synchronizing pulses can be determined by the "pulse cross" method. To do this a monitor is synchronized in such a manner that the vertical blanking bar appears horizontally near the center of the picture and the horizontal blanking bar appears vertically through the center of the picture. A substantial increase in vertical deflection amplitude of the monitor allows details to be seen more easily.

The allowable variations in timing between successive horizontal pulses is measured in terms of percent of a horizontal scanning period. This can be measured on the same monitor used to indicate the "pulse cross" if the horizontal scanning has automatic frequency control with a sufficiently long time constant to give substantially constant frequency over a period of 20 lines.

Accuracy of measurement will depend on the maximum amount of horizontal scanning available, the resolution of the cathode ray tube, and the wave front steepness of the pulses supplied to the grid of the cathode ray tube.

A frequency or a frequency deviation meter with an accuracy of ± 0.1 cycle at 60 cycles or ± 25 cycles at 15,750 cycles can be used for measuring either the frame frequency or the line frequency of the output signal from the picture line amplifier.

COMPOSITE VIDEO WAVEFORM
525/60 INTERLACED 2:1

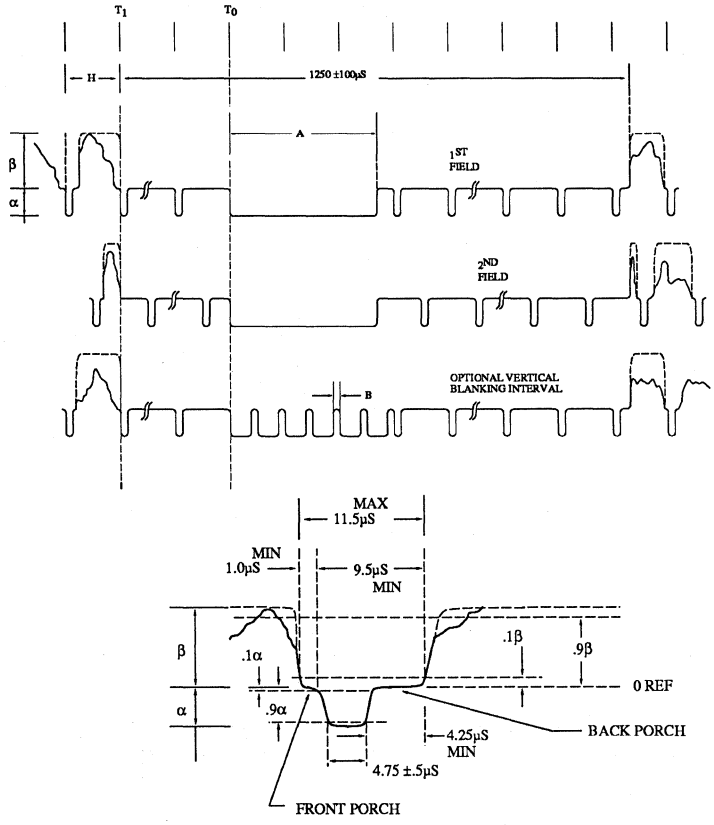


FIGURE 1

NOTES:

1. ß = 0.714 ± .1 volt (100 IRE Units).
2. α = 0.286 (40 IRE Units) nominal.
3. Sync to total signal ratio (α/(ß + α)) = (28.6 ± 5)%.
4. Blanking = 7.5 ± 5 IRE Units (2.5% to 12.5% of ß).
5. Horizontal Rise times measured from 10% to 90% amplitudes shall be less than 0.3µ/s.
6. Overshoot on horizontal blanking signal shall not exceed 0.02ß at beginning of front porch and 0.05ß at end of back porch.
7. Overshoot on sync signal shall not exceed 0.05ß.
8. T_0 = start of vertical sync pulse.
9. T_1 = start of vertical blanking.
10. $T1 = T_0 \begin{matrix} +0 \\ -250\ \mu/s \end{matrix}$
11. A - vertical sync pulse = 150 ± 50µ/s measured between 90% amplitude points.
12. Rise and fall times of vertical blanking and vertical sync pulse, measured from 10% to 90% amplitudes, shall be less than 5µ/s.
13. Tilt on vertical sync pulse shall be less than 0.1
14. If horizontal information is provided during the vertical sync pulse it must be at 2H rate and as shown in the optional vertical blanking interval waveform.
15. B - vertical serration = 4.5 ± .5µ/s measured between the 90% amplitude points. Rise times measured from 10% to 90% amplitudes shall be less than 0.3µ/s.
16. If equalizing pulses are used in the vertical blanking interval waveform they shall be 6 in number preceeding the vertical sync pulse and be at 2H rate.

ELECTRICAL PERFORMANCE STANDARDS MONOCHROME TELEVISION STUDIO FACILITIES

(From Standard TR-135 and Standards Proposal Nos. 475 and 536 formulated under the cognizance of EIA Engineering Committee TR-4 on Television Transmitters)

1. INTRODUCTION

The Electrical Performance Standards for Monochrome Television Studio Facilities given here represent, it is believed, the best agreement between the members of the Television Studio Facilities Sub-committee, who drafted these Standards, consistent with the rapidly developing state of the art.

The Standards consist of (1) Definitions, (2) Minimum Standards, and (3) Methods of Measurement, for those parameters believed to be of importance.

These Standards are intended to apply only to locally generated signals; that is, signals generated in the studio itself or at a nearby point where control can be exercised over picture quality.

2. PICTURE LINE AMPLIFIER OUTPUT

Definition - The picture line amplifier output terminals are defined as the junction between the studio facility and the line feeding either a relay transmitter, a visual transmitter, or a network. The picture line amplifier output signal is that signal which appears across the picture line amplifier output terminals.

The standard signal which will be discussed below is the signal which appears across the output terminals of the picture line amplifier when they are connected to the standard load impedance.

The signal which appears across the line feeding either a relay transmitter, a visual transmitter, or a network may be different from the standard signal. This is because the circuit may be equalized on an overall transmission basis and not with a view to keeping the input impedance of the line a specified value.

Under these conditions monitoring measurements made at the output terminals of the picture line amplifier must be properly interpreted.

2.1 Impedance

Definition - The complex ratio of voltage to current in a two terminal network, expressed in ohms.

Minimum Standard - The standard load impedance of the picture line amplifier shall have a value of 75 ohms ± 5% over the frequency range of 0 to 4.5 MC and shall be connected for single-ended operation.

The internal impedance of the picture line amplifier shall be 75 ohms ± 10% at those frequencies where the impedance of the output condenser (if used) may be neglected. The time constant of the internal impedance combined with the standard load impedance shall be 0.1 second or greater.

Method of Measurement - It is recommended that the load impedance for the picture line amplifier be measured by means of impedance bridges capable of an accuracy of ± 1% in the vicinity of 75 ohms.

The internal impedance of the picture line amplifier should be measured by the resistance variation method. This measurement should be made at the standard output level of the amplifier. The load impedance should be varied from 75 ohms to 50 ohms approximately.

2.2 Direct Current in Output

Minimum Standard - The open-circuit DC voltage of the picture line amplifier output shall not exceed 2 volts. The short-circuit DC current shall not exceed 2 milliamperes. These DC values are presumed to be independent of the output signal.

Method of Measurement - The open-circuit DC voltage should be measured with a voltmeter of at least 20,000 ohms per volt. The short-circuit DC current should be measured with a milliammeter of, at most, 10 ohms internal resistance.

2.3 Polarity

Definition - The sense of the potential of a portion of the signal representing a dark area of a scene relative to the potential of a portion of the signal representing a light area. Polarity is stated as "black-negative" or "black-positive".

Standard - The standard polarity of the picture line amplifier shall be black-negative.

Method of Measurement - It is recommended that signal polarity be measured by means of an oscilloscope of known deflection polarity.

2.4 Composite Picture Signal*

Definitions:

Picture Signal - The signal resulting from the scanning process.

Sync Signal - The signal employed for the synchronization of scanning.

Sync Level - The level of the peaks of the sync signal.

Blanking Level - That level of a composite picture signal which separates the range containing picture information from the range containing synchronizing information.

Black Peak - A peak excursion of the picture signal in the black direction.

White Peak - A peak excursion of the picture signal in the white direction.

Reference White Level - The picture signal level corresponding to a specified maximum limit for white peaks.

Reference Black Level - The picture signal level corresponding to a specified maximum limit for black peaks.

Setup - In television, the ratio between reference black level and reference white level both measured from blanking level. It is usually expressed in percent.

Composite Picture Signal - The signal which results from combining a blanked picture signal with the sync signal.

Blanked Picture Signal - The signal resulting from blanking a picture signal.

Level (in television) - Signal amplitude measured in accordance with specified techniques.
A specified position on an amplitude scale applied to a signal waveform.

Minimum Standard - It shall be standard that the picture signal, as measured from blanking level to reference white level across the standard load impedance of the picture line amplifier, be 1.0 ± 0.05 volt.

**A level of .70 volts for color TV applications has received preliminary approval. Where monochrome equipment is used in the same studio facilities with color equipment, it is expected that both will be adjusted to the .70 volt level. Where monochrome equipment is used by istelf, it may be desirable to continue with the 1.0 volt level that has been standard for some time. The primary intent in reaffirming the 1.0 volt standard is to provide assurance that new monochrome equipment will function properly when used with earlier types of monochrome equipment.*

It shall be standard that the synchronizing signal as measured across the standard load impedance of the picture line amplifier be 40 ± 5% of the picture signal.

It shall be standard that throughout a given transmission the synchronizing signal be maintained constant within ± 4% as measured across the standard load impedance of the picture line amplifier. This variation may take place on a long time basis only and not during successive cycles. The allowable amplitude variation over one frame should be considerably smaller.

The amplitude of blanking level referred to the AC axis of the signal at the picture line amplifier output shall not vary more than ± 5% of the sync signal amplitude during one field. The AC axis of the signal shall be determined by averaging the signals over one field. The sync amplitude is designated as "α" in the drawing entitled "Picture Line Amplifier Standard Output".

It shall be standard that the minimum setup be 7.5 ± 2.5%.

Method of Measurement - It is recommended that the signal voltage output of the picture line amplifier be measured by means of an oscilloscope capable of measuring such a signal with an accuracy of ± 2% of the actual value over the voltage range of 0.2 to 2.0 volts. The oscilloscope should incorporate a linear scale having a zero line which can be alligned with blanking level and divisions extending to at least 100 in the white direction and to at least 50 in the black direction. Some means of calibration should be provided so that signal level measurements can be made in volts as well as sync and other measurements in percent of picture signal. The oscilloscope amplifier characteristics should be such as to introduce negligible measurement errors due to low frequency distortion or overshoot. In order to provide the minimum band-width consistent with satisfactory readings of levels it is recommended that the amplitude response at 3 megacycles be minus 6 plus 2 minus 3db relative to the response at low frequencies, and that the rise time be approximately 0.175 microsecond without overshoots.

SECTION 2.5 PICTURE FIDELITY - DELETED

2.6 SYNC SIGNAL TOLERANCE

Definition - It shall be standard that the synchronizing signal waveform at the output of the picture line amplifier conform with the drawing "Picture Line Amplifier Standard Output".

Miniumum Standard - It shall be standard that the time of occurrence of the leading edge of any horizontal pulse "N" of any group of twenty horizontal pulses not differ from "NH" by more than 0.001H where "H" is the average interval between the leading edges of horizontal pulses as determined by an averaging process carried out over a period of not less than 20 or more than 100 lines.

It shall be standard that the rate of change of frequency of recurrence of the leading edges of the horizontal sync pulses appearing in the picture line amplifier output be not greater than 0.15 percent per second, the frequency to be determined by an averaging process carried out over a period of not less than 20 or more than 100 lines, such lines not to include any portion of the vertical blanking signal.

It shall be standard that the frequency of horizontal and vertical scanning pulses not vary from the values established by the standards of frame frequency and number of scanning lines by more than ± 1% regardless of variations in frequency of the power source supplying the television station.

It shall be standard that the rate of change of frequency and the time interval between successive pulses that has been made standard for the horizontal synchronizing pulses appearing across the output of the picture line amplifier also be standard for the horizontal scanning of the pickup tube.

Method of Measurement - It is recommended that pulse amplitudes be measured in peak-to-peak volts. This can be done satisfactorily with an oscilloscope and a calibrated comparison signal. Accuracy of measurement should be at least ± 2%. The time of rise is the time required for changing from 10 percent to 90 percent of normal amplitude. The time of decay is the time required for changing from 90 percent to 10 percent amplitude. Peak pulse width should be the width measured at 90 percent amplitude. Base pulse width should be the width measured at 10 percent amplitude. The width and the time of rise or decay of pulses should be measured in fractions of the horizontal or vertical scanning period. Pulse interval measurements should be made between corresponding points on the pulses. This can be done with a suitable oscilloscope having timing pulses at appropriate frequencies synchronized with the horizontal trace of the oscilloscope. The accuracy of the timing measurements should be within 0.001H for horizontal frequency pulses and 0.0001V for vertical frequency pulses. The number of equalizing pulses, the width of the vertical pulse, as well as the phase relationship between these pulses and the other blanking and synchronizing

pulses can be determined by the "pulse cross" method. To do this a monitor is synchronized in such a manner that the vertical blanking bar appears horizontally near the center of the picture and the horizontal blanking bar appears vertically through the center of the picture. A substantial increase in vertical deflection amplitude of the monitor allows details to be seen more easily.

The rate of change of frequency of the horizontal and vertical sync pulses should be measured in per cent per second. No satisfactory method seems to be available at the present time to measure this quantity accurately. It is believed possible, however, that a satisfactory instrument somewhat similar to a frequency deviation meter can be built to serve this purpose.

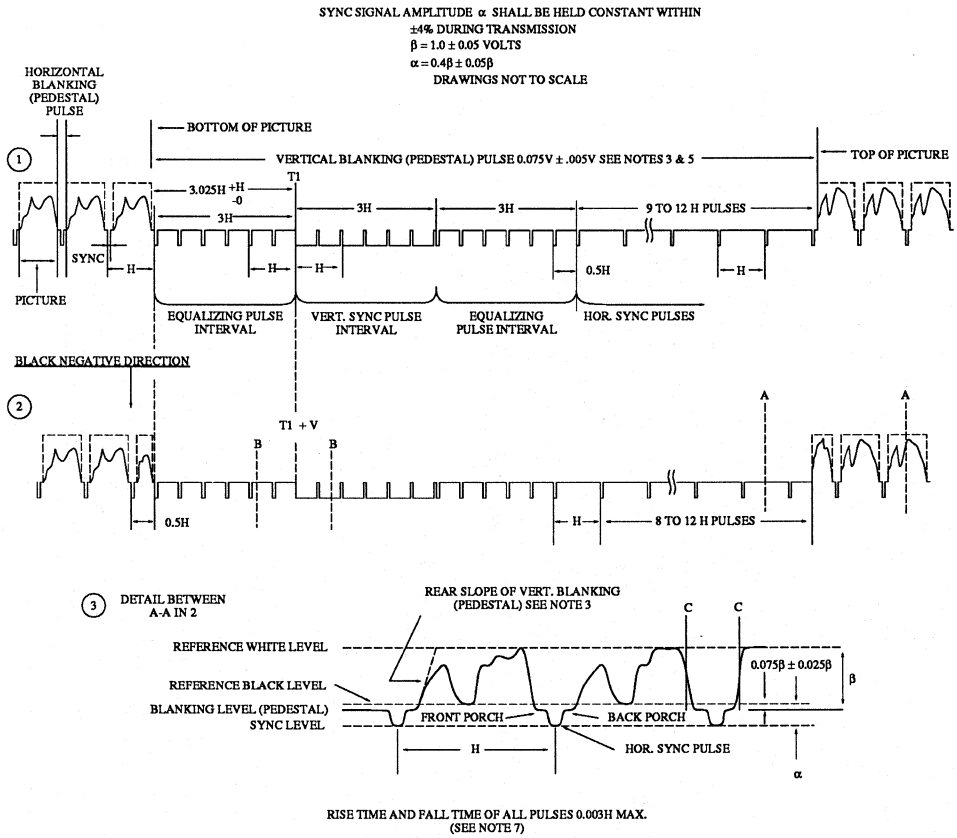
The allowable variations in timing between succesive horizontal pulses is measured in terms of percent of a horizontal scanning period. This can be measured on the same monitor used to indicate the "pulse cross" if the horizontal scanning has automatic frequency control with a sufficiently long constant to give substantially constant frequency over a period of 20 lines.

Accuracy of measurement will depend on the maximum amount of horizontal scanning available, the resolution of the cathode ray tube, and the wave front steepness of the pulses supplied to the grid of the cathode ray tube.

A frequency or a frequency deviation meter with an accuracy of ± 0.1 cycle at 60 cycles or ± 25 cycles at 15,750 cycles can be used for measuring either the frame frequency of the line frequency of the output signal from the picture line amplifier.

The phasing of the vertical blanking signals from two separate sources can be checked on an oscilloscope or a picture monitor by locking in the oscilloscope sweep with one signal and observing the other.

MONOCHROME TELEVISION PICTURE LINE AMPLIFIER STANDARD OUTPUT (VISUAL TRANSMITTER INPUT SIGNAL WAVEFORM)

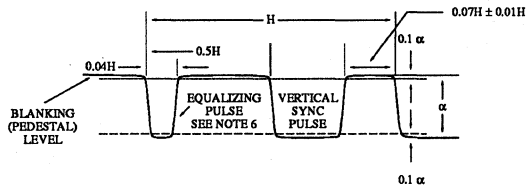


NOTES:

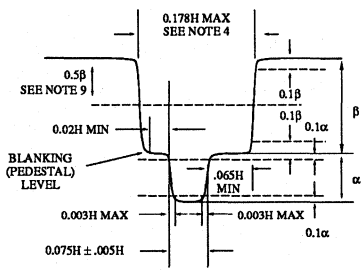
1. H = time from start of one line to start of next line.
2. V = time from start of one field to start of next field.
3. Leading and trailing edges of vertical blanking (pedestal) should be complete in less than 0.1H.
4. Leading and trailing edges of horizontal blanking (pedestal) shall be steep enough to preserve minimum and maximum values of durations under all conditions of picture content.
5. All tolerances and limits shown in this drawing are permissible only for long - time variatons.
6. Equalizing pulse area shall be between 0.45 and 0.5 of the area of a horizontal sync pulse.
7. All rise and decay times shall measure between 0.1 and 0.9 amplitude reference lines.
8. The overshoot on blanking (pedestal) signal shall not exceed 0.02ß at the beginning of the front porch and shall not exceed 0.05ß at the end of the back porch. The overshoot on sync signals shall not exceed 0.05a. Any other extraneous signals on the blanking (pedestal) signal shall not exceed .02ß.
9. For setting aspect ratio, the horizontal blanking (pedestal) duration should be set to 0.175H at the 0.5ß point.
10. Rise time and decay time of horizontal blanking shall not exceed 0.003H.

MONOCHROME TELEVISION PICTURE LINE AMPLIFIER STANDARD OUTPUT (VISUAL TRANSMITTER INPUT SIGNAL WAVEFORM)

④ DETAIL BETWEEN B-B IN 2

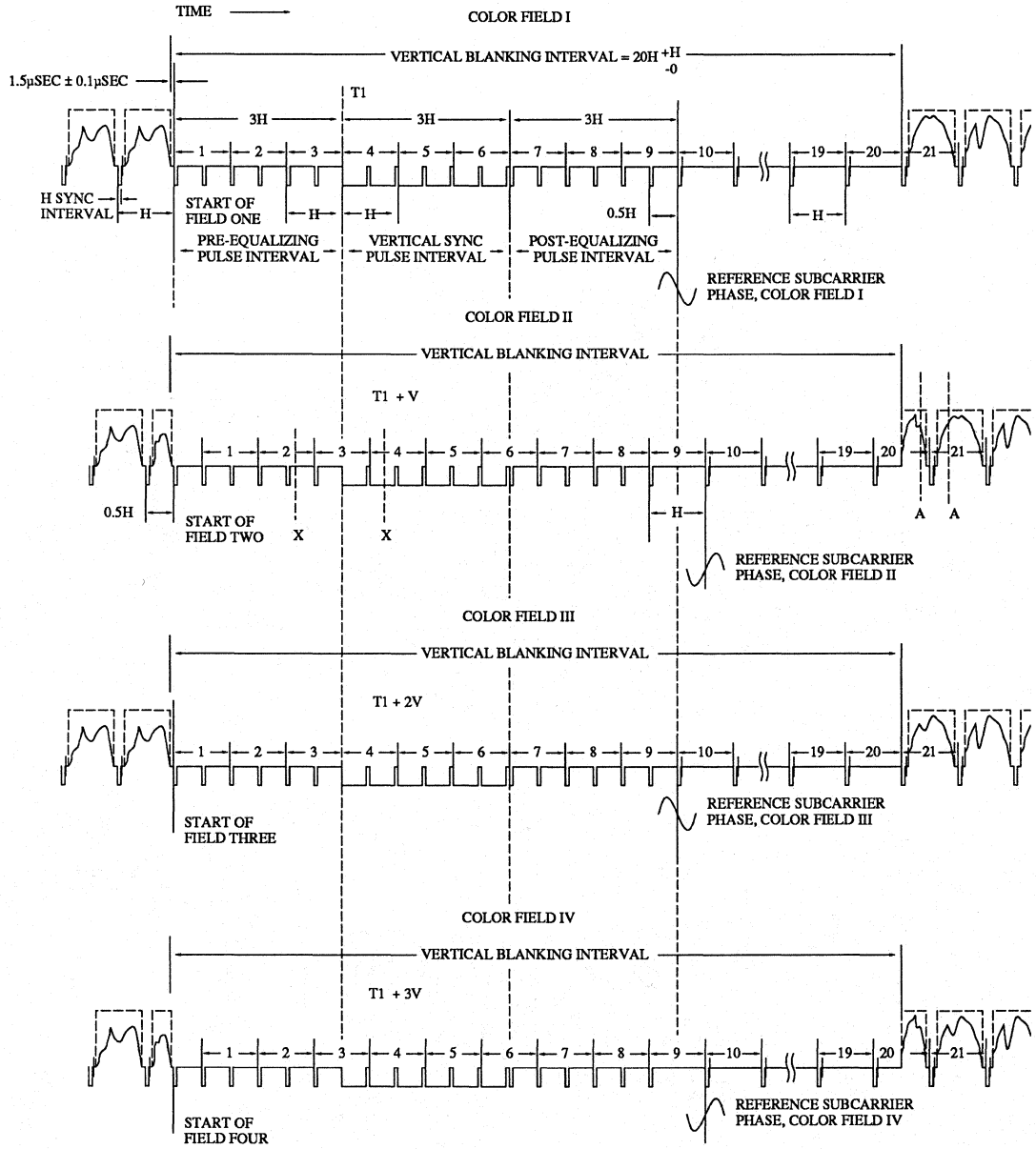


⑤ DETAIL BETWEEN C-C IN 3



RISE TIME AND DECAY TIME OF ALL PULSES 0.003H MAX. (SEE NOTE 7)

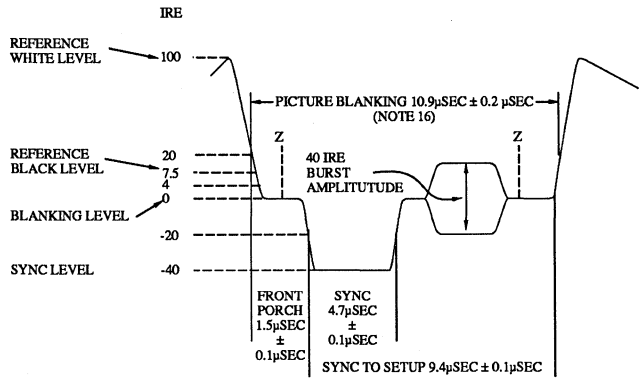
COLOR TELEVISION STUDIO
PICTURE LINE AMPLIFIER OUTPUT
RS 170 A
EIA TENTATIVE STANDARD



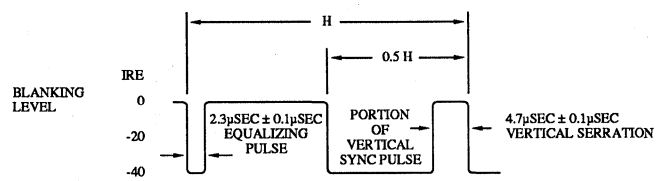
4

COLOR TELEVISION STUDIO
PICTURE LINE AMPLIFIER OUTPUT
RS 170 A
EIA TENTATIVE STANDARD

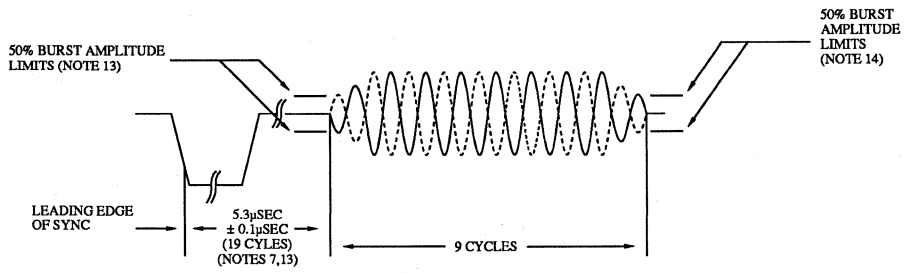
DETAIL Y-Y



DETAIL X-X



DETAIL Z-Z



COLOR TELEVISION STUDIO PICTURE LINE AMPLIFIER OUTPUT RS 170 A EIA TENTATIVE STANDARD

NOTES:

1. Specifications apply to studio facilities. Common carrier, studio to transmitter and transmitter characteristics are not included.

2. All tolerances and limits shown in this drawing permissible only for long time variations.

3. The burst frequency shall be 3.579545MHz ± 10Hz.

4. The horizontal scanning frequency shall be 2/445 times the burst frequency (one scan period (H) = 63.556μ sec).

5. The vertical scanning frequency shall be 2/525 times the horizontal scanning frequency (one scan period (V) = 16.783μ sec).

6. Start of color fields I and III is defined by a whole line between the first equalizing pulse and the preceding H sync pulse. Start of color fields II and IV is defined by a half line between the first equalizing pulse and the preceding H sync pulse. Color field I: that field with positive going zero-crossings of reference subcarrier most nearly coincident with the 50% amplitude point of the leading edges of even numbered horizontal sync pulses. Reference subcarrier is a continuous signal with the same instantaneous phase as burst.

7. The zero - crossings of reference subcarrier shall be nominally coincident with the 50% point of the leading edges of all horizontal sync pulses. For those cases where the relationshop between sync and subcarrier is critical for program integration, the tolerance on this coincidence is ± 40° of reference subcarrier.

8. All rise times and fall times unless otherwise specified are to be 0.14μ sec ± 0.02μ sec measured from 10% to 90% amplitude points. All pulse widths are measured at 90% amplitude points, unless otherwise specified.

9. Tolerance on sync level , reference black level (set up) and peak to peak burst amplitude shall be ± 2 IRE Units.

10. The interval beginning with line 17 and extending through line 20 of each field may be used for test, cue and control signals.

11. Extraneous synchronous signals during blanking intervals, including residual subcarrier, shall not exceed 1 IRE Unit. Extraneous non-synchronous signals during blanking intervals shall not exceed 0.5 IRE Unit. All special purpose signals (VITS,VIR,etc.) when added to the vertical blanking interval are excepted. Overshoot on all pulses during sync and blanking, vertical and horizontal, shall not exceed 2 IRE Units.

12. Burst envelope rise time is 0.3μ sec + 0.2μ sec - 0.1μ sec measured between the 10% and 90% amplitude points. Burst is not present during the nine line vertical interval.

13. The start of burst is defined by the zero-crossing (positive or negative slope) that precedes the first half cycle of subcarrier that is 50% or greater of the burst amplitude. Its position is nominally 19 cycles of subcarrier from the 50% amplitude point of leading edge of sync. (See detail ZZ)

14.The end of burst is defined by the zero-crossing (positive or negative slope) that follows the last half cycle of subcarrier that is 50% or greater of the burst amplitude.

15. Monochrome signals shall be in accordance with this drawing except that burst is omitted, and fields III and IV are identical to fields I and II respectively.

16. Occasionally, measurement of picture blanking at 20 IRE Units is not possible because of scene content as verified on a picture monitor.

Rec. 601-1

SECTION 11F: DIGITAL METHODS OF TRANSMITTING TELEVISION INFORMATION

Recommendations and Reports

RECOMMENDATION 601-1

ENCODING PARAMETERS OF DIGITAL TELEVISION FOR STUDIOS*

(Question 25/11, Study Programmes 25G/11, 25H/11)

(1982-1986)
The CCIR,

CONSIDERING

(a) that there are clear advantages for television broadcasters and programme producers in digital studio standards which have the greatest number of significant parameter values common to 525-line and 625-line systems;

(b) that a world-wide compatible digital approach will permit the development of equipment with many common features, permit operating economies and facilitate the international exchange of programmes;

(c) that an extensible family of compatible digital coding standards is desirable. Members of such a family could correspond to different quality levels, facilitate additional processing required by present production techniques, and cater for future needs;

(d) that a system based on the coding of components is able to meet some, and perhaps all, of these desirable objectives;

(e) that the co-siting of samples representing luminance and colour-difference signals (or, if used, the red, green and blue signals) facilitates the processing of digital component signals, required by present production techniques,

UNANIMOUSLY RECOMMENDS

that the following be used as a basis for digital coding standards for television studios in countries using the 525-line system as well as in those using the 625-line system:

1. Component coding

The digital coding should be based on the use of one luminance and two colour-difference signals (or, if used, the red, green and blue signals).

The spectral characteristics of the signals must be restricted to eliminate aliasing. When using one luminance and two colour-difference signals as defined in Table I, this can be achieved by using filters as defined in Annex III, Figs. 1 and 2. When using E'_R, E'_G, E'_B signals or luminance and colour-difference signals as defined in Table II of Annex I, the characteristics defined by Fig. 1 of Annex III will apply.

Note - The values shown for the luminance filter, used when sampling at 13.5 MHz, given in Fig. 1 of Annex III should be considered as provisional. Administrations are requested to perform urgent studies to confirm these values.

* Main digital television terms used in the Recommendation are defined in Report 629.

2. Extensible family of compatible digital coding standards

The digital coding should allow the establishment and evolution of an extensible family of compatible digital coding standards.

It should be possible to interface simply between any two members of the family.

The member of the family to be used for the standard digital interface between main digital studio equipment, and for international programme exchange (i.e. for the interface with video recording equipment and for the interface with the transmission system) should be that in which the luminance and colour-difference sampling frequencies are related in the ratio 4: 2: 2.

In a possible higher member of the family the sampling frequencies of the luminance and colour-difference signals (or, if used, the red, green and blue signals) could be related by the ratio 4 : 4 : 4. Tentative specifications for the 4 : 4 : 4 member are included in Annex I (see Note).

Note - Administrations are urgently requested to conduct further studies in order to specify parameters of the digital standards for other members of the family. Priority should be accorded to the members of the family below 4 : 2 : 2. The number of additional standards specified should be kept to a minimum.

3. Specifications applicable to any member of the family

3.1 Sampling structures should be spatially static. This is the case, for example, for the orthogonal sampling structure specified in § 4 of the present Recommendation for the 4 : 2 : 2 member of the family.

3.2 If the samples represent luminance and two simultaneous colour-difference signals, each pair of colour-difference samples should be spatially co-sited. If samples representing red, green and blue signals are used they should be co-sited.

3.3 The digital standard adopted for each member of the family should permit world-wide acceptance and application in operation; one condition to achieve this goal is that, for each member of the family, the number of samples per line specified for 525-line and 625-line systems shall be compatible (preferably the same number of samples per line).

4. Encoding parameter values for the 4 : 2 : 2 member of the family

The following specification (Table I) applies to the 4 : 2 : 2 member of the family, to be used for the standard digital interface between main digital studio equipment and for international programme exchange.

TABLE I - *Encoding parameter values for the 4: 2: 2 member of the family*

Parameters	525-line, 60 field/s (1) systems	625-line, 50 field/s (1) systems
1. Coded signals: Y, C_R, C_B	These signals are obtained from gamma pre-corrected signals, namely: E'_Y, $E'_R - E'_Y$, $E'_B - E'_Y$ (Annex II, § 2 refers)	
2. Number of samples per total line: - luminance signal - each colour-difference signal (C_R, C_B)	858 429	864 432
3. Sampling structure	Orthogonal, line, field and frame repetitive. C_R and C_B samples co-sited with odd (1st, 3rd, 5th, etc.) Y samples in each line.	
4. Sampling frequency - luminance signal - each colour-difference signal	13.5 MHz (2) 6.75 MHz (2) The tolerance for the sampling frequencies should coincide with the tolerance for the line frequency of the relevant colour television standard	
5. Form of coding	Uniformly quantized PCM, 8 bits per sample, for the luminance signal and each colour-difference signal	
6. Number of samples per digital active line: - luminance signal -each colour-difference signal	720 360	
7. Analog-to-digital horizontal timing relationship: - from end of digital active line to 0_H	16 luminance clock periods	12 luminance clock periods
8. Correspondence between video signal levels and quantization levels: - scale - luminance signal - each colour-difference signal	0 to 255 220 quantization levels with the black level corresponding to level 16 and the peak white level corresponding to level 235. The signal level may occasionally excurse beyond level 235 225 quantization levels in the centre part of the quantization scale with zero signal corresponding to level 128	
9. Code-word usage	Code-words corresponding to quantization levels 0 and 255 are used exclusively for synchronization. Levels 1 to 254 are available for video	

(1) See Report 624, Table I.

(2) The sampling frequencies of 13.5 MHz (luminance) and 6.75 MHz (colour-difference) are integer multiples of 2.25 MHz, the lowest common multiple of the line frequencies in 525/60 and 625/50 systems, resulting in a static orthogonal sampling pattern for both.

ANNEX I

TENTATIVE SPECIFICATION OF THE 4 : 4 : 4 MEMBER OF THE FAMILY

This Annex provides for information purposes a tentative specification for the 4 : 4 : 4 member of the family of digital coding standards.

The following specification could apply to the 4 : 4 : 4 member of the family suitable for television source equipment and high quality video signal processing applications.

TABLE II - *A tentative specification for the 4 : 4 : 4 member of the family*

Parameters	525-line, 60 field/s systems	625-line, 50 field/s systems
1. Coded signals: Y, C_R, C_B or R, G, B	These signals are obtained from gamma pre-corrected signals, namely: E'_Y, E'_R - E'_Y, E'_B - E'_Y or E'_R, E'_G, E'_B	
2. Number of samples per total line for each signal	858	864
3. Sampling structure	Orthogonal, line, field and frame repetitive. The three sampling structures to be coincident and coincident also with the luminance sampling structure of the 4 : 2 : 2 member.	
4. Sampling frequency for each signal	13.5 MHz	
5. Form of coding	Uniformly quantized PCM. At least 8 bits per sample	
6. Duration of the digital active line expressed in number of samples	At least 720	
7. Correspondence between video signal levels and the 8 most significant bits (MBS) of the quantization level for each sample:		
- scale	0 to 255	
- R, G, B or luminance signal (1)	220 quantization levels with the black level corresponding to level 16 and the peak white level corresponding to level 235. The signal level may occasionally excurse beyond level 235	
- each colour-difference signal (1)	225 quantization levels in the centre part of the quantization scale with zero signal corresponding to level 128	

(1) If used.

ANNEX II

DEFINITION OF SIGNALS USED IN THE DIGITAL CODING STANDARDS

1. Relationship of digital active line to analogue sync. reference

The relationship between 720 digital active line luminance samples and the analogue aynchronizing references for 625-line and 525-line systems is shown below.

TABLE III

525-line, 60 field/s systems	122 *T*	720 *T*	16 *T*	
	0_H (leading edge of line syncs., half-amplitude reference)	Digital active-line period		Next line 0_H
625-line, 50 field/s systems	132 *T*	720 *T*	12 *T*	

T : one liminance sampling clock period (74 ns nominal).

The respective numbers of colour-difference samples can be obtained by dividing the number of luminance samples by two. The (12, 132) and (16, 122) were chosen symmetrically to dispose of the digital active line about the permitted variations. They do not form part of the digital line specification and relate only to the analogue interface.

4

2. Definition of the digital signals Y, C_R, C_B, from the primary (analogue) signals E'_R, E'_G and E'_B

This section describes, with a view to defining the signals Y, C_R, C_B, the rules for construction of these signals from the primary analogue signals E'_R, E'_G and E'_B. The signals are constructed by following the three stages described in § 2.1, 2.2 and 2.3 below. The method is given as an example, and in practice other methods of construction from these primary signals of other analogue or digital signals may produce identical results. An example is given in § 2.4.

2.1 *Construction of luminance (E'_Y) and colour-difference ($E'_R - E'_Y$) and ($E'_B - E'_Y$) signals*

The construction of luminance and colour-difference signals is as follows:

$$E'_Y = 0.299\,E'_R + 0.587E'_G + 0.114\,E'_B \quad \text{(See Note)}$$

whence:

$$(E'_R - E'_Y) = E'_R - 0.299E'_R - 0.587E'_G - 0.114E'_B$$
$$= 0.701E'_R - 0.587E'_G - 0.114E'_B$$

and:

$$(E'_B - E'_Y) = E'_B - 0.299E'_R - 0.587E'_G - 0.114E'_B$$
$$= -0.299E'_R - 0.587E'_G + 0.886E'_B$$

Note - Report 624 Table II refers.

Taking the signal values as normalized to unity (e.g., 1.0 V maximum levels), the values obtained for white, black and the saturated primary and complimentary colours are as follows:

TABLE IV

Condition	E'_R	E'_G	E'_B	E'_Y	$E'_R - E'_Y$	$E'_B - E'_Y$
White	1.0	1.0	1.0	1.0	0	0
Black	0	0	0	0	0	0
Red	1.0	0	0	0.299	0.701	- 0.299
Green	0	1.0	0	0.587	- 0.587	- 0.587
Blue	0	0	1.0	0.114	- 0.114	0.886
Yellow	1.0	1.0	0	0.886	0.114	- 0.886
Cyan	0	1.0	1.0	0.701	- 0.701	0.299
Magenta	1.0	0	1.0	0.413	0.587	0.587

2.2 *Construction of re-normalized colour-difference signals (E'_{CR} and E'_{CB})*

Whilst the values for E'_Y have a range of 1.0 to 0, those for ($E'_R - E'_Y$) have a range of + 0.701 to - 0.701 and for ($E'_B - E'_Y$) a range of + 0.886 to - 0.886. To restore the signal excursion of the colour-difference signals to unity (i.e. + 0.5 to - 0.5), coefficients can be calculated as follows:

$$K_R = (0.5 / 0.701) = 0.713; K_B = (0.5 / 0.886) = 0.564$$

Then:

$$E'_{CR} = 0.713\ (E'_B - E'_Y) = 0.500\,E'_R - 0.419E'_G - 0.081E'_B$$

and:

$$E'_{CB} = 0.564\ (E'_B - E'_Y) = -0.169E'_R - 0.331E'_G + 0.500E'_B$$

where E'_{CR} and E'_{CB} are the re-normalized red and blue colour-difference signals respectively (see Notes 1 and 2).

Note 1. - The symbols E'_{CR} and E'_{CB} will be used only to designate re-normalized colour-difference signals, i.e. having the same nominal peak-to-peak amplitude as the luminance signal E'_Y, thus selected as the reference amplitude.

Note 2. - In circumstances when the component signals are not normalized to a range of 1 to 0, for example, when converting from analogue component signals with unequal luminance and colour-difference amplitudes, and additional gain factor will be necessary and the gain factors K_R , K_B should be modified accordingly.

2.3 *Quantization*

In the case of a uniformly-quantized 8-bit binary encoding, 2^8, i.e. 256, equally spaced quantization levels are specified, so that the range of the binary numbers available is from 0000 0000 to 1111 1111 (00 to FF in hexadecimal notation), the equivalent decimal numbers being 0 to 255, inclusive.

In the case of the 4 : 2 : 2 system described in this Recommendation, levels 0 and 255 are reserved for synchronization data, while levels 1 to 254 are available for video.

Given that the luminance signal is to occupy only 220 levels, to provide working margins, and that black is to be at level 16, the decimal value of the luminance signal, Y, prior to quantization, is:

$$Y = 219\,(E'_Y) + 16,$$

and the corresponding level number after quantization is the nearest integer value.

Similarly, given that the colour-difference signals are to occupy 225 levels and that the zero level is to be level 128, the decimal values of the colour-difference signals, C_R and C_B, prior to quantization are:

$$C_R = 224\,[0.713\,(E'_R - E'_Y)] + 128$$

and:

$$C_B = 224\,[0.564\,(E'_B - E'_Y)] + 128$$

which simplify to the following:

$$C_R = 160\,(E'_R - E'_Y)] + 128$$

and:

$$C_B = 126\,(E'_B - E'_Y)] + 128$$

and the corresponding level number, after quantization, is the nearest integer value.

The digital equivalents are termed Y, C_R and C_B.

2.4 *Construction of Y, C_R, C_B via quantization of E'_R, E'_G, E'_B*

In the case where the components are derived directly from the gamma pre-corrected component signals E'_R, E'_G, E'_B, or directly generated in digital form, then the quantization encoding shall be equivalent to:

$$E'_{RD} \text{ (in digital form)} = \text{int}\,(219\,E'_R) + 16$$

$$E'_{GD} \text{ (in digital form)} = \text{int}\,(219\,E'_G) + 16$$

$$E'_{BD} \text{ (in digital form)} = \text{int}\,(219\,E'_B) + 16$$

Then:

$$Y = (77/256)\,E'_{RD} + (150/256)\,E'_{GD} + (29/256)\,E'_{BD}$$

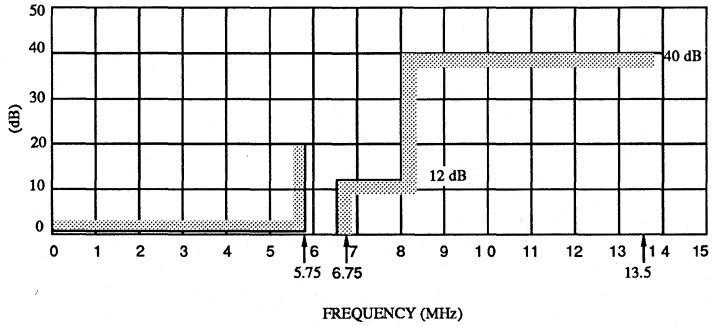
$$C_R = (131/256)E'_{RD} - (110/256)\,E'_{GD} - (21/256)\,E'_{BD} + 128$$

$$C_B = -(44/256)\,E'_{RD} - (87/256)\,E'_{GD} + (131/256)\,E'_{BD} + 128$$

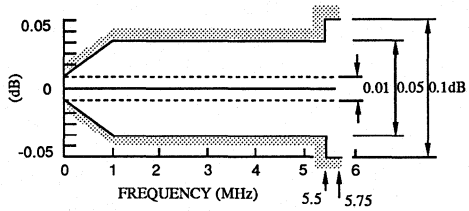
taking the nearest integer coefficients, base 256. To obtain the 4 : 2 : 2 components Y, C_R, C_B , low-pass filtering and sub-sampling must be performed on the 4 : 4 : 4 C_R, C_B signals described above. Note should be taken that slight differences could exist between C_R, C_B components derived in this way and those derived by analogue filtering prior to sampling.

ANNEX III

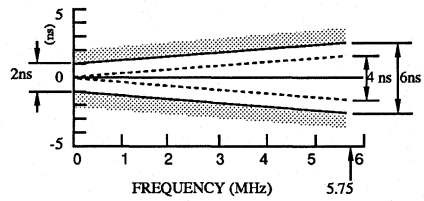
FILTERING CHARACTERISTICS



a) Template for insertion loss / frequency characteristic



b) Passband ripple tolerance

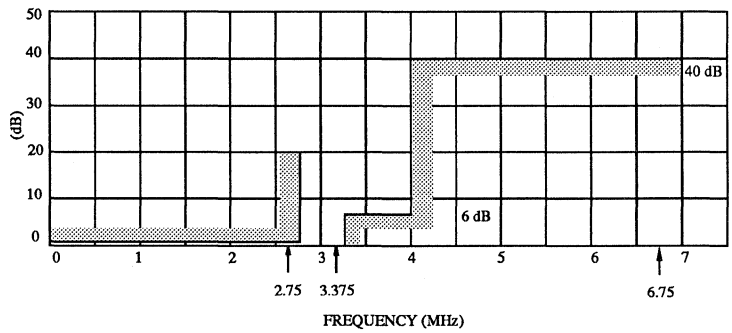


c) Passband group-delay tolerance

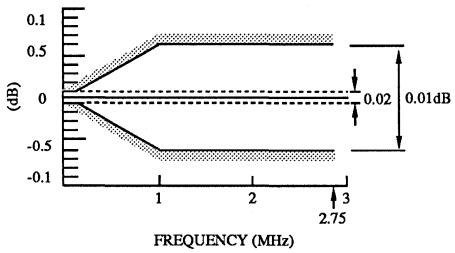
FIGURE 1 - *Specification for a luminance or RGB signal filter used when sampling at 13.5 MHz*

Note. - The lowest indicated values in *b)* and *c)* are for 1 kHz (instead of 0 MHz).

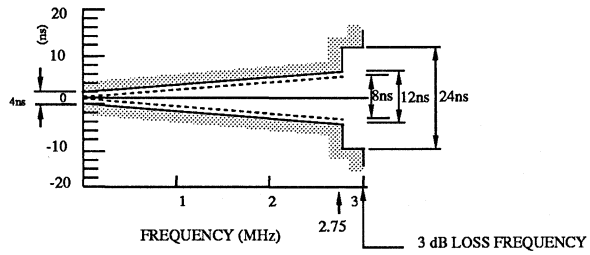
4



a) Template for insertion loss / frequency characteristic



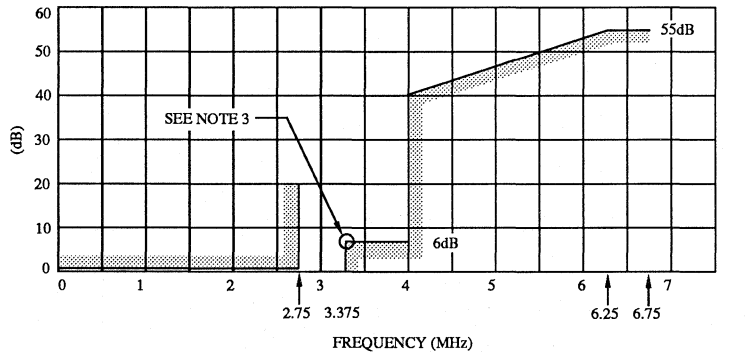
b) Passband ripple tolerance



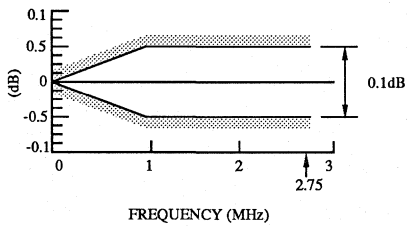
c) Passband group-delay tolerance

FIGURE 2 - *Specification for a colour-difference signal filter used when sampling at 6.75 MHz*

Note. - The lowest indicated values in *b)* and *c)* are for 1 kHz (instead of 0 MHz).



a) Template for insertion loss / frequency characteristic



b) Passband ripple tolerance

FIGURE 3 - *Specification for a digital filter for sampling-rate conversion from 4 : 4 : 4 to 4 : 2 : 2 colour-difference signals*

Notes to Figs. 1, 2 and 3:

Note 1. - Ripple and group delay are specified relative to their values at 1 kHz. The full lines are practical limits and the dashed lines give suggested limits for the theoretical design.

Note 2. - In the digital filter, the practical and design limits are the same. The delay distortion is zero, by design.

Note 3. - In the digital filter (Fig. 3), the amplitude / frequency characteristic (on linear scales) should be skew-symmetrical about the half-amplitude point, which is indicated on the figure.

Note 4. - In the proposals for the filters used in the encoding and decoding processes, it has been assumed that, in the post-filters which follow digital-to-analogue conversion, correction for the (sin x/x) characteristic of the sample-and-hold circuits is provided.

SECTION 11A: CHARACTERISTICS OF SYSTEMS FOR MONOCHROME AND COLOUR TELEVISION

Recommendations and Reports

Report 624-3

CHARACTERISTICS OF TELEVISION SYSTEMS

(1974 - 1978 - 1982 - 1986)

The following Tables, given for information purposes, contain details of a number of different television systems in use at the time of the XVIth Plenary Assembly of the CCIR, Dubrovnik, 1986.

A list of countries and geographical areas, and the television systems used, are given in Annex I.

Specifications of the SECAM IV colour television system, which is still under consideration, are given in Annex II.

TABLE I - *Basic characteristics of video and synchronizing signals.*

Item	Characteristics		System								
			M	N	B,G	H	I	D,K	K1	L	Rec. 472 (2)
1	Number of lines per picture (frame)		525	625	625	625	625	625	625	625	625
2	Field frequency, nominal value (fields/second) (3)		60 (59.94)	50	50	50	50	50	50	50	50
3	Line frequency *fH* and tolerance when operated non-synchronously (Hz) (3) (4)		15 750 (15734.264 ± 0.0003%)	15 625 ± 0.15% (±0.00014%)	15 625 (5) ± 0.02% (±0.0001%)	15 625 ± 0.02% (±0.0001%)	15 625 ± 0.0001% (6)	15 625(5) ± 0.02% (±0.0001%)	15 625 ± 0.02% (±0.0001%)	15 625 ± 0.02% (±0.0001%)	15 625 ± 0.02% (±0.0001%)
3(a)	Maximum variation rate of line frequency valid for monochrome transmission (%/s)(7) (8)		0.15 (9)		0.05	0.05	0.05	0.05	0.05	0.05	
4(10)	Nominal levels of the composite video signal (see Fig. 1) (%)	blanking level (reference level)	0	0	0	0	0	0	0	0	
		peak-white level	100	100	100	100	100	100	100	100	
		synchronizing level	- 40	–40 (-43)	–43	–43	–43	–43	–43	–43	
		difference between black and blanking level	7.5 ± 2.5	7.5 ± 2.5 (0)	0	0	0	0-7	0 (colour) 0-7 (mono.)	0 (colour) 0-7 (mono.)	0 +5 –0
		peak level including chrominance signal	120		133 (11)		133	115 (12)	115 (12)	124 (12)	
5	Assumed gamma of display device for which pre-correction of monochrome signal is made		2.2	2.2	2.8 (13)						(14)
6	Nominal video bandwidth (MHz)		4.2	4.2	5	5	5.5	6	6	6	5.0 or 5.5 or 6.0
7	Line synchronization				see Table I-1						
8	Field synchronization		see Table I-2								

Notes for previous page:

(1) The values in brackets apply to the combination N/PAL used in Argentina.

(2) Figures are given for comparison.

(3) Figures in brackets are valid for colour transmission.

(4) In order to take full advantage of precision offset when the interfering carrier falls in the sideband of the upper video range (greater than 2 MHz) of the wanted signal a line-frequency stability of at least 2×10^{-7} is necessary.

(5) The exact value of the tolerance for line frequency when the reference of synchronism is being changed requires further study.

(6) When the reference of synchronism is being changed, this may be relaxed to 15 625 ± 0.02%.

(7) These values are not valid when the reference of synchronism is being changed.

(8) Further study is required to define maximum variation rate of line frequency valid for colour transmission. See in this regard [CCIR, 1978-82]. In the UK this is 0.1 Hz/s [CCIR, 1982-86b].

(9) The values used in Japan are ± 0.1.

(10) It is also customary to define certain signal levels in 625-line systems, as follows:

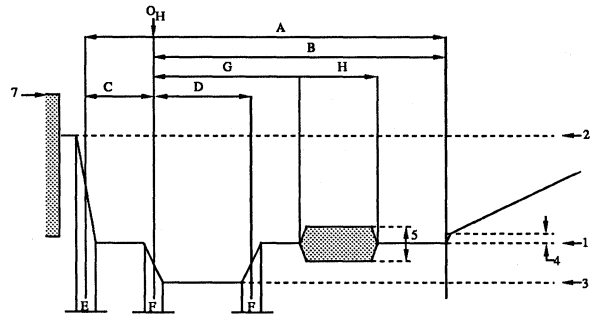
Synchronizing level — 0
Blanking level — 30
Peak white-level — 100
For this scale, the peak level including chrominance signal for system D, K/SECAM equals 110.7. (See [CCIR, 1982-86a].)

(11) Value applies to PAL signals.

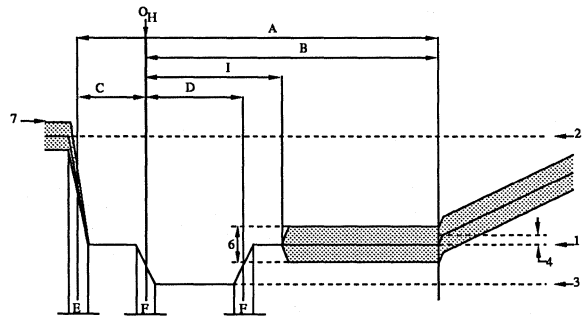
(12) Values apply to SECAM signals. For programme exchange the value is 115.

(13) Assumed value for overall gamma approximately 1.2. The gamma of the picture tube is defined as the slope of the curve giving the logarithm of the luminance reproduced as a function of the logarithm of the video signal voltage when the brightness control of the receiver is set so as to make this curve as straight as possible in a luminance range corresponding to a contrast of at least 1/40.

(14) In Recommendation 472, a gamma value for the picture signal is given as approximately 0.4.



(a) NTSC and PAL systems



(b) SECAM system

FIGURE 1 - *Levels in the composite signal and details of line-synchronizing signals*

1 blanking level

2 peak white-level

3 synchronizing level

4 difference between black and blanking levels

5 peak-to-peak value of burst

6 peak-to-peak value of colour sub-carrier

7 peak level including chrominance signal

TABLE I-1 - *Details of line synchronizing signals (see Fig. 1)*

Durations (measured between half-amplitude points on the appropriate edges) for various system

Symbol	Characteristics	M (1)	N(2)	B,G,H,I,D,K,K1,L (see also Rec. 472)
H	Nominal line period (µs)	63.492 (63.5555)	64	64 (3)
A	Line-blanking interval (µs)	10.2 to11.4 (10.9 ± 0.2)	10.24 to 11.52 (12 ± 0.3)	12 ± 0.3 (4)
B	Interval between time datum (O_H) and back edge of line-blanking signal (µs)	8.9 to 10.3 (9.2 to10.3)	8.96 to 10.24 (10.5)	10.5 (5)
C	Front porch (µs)	1.27 to 2.54 (1.27 to 2.22)	1.28 to 2.56 (1.5 ± 0.3)	1.5 ± 0.3 (4) (6)
D	Synchronizing pulse (µs)	4.19 to 5.71 (4.7 ± 0.1)	4.22 to 5.76 (4.7 ± 0.2)	4.7 ± 0.2
E	Build-up time (10 to 90%) of the edges of the line-blanking signal (µs)	<= 0.64 (<= 0.48)	<= 0.64 (0.3 ± 0.1)	0.3 ± 0.1
F	Build-up time (10 to 90%) of the line-synchronizing pulses (µs)	<= 0.25	<= 0.25 (0.2 ± 0.1)	0.2 ± 0.1(7)

(1) Values in brackets apply to M/NTSC.

(2) The values in brackets apply to the combination N/PAL used in Argentina.

(3) In France, and the countries of the OIRT, the tolerance for the instantaneous line period value is ± 0.032 µs.

(4) In 625-line countries using Teletext System B as specified in the Annex to Recommendation 653 to reduce the possibilities of data loss, the following values are preferred [CCIR, 1982-86c and d]:

a) line blanking interval: $12 \begin{smallmatrix} + 0.0 \\ - 0.3 \end{smallmatrix}$ µs

b) front porch: $1.5 \begin{smallmatrix} + 0.3 \\ - 0.3 \end{smallmatrix}$ µs

(5) Average calculated value, for information. For system I the value is 10.4 [CCIR, 1982-86b].

(6) For system I, the values are 1.65 ± 0.1.

(7) For system I, the values are 0.25 ± 0.05.

FIGURE 2- *Details of field-synchronizing waveforms*

FIGURES 2.1 - *Diagrams applicable to all systems except M*

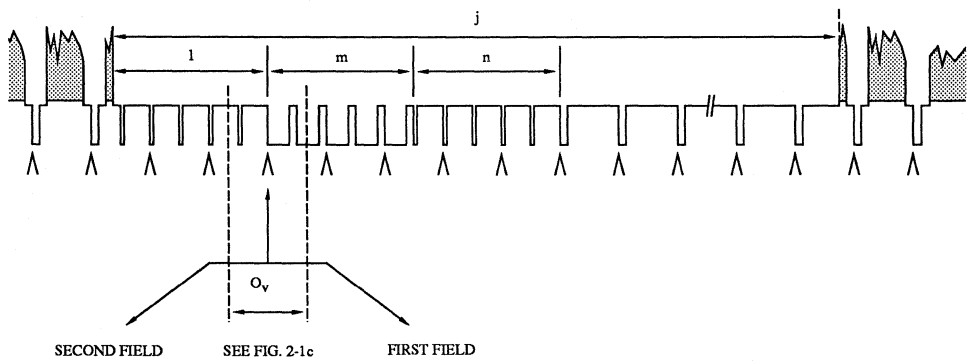


FIGURE 2.1*a* *- Signal at beginning of each first field*

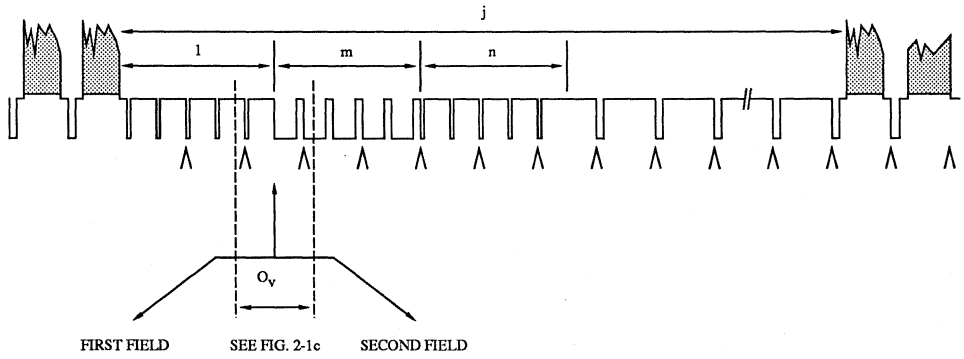
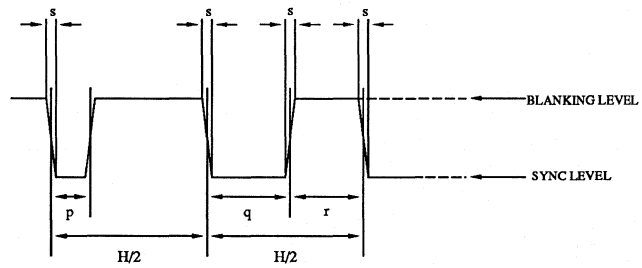


FIGURE 2.1*b* *- Signal at beginning of each second field*

Note 1. -- ΔΔΔ indicates an unbroken sequence of edges of line-synchronizing pulses throughout the field-blanking period.

Note 2. -- At the beginning of each first field, the edge of the field-synchronizing pulse, O_V, coincides with the edge of a line-synchronizing pulse if *l* is an *odd* number of half-line periods as shown.

Note 3. -- At the beginning of each second field, the edge of the field-synchronizing pulse, O_V, falls midway between the edges of two line-synchronizing pulses if *l* is an *odd* number of half-line periods as shown.



(The durations are measured to the half-amplitude points on the appropriate edges)

FIGURE 2.1c - *Details of equalizing and synchronizing pulses*

FIGURE 2- *Details of field-synchronizing waveforms*

FIGURES 2.2 - *Diagrams applicable to system M*

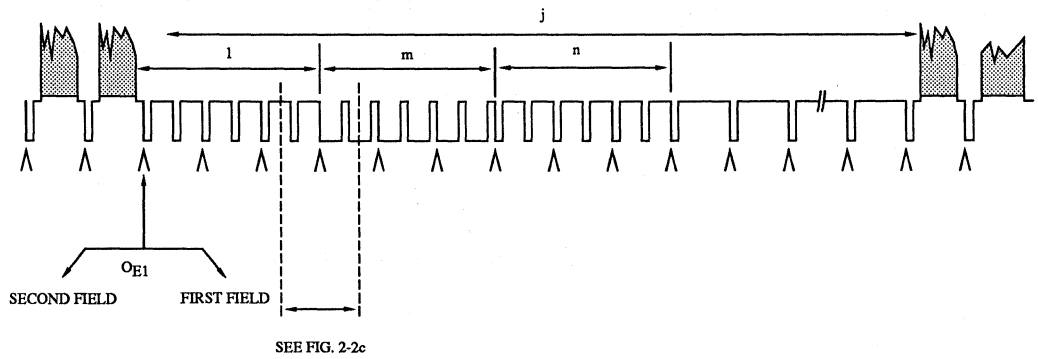


FIGURE 2.2*a* *- Signal at beginning of each first field*

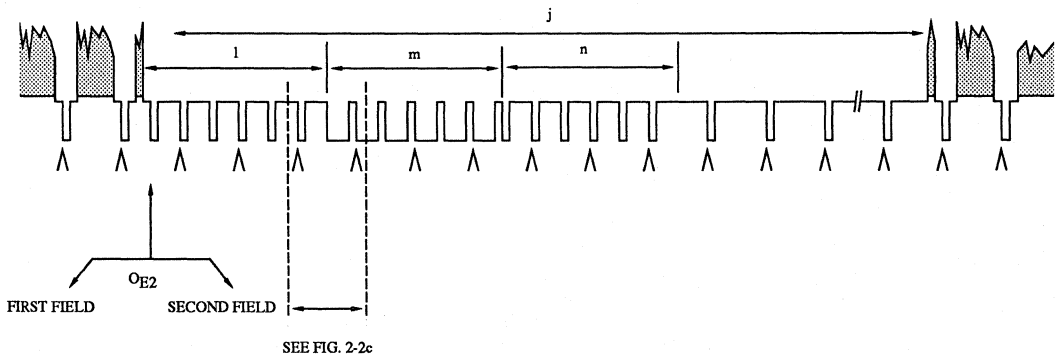


FIGURE 2.2*b* *- Signal at beginning of each second field*

Note 1. -- ΔΔΔ indicates an unbroken sequence of edges of line-synchronizing pulses throughout the field-blanking period.

Note 2. -- Field-one line numbers start with the first equalizing pulse in Field 1, designated O_{E1} in Fig. 2.2*a*.

Note 3. -- Field-two line numbers start with the second equalizing pulse in Field 2, one-half-line period after O_{E2} in Fig. 2.2*b*.

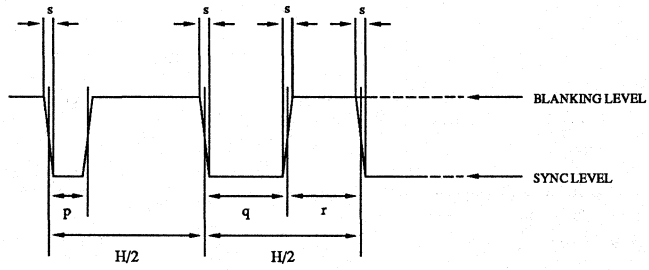


FIGURE 2.2c - *Details of equalizing and synchronizing pulses*

TABLE I-2 - *Details of field synchronizing signals (see Fig. 2)*

Durations (measured between half-amplitude points on the appropriate edges) for various systems

Symbol	Characteristics	M	N	B,G,H,I,D,K,K1,L (see also Rec. 472)
v	Field period (ms)	16.667 (2) (16.6833)	20	20
j	Field-blanking period (for *H* and *a*, see Table I-1)	(19 to 21) *H* + *a* (3)	(19 to 25) *H* + *a* (25 *H*+ *a*)	25 *H* + *a*
j' (4)	Build-up time (10 to 90%) of the edges of field-blanking pulses (µs)	<= 6.35	<= 6.35 (0.3 ± 0.1)	0.3 ± 0.1
k (4)	Interval between front edge of field-blanking interval and front edge of first equalizing pulse (µs)	(1.5 ± 0.1)		3 ± 2 (5) (systems B/SECAM, G/SECAM, D, K, K1 and L only; no ref. in Rec. 472)
l	Duration of first sequence of equalizing pulses	3 *H*	3 *H* (2.5 *H*)	2.5 *H*
m	Duration of sequence of synchronizing pulses	3 *H*	3 *H* (2.5 *H*)	2.5 *H*
n	Duration of second sequence of equalizing pulses	3 *H*	3 *H* (2.5 *H*)	2.5 *H*
p	Duration of equalizing pulse (µs)	(2.3 ± 0.1) (6)	2.30 to 2.56 (2.35 ± 0.1)	2.35 ± 0.1
q	Duration of field-synchronizing pulse (µs)	27.1 (nominal value)	26.52 to 28.16 (27.3)	27.3 (7) (nominal value)
r	Interval between field-synchronizing pulses (µs)	(4.7 ± 0.1)	3.84 to 5.63 (4.7 ± 0.2)	4.7 ± 0.2 (8)
s	Build-up time (10 to 90%) of synchronizing and equalizing pulses (µs)	<= 0.25	<= 0.25 (0.2 ± 0.1)	0.2 ± 0.1 (9)

(1) The value in brackets apply to the combination N/PAL used in Argentina.

(2) The value in brackets applies to the M/NTSC system.

(3) The following values are used in Japan:

$0.07v \; {}^{+0.01v}_{-0v}$ for colour transmission,

$0.05v = {}^{+0.03v}_{-0v}$ for monochrome transmission,

where v is the field period.

(4) Not indicated in the diagram.

(5) This value is to be specified more precisely at a later date.

(6) The following specification is also applied in Japan: an equalizing pulse has 0.45 to 0.5 times the area of a line-synchronizing pulse.

(7) For system I : 27.3 ± 0.1.

(8) For system I : 4.7 ± 0.1.

(9) For system I : 0.25 ± 0.05.

TABLE II - *Characteristics of video signal for colour television*

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, KI, L/SECAM	N/PAL (1)
2.1	Assumed chromaticity coordinates (CIE, 1931) for primary colours of receiver	x y Red 0.67 0.33 Green 0.21 0.71 Blue 0.14 0.08		x y Red 0.64 0.33 Green 0.29 0.60 Blue 0.15 0.06			(2)
2.2	Chromaticity coordinates for equal primary signals $E'_R=E'_G=E'_B$	Illuminant C $x = 0.310$ $y = 0.316$ (3)		Illuminant D_{65} $x = 0.313$ $y = 0.329$			(2)
2.3	Assumed gamma value of the receiver for which the primary signals are pre-corrected (4)	2.2	2.8				
2.4	Luminance signal	$E'_Y = 0.299\,E'_R + 0.587\,E'_G + 0.114\,E'_B$ (5) E'_R, E'_G and E'_B are gamma - pre-corrected primary signals (6)					
2.5	Chrominance signals (Colour-difference)	$E'_I = -0.27(E'_B - E'_Y) + 0.74(E'_R - E'_Y)$ $E'_Q = 0.41(E'_B - E'_Y) + 0.48(E'_R - E'_Y)$	$E'_U = 0.493(E'_B - E'_Y)$ $E'_V = 0.877(E'_R - E'_Y)$			$D'_R = -1.9(E'_R - E'_Y)$ $D'_B = 1.5(E'_B - E'_Y)$	
2.6	Attenuation of colour-difference signals	dB MHz E'_I { < 3 at 1.3 >= 20 at 3.6 E'_Q { < 2 at 0.4 < 6 at 0.5 <= 6 at 0.6	dB MHz E'_U { < 2 at 1.3 E'_V { > 20 at 3.6	dB MHz E'_U {<= 3 at 1.3 E'_V {>= 20 at 4		dB MHz D'_R {<= 3 at 1.3 D'_B {>= 30 at 3.5 Low frequency pre-correction not taken into acount (7)	dB MHz E'_U < 3 at 1.3 E'_V > 20 at 3.6

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, KI, L/SECAM	N/PAL (1)
2.7	Low Frequency pre-correction of colour difference signals					For sinusoidal signals: $D'_R{}^* = A_{BF}(f) D'_R$ $D'_B{}^* = A_{BF}(f) D'_B$ $A_{BF}(f) = \frac{1 + j(f/f_1)}{1 + j(f/3f_1)}$ f = signal frequency (kHz) f_1 = 85 kHz (See Fig. 6 for the amplitude response) (8)	
2.8	Time-coincidence error between luminance and chrominance signals (μs)	< 0.05 Excluding pre-correction for receiver response					
2.9	Equation of composite colour signal	$E_M = E'_Y + {}$ $+E'_Q \sin(2\pi f_{sc}' + 33°) +$ $+E'_I \cos(2\pi f_{sc}' + 33°)$ where: E'_Y, see item 2.4 E'_Q and E'_I, see item 2.5 f_{sc} see item 2.11 (See also Fig. 4*a*)	$E_M = E'_Y + E'_U \sin 2\pi f_{sc}' \pm E'_V \cos 2\pi f_{sc}'$ where: E'_Y, see item 2.4 E'_U and E'_V, see item 2.5 f_{sc}, see item 2.11 The sign of the E'_V component is the same as that of the sub-carrier burst (changing for each line) (see item 2.16 and Fig. 4b)			$E_M = E'_Y + G \cos 2\pi$ $(f_{OR}' + \Delta f_{OR} \int_0^t D'_R{}^* \, dt)$ or $E_M = E'_Y + G \cos 2\pi$ $(f_{OB}' + \Delta f_{OB} \int_0^t D'_B{}^* dt)$ alternately from line to line where: E'_Y, see item 2.4 f_{OR} and f_{OB}, see item 2.11 Δf_{OR} and Δf_{OB}, see item 2.12 $D'_R{}^*$ and $D'_B{}^*$, see item 2.7 G, see item 2.13	
2.10	Type of chrominance sub-carrier modulation	Suppressed-carrier amplitude-modulation of two sub-carriers in quadrature				Frequency modulation	

Item	Characteristics	Colour television system						
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, KI, L/SECAM		N/PAL (1)
2.11	Chrominance sub-carrier frequency *(a)*nominal value and tolerance (Hz)	3 579 545 ± 10	3 575 611.49 ± 10	4 433 618.75 ± 5	4 433 618.75 ± 1 (9) (10)	f_{OR} = 4 406 250 ± 2000 f_{OR} = 4 250 000 ± 2000 (11)		3 582 056.25 ± 5
	*(b)*relationship between chrominance sub-carrier frequency f_{sc} and line frequncy f_H	$f_{sc} = \frac{455}{2} f_H$	$f_{sc} = \frac{909}{4} f_H$	$f_{sc} = \left(\frac{1135}{4} + \frac{1}{625}\right) f_H$		Unmodulated sub-carrier at beginning of line 282 f_H *for* f_{OR} 272 f_H *for* f_{OB} (12)		$f_{sc} = \left(\frac{917}{4} + \frac{1}{625}\right) f_H$
2.12	Bandwidth of chrominance sidebands (quadrature modulation of sub-carrier) (kHz) or Frequency deviation of chrominance sub-carrier (frequency modulation of sub-carrier) (kHz)	$f_{sc}^{+620}_{-1300}$	$f_{sc}^{+600}_{-1300}$	$f_{sc}^{+570}_{-1300}$	$f_{sc}^{+1066}_{-1300}$		Nominal deviation D'* = 1 (14)	Maximum deviation
						Δf_{OR} (15)	280 ± 9 (± 14)	+ 350 ± 18 (± 35) - 506 ± 25 (± 50)
						ΔfOB (15)	230 ± 7 (± 11.5)	+ 506 ± 25 (± 50) - 350 ± 18 (± 35)
								$f_{sc}^{+620}_{-1300}$

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, KI, L/SECAM	N/PAL (1)
2.13	Amplitude of chrominance sub-carrier	$G = \sqrt{E'_I{}^2 + E'_Q{}^2}$	$G = \sqrt{E'_U{}^2 + E'_V{}^2}$			$G = M_0 \frac{1 + j16F}{1 + j1.26F}$ where the peak-to-peak amplitude, $2M_0$, is 23 ± 2.5% of the luminance amplitude (between blanking level and peak-white) $F = \frac{f}{f_0} - \frac{f_0}{f}$ where f_0 = 4286 kHz and f_0 is the instantaneous sub-carrier frequency. The deviation of frequency f_0, from its nominal value due to misalignment of the circuits concerned should not exceed ± 20 kHz. (See Fig. 7 for the amplitude response)	
2.14	Synchronization of chrominance sub-carrier	Sub-carrier burst on blanking back porch	Sub-carrier burst on blanking back porch				
	(g) Start of sub-carrier burst (see Fig. 1a) (µs)	4.71 to 5.71 (5.3 nominal) at least 0.38 µs after the trailing edge of line synchronization signal	5.8 ± 0.1 after epoch O_H	5.6 ± 0.1 after epoch O_H (18)			
	(h) Duration of sub-carrier burst (see Fig. 1a) (µs)	2.23 to 3.11 (9 ± 1 cycles)	2.52 ± 0.28 (9 ± 1 cycles)	2.25 ± 0.23 (10 ± 1 cycles)			2.51 ± 0.28 (9 ± 1 cycles)

<table>
<tr><th rowspan="2">Item</th><th rowspan="2">Characteristics</th><th colspan="6">Colour television system</th></tr>
<tr><th>M/NTSC</th><th>M/PAL</th><th>B, D, G, H, N/PAL</th><th>I/PAL</th><th>B, D, G, H, K, KI, L/SECAM</th><th>N/PAL (1)</th></tr>
<tr><td>2.15</td><td>Peak-to-peak value of chrominance sub-carrier burst
(see Fig. 1a) (19)</td><td>4/10 of difference between blanking level and peak white-level ± 10%</td><td colspan="3">3/7 of difference between blanking level and peak white-level ± 10% For systems D and I, the tolerance is ± 3%
(16)(17) (16)</td><td></td><td></td></tr>
<tr><td>2.16</td><td>Phase of chrominance sub-carrier burst
(see Fig 1a)</td><td>180° relative to ($E'_B - E'_Y$) axis
(see Fig. 4a)
In the NTSC sequence of four colour fields, field 1 is identified with Note (20)
(see also Fig. 5c)</td><td colspan="3">135° relative to E'_U axis with the following sign (see Fig. 4b)
<table><tr><td rowspan="2">Line</td><td>Field Number (21)</td></tr><tr><td>1 2 3 4 5 6 7 8</td></tr><tr><td></td><td>Burst blanking sequence (see Figs. 5a and 5b)</td></tr><tr><td></td><td>I II III IV I II III IV</td></tr><tr><td>even
odd</td><td>- - + + - - + +
+ + - - + + - -</td></tr></table></td><td></td><td></td></tr>
<tr><td>2.17</td><td>Blanking of chrominance sub-carrier</td><td>Following each equalizing pulse and also during the broad synchronizing pulses in the field-blanking interval</td><td>11 lines of field-blanking interval:
260 to 270
522 to 7
259 to 269
223 to 8
(see Fig. 5b)</td><td>9 lines of the field-blanking interval:
lines 311 to 319 inclusive
623 to 6 inclusive
310 to 318 inclusive
622 to 5 inclusive
(See Fig. 5a)</td><td>(a) from leading edge of line-blanking signal up to $i = 5.6 \pm 0.2$ (µs) after epoch O_H,
i.e. during $c + i$
(see Fig. 1b) (13)
(b) During field-blanking interval, excluding frame identification signals, or, in countries where this is possible, during the whole of the field-blanking interval
(See item 2.18)</td><td></td></tr>
</table>

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, KI, L/SECAM	N/PAL (1)
2.18	Synchronization of chrominance sub-carrier switching during line blanking	See item 2.16. For signals used in programme integration, the tolerance on the coincidence between the reference sub-carrier and the horizontal synchronizing pulses in nominally $0 \pm 40°$ of the reference sub-carrier	By E'_V chrominance component of sub-carrier burst (See item 2.16)			In the SECAM system, one of two colour synchronization methods can be chosen: -line identification: by chrominance sub-carrier reference signals on the line-blanking back porch (23) -by identification signals occupying 9 lines of field-blanking period: (a) line 7 to 15 in 1st and 3rd field (b) line 320 to 328 in 2nd and 4th field (See Fig. 9) (24) *Shape of video signals corresponding to identification signals*: For lines D'_R - Trapezoid with linear variation from beginning of line on $15 \pm 5\mu s$ from 0 up to level + 1.25 and then constant at the level $+ 1.25 \pm 0.06$ (± 0.13) (See Fig. 8)	

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, KI, L/SECAM	N/PAL (1)
						For lines D'_B - Trapezoid with linear variation from the beginning of the line on 18 ± 6 µs (20 ± 10 µs) from 0 down to level −1.52 and then constant at the level −1.52 ± 0.07 (± 0.15) (see Fig. 8) (15) *Peak-to-peak amplitude of identification signals*: For lines D^1_B: 500 ± 50mV For lines D^1_R: $540\ ^{+40mV}_{-50mV}$ if amplitude of luminance signal (between blanking level and peak white) equals 700mV *Maximum deviation during transmission of identification signals (kHz):* For lines D'_R: +350 ±18 (±35) For lines D'_B: −350 ±18 (±35) (15)	

(1) These values apply to the combination N/PAL used in Argentina. Only those values are given in this column which are different from the values given in the column B, G, H, N/PAL.

(2) For SECAM systems and for existing sets, it is provisionally allowed to use the following chromaticity coordinates for the primary colours and white:

	x	y
Red	0.67	0.33
Green	0.21	0.71
Blue	0.14	0.08
White	0.310	0.316 (C– white)

(3) In Japan, the chromaticity of studio monitors is adjusted to a D–white at 9300 K.

(4) The primary signals are pre-corrected so that the optimum quality is obtained with a display having the indicated value of gamma.

(5) In certain countries using the SECAM systems and in Japan it is also permitted to obtain the luminance signal as a direct output from an independent photo-electric analyser instead of from the primary signals.

(6) For the SECAM system, it is allowable to apply a correction to reduce interference distortions between the luminance and chrominance signals by an attenuation of the luminance signal components as a function of the amplitude of the luminance components in the chrominance band.

(7) This value will be defined more precisely later.

(8) The maximum deviations from the nominal shape of the curve (see Fig. 6) should not exceed ± 0.5 dB in the frequency range from 0.1 to 0.5 MHz and ± 1.0dB in the frequency range from 0.5 to 1.3 MHz.

(9) When the signal originates from a portable of overseas source the tolerance on the frequency may be relaxed to ± 5 Hz. Maximum rate of variation of f_{sc}: 0.1 Hz/s.

(10) This tolerance may not be maintained during such operational procedures as "genlock".

(11) A reduction of the tolerance is desirable.

(12) The initial phase of the sub-carrier undergoes in each line a variation defined by the following rule:
From frame to frame: by 0°: 180°: 0°: 180°: and so on, and also from line to line in either one of the following two patterns:
0°: 0°: 180°: 0°: 0°: 180°: and so on,
or 0°: 0°: 0°: 180°: 180°: 180°: and so on.

(13) f_{sc} ± 1300 kHz is adopted in the People's Republic of China.

(14) The unity value represents the amplitude of the luminance signal between the blanking level and the peak white-level.

(15) Provisionally, the tolerances may be extended up to the values given in brackets.

(16) During transmission of a monochrome programme of significant duration, in order to ensure satisfactory operation of colour-killers in receivers, all signals having the same nominal frequency as the colour sub-carrier that appears in the line-blanking interval, should be attenuated by at least 35 dB below the peak-to-peak value of the burst given in item 2.15, column 3 of Table II, and shown as Item 5 in Fig.1.

(17) The value given in Note (16) is accepted on a tentative basis.

(18) Transmitter pre-correction for receiver group delay is not included.

(19) For the use of automatic gain control circuits, it is important that the burst amplitude should maintain the correct ratio with the chrominance signal amplitude.

(20) Field 1 of the sequence of four fields in the NTSC video signal is defined by a whole line between the first equalizing pulse and the preceding horizontal synchronizing pulse and a negative-going zero-crossing of the reference sub-carrier nominally at the 50% point of the first equalizing pulse. The zero-crossing of the reference sub-carrier shall be nominally coincident with the 50% point of the leading edges of all horizontal synchronizing pulses for programme integration at the studio.

(21) Field 1 of the sequence of eight colour fields is defined as that field, where the phase $\varphi E'_U$ of the extrapolated E'_U component (see item 2.5 of Table II) of the video burst at the hall amplitude point of the line synchronizing pulse of line 1 is in the range $-90° <= \varphi E'_U < 90°$.

(22) The value of the tolerance will be defined more precisely later.

(23) The line identification method is preferable, because it will enable agreements to be reached subsequently on the suppression of frame identification signals in international programme exchanges. In the absence of such agreements, signals meeting the SECAM standard are regarded as comprising such identification signals.
In France, a decree of 14 March 1978 specified that colour TV receivers placed on sale on or after 1 December 1979 must use the line identification method of decoding [CCIR, 1982-86c].

(24) The order in which the identification signals D_R* and D_B* appear on the four fields of a complete cycle given in Fig. 9 is in conformity with Recommendation 469-1.

TABLE III - *Characteristics of the radiated signals (monochrome and colour)*

Item	Characteristics		M	N (1)	B,G	H	I	D,K	K1	L
1	Frequency spacing (See Fig. 10)	Nominal radio-frequency channel bandwidth (MHz)	6	6	B:7 G:8	8	8	8	8	8
2		Sound carrier relative to vision carrier (MHz)	+ 4.5 (2)	+ 4.5	+ 5.5 ± 0.001 (3), (4), (5)	+ 5.5	+ 5.9996 ± 0.0005	+ 6.5 ± 0.001	+ 6.5	+ 6.5
3		Nearest edge of channel relative to vision carrier (MHz)	– 1.25	– 1.25	– 1.25	– 1.25	– 1.25	– 1.25	– 1.25	– 1.25
4		Nominal width of main sideband (MHz)	4.2	4.2	5	5	5.5	6	6	6
5		Nominal width of vestigial sideband (MHz)	0.75	0.75	0.75	1.25	1.25	0.75	1.25	1.25
6	Minimum attenuation of vestigial sideband (dB at MHz)(1)		20 (–1.25) 42 (- 3.58)	20 (–1.25) 42 (–3.5)	20 (–1.25) 20 (–3.0) 30 (–4.43) (7)	20 (–1.75) 20 (–3.0)	20 (–3.0) 30 (–4.43)	20 (–1.25) 30 (–4.33 ± 0.1) (8) (9)	20 (- 2.7) 30 (- 4.3) ref.: 0 (+ 0.8)	15 (- 2.7) 30 (- 4.3) ref.: 0 (+ 0.8)
7	Type and polarity of vision modulations		C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F pos.
8	Levels in the radiated signal (% of peak carrier)	synchronizing level	100	100	100	100	100	100	100	< 6
		blanking level	72.5 to 77.5	72.5 to 77.5 (75 ± 2.5)	75 ± 2.5 (10)	72.5 to 77.5	76 ± 2	75 ± 2.5	75 ± 2.5	30 ± 2
		difference between black and blanking level	2.88 to 6.75	2.88 to 6.75	0 to 2 (nominal)	0 to 7	0 (nominal)	0 to 4.5 (11)	0 to 4.5	0 to 4.5
		peak-white level	10 to 15	10 to 15 (10 to 12.5)	10 to 12.5 (10) (12)	10 to 12.5	20 ± 2	10 to 12.5 (13) (14)	10 to 12.5	100 (≈ 110) (15)

Item	Characteristics	M	N(1)	B, G	H	I	D, K	KI	L
9	Type of sound modulation	F3E	F3E	F3E	F3E	F3E	F3E	F3E	A3E
10	Frequency deviation (kHz)	± 25	± 25	± 50	± 50	± 50	± 50	± 50	
11	Pre-emphasis for modulation (μs)	75	75	50	50	50	50	50	
12	Ratio of effective radiated powers of vision and sound (16)	10/1 to 5/1 (17)	10/1 to 5/1	20/1 to 10/1 (3) (18) (19)	5/1 to 10/1	5/1 10/1 (20)	10/1 to 5/1 (21)	10/1	10/1
13	Pre-correction for receiver group-delay characteristics at medium video frequencies (ns) (see also Fig. 3)	0	1 MHz 0 ± 100 1 MHz 0 ± 100 1 MHz 0 ± 60	(22)			(23a)		
14	Pre-correction for receiver group-delay characteristics at colour subcarrier frequency (ns) (see Fig. 3)	– 170 (nominal)	+ 60 -170 -40	– 170 (nominal) (22)			(23b)		

(1) The values in brackets apply to the combination N/PAL used in Argentina.

(2) In Japan, the values + 4.5 ± 0.001 are used.

(3) In the Federal Republic of Germany a system of two sound carriers is used, the frequency of the second carrier being 242.1875 kHz above the frequency of the first sound carrier. The ratio between vision /sound e.r.p. for this second carrier is 100/1. For further information on this system see Report 795. For stereophonic sound transmissions a similar system is used in Australia with vision/sound power ratios being 20/1 and 100/1 for the first and second sound carriers respectively.

(4) New Zealand uses a sound carrier displaced 5.4996 MHz from the vision carrier.

(5) The sound carrier for single carrier sound transmissions in Australia may be displaced 5.5 ± 0.005 MHz from the vision carrier.

(6) In some cases, low-power transmitters are operated without vestigial-sideband filter.

(7) For B/SECAM and G/SECAM: 30 dB at - 4.43 MHz, within the limits of ± 0.1 MHz.

(8) In some countries, members of the OIRT, additional specifications are in use:
(*a*) not less than 40 dB at - 4.286 MHz ± 0.5 MHz,
(*b*) 0 dB from -0.75 MHz to + 6.0 MHz,
(*c*) not less than 20 dB at ± 6.375 MHz and higher;
Reference: 0 dB at + 1.5 MHz.

(9) In the People's Republic of China, the attenuation value at the point (- 4.33 ± 0.1) has not yet been determined.

(10) Australia uses the nominal modulation levels specified for system I.

(11) In the People's Republic of China, the values 0 to 5 have been adopted.

(12) Italy is considering the possibility of controlling the peak white-level after weighting the video frequency signal by a low-pass filter, so as to take account only those spectrum components of the signal that are likely to produce inter-carrier noise in certain receivers when the nominal level is exceeded. Studies should be continued with a view to optimizing the response of the weighted filter to be used.

(13) The USSR has adopted the value 15 ± 2%.

(14) A new parameter "white level with sub-carrier" should be specified at a later date. For that parameter, the USSR has adopted a value of 7 ± 2%.

(15) The peak white-level refers to a transmission without color sub-carrier. The figure in brackets corresponds to the peak value of the transmitted signal, taking into account the colour sub-carrier of the respective colour television system.

(16) The values to be considered are:
- the r.m.s. value of the carrier at the peak of the modulation envelope for the vision signal. For system L, only the luminance signal is to be considered. (see Note (15) above);
- the r.m.s value of the unmodulated carrier for amplitude-modulated and frequency-modulated sound transmissions.

(17) In Japan. a ratio of 1/0.15 to 1/0.35 is used. In the United States, the sound carrier e.r.p. is not to exceed 22% of the authorized vision e.r.p.

(18) It may be that the Austrian Administration will continue to use a 5/1 power ratio in certain cases, when necessary.

(19) Recent studies in India [CCIR, 1982-86f] confirm the suitability of a 20/1 ratio of effective radiated powers of vision and sound. This ratio still enables the introduction of a second sound carrier.

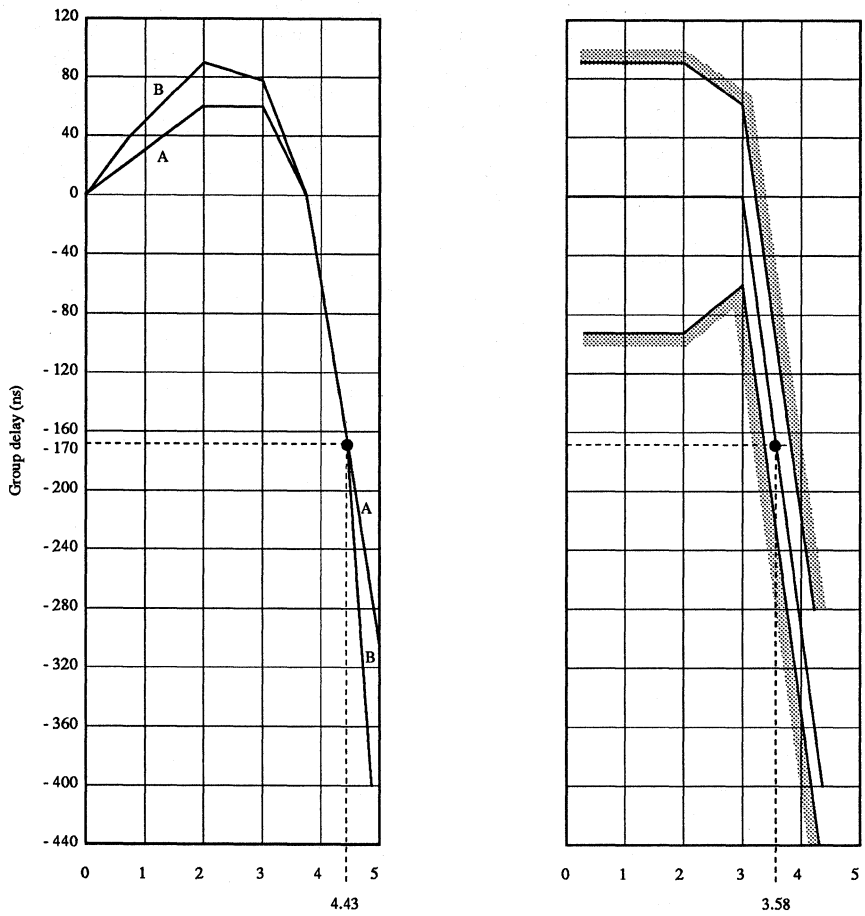
(20) The ratio 10/1 is used in the Republic of South Africa.

(21) In the People's Republic of China, the value 10/1 has been adopted.

(22) In the Federal Republic of Germany and the Netherlands the correction for receiver group delay is made according to curve B in Fig. 3*a)*. Tolerances are shown in the table under Fig. 3*a)*. From [CCIR, 1966-69] it is learned that Spain uses curve A. The OIRT countries using the B/SECAM and G/SECAM systems use a nominal pre-correction of 90 ns at medium video frequencies. In Sweden, the pre-correction is 0 ± 40 ns up to 3.6 MHz. For 4.43 MHz, the correction is - 170 ± 20 ns and for 5 MHz it is 350 ± 80 ns. In New Zealand the pre-correction increases linearly from 0 ± 20 ns at 0 MHz to 60 ± 50 ns at 2.25 MHz, follows curve A of Fig. 3a from 2.25 MHz to 4.43 MHz and then decreases linearly to - 300 ± 75 ns at 5 MHz. In Australia, the nominal pre-correction follows curve A up to 2.5 MHz, the decreases 0 ns at 3.5 MHz, - 170 at 4.43 MHz and -280 at 5 MHz. Based on studies on receivers in India, the receiver group delay pre-equalization proposed to be adopted in India at 1 MHz, 2 MHz, 3 MHz, 4.43 MHz and 4.8 Mhz are + 125 ns, + 150 ns, + 142 ns, - 75 ns, and - 200 ns respectively.

(23a) Not yet determined. The Czechoslovak Socialist Republic proposes + 90 ns (nominal value).

(23b) Not yet determined. The Czechoslovak Socialist Republic proposes + 25 ns (nominal value).



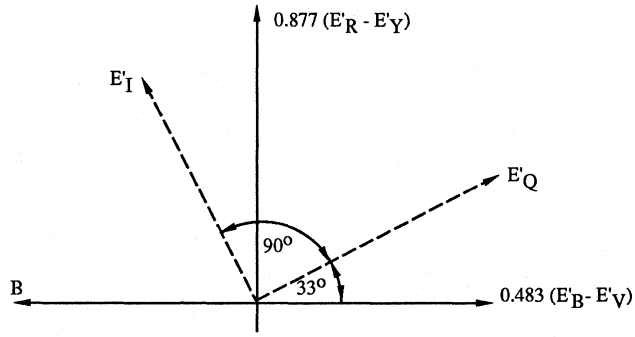
(a) B/PAL and G/PAL systems (See Table III ([22]))

(b) M/PAL and M/NTSC systems

FIGURE 3 - *Curve of pre-correction for reciever group delay characteristics*

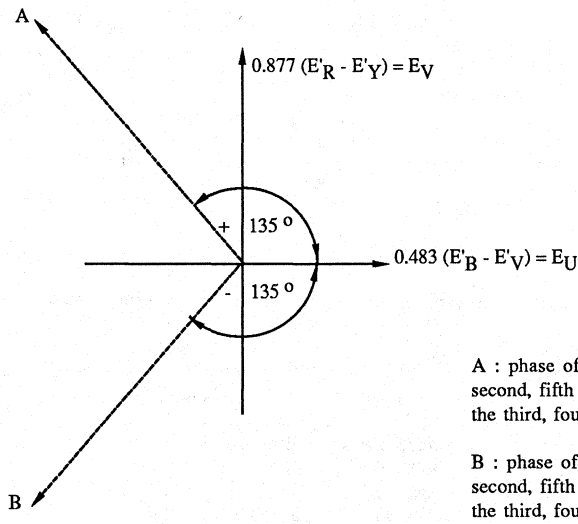
Nominal values and tolerances (ns)

Frequncy (MHz)	Curve A	Curve B
0.25		+ 5 ± 0
1.00	+ 30 ± 50	+ 53 ± 40
2.00	+ 60 ± 50	+ 90 ± 40
3.00	+ 60 ± 50	+ 75 ± 40
3.75	0 ± 50	0 ± 40
4.43	- 170 ± 35	- 170 ± 40
4.80	- 260 ± 75	- 400 ± 90



B: phase of the burst

(a) NTSC system



A : phase of the burst in odd lines of the first, second, fifth and sixth fields and in even lines of the third, fourth, seventh and eighth fields.

B : phase of the burst in even lines of the first, second, fifth and sixth fields and in odd lines of the third, fourth, seventh and eighth fields.

(b) PAL system

FIGURE 4 - *Chrominance axes and phase of the burst*

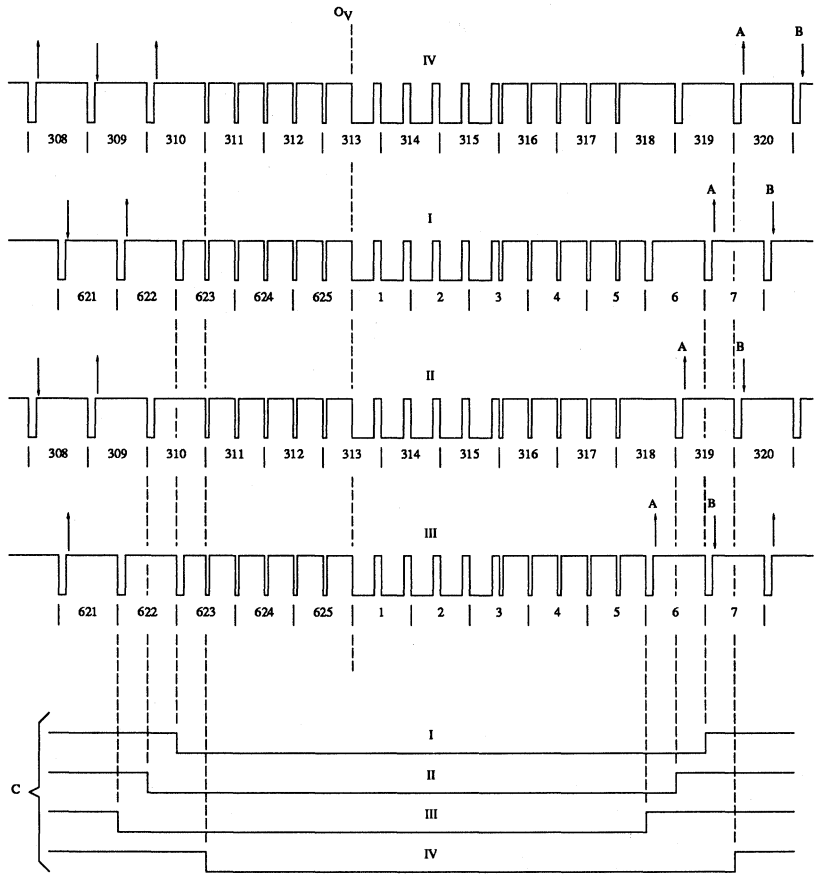


FIGURE 5a - *Burst blanking sequence in the B, G, H and I/PAL systems*

O_V:	field-synchronizing datum.
I, II, III, IV:	first and fifth, second and sixth, third and seventh, fourth and eighth fields (see item 2.16 of Table II)
A:	phase of burst; nominal value + 135°
B:	phase of burst; nominal value – 135°
C:	burst-blanking intervals

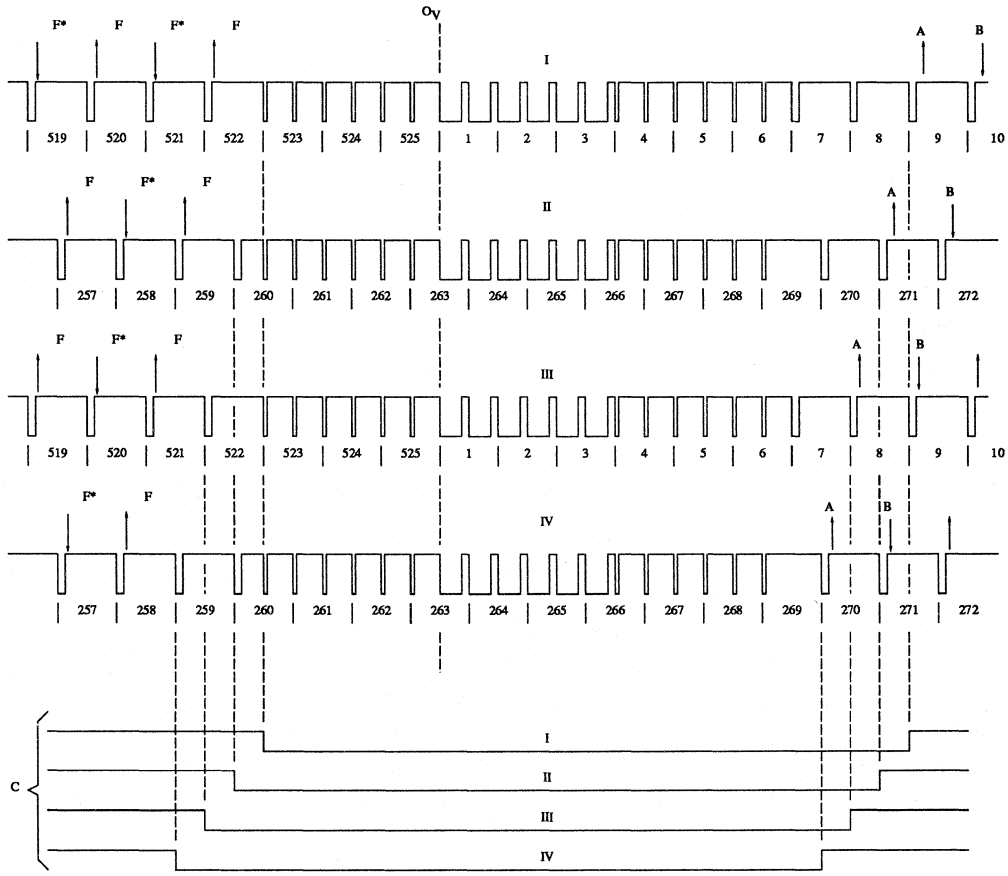


FIGURE 5b - *Burst blanking sequence in the M/PAL system*

O_V:	field-synchronizing datum
I, II, III, IV:	first and fifth, second and sixth, third and seventh, fourth and eighth fields (see item 2.16 of Table II
A:	phase of burst; nominal value + 135°
B:	phase of burst; nominal value – 135°
C:	burst-blanking intervals

Sources for Consumer Electronics Standards

CCIR	The International Radio Consultive Committee International Telecommunications Union Place Des Nations CH-1211 Geneva 20 Switzerland (011) 4122 730 5800
CCITT	The International Telephone and Telegraph Consultive Committee International Telecommunications Union Place Des Nations CH-1211 Geneva 20 Switzerland (011) 4122 730 5851
EBU	European Broadcasting Union The Technical Center of the EBU 32, Avenue Albert Lancaster B-1180 Brussels Belgium
EIA	Electronic Industries Association 1722 Eye Street, NW Suite 440 Washington, DC 20006 Headquaters: (202) 457 4936 Standards: (202) 457 4966
IEEE	Institute of Electrical and Electronics Engineers Headquarters: 345 East 47th Street New York, NY 10017 (212) 705 7900 Standards Offics: (IEEE Service Center) P.O. Box 1331 Piscataway, NJ 00855 (201) 981 0060
SMPTE	Society of Motion Picture and Television Engineers 595 W. Hartsdale Ave. White Plains, NY 10607 (914) 761 1100

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