USER-CONFIGURABLE ADAPTER INTERFACE CHIPS FOR PS/2 MICRO CHANNEL

EPB2001 EPB2002

FEATURES

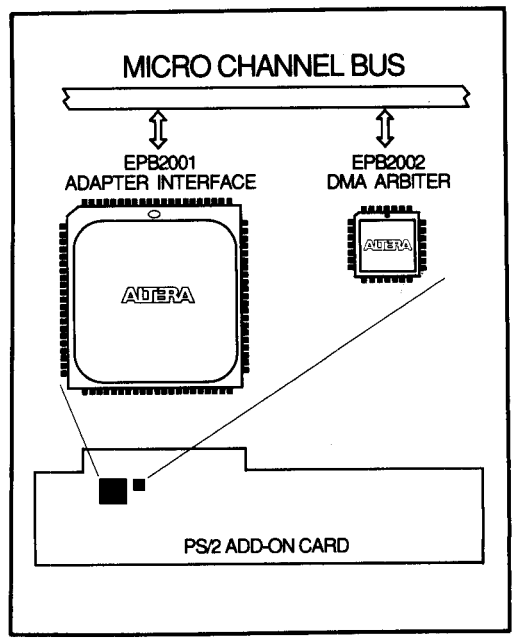
- User-Configurable Adapter Interface Chip Set for PS/2 Micro Channel Bus Add-On Boards:
  - —EPB2001 Single-Chip Adapter Interface Device for Micro Channel Bus
  - —EPB2002 DMA Arbitration Support Device for Micro Channel Bus
- EPB2001 CMOS EPROM Device Integrates Basic Interface Functions into a Single 84-Lead Device:
  - —Programmable Option Select (POS) Registers 0102-0105 with 16 Programmable Adapter Interface I/O Lines
  - —Two-Byte Programmable Adapter I.D. EPROM (POS Registers 0100 & 0101)
  - —24mA Micro Channel Data Bus Port (Byte-Wide)
  - —Adapter Address Remapping/Chip Select Decode Function Provided by Eight Chip Select Blocks with Eight Programmable Address Ranges Each
  - —Adapter Control Lines Provided for Control of Board Memory, I/O and Transceivers
  - —Support of Channel Check and Card Enable Functions
- EPB2002 CMOS Device Integrates All DMA Interface/Arbitration Functions into a Single 28-Lead Device:
  - —Supports Micro Channel Arbitration Protocol for Slave DMA Adapters
  - —User-Mappable POS Register Bits for Arbitration Level and Fairness
  - —Single-Transfer and Burst Cycle Modes
- 100% Compatible with Micro Channel A.C. Timing and D.C. Output Drive Specifications.
- EPROM Security Bit Insures Proprietary Designs.
- Quick PC-based Design Entry Using MC Map Design Software.

PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

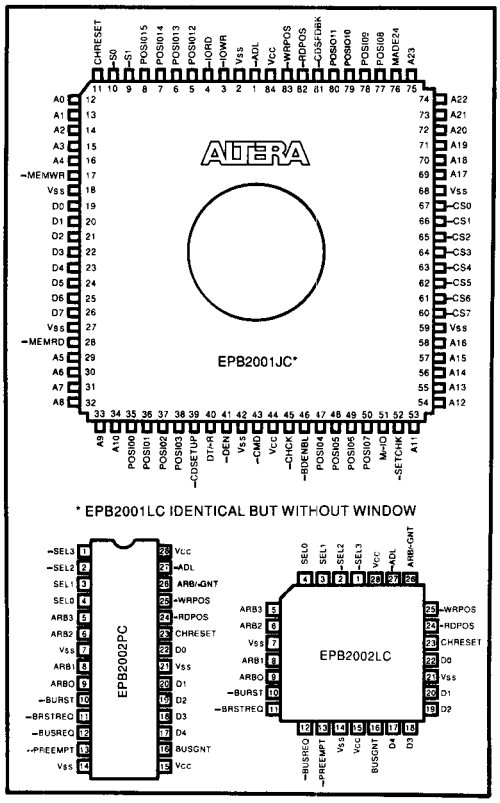
GENERAL DESCRIPTION

The Altera EPB2001 and EPB2002 are interface devices for use by manufacturers of add-on boards for IBM PS/2 computers. The EPB2001 provides in a single chip all essential interface functions required between a PS/2 add-on card, or adapter, and the Micro Channel Bus. The EPB2002 integrates optional DMA support functions needed to provide Micro Channel DMA arbitration capability. Implemented in CMOS EPROM technology, the devices provide full a.c. and d.c. interface compatibility with the Micro Channel Bus. Typically, no additional glue logic components are required. The devices are function-specific Erasable Programmable Logic Devices (EPLDs): specific board characteristics are programmable by the user for a given application. The functions integrated replace eighteen or more MSI/TTL and standard PLD devices. The 84-Lead EPB2001 and 28-Lead EPB2002 provide good p.c. board footprint efficiency (less than 2 square inches total), and may be used in tandem or independently as the design requires.



REV. 1.1

CONNECTION DIAGRAM



The EPB2001 provides in a single chip all general-purpose interface functions, such as required Programmable Option Select (POS) Registers 0100-0105 (including board I.D.), access to POS Register contents on adapter-accessible I/O lines (replacing jumpers and DIP switches on the board), adapter address remapping via programmable chip select logic, and board control signals (-MEMWR, -IORD, etc.). CMOS EPROM technology is used in the device to provide non-volatile storage of board I.D., chip select ranges and POS I/O selection for reduced component count and added design security. The device is available in both One-Time-Programmable plastic and erasable/reprogrammable ceramic J-Lead chip carrier packages.

The EPB2002 provides DMA arbitration functions for those adapters requiring it. Arbitration Level POS bits, support of arbitration "fairness," burst or non-burst transfers, and full support of the arbitration protocol are all provided by the CMOS device. Pin strapping options allow mapping of the POS bits provided into any valid locations. When used in conjunction with the EPB2001, no additional components are required to provide a slave DMA adapter interface.

Programming of the EPB2001 EPROM elements is provided via PC-based MC Map Design Software. This quick, easy-to-use table-driven software leads the designer through a series of design menus. The resulting design is converted to a JEDEC file. The EPB2001 can then be programmed in seconds using Altera's PLP4 programming card, PLE3-12 programming unit and PLEJ2001 device adapter.

EPB2001 FUNCTIONAL DESCRIPTION

BUS CONTROL SECTION

A block diagram of the EPB2001 chip is shown in Figure 2. Micro Channel Interface signals are shown on the left side of the diagram, board interface signals on the right. The upper portion of the diagram contains the bus control logic, and includes in particular the -CDSETUP, -S0, -S1, -CMD and M/-IO inputs on the Micro Channel side, and the -DEN, DT/-R, -IOWR, -IORD, -MEMWR, -MEMRD, -RDPOS and -WRPOS outputs on the board side. This section generates read and write signals for the internal POS registers, as well as the board control signals noted above.

This block is "activated" by either an active -CDSETUP line in conjunction with an I/O Read or Write cycle from the processor (indicating a POS set-up or boot configuration cycle), or a valid bus cycle (I/O Read or Write, Memory Read or Write) in conjunction with -CDSFDBK active (indicating a bus cycle for **this** adapter). This assumes the board has already been enabled (see POS Register File section below). Under all other circumstances, the outputs of this block remain quiescent.

The bus control block decodes the Micro Channel Bus (MC Bus) cycles as valid combinations of the -S0, -S1 and M/-IO signals. The coding for these signals is:

M/-IO	-S0	-S1	Cycle Type
0	0	0	No Op
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	No Op
1	0	0	No Op
1	0	1	Mem Write
1	1	0	Mem Read
1	1	1	No Op

The state of these lines, along with -CDSETUP and -CDSFDBK is latched by the leading (falling) edge of -ADL for the duration of the cycle. Either -CDSETUP or -CDSFDBK must be active when -ADL falls for these actions to occur.

The -CMD signal acts as a command strobe and times the generation of the appropriate control lines. Therefore, -MEMRD, -MEMWR, -IORD and -IOWR have a duration approximating that of -CMD.

DT/-R controls the direction of data flow through an external data transceiver. It changes after -ADL falls, and remains latched for the duration of the

2

Figure 1. Micro Channel Interface Connection

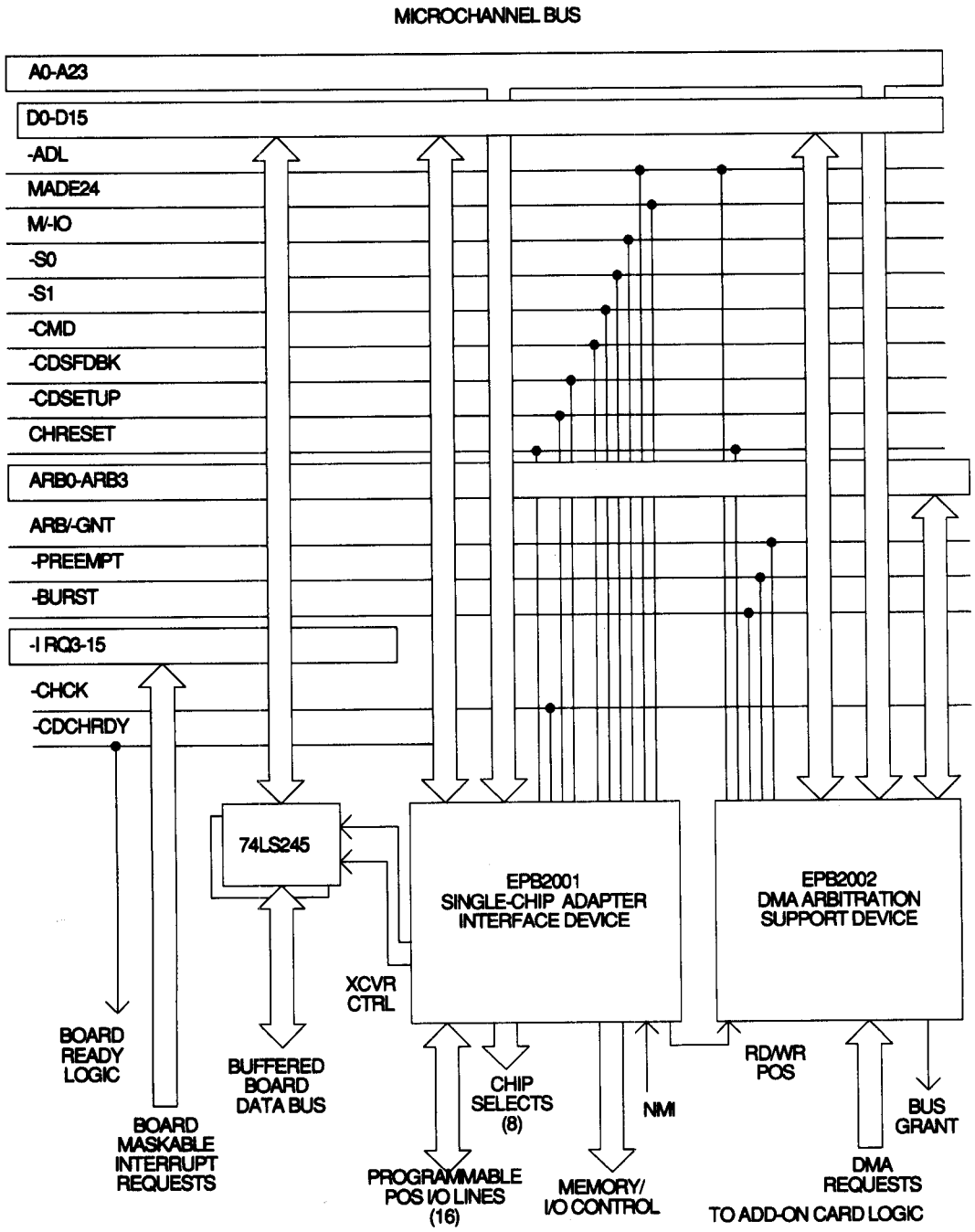
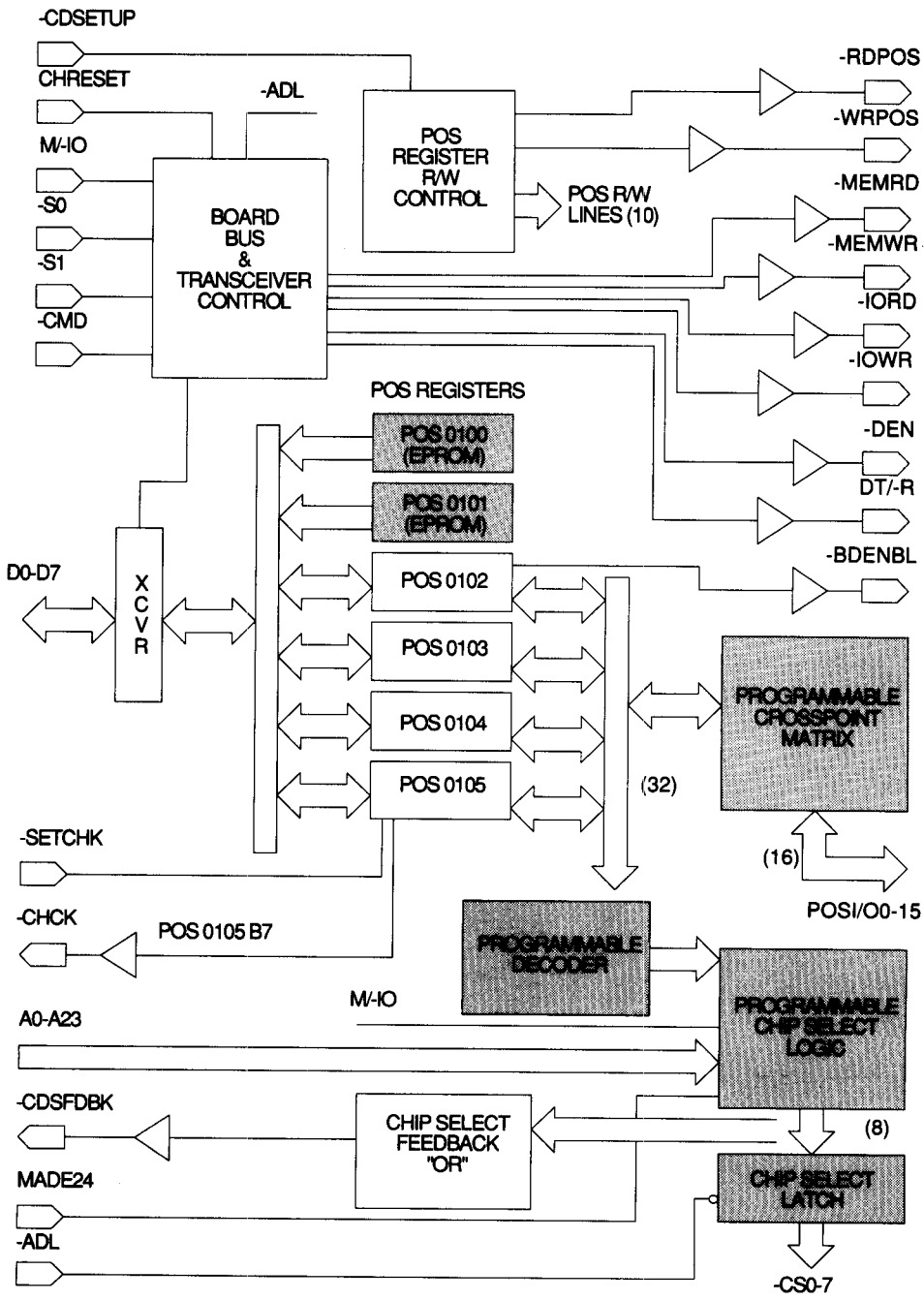


Figure 2. EPB2001 Block Diagram



EPB2001 PIN DESCRIPTION

SIGNAL	TYPE	OUTPUT DRIVE (mA) IOH	IOL	DESCRIPTION
-CDSFDBK	TP	2	6	Active LOW bus cycle acknowledge output generated by the EPB2001 for any I/O or memory cycle which activates one of the -CS outputs. Derived as an unlatched decode of Addresses, M/-IO and MADE24.
-CHCK	OD		24	Active LOW channel check output used to signal Non-Maskable Interrupt errors. Reflects the state of POS register 0105 bit 7. Activated by an active LOW input pulse on the -SETCHK line.
D0-D7 (8x)	TS	4	24	Tristate bidirectional data bus lines. POS register read/write data access path. Enabled to the MC Bus only during a valid I/O read cycle.
-CDSETUP	I			Active LOW set-up input. Signals a read or write cycle to the EPB2001's POS registers.
M/-IO	I			Memory/I/O cycle input from the MC Bus. HIGH for memory cycles, LOW for I/O cycles.
-S0, -S1	I			Bus cycle status input lines from the MC Bus. (Codings for various cycles are shown earlier.) In conjunction with -CMD, used to generate board control lines (-MEMWR, -DEN, etc.).
-CMD	I			Active LOW MC Bus cycle strobe input. Used to time data transfers during read and write operations.
CHRESET	I			Active HIGH channel reset input. The EPB2001 deasserts all active outputs a short time after CHRESET rises. POS register 0102 bit 0 is also reset by this input, deactivating -BDENBL.
MADE24	I			Active HIGH input which indicates a 24 bit address is present on the MC Bus for the current cycle. When LOW, indicates an extended address (32 bits) is present.
A0-A23 (24x)	I			MC Bus address inputs. Valid while -ADL is LOW.
-ADL	I			Active LOW address latch input. Trailing edge of this signal is used to latch addresses and (optionally) chip select lines.
-MEMRD	TP	4	24	Active LOW memory read strobe output. Generated as a decode of -S0=1, -S1=0 and M/-IO=1, timed by -CMD.
-MEMWR	TP	4	24	Active LOW memory write strobe output. Generated as a decode of -S0=0, -S1=1 and M/-IO=1, timed by -CMD.
-IORD	TP	4	24	Active LOW I/O read strobe output. Generated as a decode of -S0=1, -S1=0 and M/-IO=0, timed by -CMD.
-IOWR	TP	4	24	Active LOW I/O write strobe output. Generated as a decode of -S0=0, -S1=1 and M/-IO=0, timed by -CMD.
-DEN	TP	4	6	Active LOW transceiver enable output. LOW during data transfer portion of selected MC Bus cycles.

EPB2002 PIN DESCRIPTION (continued)

SIGNAL	TYPE	OUTPUT DRIVE (mA) IOH	IOL	DESCRIPTION
DT/-R	TP	4	6	Data transceiver direction control output. HIGH during selected MC Bus read cycles, and LOW during selected MC Bus write cycles.
-CS0-7 (8x)	TP	4	6	Active LOW chip select outputs. Derived as a decode of Addresses, M/-IO and MADE24. May be optionally latched on an individual basis by -ADL. Eight user-defined address ranges per output, enabled by groups of POS register bits.
POSI/O0-15 (16x)	I/OD		6	Bidirectional POSI/O lines. Each open drain output is driven by user-defined POS register bit. State of POSI/O pin is reflected when corresponding POS bit is read through MC Bus port. This allows board logic status reporting when POS register contents equal one (default).
-WRPOS	TP	4	6	Active LOW write POS register strobe. Active for POS set-up cycle. Used to drive EPB2002 -WRPOS inputs or control optional POS functions external to the EPB2001.
-RDPOS	TP	4	6	Active LOW read POS register strobe. Active for POS set-up cycle. Used to drive EPB2002 -RDPOS inputs or control optional POS functions external to the EPB2001.
-BDENBL	OD		24	Active LOW board enable output. Open drain output reflects the state of POS register 0102 bit 0. Active low when this register bit is set to a one. Deactivated by CHRESET.
-SETCHK	I			Active LOW set channel check input. A low pulse on this level-sensitive input resets POS register 0105 bit 7, and therefore activates the -CHCK output to the MC Bus.
VCC (2x)				+5 Volt Power Supply.
VSS (6x)				Ground.

Signal Types:
I = Input
TP = Totem-Pole (Push-Pull) Output
OD = Open-Drain Output
TS = Bidirectional Tristate Output I/O

cycle. It is low for all write cycles.

-DEN controls external data transceiver output enables. -DEN is active during a valid Read cycle for essentially the same duration as -CMD. For a Write cycle, however, to give maximum data setup time for the board, it becomes active a short time after -ADL falls. It goes inactive after -MEMWR or -IOWR goes inactive.

The adapter setup or configuration (sometimes called POST for Power-On System Test) can occur only when -CDSETUP is active on the rising edge of -ADL (address latch input from the MC Bus) followed by an I/O read or write cycle. The rising edge of -ADL may be used to latch addresses for any type of cycle, and during setup is used to latch A0-A2 so that the correct POS register may be accessed.

The -RDPOS and -WRPOS signals are used to control optional external POS register functions. They are valid for any POS read or write operation accompanied by -CDSETUP. The timing for these signals approximates that of -IOWR and -IORD.

If CHRESET is asserted at any time, any bus cycle in progress is immediately halted and the D0-D7 outputs of the EPB2001 chip tristated. Similarly, the board control lines go immediately to an inactive state.

The -MEMRD, -MEMWR, -IORD, and -IOWR out-

puts have 24mA push-pull output drivers. The -DEN, DT/-R, -RDPOS and -WRPOS outputs have 6mA push-pull drivers.

The only time the EPB2001's internal transceiver (connected to D0-D7) is enabled to the MC Bus is during an I/O Read or -CDSETUP.

POS REGISTER FILE

The POS register file is accessible through the dedicated transceiver associated with pins D0-D7 on the EPB2001. Data is transferred to the selected POS register (during a write operation) while -CMD is low. The rising edge of -CMD latches the input data into the register. Data is read from the POS registers while -CMD is low, and will become valid at the D0-D7 pins within the period specified below from the -CMD leading (falling) edge.

The POS register section contains required POS registers. These reside in a block at I/O addresses 0100-0105Hex for all adapters. All registers are byte-wide. Locations 0100 and 0101 are the board I.D., and are read-only non-volatile ERPOM locations. POS registers 0102-0105 are user-defined, with the exception of three bit locations.

POS register 0102, bit 0 is used as a card enable bit for all adapters. This bit is reset by CHRESET, or by the processor writing a "zero" to this bit during a -CDSETUP cycle. When zero, the EPB2001 (and adapter) will not respond to any normal bus cycles. Ony setup reads and writes are allowed. When set to a "one" by the processor, the card is enabled. This bit may not be written by normal I/O Write operations to location 0102. The -BDENBL signal on the board interface reflects the state of this bit for on-board use. This pin uses a 24mA open drain output structure.

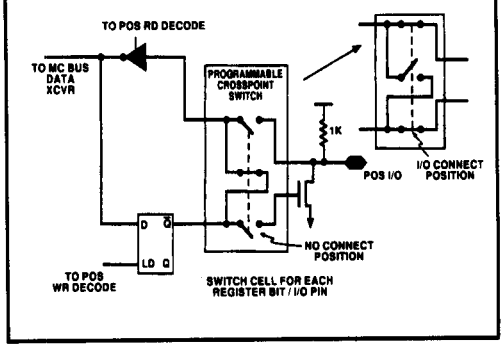
POS register 0105, bit 7 is used as a channel check flag. A card reports non-maskable interrupts (NMI) to the processor by asserting the -CHCK (channel check) line, which is wire-ORed to all cards. On the EPB2001, a pulse on the -SETCHK input will reset this bit to a -CHCK output on the MC Bus. This bit is set by a CHRESET or a write to this location with a one in the bit 7 position. The bit may also be reset by a write to 0105 with zero data in the bit 7 location.

Bit 6 of register 0105 is used if channel check exception status is provided in optional POS registers 0106 and 0107. If used, these registers would typically be implemented in components such as 74LS374's. If status is available, a zero will be found in this location. If status is not provided, a one will be found there. If this bit is used for this purpose on the EPB2001 chip, one of the programmable POS I/O pins on the board interface may be used to force the appropriate value.

All remaining bits are user-defineable. These bits may be used for address remapping control or just general input or output port functions on the board (software-controlled "jumpers" or status bits). Each POS I/O pin is independently programmable as input or output, and may be assigned to any POS register bit. The remapping function will be covered in the Chip Select Logic section below.

The connection of any of the 32 POS register bits (locations 0102-0105, exclusive 0102 bit 0) with the 16 dedicated POS I/O pins on the board interface is controlled by a user-programmable cross-point switch arrangement. Each POS I/O pin has a 6mA open drain output structure as well as an input path. On the output side, a programmable matrix takes the output of any of the POS register bits and assigns it to any of the 16 output lines. Since the pins are open drain, if a "one" is written to a given POS Register bit from the MC Bus, the associated I/O pin is not driven. This allows the I/O pin to be driven by an external signal source, and subsequently for its value to be read through the corresponding POS Register bit location. Forcing a value from the POS I/O pins does not, however, change the value in the POS Register location (see Figure 3).

Figure 3. POS I/O Configuration



CHIP SELECT LOGIC

The Chip Select logic on the EPB2001 provides up to 8 user-programmable Chip Selects. Each chip select (-CS0-7) output may have up to eight pre-programmed address ranges over which it is active. The granularity of these chip selects may range from one location to the entire 24-bit (16Megabyte) available physical address range. Each may be defined for either memory or I/O mapping. All 24 MC Bus addresses and the M/-IO input enter the programmable logic arrays.

An additional input to the programmable chip select arrays is provided to act as an enable for the chip selects if so desired. Typically, this would be connected to the MADE24 MC Bus signal, to qualify chip selects when 32 bit addressing is involved.

Normally, chip select outputs are not latched in any fashion, and are valid only for the duration of a valid address/M/-IO combination on the bus. Optionally, the chip select outputs may be latched by user-programmable flow-through latches using -ADL. This may be done on an individual chip select basis. This results in the affected -CS output(s) going active a short time after -ADL has gone active low (the A0-A23 address lines and

M/-IO input having stabilized well before -ADL falls). The outputs are then latched on the -ADL rising edge and remain active until the next bus cycle (-ADL goes low again). Latched/non-latched operation for each chip select output is determined by the user when the device is programmed.

The chip select logic is implemented as eight distinct logic blocks (one per chip select). Each block consists of an eight word by 52 bit programmable memory (416 bits) feeding a comparator along with the address and other required inputs. Each word corresponds to a desired chip select active range. Effectively, any input bit may be compared for zero, one or don't care in determining an address match. Thus, the need for two bits per input (26 inputs × 2 = 52 bits) to encode these possibilities.

The selection of one of the eight available chip select ranges to be used for a particular chip select output (corresponding to one of the eight words in each of the blocks) is done by user-defined combinations of POS register bits. A user may define which POS register bits, and which bit combinations, will activate a given chip select range. This information is coded into a programmable decoder on the device which generates an enable for each range. The PS/2 operating system may remap address ranges during the POST if there is a conflict, i.e., two cards which might respond to the same address ranges. This is done by changing (writing) the POS register bits controlling the chip selects, and hence enabling a new address range.

All of the chip select outputs (active low) are logically ANDed together to form the -CDSFDBK signal presented to the MC Bus. This output signals a valid bus cycle for the adapter to the PS/2 MPU, acting as a cycle acknowledge line. -CDSFDBK is active low, and has a 6mA push-pull driver.

In the case of CHRESET active, all the chip select latches are immediately cleared to the inactive (high) state.

Each -CS output has a 6mA push-pull driver, and is active low.

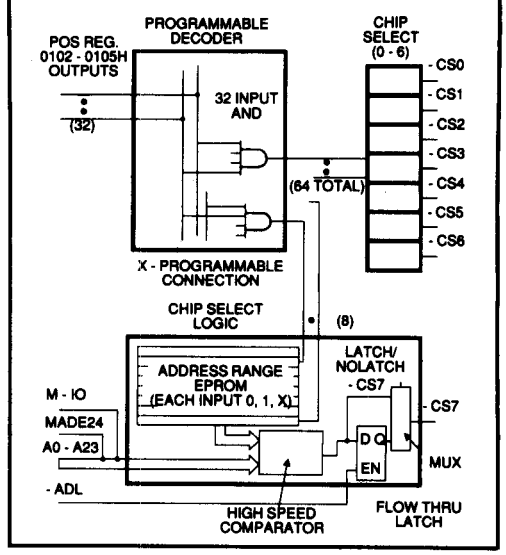
EPB2002 FUNCTIONAL DESCRIPTION

The EPB2002 device performs the bus arbitration functions for the Micro Channel interface. There are two primary sections to the chip, one the POS register function, the other the bus arbitration state machine.

POS REGISTER

The Micro Channel Bus specification requires that each adapter interface that supports DMA functions have an MPU-programmable DMA arbitration/priority level (4 bits) and a so-called arbitration Fairness bit. These bits configure a given board's DMA function at PC boot time. These five bits may be placed anywhere in the 31 available POS Register bits, as defined by the board designer. The EPB2002 chip has five bi-directional

Figure 4. Chip Select Logic



data bus lines, D0-D4, capable of driving the Micro Channel data bus. The block diagram of the device is shown in Figure 6. Since these pins can be connected to any of the Micro Channel bus lines arbitrarily (device D0 pin could be connected to MC Bus D7), it is possible to map any of these bits into any arbitrary set of five POS register bit positions. The bit position is programmable by virtue of the connections to the device in the actual p.c. board.

In order to program which POS byte these bits will reside in, the SEL0-3 lines come into play. These lines act as multiple chip select inputs for the EPB2002 device. SEL0-1 are active high, while -SEL2-3 are active low. By connecting the SEL lines to the appropriate MC Bus address lines, the registers may be placed into any of the four valid POS register positions.

	MC Bus Address			EPB2002 Connection SELI			
REGISTER	A2	A1	A0	3	2	1	0
0102H	0	1	0	A2	A0	A1	1
0103H	0	1	1	A2	0	A1	A0
0104H	1	0	0	A1	A0	A2	1
0105H	1	0	1	A1	A2	A0	

"0" and "1" in the Connections section correspond to hard strapping these pins to either ground or Vcc to obtain the corresponding mapping.

Note that all five bits must, as a result, be in the same POS Register byte.

The -RDPOS and -WRPOS signals provided by the EPB2001 chip act as read and write strobes for

the EPB2002 chip. Since there is only one five bit register on the EPB2002, any -RDPOS in conjunction with valid inputs on SEL0-3 will read the MC2 register to the D0-4 pins, and any -WRPOS signal with appropriate SEL inputs will write the EPB2002 register. -ADL latches the SEL inputs just as with addresses on the EPB2001. Timing for these operations is shown below.

ARBITRATION LOGIC

Arbitration for the MC Bus occurs during defined periods, centrally coordinated by the PC MPU. The ARB/-GNT line is the system control line which signals periods during which arbitration may occur. When high, it signals that an arbitration cycle is in progress. An adapter signals that it would like to obtain control of the bus (initiate an arbitration cycle) by driving the -PREEMPT signal low. When ARB/-GNT goes high in response, all adapters wishing bus control participate in the bus arbitration process (with one exception, see Fairness discussion below).

Arbitration levels are the means whereby the system configures the priority of a given adapter's DMA requests at system configuration. The four bits in the EPB2002's registers, as defined by the Micro Channel spec, allow sixteen different arbitration levels or priorities. Lower numbers are higher priority, so 0000 would correspond to highest priority, 1111 lowest. During arbitration, the highest priority (lowest arbitration level) adapter will win the next bus cycle.

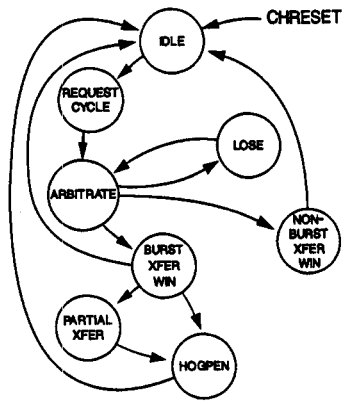
The basic arbitration process is straightforward. When ARB/-GNT goes high, all adapters wishing control of the bus place their arbitration levels on the ARB0-3 lines. (All adapter outputs are wire-ORed together.) If a value lower than the arbitration level of a given adapter is detected on the ARB0-3 lines by that adapter, it realizes a higher priority device is requesting the bus. As a result, it releases the low-order bits of its arbitration level. This allows the arbitration level of the highest priority requestor to appear on the bus after some settling time. When ARB/-GNT goes low, the highest priority device sees its arbitration level on the bus and has control of the bus (one cycle only in the case of non-burst mode). Devices which lose the arbitration cycle continue to assert -PREEMPT until the request is satisfied.

Should ARB/-GNT go to arbitrate unexpectedly, devices are expected to reenter arbitration immediately, even if ownership of the next bus cycle has already been granted.

The EPB2002 device supports this operation. If the -BUSREQ line is asserted, the EPB2002 will assert -PREEMPT and arbitrate as described for the next cycle using the arbitration level programmed into its register. When the bus is granted, BUSGNT will be asserted until -BUSREQ rises, signalling end of transfer.

Burst operation allows a device to hold the bus for multiple contiguous cycles. This can give greater transfer efficiency since every bus cycle does not have to be arbitrated for. The obvious danger is that a device may hog the bus, starving other adapters. The MC Bus spec specifies a fairness mechanism to avoid this. The process is as follows:

Figure 5. EPB2002 State Machine

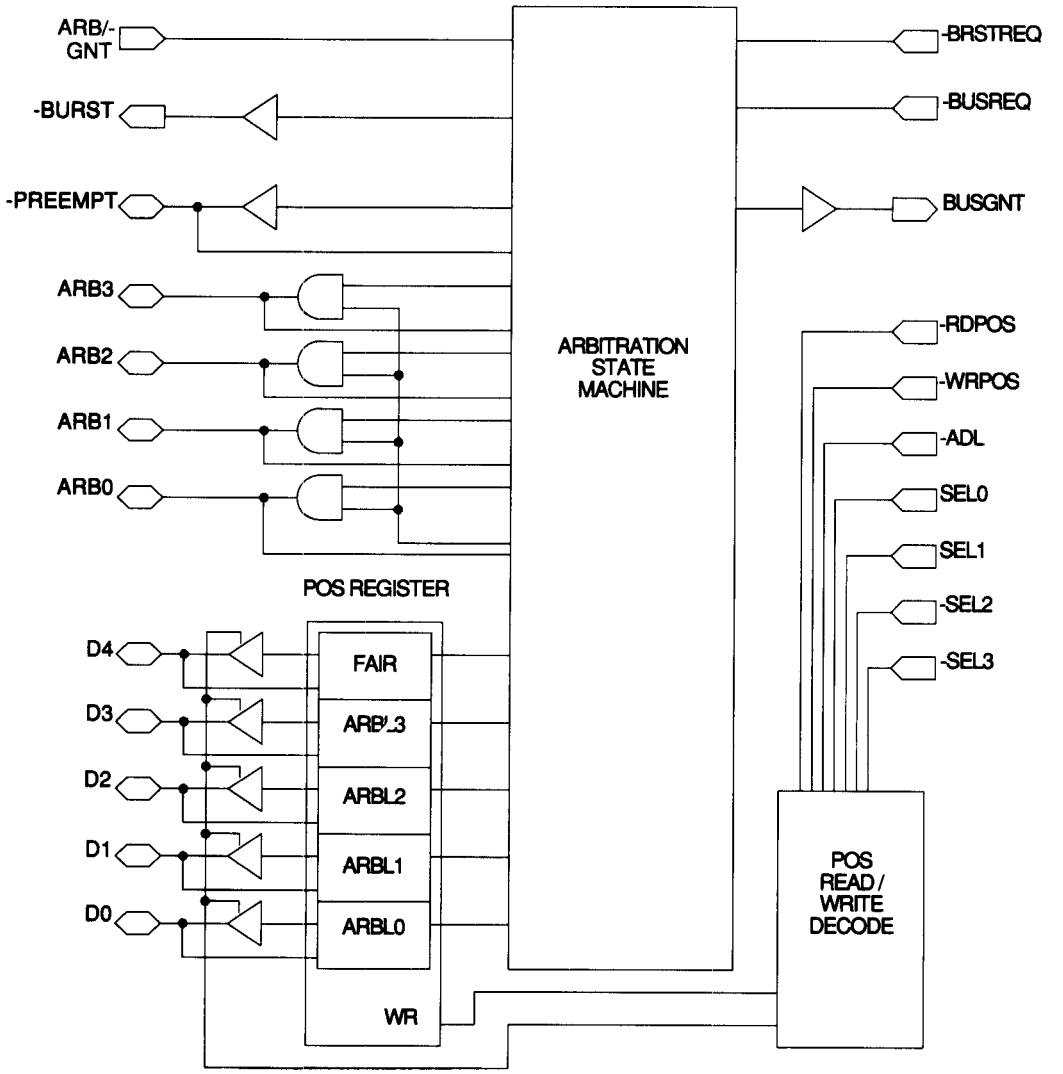


A device enters a burst transfer by arbitrating for the bus in a normal fashion and then asserting -BURST when the bus is granted. The -BURST line is asserted as long as the burst transfer lasts. The PS/2 processor will not honor any -PREEMPT bus requests while -BURST is low. As a result arbitration cycles will be suspended. The manner in which bus hogging is avoided is that the adapter which has control of the bus monitors the common -PREEMPT line. If -PREEMPT is asserted during its burst transfer, the adapter must finish-up its transfer in an orderly fashion and then release -BURST. Once -BURST is released, the PS/2 MPU is free to run a new arbitration cycle. During this arbitration cycle, the adapter releasing the bus does not participate to avoid bus hogging.

The EPB2002 supports burst operation by means of a -BRSTREQ input. If -BRSTREQ is asserted, a bus cycle is arbitrated for and when obtained, -BURST is asserted. It is assumed -BRSTTREQ is asserted for as long as the burst transfer is to occur. If preemption of the burst transfer occurs, -BUSGNT will be deasserted immediately. When -BRSTREQ is deasserted in response, -BURST is deasserted. The EPB2002 arbiter will not rearbitrate until the -PREEMPT bus line has gone high. A -BRSTREQ input after this will initiate a new arbitration cycle.

The above burst transfer discussion includes the notion of "fairness"; that is, if a burst transfer is preempted, the device which is "bumped" must wait until all other arbitration requests have been satisfied (signalled by -PREEMPT going high) before re-entering arbitration. The device(s) waiting for this to occur are said to be in the "hog pen". This mode of operation is employed when the fairness bit in the EPB2002 control register is programmed to a one. If this bit is programmed to

Figure 6. EPB2002 Block Diagram



a zero, the burst operation reflects Linear priority. With Linear priority, a bursting adapter which is preempted MAY reenter arbitration on the first available cycle. Obviously, the risk of hogging the bus is now present. The EPB2002 employs the fairness algorithm by default.

PROGRAM ERASURE

Erasure of the programmed connections on the EPB2001 begins to occur on exposure to light wavelengths shorter than 4000 Angstroms. Sunlight and certain types of fluorescent lighting emit wavelengths in the range of 3000 to 4000 Angstroms and can erase a windowed EPB2001 (plastic packaged devices are obviously protected). Constant exposure to room level fluorescent lighting could erase an EPB2001 in approximately 3 years. Direct sunlight thus chould cause erasure in approximately 1 week. If the windowed EPB2001 is to be exposed to these conditions for extended

EPB2002 PIN DESCRIPTION

SIGNAL	TYPE	OUTPUT DRIVE (mA) IOH	IOL	DESCRIPTION
ARB/-GNT	I			Arbitration cycle strobe input from the MC Bus. When HIGH, arbitration for the MC Bus is occurring. If the EPB2002 has a pending DMA request of either type, it enables ARB0-ARB3 during this interval to compete for the bus.
-BURST	OD		24	Active LOW burst DMA cycle output. Asserted for the duration of a burst DMA transfer if the bus is granted as a result of -BRSTREQ active. Deasserted on CHRESET.
-PREEMPT	I/OD		24	Bidirectional bus preempt output and input. Driven LOW by the EPB2002 upon a -BUSREQ or -BRSTREQ input to request a bus arbitration cycle. Released when the bus is granted. Deasserted on CHRESET. If detected asserted during burst DMA transfer, indicates premature termination request from another adapter, and transfer is terminated.
D0-D4 (5x)	TS	4	24	Tristate bidirectional data bus lines. POS register read/write data access path. Enabled to the MC Bus when SEL inputs select the device and -RDPOS is asserted. D0-D3 are associated with POS register bits ARBL0-ARBL3, respectively, D4 with Fairness bit.
ARB0-ARB3 (4x)	I/OD		24	Bidirectional arbitration bus lines. Initially, adapter's arbitration level is output when ARB/-GNT is HIGH and DMA request is pending. Final bus value matches highest priority request. If value on bus matches adapter's arbitration level when ARB/-GNT returns LOW, adapter has won the bus.
-ADL	I			Active LOW address input latch. Trailing edge of this signal is used to latch SEL inputs.
SEL0, SEL1, -SEL2, -SEL3	I			POS register select inputs. SEL0 and SEL1 must be HIGH while -SEL2 and -SEL3 are LOW to access the POS register. Latched by -ADL on its rising edge.
CHRESET	I			Active HIGH channel reset input. The EPB2002 deasserts all active outputs a short time after CHRESET rises, and the arbitration state machine returns to IDLE.
-BRSTREQ	I			Active LOW burst DMA transfer request. Input is unlatched and must remain valid for the duration of the cycle request and subsequent transfer. Must be deasserted during last DMA bus cycle to terminate bus ownership.
-BUSREQ	I			Active LOW single transfer DMA request input. Input is unlatched and must remain valid for duration of the request until BUSGNT is asserted. Must be deasserted following BUSGNT to terminate bus ownership.

EPB2002 PIN DESCRIPTION (continued)

SIGNAL	TYPE	OUTPUT DRIVE (mA) IOH	IOL	DESCRIPTION
BUSGNT	TP	4	6	Active HIGH bus grant output. Driven active when bus ownership is won as a result of arbitration cycle. Remains active until DMA request is dropped or -PREEMPT is detected signalling early burst termination request. Goes inactive on CHRESET.
-WRPOS	I			Active LOW write POS register strobe input. Data is written from D0-D4 to the register when the chip is selected and -WRPOS is LOW.
-RDPOS	I			Active LOW read POS register strobe. POS register data is presented on D0-D5 when the device is selected and -RDPOS is LOW.
VCC (2x)				+5 Volt Power Supply.
VSS (3x)				Ground.

Signal Types:
I = Input
TP = Totem-Pole (Push-Pull) Output
OD = Open-Drain Output
TS = Bidirectional Tristate Output I/O
I/OD = Bidirectional Open-Drain Output I/O

periods, an opaque label should be placed over the window.

The EPB2001 may be erased and reprogrammed as many times as needed within the limits described and using the recommended procedure.

LATCH UP & ESD PROTECTION

The EPB2001 and EPB2002 input, output and I/O pins have been designed to resist electro-static discharge (ESD) and latch-up damage. Each of the device pins will withstand voltage energy levels exceeding those specified by MIL STD 883C. Pins will not latch-up for input voltages between -1V and V_{CC} + 1V with currents up to 100mA. During transitions the inputs may undershoot to -2.0V for periods less than 20nS. Additionally, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DESIGN SECURITY

The EPB2001 contains a programmable design security feature that controls access to information programmed into the device. If this programmable feature is used, the custom pattern in the device is secured from external interrogation and possible reverse engineering. On an erasable EPB2001 the bit that controls this function, along with other design data stored in EPROM, may be erased using ultraviolet light as described above. This feature may be invoked by the user as part of the design entry process while using MCMap.

MCMAP DEVELOPMENT SYSTEM

Altera provides a PC-based design development system called MCMap to support efficient design and use of the EPB2001. This software package features an interactive, table-driven input scheme. The designer is prompted for information concerning the programmable portions of his design: board i.d., chip select ranges, POS register bit combinations used as enables, etc. Real-time error checking reports any errors as they are entered. When entry is complete, a JEDEC programming file for the EPB2001 is compiled in seconds.

Programming of the EPB2001 also occurs on the PC, using Altera's PLP4 programming card and PLE3-12 Master Programming Unit. The PLEJ2001 Programming Adapter provides an interface between this general-purpose hardware and the 84 lead EPB2001 chip carrier package. For more information concerning Development Systems, please contact Altera Corporation.

The recommended PC system requirements for Altera's MC Map software and hardware are:

- IBM XT, AT or Compatible PC
- EGA (extended memory), CGA, or Hercules Graphics Adapter
- 640 KBytes RAM
- 10MByte Hard Disk and 5.25 inch Floppy Drive
- DOS Version 3.3 or later

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	With respect to GND (note 2)	-2.0	7.0	V
V_{PP}	Programming Supply Voltage		-2.0	13.5	V
V_I	DC Input Voltage	(Note 2)	-2.0	V_{CC} + 1.0	V
I_{MAX}	DC V_{CC} or GND Current		-500	+500	mA
I_{OUT}	DC Output Current per Output Pin		-50	+50	mA
P_D	Power Dissipation			1000	mW
T_{STG}	Storage Temperature	No Bias	-65	+150	°C
T_{AMB}	Ambient Temperature	Under Bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	Input Voltage		0	V_{CC}	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		0	70	°C
T_R	Input Rise Time			250	nS
T_F	Input Fall Time			250	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH Level Input Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW Level Input Voltage		-0.3		0.8	V
V_{OH}	HIGH Level Output Voltage	See Table 1 & 2	2.4			V
V_{OL}	LOW Level Output Voltage	See Table 1 & 2			0.50	V
I_I	Input Leakage Current	V_I = GND or V_{CC}	-10		+10	μA
I_{OZ}	Output Hi-Z Leakage Current	V_O = GND or V_{CC}	-10		+10	μA
I_{CC} EPB2001 EPB2002	V_{CC} Supply Current	V_I = GND or V_{CC} No Load				 mA mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{OUT} = 0V f = 1.0 MHz note (3)			pF
$C_{I/O}$	I/O Capacitance				pF
C_{OD}	Output Capacitance				pF

AC OPERATING CHARACTERISTICS

EPB2001

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T1	-ADL Width		40			ns
T2	-ADL HIGH to -S0, -S1 HIGH		25			ns
T3	-S0, -S1 LOW to -ADL LOW		12			ns
T4	-ADL LOW to -CMD LOW		40			ns
T5	MADE24, M/-IO, A0-A23 Valid to -S0, -S1 LOW		10			ns
T6	-S0, -S1 LOW to -CMD LOW		55			ns
T7	-CMD LOW to -S0, -S1 HIGH		30			ns
T8	-CMD Width		90			ns
T9	-CMD LOW to -MEMRD, -MEMWR, -IORD, -IOWR, -RDPOS, -WRPOS LOW				20	ns
T10	-CMD HIGH to -MEMRD, -MEMWR, -IORD, -IOWR, -RDPOS, -WRPOS HIGH				20	ns
T11	-ADL LOW to DT/-R HIGH				20	ns
T12	-ADL LOW to DT/-R LOW				20	ns
T13	-CMD LOW to -DEN LOW (READ Cycle)				20	ns
T14	-CMD HIGH to -DEN HIGH (READ Cycle)				20	ns
T15	DT/-R LOW to -DEN LOW (WRITE Cycle)				20	ns
T16	-MEMWR, -IOWR HIGH to -DEN HIGH				20	ns
T17	MADE24, M/-IO, A0-A23 Valid to -ADL LOW		45			ns
T18	MADE24, M/-IO, A0-A23 Hold from -ADL HIGH		25			ns
T19	MADE24, M/-IO, A0-A23 Valid to -CS0-7 LOW				30	ns
T20	MADE24, M/-IO, A0-A23 Valid to -CDSFDBK LOW				60	ns
T21	MADE24, M/-IO, A0-A23 Invalid to -CDSFDBK HIGH				60	ns
T22	-CMD LOW to D0-D7 Valid (READ Cycle)				60	ns
T23	-CMD HIGH to D0-D7 Tristate				40	ns
T24	D0-D7 Valid to -CMD LOW (WRITE Cycle)		0			ns
T25	D0-D7 Hold from -CMD HIGH (WRITE Cycle)		30			ns
T26	POSI/O Input Valid to POS Data Valid				175	ns
T27	-CMD LOW to POS Register Data Valid				30	ns
T28	POS Register Data Valid to POSI/O Valid				500	ns
T29	CHRESET Width		100			ns
T30	-SETCHK LOW to -CHCK LOW				30	ns
T31	CHRESET HIGH to -CHCK, -BDENBL, -DEN, -MEMWR, -MEMRD, -IOWR, -IORD, HIGH				30	ns
T32	CHRESET HIGH to D0-D7 Tristate				30	ns

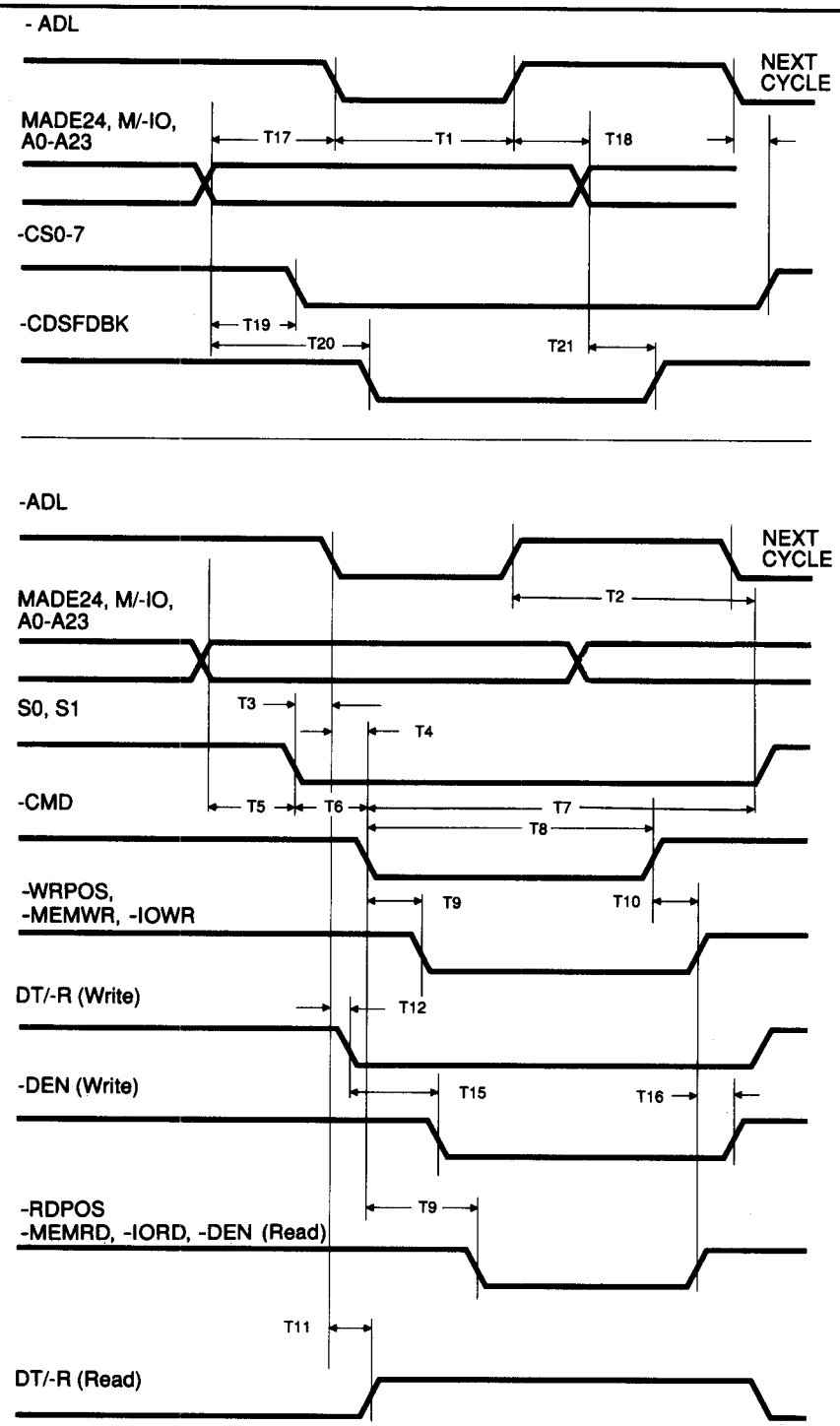
Notes:
1. Typical Values are at T_A = 25°C, V_{CC} = 5V.
2. Minimum DC input is -0.3V. During transitions, inputs may undershoot to -2.0V for periods less than 20ns.
3. Capacitances measured at 25°C. Sample tested only.

AC TIMING OUTPUT CAPACITANCE LOADINGS

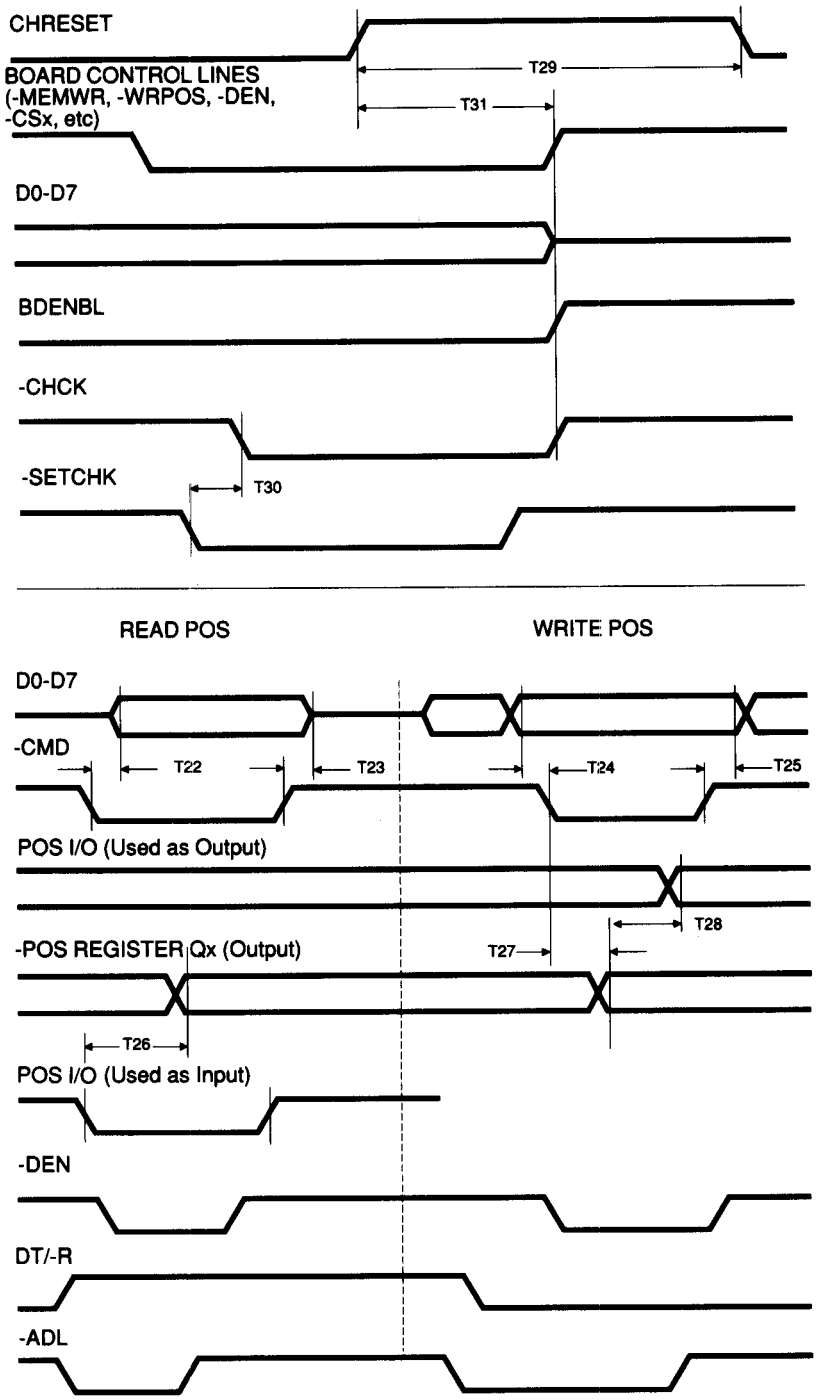
EPB2001

OUTPUT PINS	LOAD CAPACITANCE
-CS0-7, -DEN, DT/-R, POSI/O 0-15, -WRPOS, -RDPOS	50pF
-BDENBL, -MEMRD, -MEMWR, -IORD, -IOWR	200pF
-CDSFDBK, -CHCK, D0-D7	240pF

EPB2001 WAVEFORMS



EPB2001 WAVEFORMS (continued)



AC OPERATING CHARACTERISTICS

EPB2002

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T40	-ADL Width		40			ns
T41	-RDPOS LOW to D0-D4 Valid				50	ns
T42	D0-D4 Hold from -RDPOS HIGH		30			ns
T43	D0-D4 Set-up to -WRPOS LOW		0			ns
T44	D0-D4 Hold from -WRPOS HIGH		20			ns
T45	D0-D4 Valid to POS Register Output Valid				20	ns
T46	SEL0-1, -SEL2-3 Set-up to -ADL LOW		10			ns
T47	SEL0-1, -SEL2-3 Hold from -ADL HIGH		25			ns
T48	-BUSREQ, -BRSTREQ to -PREEMPT LOW				70	ns
T49	ARB/-GNT LOW to -PREEMPT HIGH				50	ns
T50	-BUSREQ, -BRSTREQ HIGH to BUSGNT LOW				40	ns
T51	-BRSTREQ HIGH to -BURST HIGH				45	ns
T52	ARB/-GNT Width			300		ns
T53	ARB/-GNT LOW to -BURST LOW				50	ns
T54	ARB/-GNT LOW to BUSGNT HIGH				60	ns
T55	ARB/-GNT HIGH to ARB0-ARB3 Valid				50	ns
T56	ARB/-GNT LOW to ARB0-ARB3 Hi-Z				50	ns
T57	ARB0-ARB3 Set-up to ARB/-GNT LOW		50			ns
T58	CHRESET HIGH to BUSGNT, -BURST, -PREEMPT, ARB0-ARB3 inactive				50	ns

Notes:
1. Typical Values are at T_A = 25°C, V_{CC} = 5V.
2. Minimum DC input is -0.3V. During transitions, inputs may undershoot to -2.0V for periods less than 20ns.
3. Capacitances measured at 25°C. Sample tested only.

AC TIMING OUTPUT CAPACITANCE LOADINGS

EPB2002

OUTPUT PINS	LOAD CAPACITANCE
-BURST, -PREEMPT, ARB0-ARB3	200pF
D0-D4	240pF
BUSGNT	50pF

EPB2002 WAVEFORMS