AZ9031

Memory / Bus Controller*

Introduction

The Dual Port Memory Controller / Bus and Processor Controller described herein, acts as the functional control link between the synchronous and asynchronous environments found in the SLIK™ bus, and the Micro Channel® bus. This part provides the signals necessary to control the data flow between these two different environments.

The AZ9031 Memory / Bus Controller consists of three major sections:

- Processor to Memory control
- Processor to Micro Channel bus control
- Micro Channel bus to Memory control

Memory accesses between the CPU and main memory are controlled by a synchronous state machine. The interface between the CPU and Micro Channel bus is controlled by a separate synchronous state machine. Memory accesses between the Micro Channel bus and main memory are controlled by an asynchronous DRAM controller. The AZ9031 supports the 80486 CPU with maximum frequencies of 25 MHZ and 33 MHZ.

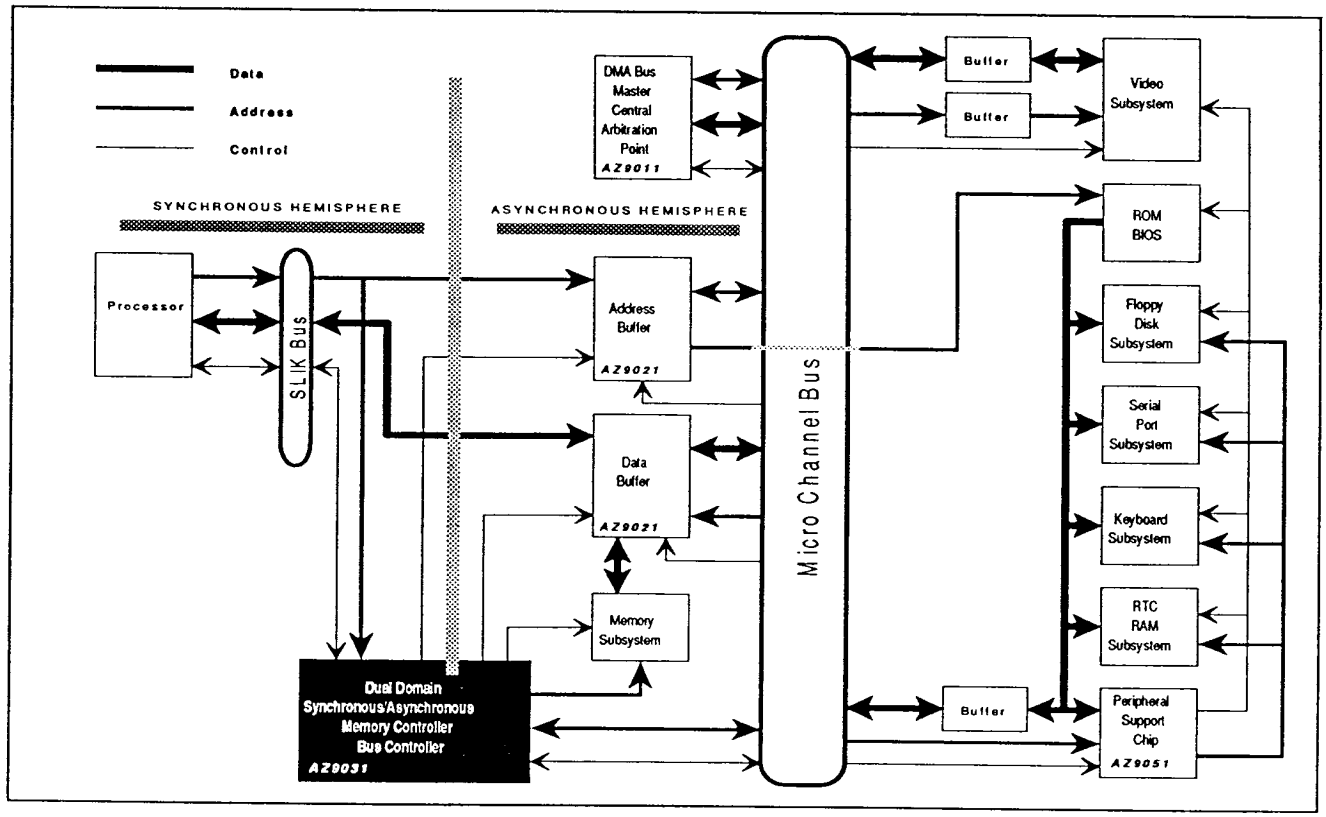


Figure 1. System Block Diagram

BMA

* Patent Pending

Memory Controller

The purpose of the Memory Controller is to interface the DRAM to the rest of the system. It does this by converting control signals from the Micro Channel bus and SLIK bus into control signals for the DRAM. The Memory Controller also produces signals to control the buffers connected between the DRAM and the various buses.

The BIOS ROM address range (0E0000H - 0FFFFH) can be duplicated in DRAM at the same address to speed up BIOS accesses.

Address multiplexing is performed internally. The Memory Controller determines if the address is from the processor or the Micro Channel bus and sends this address to the DRAMs. Address decode logic checks valid memory addresses.

Split memory is controlled by the address multiplexers. The memory physically installed above 512K or 640K and within the first 1M page can be reassigned to an address specified in a register.

Memory Bank Organization

The Memory Controller can support four banks of four megabyte memory for a total of sixteen megabytes. 1MX1 Drams are supported. To get 16 Mbytes, 144 1MX1 chips are required.

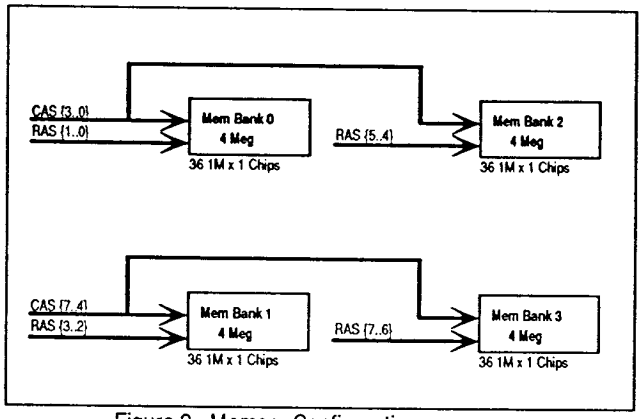


Figure 2. Memory Configuration

The DRAM address is buffered externally to the Memory Controller. One driver per bank is preferred. WEN is also buffered externally to the part.

RAS and CAS lines drive the DRAMs directly. Each CAS line drives two banks. There are two RAS lines per bank.

See figure 2.

Page Mode

The memory uses 4K byte pages. If a memory request accesses the current page, a page mode hit occurs and the access time is reduced. The Memory Controller does this with page mode compare logic. This logic stores the previous RAS address. The current RAS address is then compared to this to determine if a Page Mode hit occurred.

Memory Cycle Times

	486 Burst
Read Page Hit	4,3,3,3
Read Page Miss	9,3,3,3
Write Page Hit	3
Write Page Miss	8

Memory Access

The Memory Controller allows the CPU and coprocessors to address DRAM from one bus and the Micro Channel bus from another. This speeds private bus accesses to memory because they are independent of Micro Channel control. The DMA controller and bus masters access system memory through the Micro Channel bus.

A synchronous memory control state machine cycles the DRAM control signals for private bus access. It operates from the processor clock to meet the CPU timing requirements.

An asynchronous memory control state machine cycles the DRAM control signals for Micro Channel accesses to memory. It is operated from Micro Channel control signals to meet Micro Channel timing requirements.

Second Level Cache

The Memory Controller supports a second level cache solution. The Memory Controller will recognize second level cache Hit or Miss information via the STARTN input.

Bus Controller

The Bus Controller generates the control strobes necessary to facilitate communication between the processor on the SLIK bus and devices of 8, 16, or 32 bits in width on the Micro Channel bus. The interface between the processors on the SLIK bus and the Bus Controller is synchronous in nature. The Micro Channel bus is asynchronous. The processor has a data width of 32 bits. The devices on the channel can have data widths of 8, 16 or 32 bits. Any discrepency between the data sizes of the processor, and the device accessed, will be taken care of by the data buffer part which is controlled by the Bus Controller.

The state machine in the Bus Controller first senses that an access has been requested. If a read access to onboard system memory is requested, then the Bus State Machine, and thus bus control strobes for this access can be disabled, thereby allowing a much faster access than could be achieved through the Micro Channel bus.

The Bus controller is made up of 2 basic blocks. These blocks are the Status Interpreter, and the Bus State Machine.

Status Interpreter

This portion of the Bus Controller interprets the status information and detects that a processor has requested a bus access or an access to system board memory. It determines what type of access has been requested. This section also provides the stimulus to the Bus State Machine to start its bus cycle activity.

See Table 1.

Bus State Machine

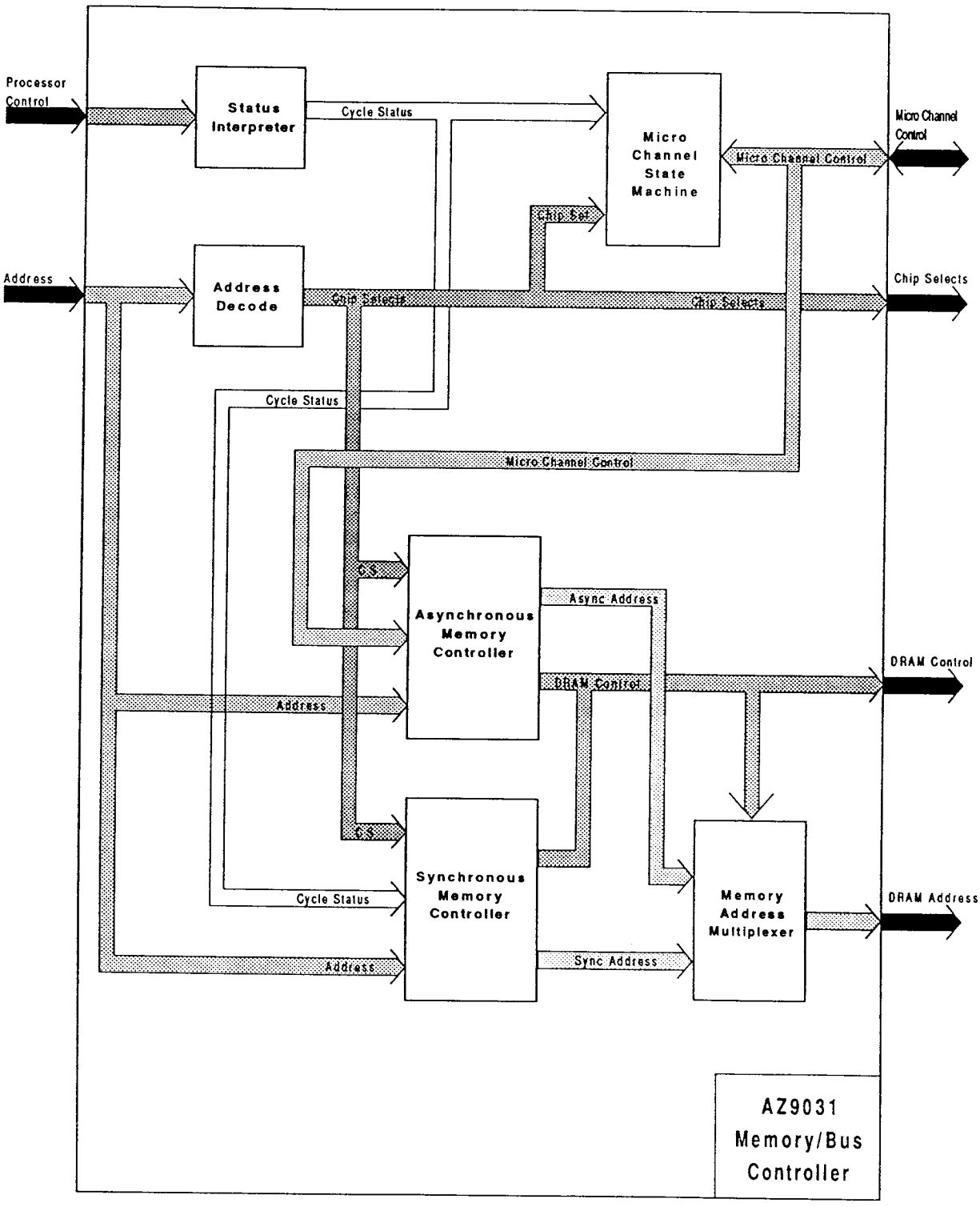
This portion of the Bus Controller drives the bus control strobes for the Micro Channel bus, when a processor on the SLIK bus has requested a Micro Channel bus access. It also provides information internally to the Bus Controller to indicate which portion of the cycle is presently being executed. The Bus State Machine also generates the ready line to the processor. This is generated from information present in the bus controller state machine, in addition to the I/O Ready lines provided as inputs to the chip, and strobe disable information used in a fast onboard memory access.

STATUS DEFINITION:

	PWRI	PDAT	PMEM	S0N	S1N
INTERRUPT ACKNOWLEDGE	0	0	0	0	0
CODE READ {memory read}	0	0	1	1	0
IO READ	0	1	0	1	0
MEMORY READ	0	1	1	1	0
SPECIAL CYCLES	1	0	0	1	1
SHUTDOWN {PBE3N-PBE0N = E}	1	0	0	1	1
FLUSH {PBE3N-PBE0N = D}	1	0	0	1	1
HALT {PBE3N-PBE0N = B}	1	0	0	1	1
WRITE BACK {PBE3N-PBE0N = 7}	1	0	0	1	1
NA	1	0	1	1	1
IO WRITE	1	1	0	0	1
MEMORY WRITE	1	1	1	0	1

Table 1. Status Definitions

Block Diagram



System Memory Interface

RAS7N-RAS0N: Row Address Strobe. These active low outputs are used to strobe the row address into the DRAM. These signals directly drive the dynamic memory devices in the main system memory. RAS0-1 are used for bank0, RAS2-3 for bank1, RAS4-5 for bank2 and RAS6-7 for Bank3.

CAS7N-CAS0N: Column Address Strobe. These active low outputs are used to strobe the column address into the DRAM. These signals directly drive the dynamic memory devices in the main system memory. CAS3-0 are used for bytes 3-0 of banks 2 and 0. CAS7-4 are used for bytes 3-0 of banks 3 and 1.

WEN: Write Enable. This active low output indicates that the current DRAM access is a write to memory. If not asserted, the access is a memory read. This signal is buffered before driving all four banks of memory.

MA(9-0): Memory Address. These outputs transmit both row and column addresses that are strobed with RAS and CAS. These signals are buffered before driving all four banks of memory.

ROMCSN: ROM Chip Select. This active low output indicates an active ROM address decode.

SPLTENA: Split Enable. This active low input enables split memory addressing. This signal is used to determine RAM address decoding.

SPLT(23-20): Split Addresses 23:20. These active high inputs indicate the starting address of the split memory block. These signals are used to determine RAM address decoding.

BK1N,BK0N: Bank Enables. These active low inputs are used to determine which of the 4 banks of RAM are enabled.

BK0	BK1	
1	1	Bank 0 enabled
1	0	Bank 0-1 enabled
0	1	Bank 0-2 enabled
0	0	Bank 0-3 enabled

RAMCSN: RAM Chip Select. This active low output indicates that a system board memory access from the processor on the SLIK bus has been decoded.

ROMENA: ROM Enable. This active high input indicates how addresses E0000-FFFFF are assigned. When this signal is a 1, reads to this address space go out to ROM and writes to the RAM. This facillitates copying the ROM data into the RAM. When this signal is a 0, reads to this address space go to the RAM and writes are disabled.

EN640N: 640K Split Enable. This active low input indicates where the split addressing occurs. If this bit is a 0, the first 640K of memory is addressed normally and a 248K split address block is mapped to the address range specified by the split address bits. If this bit is a 1, the first 512K of memory is addressed normally and a 384K split address block is mapped to the address range specified by the split address bits.

WDTCLK: Watch Dog Timer Clock. This input is a 14 MHZ clock used to determine if a RAS timeout condition occurs during page mode operation.

STARTN: Start. This active low input indicates that the memory system must complete the current cycle. This signal works with a second level cache.

SLIK Interface

PA(31-2): Processor Address. These inputs, which come from the SLIK address bus, are decoded by the Memory Controller to provide the addressing for the memory.

PBE3N-PBE0N: Processor Byte Enables. These active low inputs come from the SLIK bus and are used to interpret which bytes will be accessed by the processor on the SLIK bus.

PROCLK: Processor Clock. This input is the processor clock pulse. For a 486 system PROCLK is either 33 or 25 MHZ. The AZ9031 uses PROCLK to run the Bus Controller and Synchronous Memory Controller sychronously with the processor.

PADSN: Processor Address / Status. This active low input from the processor indicates that an access has been requested and that a valid address is present on the processor output pins.

PDAT: Processor Data / -Control. This input from the processor indicates whether the current cycle is a Data (high) or Control (low) operation.

PENAN: Processor Enabled. This active low input is the hold acknowledge from the processor or a similiar function from the DMA. If it is not active, the processor releases the SLIK bus and the system board memory to other devices and thus prevents contention.

PMEM: Processor Memory / -IO. This input from the processor indicates whether the current cycle is a Memory (high) or I/O (low) operation.

PWRI: Processor Write / -Read. This input from the processor indicates whether the current cycle is a Write (high) or a Read (low).

RAWRESETN: Raw Reset. This active low input causes the system including the processor to reset for as long as this input is low.

READYN: Ready. This active low output is the READY signal for a return to the processor on the SLIK bus.

EADSN: External Address Valid. This active low output is used by the 486 to invalidate an address in the internal cache memory. The invalid address is presented on the SLIK address bus.

KEN: Cache Enable. This active low output is sent to the 486 to indicate whether the data being returned on the current cycle is cacheable.

BSTRDYN: Burst Ready. This active low output is used to indicate to the 486 that read data is valid during a burst cycle. This signal is sent for the first 3 data transfers of a burst cycle. The burst cycle is terminated with the normal READYN signal. The only type of burst cycle that is performed by the AZ9031 part is a cache line fill from system board memory.

SCEN: Active low secondary cache enable.

PCD: Page Cache Disable. This active high input is used to disable cacheing. When this signal is active the memory control will not do a cache line fill or return KEN.

LOCKN: This active low input indicates that the current bus cycle is locked.

Micro Channel Interface

CBE3N-CBE0N: Micro Channel Byte Enables. These active low inputs are used to designate which bytes will be accessed by the processor on the Micro Channel bus.

CMADE24: Micro Channel Memory Address 24 Bits. This active high input is used to indicate that the device driving the bus is only generating 24 address bits for RAM and ROM decoding, thus address bits CA31-24 should be ignored.

CREFRESHN: Micro Channel Memory Refresh. This active low input is used to accomplish the refresh of the main system memory as well as any other memory on the Micro Channel bus.

ADLN: Address Decode Latch (Micro Channel signal). This active low bi-directional signal is used by channel devices to latch valid address and status bits.

CCMDN: Channel Command (Micro Channel signal). This active low bi-directional signal is used to execute read and write commands on the Micro Channel bus.

IOCHRDY: I/O Channel Ready (Micro Channel signal - CD CHRDY). This input is used by a channel device to extend the time needed to complete an operation. This signal is driven low by a device on the channel if it wishes to extend the cycle.

S1N,S0N: Status Bits 1 and 0 (Micro Channel signals). These bi-directional signals indicate the start and type of a channel cycle.

CMEM: Channel Memory / -IO (Micro Channel signal). This input from the Micro Channel bus indicates whether a memory (high) or I/O (low) cycle is being performed.

DELCMDN: Delayed CCMDN. This active low input is the CCMDN signal delayed by 50 ns. This signal is used to drive RAS high for asynchronous memory accesses.

DELCMD30N: Delayed CCMDN. This active low input is the CCMDN signal delayed by 30 ns. This signal is used to control CAS for asynchronous memory writes.

DELADLN: Delayed ADLN. This active low input is the ADLN signal delayed by 10 ns. This signal is used to switch the address mux during asynchronous memory accesses.

Buffer Control Signals

DT: Bus Data Transmit. When this output is high, it enables data from the processor (SLIK bus) to the Micro Channel. When it is low, the data direction is from the Micro Channel bus to the processor.

PDT: Private Data Transmit. When this output is high, it enables data from the processor (SLIK bus) to the memory bus. When it is low, the data direction is from the memory bus to the processor.

PABLEN: Processor Address Bus Latch Enable. This active low output signal is used to latch various control signals to the address buffers.

BUSY: Busy. This active high output indicates that a processor request from the SLIK bus is being serviced.

PMACN: Private Memory Access. This active low output indicates to the data buffers that a processor request is being made to the main system memory.

LASTCYCN: Last Cycle. This active low input indicates that no more Micro Channel accesses are required to satisfy the SLIK requested access.

3.5 Miscellaneous

SCLK: System Clock. For the 486 mode this signal is not used and should be biased high.

P486: Processor is a 486. This input indicates that a 486 processor is on the SLIK bus.

P33MHZN: Processor runs at 33 MHZ. This input indicates the operating frequency of the processor. This signal is low for a 33 MHZ processor and high for a 25 MHZ processor. PROCLK should be running at the corresponding frequency.

CACHE8MN: Cache 2nd 8 Meg. This active low input indicates whether the 2nd 8 Meg of offboard memory will be cached (i.e. KEN will be returned for memory accesses to the second 8 Meg of memory). This signal only affects offboard memory. All system board memory is cacheable. This signal only affects a 486 system.

CACHE16MN: This active low input indicates whether the system memory from 16 Meg to 256 Meg is cacheable.

Test Signals

TESTN: Test. This active low input signal will tristate all of the bi-direct outputs.

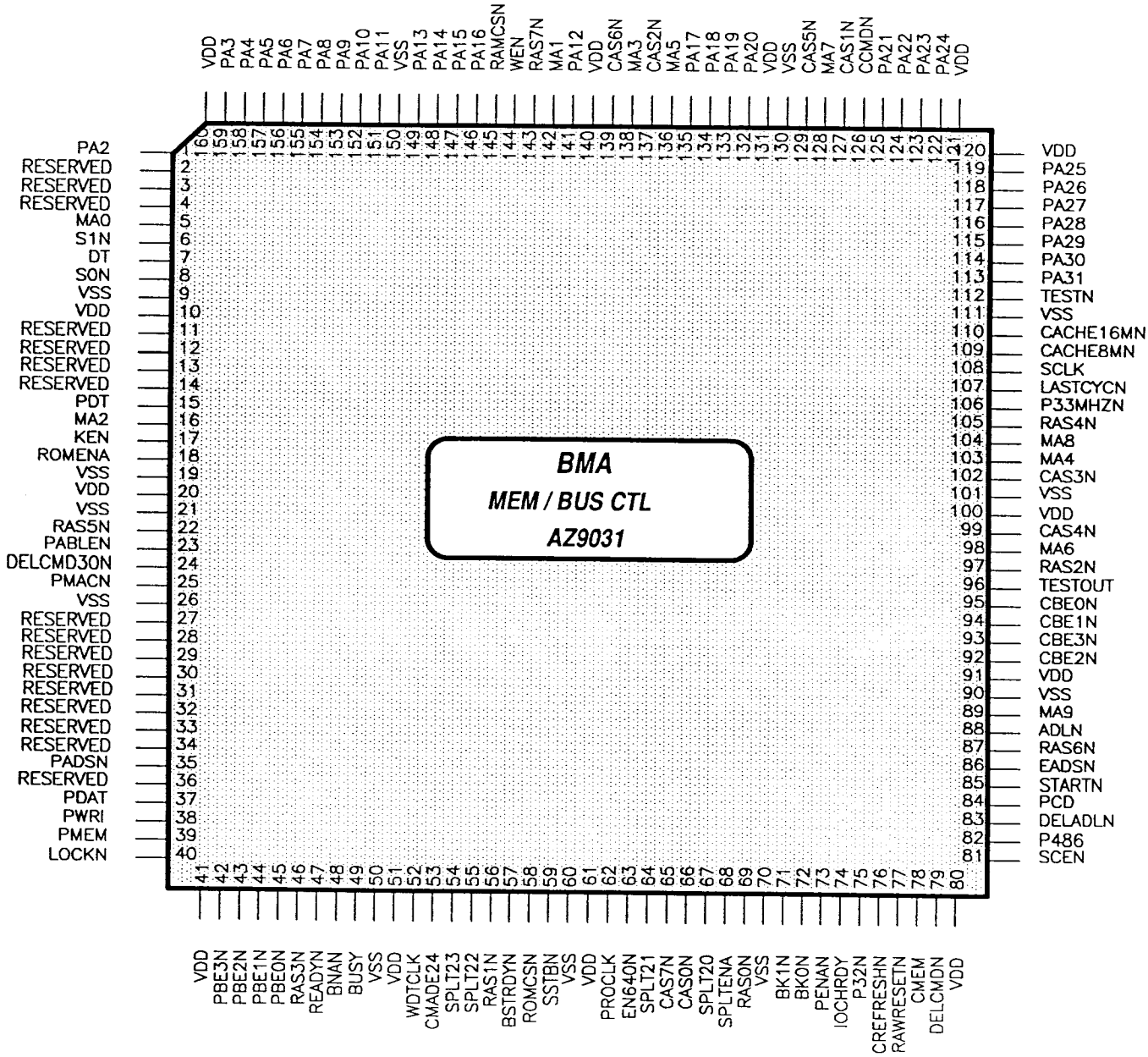
TESTOUT: Testout. This output is the output of the parametric tree that is used during the parametric test.

Others

VDD: Power.

VSS: Ground.

Figure 4. AZ9031 Package Outline



Electrical Specification

Buffer	Type	Attribute	Parameter	Condition	Pins
	I	TTL	VIL=(VSS,0.8V)	4.75V<VDD<5.25V	PROCLK
			VIH=(2.0V,VDD)	4.75V<VDD<5.25V	
			IIL=(-10UA,N/A)	VIN=0.00V	
			IIH=(N/A,10UA)	VIN=VDD	

Buffer	Type	Attribute	Parameter	Condition	Pins
	I	CMOS,PU			TESTB

Buffer	Type	Attribute	Parameter	Condition	Pins
	I	TTL	VIL=(VSS,0.8V)	4.75V<VDD<5.25V	PA12
			VIH=(2.0V,VDD)	4.75V<VDD<5.25V	PA13
			IIL=(-10UA,N/A)	VIN=0.00V	PA10
			IIH=(N/A,10UA)	VIN=VDD	PA11
					PA4
					PA5
					PA3
					DELCMDN
					RESERVED
					RESERVED
					RESERVED
					RESERVED
					RESERVED
					RESERVED
					PWRI
					PDAT
					PMEM
					PBE0N
					STARTN
					CBE2N
					CBE1N
					CBE3N
					CBE0N
					P33MHZN
					SCLK
					LASTCYCN
					CACHE16MN
					CACHE8MN
					PA30
					PA31
					PA28
					PA29
					PA26
					PA27
					PA25
					PA24
					PA22
					PA23

PA21
PA20
PA18
PA19
PA17
PA16
PA14
PA15
SPLT23
CMADE24
SPLT22
SPLT21
SPLTENA
SPLT20
EN640N
BK0N
BK1N
IOCHRDY
PENAN
CREFRESHN
P32N
CMEM
RAWRESETN
DELCMDN
P486
PCD
DELADLN
PA8
PA9
PA6
PA7
PA2
RESERVED
RESERVED
RESERVED
RESERVED
RESERVED
RESERVED
RESERVED
RESERVED
RESERVED
RESERVED
ROMENA
PADSN
PBE3N
PBE1N
PBE2N
WDTCL
SCEN
LOCKN

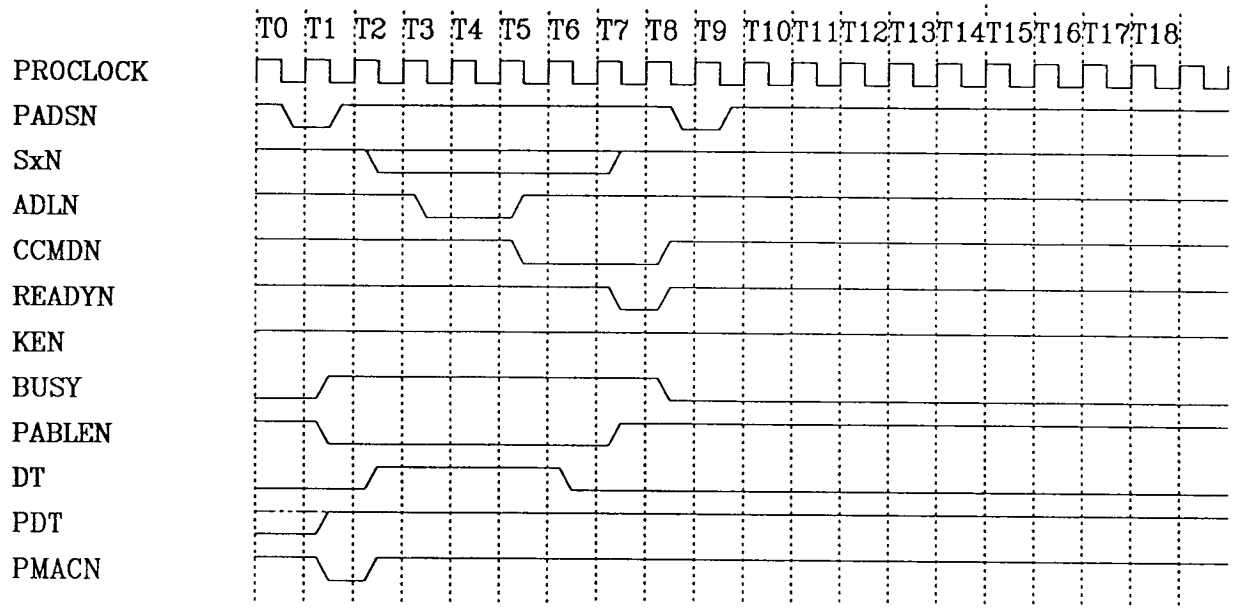
Electrical Specification (Continued)

Buffer	Type	Attribute	Parameter	Condition	Pins
	B	TTL	VIL=(VSS,0.8V)	4.75V<VDD<5.25V	S1N
			VIH=(2.0V,VDD)	4.75V<VDD<5.25V	S0N
			IIL=(-10UA,N/A)	VIN=0.00V	ADLN
			IIH=(N/A,-10UA)	VIN=VDD	CCMDN
		PU,Z	VOL=(VSS,0.4V)	0.0MA<IOL<24.0MA	
			VOH=(2.4V,VDD)	-40MA<IOH<-0.0MA	
			IOZL=(-10UA,N/A)	VO=VSS	
			IOZH=(N/A,10UA)	VO=VDD	

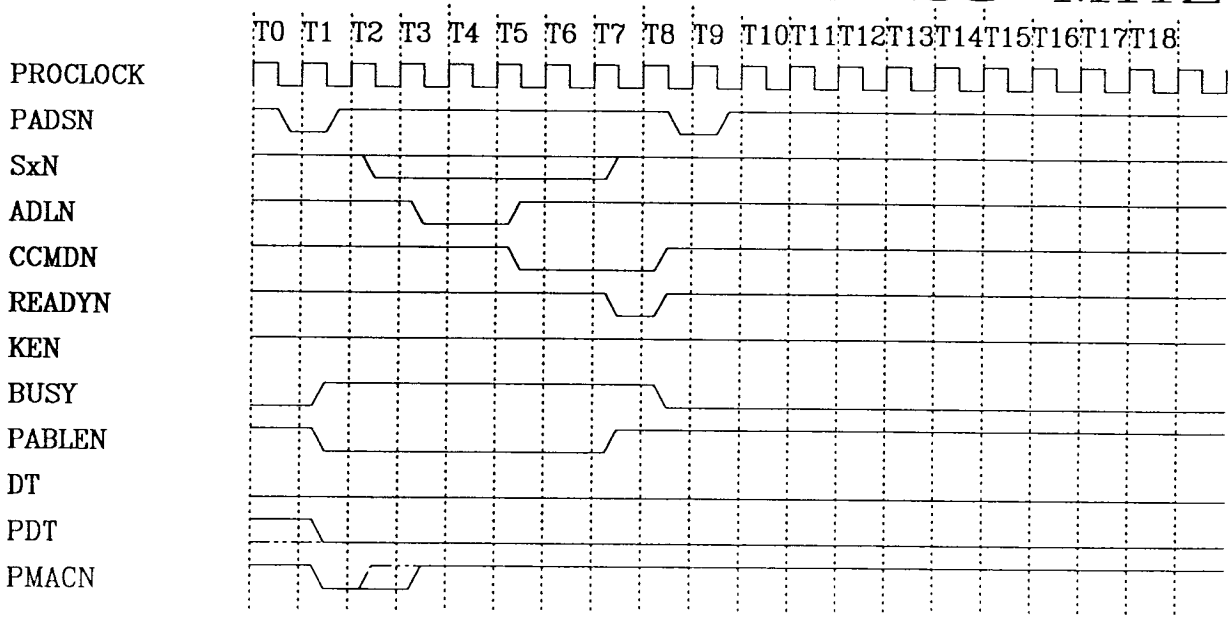
Buffer	Type	Attribute	Parameter	Condition	Pins
	O		VOL=(VSS,0.4V)	0.0MA<IOL<24.0MA	MA0
			VOH=(2.4V,.7*VDD)	-40MA<IOH<-0.0MA	DT
				VO=VDD	MA2
				VO=VSS	PDT
					RASN5
					BENADAT
					PABLEN
					RASN3
					RESERVED
					READYN
					EADSN
					RASN6
					MA9
					MA6
					RASN2
					CAS4
					CAS3
					MA8
					MA4
					RASN4
					MA7
					CAS1
					CAS5
					MA5
					MA3
					CAS2
					CAS6
					MA1
					WEN
					RASN7
					RAMCSN
					RASN1
					ROMCSN
					BSTRDYN

					RESERVED
					CAS0
					CAS7
					RASN0
					KEN
					PMACN
					BUSY
Buffer	**Type**	**Attribute**	**Parameter**	**Condition**	**Pins**
	O		VOL=(VSS,0.4V) VOH=(2.4V,VDD)	0.0MA<IOL<6.0MA -6.0MA<IOH<-0.0MA	TESTOUT

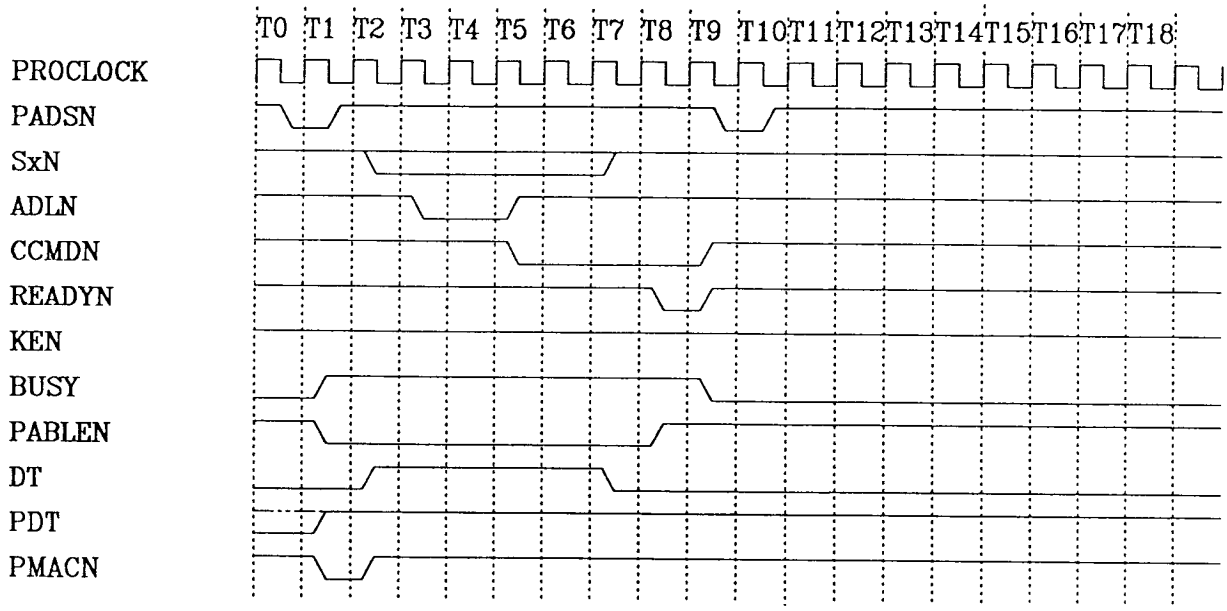
486 CHANNEL WRITE 25 MHZ



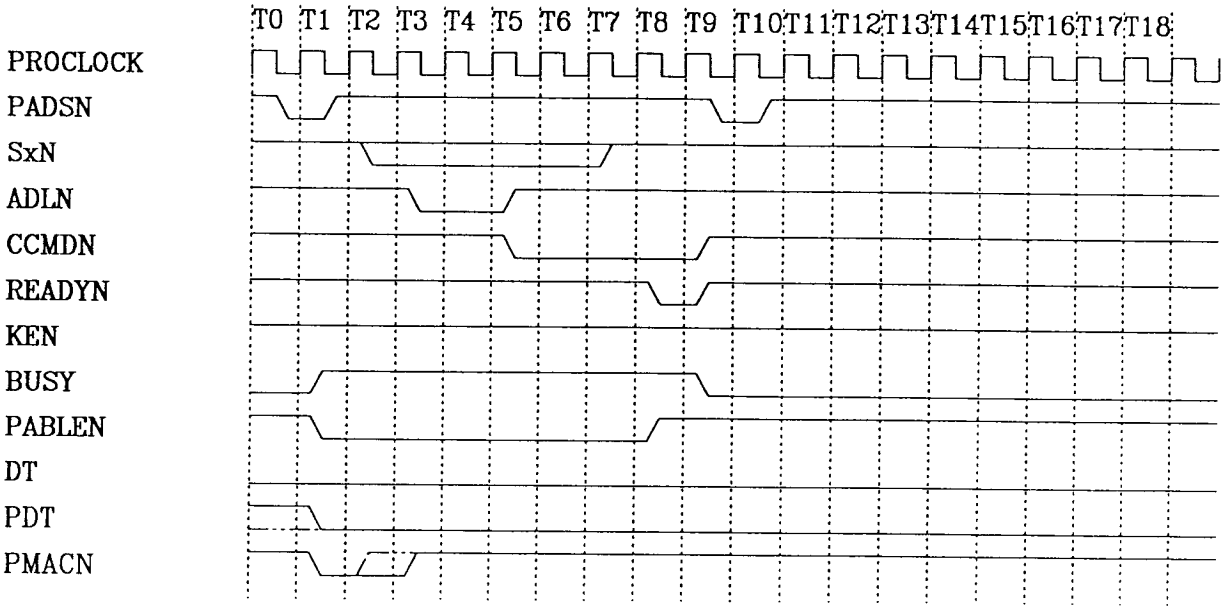
486 CHANNEL READ 25 MHZ



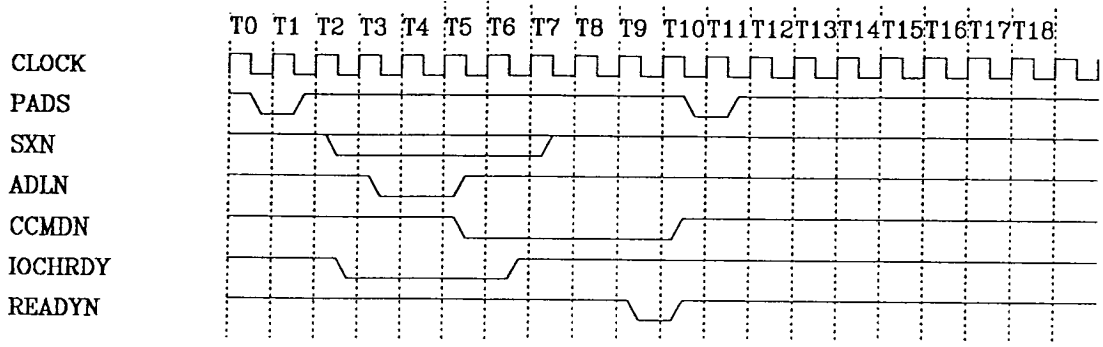
486 CHANNEL WRITE 33 MHZ



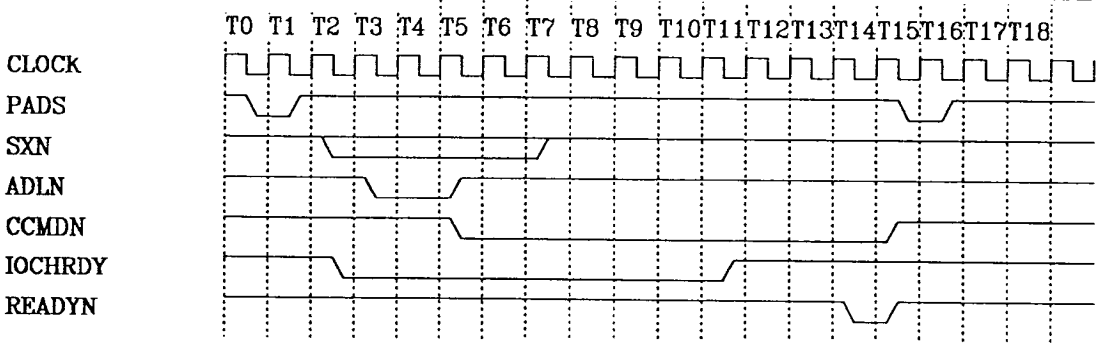
486 CHANNEL READ 33 MHZ



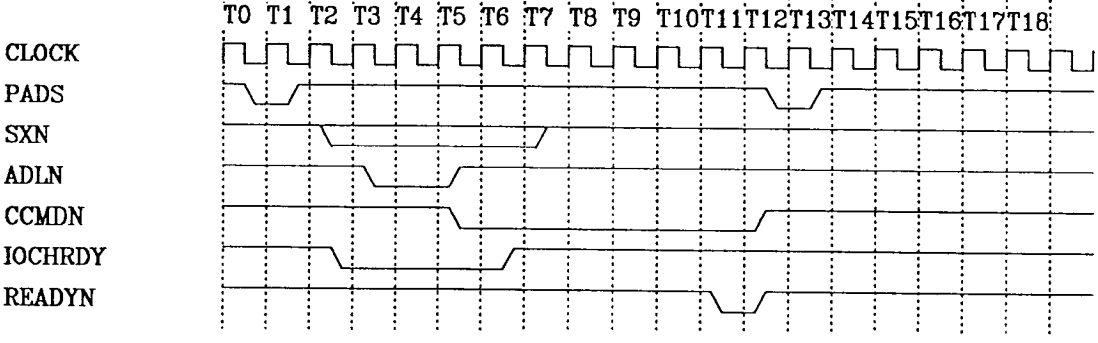
486 CHANNEL SYNCHRONOUS—EXTENDED CYCLE 25 MHZ



486 CHANNEL ASYNCHRONOUS—EXTENDED CYCLE 25 MHZ



486 CHANNEL SYNCHRONOUS—EXTENDED CYCLE 33 MHZ



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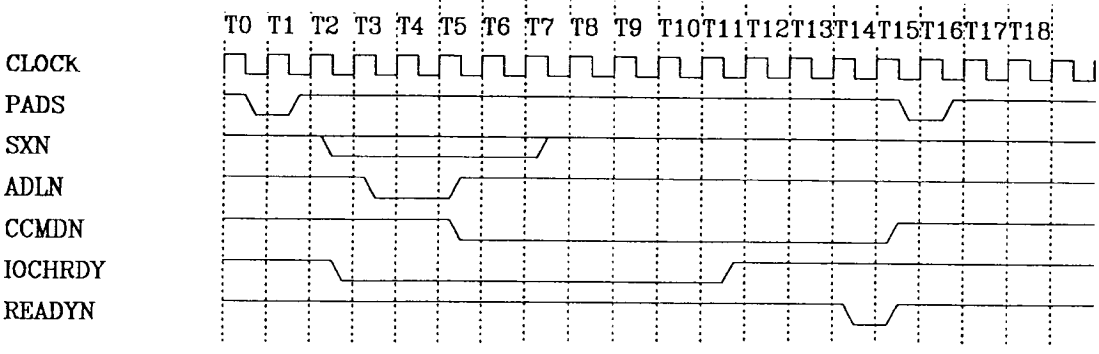
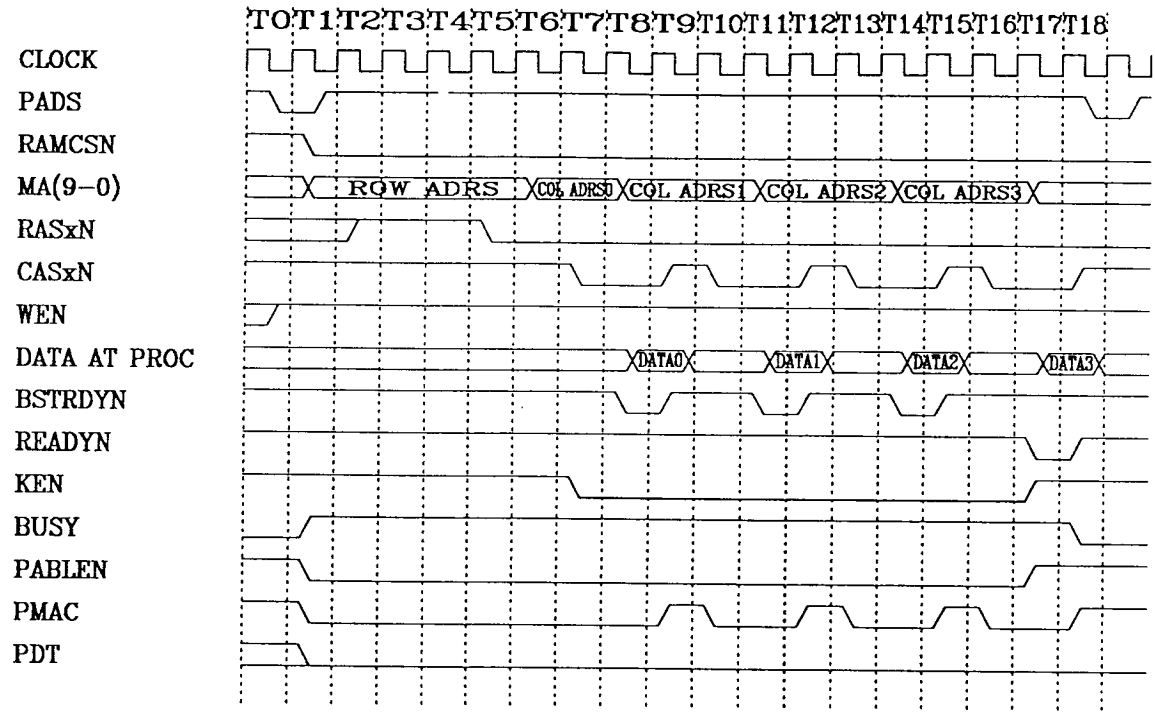
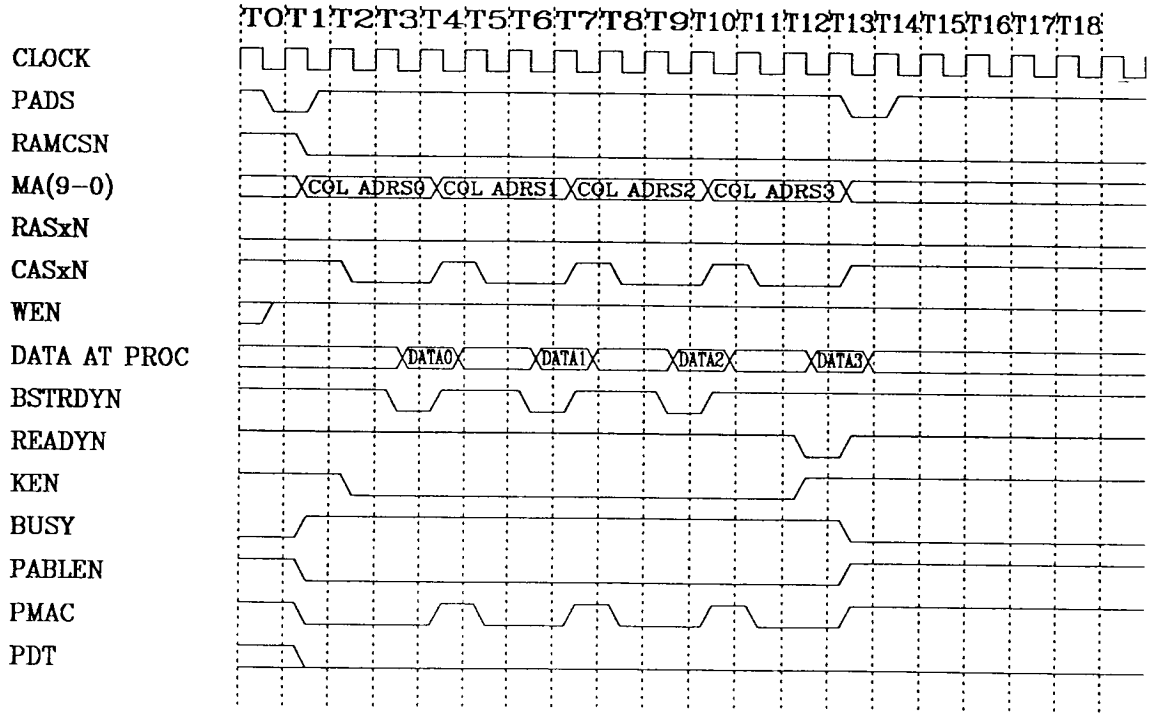


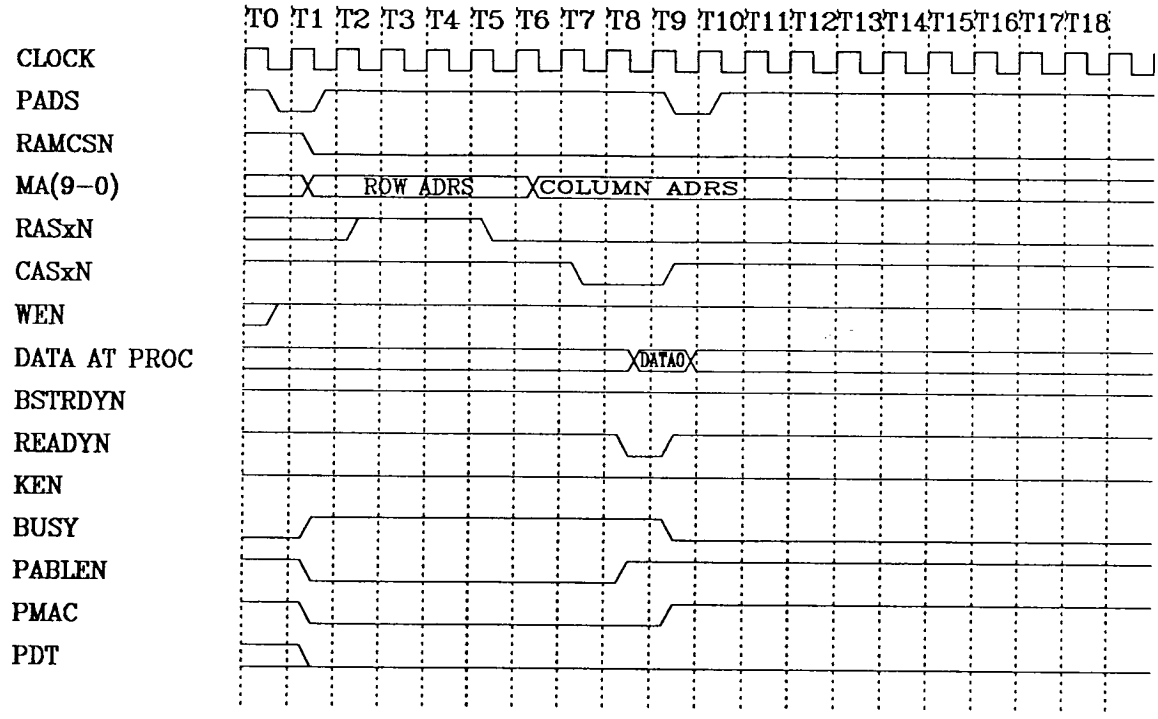
486 READ PAGE MISS CACHE LINE FILL 25 OR 33MHZ



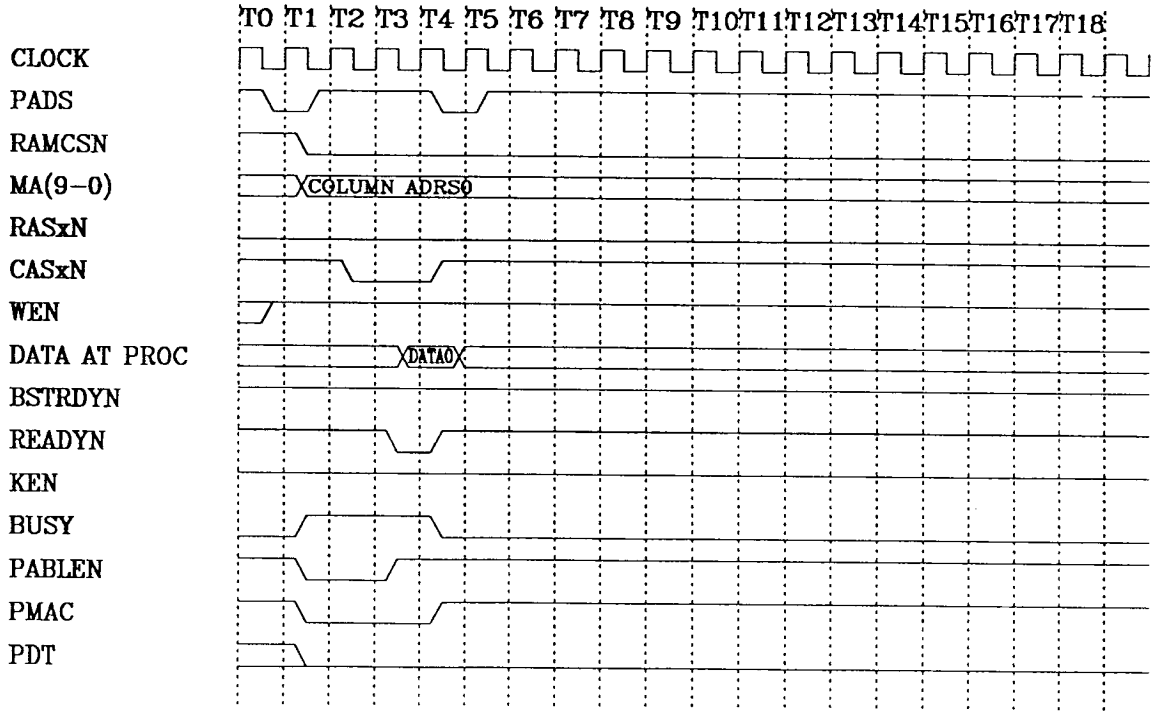
486 READ PAGE HIT CACHE LINE FILL 25 OR 33 MHZ



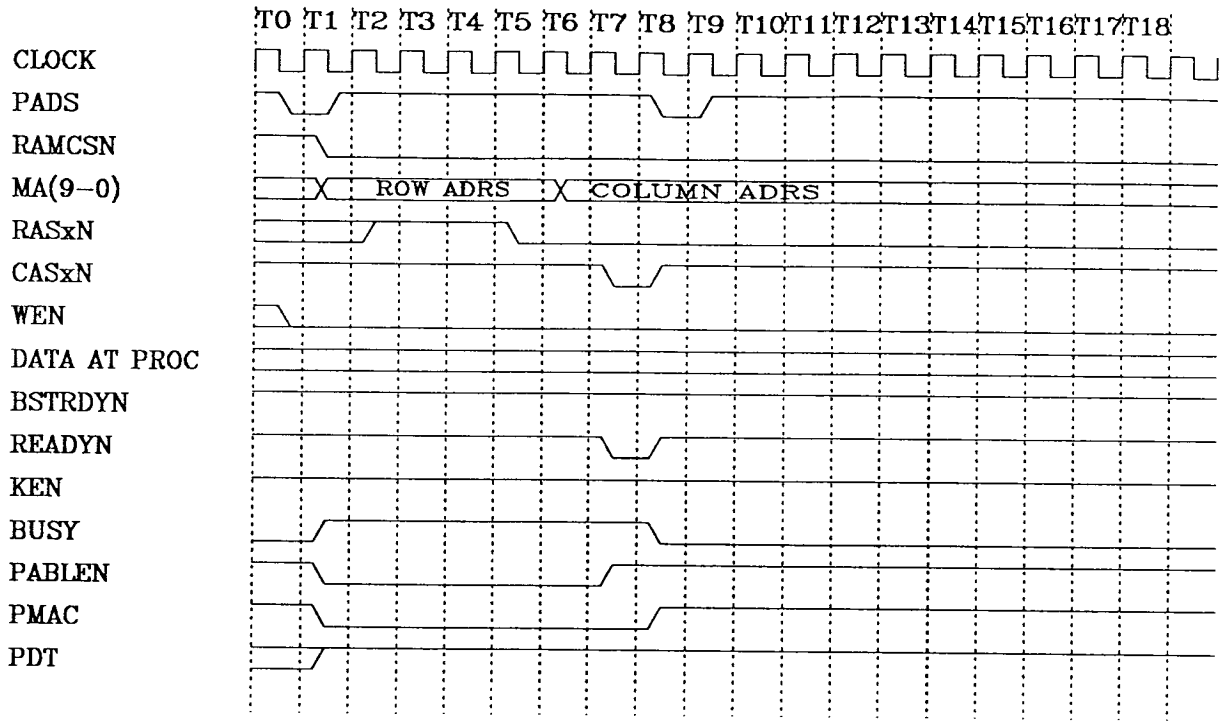
486 READ PAGE MISS NON—CACHED 25 OR 33 MHZ



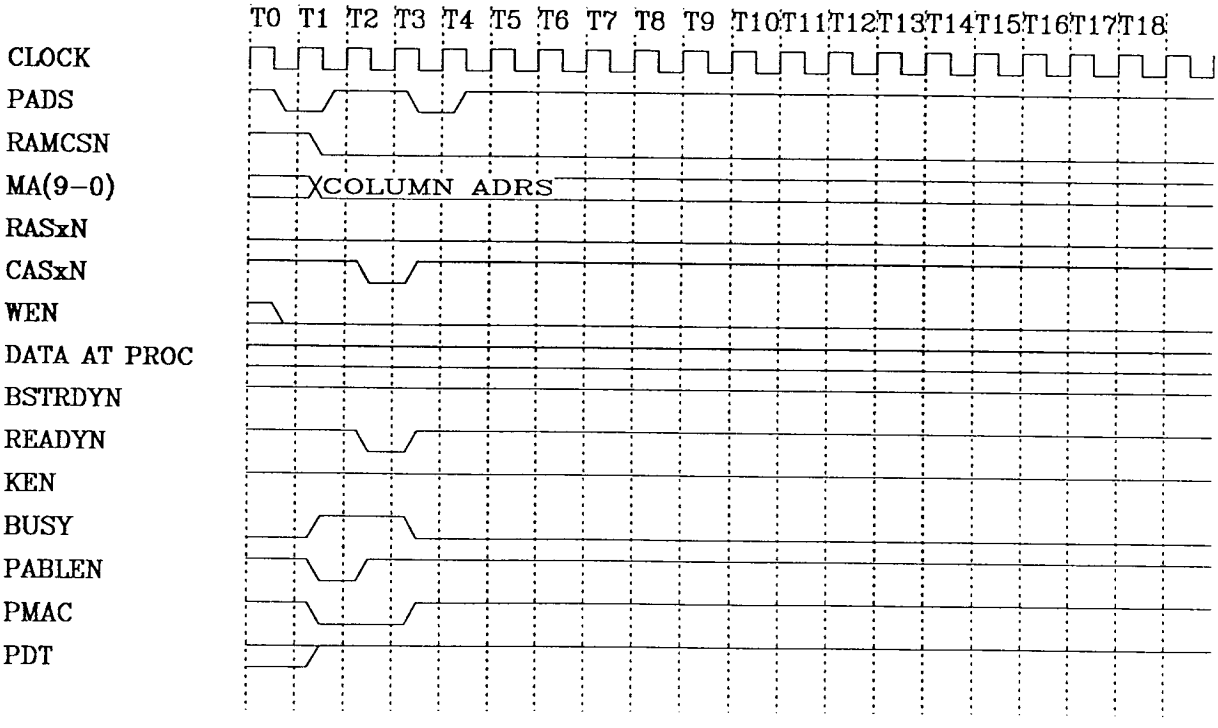
486 READ PAGE HIT NON—CACHED 25 OR 33MHZ



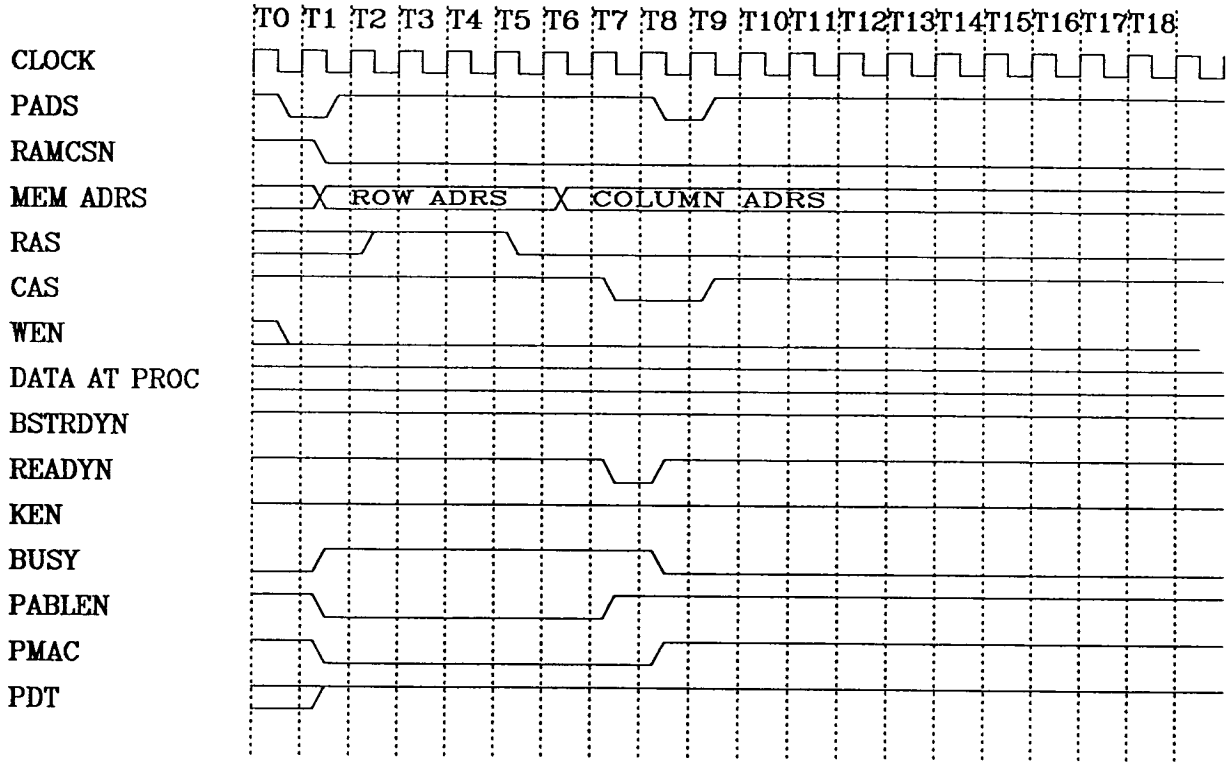
486 WRITE PAGE MISS 25 OR 33 MHZ



486 WRITE PAGE HIT 25 OR 33 MHZ



486 WRITE PAGE MISS 25 OR 33 MHZ 120NS RAMS



Timing Specifications

Bus And Processor Controller Timing

max @ ttl level, worst processing, 4.75v, 25°C
min @ ttl level, best processing, 5.25v, 0°C

DELAY TIMES (in nanoseconds)

SIGNAL:	WORST CASE Low:	WORST CASE High:	BEST CASE Low:	BEST CASE High:
S(x)N from PROCLK	18.5	18.5	4.6	4.6
ADLN from PROCLK	17.2	14.5	4.6	3.8
CCMDN from PROCLK	17.2	14.5	4.4	3.4
RAS(x)N from PROCLK	18.1	16.5	5.1	4.3
CAS(x)N from PROCLK	18.2	16.5	5.3	4.7
MA(x) from PA(x)	14.0	14.0	6.0	6.0
MA(x) from PROCLK	17.6	17.6	5.4	5.4
WEN from PADSN	21.9	18.4	6.5	5.8
ROMCSN from PADSN		25.5		
RMACSN from PADSN	29.6		8.0	
READYN from PROCLK	20.3	15.2	5.6	3.9
DT from S(x)N	12.0	10.6	3.4	2.4
BUSY from PROCLK	15.7	13.7	4.4	3.6
PABLEN from PROCLK	15.6	13.2	4.2	3.1
BENADAT from PROCLK	15.5	13.2	4.2	3.2
PMACN from PROCLK	16.1	14.3	4.4	3.4
PDT from PROCLK	18.1	14.8	5.1	3.8
KEN from PROCLK	16.1	14.3	4.4	3.4
BSTRDY from PROCLK	15.9	13.8	4.3	3.2
EADSN from ADLN	16.8		4.9	
EADSN from PROCLK		15.7		4.3

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