82C835

Integrated Cache Controller Chip

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Single CHIP 386sx AT
Cache Controller

Data Sheet

April 1991

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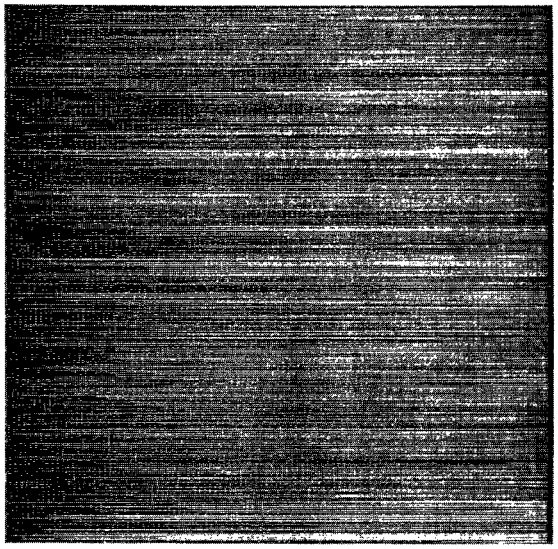
82C835

Integrated Cache Controller Chip



Single CHIP 386sx AT
Cache Controller

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April 1991

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Preface

The 82C835 integrated cache controller chip operates in conjunction with the 82C836 (Scat-sx). In combination, they form the Peak-sx CHIPSet. This manual covers the 82C835 cache controller chip only. The following related documentation is also available:

- The 82C835 Integrated Cache Controller Data Sheet
- The 82C836 Single Chip AT-sx Data Sheet
- The 82C641 Power Management/Buffer Unit Data Sheet

The Development Kit Package for each chip which includes:

- Development Kit Users Guide
- Development Kit System Board
- Development Kit Schematics

If you would like to review any of the above noted documentation, contact the CHIPS and Technologies Sales Office near you.

Contents

List of Figures

List of Tables

List of Registers

Section 1

Introduction

1.1 Features

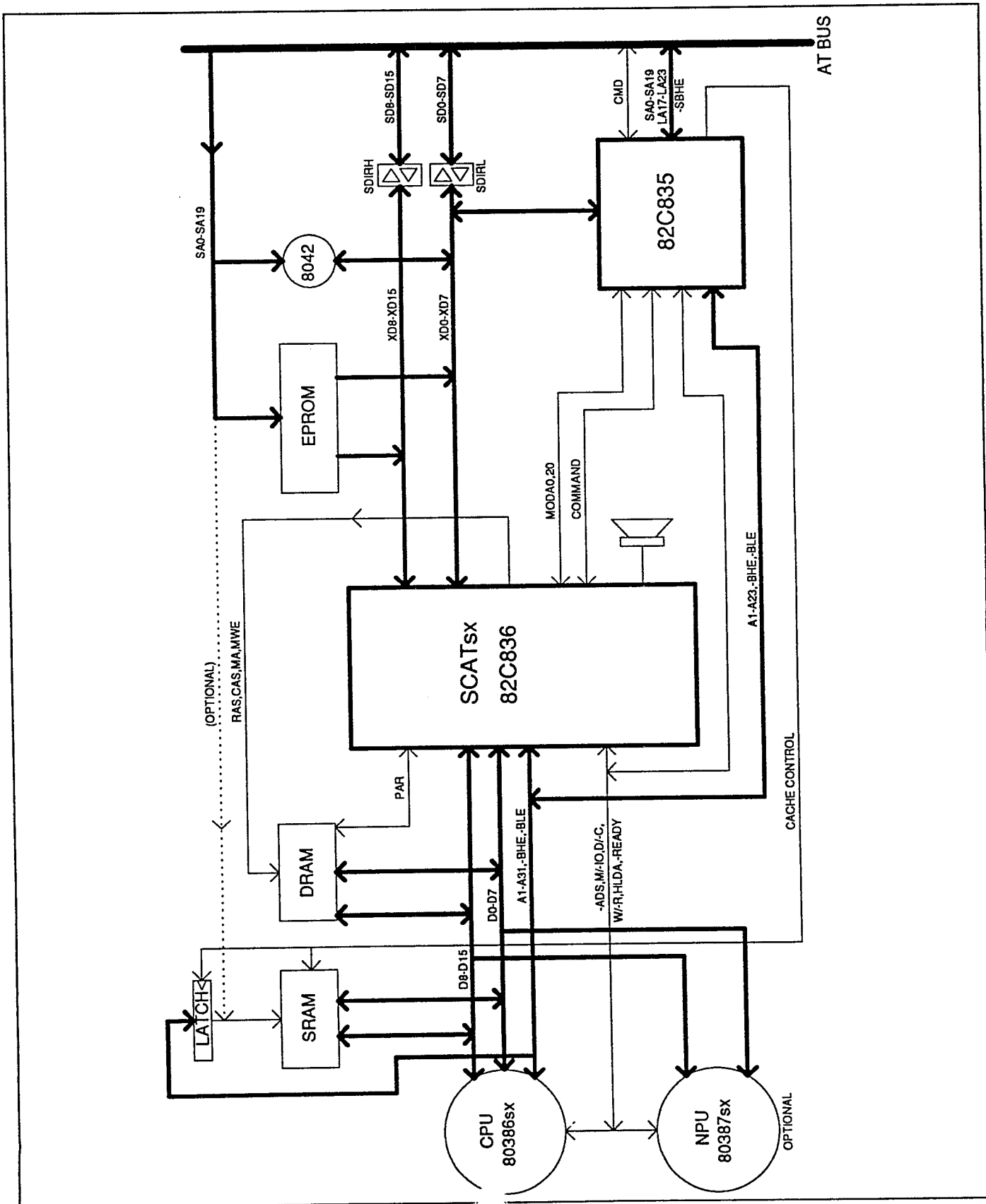
- Interfaces to the 80386sx
- Close-coupled design with the 82C836 (SCATsx) for a cache based system
- 32KB or 16KB cache
- Two-way Set-associative or Direct-mapped organization
- Supports CPU speeds up to 20MHz
- Caches AT I/O Channel memory as well as local DRAM
- Internal tag RAM and comparators
- Latches and buffers for all address lines to/from the AT expansion bus using integrated 24mA drivers
- Buffers commands to/from the expansion bus using integrated 24mA drivers
- 120-pin plastic quad flat pack

1.2 82C835 Overview

The 82C835 interfaces directly with the 386sx and has been designed to work closely with the 82C836 single chip AT (SCAT-sx). The 82C835 contains a 386sx cache controller incorporating the cache control logic and tag RAM. Also included are several programmable registers provided for configuration options. The ability to configure the cache organization (Two-Way Set-Associative or Direct Mapped) and size (16KB or 32KB) allows a flexible selection of external data SRAM.

In addition to the cache controller, the 82C835 integrates the AT I/O channel command and address buffers and the corresponding control logic. Many existing 80386sx system implementations require the use of external buffers, latches, and transceivers to drive and receive the commands and addresses. These systems also require external SSI logic to control the operation of these buffers. Systems will typically save six to seven external TTL buffers and five to six SSI gates when implementing the channel interface with the 82C835. By integrating the channel drivers and logic, the 82C835 reduces the system size and complexity.

Figure 1-1. System Block Diagram



1.3 What You Need to Know

This manual is written with the assumption that you have a basic comprehension of computer concepts, operations, and terminology. Understanding of cache organizations and operations as well as DRAM memory controller operations is essential. Most of the cache related descriptions require that you also have a basic understanding of SRAM usage. Finally, familiarity with the Industry Standard Architecture (ISA) is highly recommended.

The scope of the information presented in this manual is limited to this CHIPSet and does not include the operation of external components. It is assumed you have a working knowledge of these components. With such knowledge, combined with the information presented here, you can utilize our CHIPSet to enhance the overall performance and excellence of your final product.

If you are unfamiliar with any of the mentioned subjects, please consult the appropriate reference documentation.

1.4 About This Manual

Here's what you'll find in the rest of this manual:

- *Section 2: Functional Description* explains the functionality of the 82C835.
- *Section 3: Configuration Registers* details the internal registers within the 82C835.
- *Section 4: Pin Descriptions* provides tables describing the details of each pin.
- *Section 5: Physical Characteristics* reports the range of absolute maximum ratings, operating conditions, and capacitive characteristics.
- *Section 6: DC/AC Characteristics* lists the DC and AC Characteristics of the 82C835.
- *Section 7: Timing Diagrams* details the timings of the 82C835 signals.
- *Section 8: Physical Dimensions* identifies the dimensions of the 82C835 PFP package.
- *Appendix A: System Schematics* provides diagrams of the 82C835 minimum system.

1.5 Manual Conventions

The following conventions are used throughout this manual:

- REG*n*H identifies the internal register of index *n*, where *n* is in hexadecimal notation.
- REG*n*H <*x*:*y*> indicates the bit range from bit *x* to bit *y* of indexed register *n*.
- (xxx) signifies the default value after power-on Reset (where xxx are register bit values).

- Signal names are identified in UPPER CASE. For example, XRST.
- A dash at the beginning of the signal name indicates an active low signal. For example, -READY.
- Section titles are shown in *italic* type. For example; *Section 2.1 Functional Overview.*

The following abbreviations are used throughout this document:

- Kb = kilobit
- KB = kilobyte
- Mb = megabit
- MB = megabyte
- MHz = megahertz
- ns = nano seconds
- pF = pico Farad

Section 2

Functional Description

2.1 Functional Overview

The cache controller in the 82C835 operates in conjunction with the main memory (DRAM) controller. All CPU accesses to locations within main memory are completed by either the cache or memory controller. The cache controller services and completes all read hits in zero wait-states. All other memory cycles are completed by the memory controller.

The 82C835 operates in non-pipeline mode only. This eliminates the performance degradation attributed to switching into pipeline mode.

The cache controller monitors all 80386sx memory accesses to determine whether the desired location resides in the cache (a "hit"). Memory read hits are performed in zero wait-states, never incurring the performance penalty from additional wait-states associated with a normal system memory controller. If the location is not in the cache (a "miss"), the main memory or system controller completes the cycle. The data read during read misses may be cached regardless of the source (local memory or AT bus memory) depending upon the state of the internal configuration registers. The width of the data accessed during cacheable read misses must be 16-bits, the cache line size of the 82C835.

Frequently accessed data usually resides inside the cache. Consequently, most memory read cycles are performed by the cache controller as it responds to read hits. Maximum performance is obtained when the ratio of read hits to total cycles (read hit rate) is high. This is the predominant case with application programs because the majority of cycles are memory code fetches.

The 82C835 integrates the tag SRAM's and cache control logic required to provide either a 16KB or a 32KB cache size. Additionally, either direct mapped or two-way set organization can be chosen via software configuration registers. External SRAMs are required to store the cache data.

2.2 Bus Structure Overview

The 82C835 resides between the local bus (CPU), peripheral bus (82C836), and the AT bus. With this architecture, the 82C835 is responsible for maintaing the correct address, command and data flow or "bus direction" during CPU cycles, DMA cycles, Master cycles, and Refresh cycles. It directly monitors the CPU status and control lines as well as -MASTER, -REF and PWRGOOD signals in order to determine the type of cycle occurring and control the bus direction accordingly.

Bus command signals provided by the system controller (82C836) are buffered and driven onto the AT bus. Local addresses and byte enables are latched and driven onto the AT bus as SA<19:0>, -SBHE and LA<23:17>. The bus control logic is integrated into the 82C835 and maintains operation during DMA, Master, and Refresh cycles compatible with ISA specifications.

The data SRAM's for the cache are usually placed directly on the local data bus D<15:0>. This bus is shared by the CPU, the 82C836, the local DRAM's, and an optional coprocessor. Since data SRAM access time is critical, no buffer should be placed between the SRAM's and the local data bus for most implementations.

2.3 Address Latching and Command Buffering

The 82C835 provides high-drive slew-rate controlled buffers for the AT I/O channel. Bus command signals provided by the system controller (82C836) are buffered and driven onto the channel. Local addresses are also buffered and driven onto the channel during CPU cycles. These signals include -IOR, -IOW, -MEMR, -MEMW, -SMEMR, -SMEMW, and -REF. Signal AEN is also driven onto the channel, but derived from logic internal to the 82C835.

At the beginning of each CPU cycle, the 82C835 latches the local address bus and byte enables. The latched address lines are driven onto the AT bus as LA<23:17> and SA<19:1>. Low address bit SA<0> is also driven onto the bus, but is a buffered version of the unlatched MODA0 input. Although both byte enables are latched for use by the 82C835, only a gated version of -BHE is driven out (as signal -SBHE). The gate logic for -SBHE is enabled to provide partial support for constant AT bus memory caching (refer to the section titled *AT Chsnnel Memory Caching*). The 82C835 provides the control logic necessary to correctly generate SA<2' · by examining the state of HLDA from the CPU, GATEA20 from the keyboard controller, and fast GATEA20 from I/O Port 092H.

As previously stated, bus direction during DMA, Master, and Refresh cycles is compatible with ISA specifications (refer to Tables 2-1 and 2-2). In addition, address latches are kept open during these cycles.

2.4 Basic Cache Operation

The following sections describe the cache operation.

READY Protocol

The 82C835 uses the -READY signal to communicate servicing of read hits. When a memory read cycle is determined to be a cache read hit, the 82C835 completes the cycle by asserting -READY in the first T2 period. The 82C835 holds -READY active until sampled by the CPU at the end of T2 in order to complete a zero wait-state cycle. The main memory controller must also monitor this line at the end of the first T2 to determine whether the cache controller is claiming the cycle. If -READY is active at this time, the memory controller must not participate in the cycle. If -READY is not active, the main memory controller is free to service the read miss at the beginning of the second T2.

The 82C835 does not assert -READY for write cycles. Therefore, to improve performance, the memory controller should begin servicing all write cycles immediately. The 82C835 and 82C836 is designed to follow this protocol when the 82C836 is programmed for "Early READY" mode (CHIPS REG41H<6>=1).

Cache Flush and Enable

Before the cache is enabled, the internal cache directory must be cleared (often referred to as "flushing"). The cache is always disabled after a system reset. To guarantee that the cache does not incorrectly respond to a given location as a hit and present false data, the system software must flush the directory before the cache is enabled. Flushing is also necessary every time the cache is disabled and re-enabled in order to guarantee coherency. The software mechanics of the cache flush and cache enable functions are discussed later in this manual.

Memory Read Cycles

The first read access of a local memory location produces a read miss since the location is not initially contained in the cache directory. In response to this case, the main memory controller provides 16-bits of data (equivalent to the cache line size) and completes the cycle. At the same time, the data from main memory is stored in the external data SRAM while the cache directory is updated with the current location. Subsequent reads to this memory location results in read hits and is completed in zero wait-states until a new memory location with the same index but different tag is accessed. During read hits, the data SRAM provides the data while the 82C835 asserts -READY to complete the cycle.

Memory Write Cycles

When the system controller detects a memory write cycle, it may begin the write operation immediately; there is no need to wait for the 82C835. If the memory location of the memory write cycle is in the cache directory (a write hit), the corresponding cache data contents are updated. This update occurs in parallel with the write cycle to main memory, preventing cache data from becoming old or "stale." Write misses have no affect on the cache and are handled directly by the main memory controller.

The 82C836 system controller is optimized to produce fast DRAM write cycles in non-pipeline mode. When the 82C836 is configured for operation with the cache, local DRAM page-hit write cycles require zero wait-states, local DRAM RAS high write cycles require one wait-state, and local DRAM page-miss write cycles require three wait-states. As a result, the majority of write cycles are serviced in zero wait-states (page hits). This gives the performance of a multi-level posted write architecture without the need for expensive external FIFOs and control logic.

Other CPU Cycles

Other CPU cycles such as I/O reads and writes, interrupt acknowledge, halts, and shutdowns are not cached. For these cases, the 82C835 allows the system controller (82C836) to complete the cycle.

DMA and Master Cycles

In order to maintain AT compatability, the 82C835 does not respond to memory reads during Direct Memory Access (DMA) and Master operations. Although the read operation may produce a read hit, the cycle is serviced by the main memory controller or adapter card. In contrast to read misses originated by the CPU, read misses during DMA/Master mode do not update the cache directory. DMA/Master memory write misses have no affect on the cache. However, write hits update the contents of the data in the cache in order to maintain cache coherency. This update-on-write-hit scheme offers increased performance over cache schemes which invalidate on write hit for bus masters.

All 82C835 registers are inaccessible during DMA and Master operations.

2.5 Cache Structure

The following sections describe the two types of cache structures supported by the 82C835.

Direct Mapped Organization

In the direct mapped cache, every memory location corresponds to only one possible location in the cache. The lower order address lines (A<13:5> for cache size = 16KB, A<14:5> for size = 32KB) comprise the cache directory "index" which selects one of the directory entries. There are 1024 directory entries for 32KB cache size, or 512 entries for 16KB cache size. Each entry contains two fields:

1. A tag field (10-bits for size = 16KB, 9-bits for size 32KB).
2. A 16-bit valid field.

Each tag is associated with a block of 16 words (32 bytes) of cache SRAM data. The valid bits signify which of the 16 words are valid. During a memory access, the most significant address bits are compared with the contents of the tag field. At the same time, address lines A<4:1> determine which bit in the valid field to evaluate. The memory access is considered a "hit" if the most significant address bits and tag match, and if the valid bit is set; else, the result is a "miss." Also, the least significant address bits (A<13:1> for 16KB, A<14:1> for 32KB) form the "cache address" to the external data SRAM's.

The use of slower cache data SRAM's is a primary advantage of a direct mapped cache. Because only one address comparison is required, the hit-miss decision logic is faster than the corresponding logic in an associative cache. As a result, the external SRAM is enabled earlier for a direct-mapped cache. However, the potential drawback is a lower hit rate. In a worse case scenario, program code may jump back and forth between two addresses containing the same cache directory indices. Because no two addresses with the same index can reside in the cache memory at the same time, a miss occurs after the jump,

forcing the cache controller to invalidate the entry if the cycle is a read access. Depending on the structure of the code, this drawback can be partially or completely offset by an increase of the cache size.

Read Hits

The external cache SRAMs provide data to the CPU for read hit cycles. For all memory read cycles, the cache controller asserts the -CRD0 signal at the beginning of T2. The -CRD0 signal should be connected to the output enable of the SRAMs. Since the chip-enable to these SRAMs is typically grounded, the output enable time of the SRAMs is a critical parameter when selecting SRAM vendors. Signal -CRD0 remains asserted throughout T2 and de-activates at the beginning of the next T-state (T1 or Ti) after assuring that CPU data hold time has been met. Therefore, no other device should drive the local data bus during the first T2 state of a memory read cycle with the 82C835 configured and enabled for direct-mapped cache.

Read Misses

When a cache read miss occurs, the requested data is not in the cache memory. The system or memory controller must provide the data. The cache controller writes a copy of the data into the cache data SRAM's. It also updates the directory depending upon the type of miss. If the tag mismatches, the upper address bits are loaded into the tag field. All valid bits are cleared except for the bit corresponding to the current word which is set. If the tag matches but the valid bit is not set, only that bit is set; no other bits of the tag or valid fields are modified. The cache controller asserts the SRAM write enable signals -CWE0H and -CWE0L in the middle of the second T2, allowing data from memory to be written into the cache as it becomes available on the local data bus. These signals remain asserted until the end of the last T2 (normal) or else until one-half of a processor clock before the end of the last T2 (early) depending on the state of REG20<3>. Refer to the section titled *Write Pulse Width on Read Misses* for details of the pulse width feature.

Subsequent reads to this memory location produce zero wait-state read hit until a read from another memory location with the same directory index. If this happens, a read miss occurs prompting the 82C835 to initiate an update cycle.

Write Cycles

When a memory write cycle is initiated by the CPU, the system or memory controller should begin the cycle immediately since the 82C835 never generates -READY for normal write cycles. If a cache hit occurs during the write cycle, the cache data SRAMs are updated. Else, the result is a cache miss, and no cache operation occurs.

On write hits, the 82C835 updates its data SRAMs during the first T2. The SRAM write enable signals -CWE0H and/or -CWE0L become asserted one-half PROCCLK after the start of T2 and terminate at the end of T2 regardless of the number of T-states required by the memory controller. This allows the 82C835 to work with memory controllers capable of zero wait-state writes.

If the system controller is the 82C836 and it is configured for operation with the 82C835, the write cycle durations are as follows:

- Zero wait-states for all DRAM page hits
- One wait-state for RAS high cycles
- Three wait-states for page misses

No additional wait-states are required for "back-to-back" write cycles. These write times have the cumulative effect of producing the appearance of a system similar to a posted write architecture with a full DRAM page of buffering during consecutive write cycles of DRAM page hits.

Other Cycles Affecting the Cache

The external cache data SRAMs are not accessed for memory read cycles initiated by the DMA controller or other bus masters. Data for all memory reads during these types of cycles is provided by main memory or adapter card. For DMA and Master write cycles, the appropriate cache line is updated on write hits and unaffected by write misses. This assures coherency and eliminates the performance penalty of a cache line invalidation after every DMA or Master write cycle.

Two Way Set Organization

In addition to the direct mapped option, the 82C835 also supports 16KB and 32KB two-way set-associative organization. In this cache configuration, two sets of external data SRAM's and two sets of cache directories exist. Every memory location corresponds to two possible locations in the cache, allowing two addresses with the same cache directory index to reside in the cache concurrently. The lower order address lines (A<12:5> for 16KB and A<13:5> for size = 32KB) comprise the cache directory index. Each index corresponds to two sets and an additional field for a total of five fields (*two tag fields, two* valid fields, and a "least-recently-used" (LRU) field). Each tag field width is 11-bits for size = 16KB and 10-bits for size = 32KB. Similar to direct mapped cache, each valid field is 16-bits wide. As with direct mapped cache, each tag applies to 16 words (32 bytes) of cache SRAM data. The valid bits signify which of the 16 words are valid. One additional field for set-associative configuration is the LRU bit which tracks the set that has been least used in order to implement a least-recently-used replacement algorithm. If a hit occurs, it is generated exclusively from one set.

For the 16KB size, each SRAM bank (or set) is 4K words (4K x 16 bits = 8KB per set) and the directory consists of 256 entries. For the 32KB size, each SRAM bank (or set) is 8K words (8K x 16 bits = 16KB per set) and the directory consists of 512 entries.

A two-way set-associative cache has the potential to yield higher performance than a direct mapped cache with applications that jump frequently between memory locations which share the same address index. However, the two-way set-associative cache also requires slightly faster SRAMs than a direct mapped cache. This requirement is because the hit-miss decision logic of a set-associative cache requires additional time to check both sets.

Read Hits

The external cache SRAMs provide data to the CPU for read hit cycles. When a read hit is detected, the cache controller asserts either -CRD0 or -CRD1 one half clock after the beginning of T2. The -CRD0 and -CRD1 signals are typically connected to the output enable of the SRAMs for set 0 and set 1, respectively. Since the chip enables of these SRAMs are typically grounded, the output enable time of the SRAMs is a critical parameter when selecting SRAM vendors. The appropriate -CRD0 signal remains asserted throughout T2 and de-activates at the beginning of the next T-state (T1 or Ti) after assuring that CPU data hold time has been met.

The cache directory is also modified during read hits. The LRU field is loaded with the number (1 or 0) of the set not producing the hit. For example, if the hit is derived from set 1, the LRU bit is loaded with a value of zero.

Read Misses

When a cache read miss occurs, the requested data is not in the cache memory. The system memory controller must provide the data. The cache controller writes a copy of the data of the cache data SRAM's of the set determined by the least-recently-used algorithm. It also updates the directory depending upon the type of miss and the state of the LRU bit. If both tags mismatch, the upper address bits are loaded into the tag field of the set least-recently-used. All valid bits of the same set are cleared except for the bit corresponding to the current word which is set. If a set's tag matches but valid bit not set, only that valid bit is set; no other bits of the tag or valid fields are modified. For either type of miss, the LRU field is loaded with the number (1 or 0) of the set *not* modified.

The cache controller asserts the SRAM write enable signals -CWE0H and -CWE0L, or -CWE1H and -CWE1L (depending on which set is chosen) in the middle of the second T2, allowing data from memory to be written into the cache as it becomes available on the local data bus. These signals remain asserted until the end of the last T2 (normal) or until one-half of a processor clock before the end of the last T2 (early) depending on the state of REG20<3>. Refer to the section titled *Write Pulse Width on Read Misses* for details for the pulse width feature.

Subsequent reads to the same memory location produce zero wait-state read hits until the tag is removed from the directory. The removal is a result of a read miss to a different location with the same index and different tag in combination with the LRU pointing the corresponding set.

Write Cycles

When a memory write cycle is initiated by the CPU, the system or memory controller should begin the cycle immediately since the 82C835 never generates -READY for normal cycles. If a cache hit occurs during the write cycle, then the data SRAMs are updated. Else, if the result is a cache miss, then no cache operation occurs.

On write hits, 82C835 updates its data SRAMs during the first T2. The SRAM write enable signals (-CWE0H and/or -CWE0L for set 0 and -CWE0H and/or -CWE0L for set 1) become asserted after the start of T2 and terminate at the end of T2 regardless of the number of T-states required by the memory controller. This allows the 82C835 to work with memory controllers capable of zero wait state writes.

The cache directory is also modified during write hits. The LRU field is loaded with the number (1 or 0) of the set not producing the hit.

Other Cycles Affecting the Cache

The external cache data SRAMs are not accessed for memory read cycles initiated by the DMA controller or other bus masters. Data for all memory reads during these types of cycles is provided by main memory or adapter card. For DMA and Master write cycles, the appropriate cache line is updated on write hits and unaffected by write misses. This assures coherency and eliminates the performance penalty of a cache line invalidation after every DMA or Master write cycle.

2.6 Hardware Interface

This section gives a brief description of the 82C835 hardware interface.

CPU Interface

The processor clock signal (PROCCLK) provides the fundamental timing for the 82C835 state machines. This signal is synchronized on the trailing edge of the system reset signal XRST. SCLK is a diagnostic output signal that is in phase with the 82C835 clock. It can be used to monitor CPU-82C835 synchronization. SCLK is low during phase one of a T-state and high during phase two.

The CPU control, status, address lines, and byte enables M/-IO, D/-C, W/-R, A<23:0>, -BHE, -BLE connect directly from the CPU to the 82C835. Signal MODA0 is connected to the system controller (82C836) driven out as SA0.

In order to minimize the external interface, a portion of the "GATEA20" logic is duplicated inside the 82C835. The GATEA20 signal from the keyboard controller is brought into the chip and combined with the FAST GATEA20 signal from the write only register 92H<1> (duplicated in the 82C835) and HLDA and A20 from the CPU to create an internal version of the MODA20 signal. Since Port 092H is write-only, the current state of the duplicated bit is readable only through 82C835 configuration REG20H<1>. The state of the keyboard GATEA20 pin is readable in REG20H<0>.

Signals -ADS and -READY are connected directly to the CPU. Since -READY is an open collector signal that is shared by several devices, determining which device is driving it during troubleshooting is often difficult. To alleviate this problem, the -READYO diagnostic pin can be used to monitor the 82C835 contribution to -READY during the normal CPU cycles. During Hold Acknowledge State (DMA and Master), the state of -READYO diagnostic pin is indeterminate and may assert low.

Cache Address Bus

There are two options for the source of the cache address bus. The most direct method is to connect the AT addresses bus directly to the cache data SRAMs as follows:

- 16KB direct mapped = SA<13:1>
- 32KB direct mapped = SA<14:1>
- 16KB two-way set-associative = SA<12:1>
- 32KB two-way set-associative SA<13:1>

This approach is the simplest and does not require any additional TTL parts. The SA bus is latched inside the 82C835 to guarantee address hold times at the end of cache updates. When this address interface is used, care must be taken that any add-on cards to the AT bus do not significantly degrade the signal quality of the SA bus.

The other method is to place latches between the CPU local address bus and the cache address bus (2 x 74F373 or equivalent). The 82C835 provides the cache address latch enable signal CALE so that no additional external logic is required to control these latches. Although this approach requires two additional parts, it has the advantage of making the cache address immune to the effects of loading on the AT bus.

Cache Data Bus

The cache data bus should be connected directly to the CPU local data bus. This connection allows the SRAMs to read the same data the CPU receives from memory.

Channel Address Bus

The 82C835 provides high drive buffers (24 mA) for the AT bus address lines LA<23:17>, SA<19:0> and -SBHE. These signals can directly drive the bus, and as previously stated, one architectural option is to connect the cache data SRAMs directly to the low order SA lines.

The following table summarizes the local and AT address bus direction provided by the 82C835:

Table 2-1. 82C835 Local and AT Address Bus Direction

	PWRGOOD=0 -MASTER=x -MREF=x (Stand-by)	PWRGOOD=1 -MASTER=1 -MREF=1 (Normal)	PWRGOOD=1 -MASTER=1 -MREF=0 (Norm Ref)	PWRGOOD=1 -MASTER=0 -MREF=1 (Master)	PWRGOOD=1 -MASTER=0 -MREF=0 (Master Ref)
A<23:21>, A<19:1>, -BHE	Input	Input	Input	Output	Input
MODA0	Input	Input	Input	Output	Input
MODA20	Tri-state	Tri-state	Tri-state	Output	Tri-state
LA<23:17>	Input	Output	Output	Input	Output
SA<19:17>	Tri-state	Output	Output	Tri-state	Tri-state
SA<16:0>, -SBHE	Input	Output	Output	Input	Output
A20, -BLE	Input	Input	Input	Input	Input

Channel Command Bus

In addition to buffering the AT bus address lines, the 82C835 also buffers the AT bus command signals. The buffer control logic required to support DMA and Master cycles is integrated in the 82C835.

The following table summarizes the local and AT bus command direction provided by the 82C835:

Table 2-2. 82C835 Local and AT Bus Command Direction

	PWRGOOD=0 -MASTER=x -MREF=x (Stand-by)	PWRGOOD=1 -MASTER=1 -MREF=1 (Normal)	PWRGOOD=1 -MASTER=1 -MREF=0 (Norm Ref)	PWRGOOD=1 -MASTER=0 -MREF=1 (Master)	PWRGOOD=1 -MASTER=0 -MREF=0 (Master Ref)
-XIOR, -XIOW, -XMEMW	Input	Input	Input	Output	Input
-IOR, -IOW, -MEMW	Input	Output	Input	Input	Input
-XMEMR	Input	Input	Input	Output	Input
-MEMR	Input	Output	Output	Input	Output
-SMEMR, -SMEMW	Tri-state	†	Output	†	Output

† Output if address is below 1MB; otherwise, tri-stated.

The 82C835 also generates and buffers the AEN signal to the AT bus. AEN is active during DMA cycles (i.e., -MASTER = 1 and HLDA = 1). In addition, the bi-directional refresh request signal is also buffered to/from the AT bus. -MREF from the system controller is an input during normal cycles and an output during master cycles. -REF is driven onto the AT bus except during Master cycles when it becomes an input. Note that all 82C835 registers are inaccessible during DMA and Master cycles.

Cache Control Signals

The -CRD1 and -CRD0 signals are the SRAM output enables. For direct map operation, only -CRD0 is connected. For two-way set mode, -CRD1 corresponds to set 1 and -CRD0 corresponds to set 0. Signals -CWE1H, -CWE1L, -CWE0H, and -CWE0L are the SRAM write enable. These enables may be tied directly to the write enable inputs of the SRAMs. -CWE0H and -CWE0L are used for direct map as well as set 0 in the two-way set organization. -CWE1H and -CWE1L are only used for set 1 of a two-way set-associative configuration. For direct map, they should remain unconnected.

The -EXTNC (external non-cacheable area) input is provided to allow the option of selecting non-cacheable areas via external hardware decodes. An active low signal on this input indicates that the current memory location is not to be cached. This signal is monitored by the 82C835 only during read miss cycles which allows a relaxed timing requirement for this signal. Signal -EXTNC must be active before the middle of the second T2 and must remain active until the end of the read cycle. The external non-cacheable area definition cannot change without being preceded by a cache flush.

Reset

The system reset signal XRST should be directly connected to the 82C835. This signal, in conjunction with the processor clock signal, synchronizes the internal phase clocks and resets state machines.

Signal PWRGOOD is an active high input from the power supply. When this signal is high, it indicates that all power supply voltages have reached their operating levels. The 82C835 tri-states its outputs while PWRGOOD is low. This signal is also used by the 82C836.

2.7 Programmable Features

The following sections list the features that are selectable via the configuration registers in the 82C835. A brief description of each programmable function is included. Refer to *Section 3.1 CHIPS Configuration Registers* for a complete listing of the 82C835 registers.

Cache Enable

The cache is enabled (or disabled) by programming REG20H<7>. Writing a '1' to this bit enables the cache and writing a '0' disables it. The cache must be flushed before it is enabled or unreliable operation may result. The cache is disabled when the 82C835 is reset and remains disabled until explicitly enabled by software.

Directory Freeze

This is a diagnostic mode that prevents the cache directory from being updated on read misses. When this mode is selected, only write hits update the cache data SRAMs. This feature is a useful diagnostic tool for isolating write hits and examining the contents of the cache directory. This mode is enabled by writing a '1' to REG20H<5>. The default value after a reset is '0,' which produces normal directory operation when the cache is enabled.

Write Pulse Width on Read Misses

This option determines when the write enables to the SRAMs are deactivated during read misses. It has no effect and is not needed during write hit cycles since data will remain available until the middle of the T-state following a write cycle. Two modes are available: "Normal CWE mode" causes the -CWExx signals to be disabled at the end of the first T2 of a read miss; "Early CWE mode" de-asserts the signals one half of a processor clock earlier.

The early mode is intended for systems that would otherwise have difficulty satisfying the local data bus hold times of both the CPU and SRAMs. When this mode is selected, the memory controller must only meet the CPU required hold time for the local data bus. It need not satisfy the SRAM hold time because the SRAM update finishes before the CPU read is completed. The disadvantage of this mode is that the DRAM controller MUST provide data earlier to guarantee that the SRAM parameter tDW (tDW = minimum time required for data to be valid until the end of the SRAM write) is satisfied. *Typically, with the early*

mode selected, the memory controller inserts one wait-state during read misses to satisfy this parameter.

The normal mode requires the memory controller to hold data on the local bus long enough to satisy both the CPU and the data SRAMs. The 82C836 has been designed to satisfy the 82C835 by guaranteeing that the memory CAS signals remain active long enough into the beginning of the following T-state to meet the cache SRAM's hold time requirement. This means that the 82C835 provides data on the local bus in time to meet the CPU data setup specification and holds it long enough to meet the cache data SRAM. As a result, the 82C836 can be programmed for zero CAS extended wait states and still meet the SRAM setup time. REG20<3> is used to select this option. A value of '1' enables the early -CWExx mode and a '0' sets the 82C835 to normal -CWExx mode (default).

Directory Flush

The cache directory should always be flushed before the cache is enabled. The flush invalidates all entries, preventing erroneous hits and hits to locations containing stale data. Flushing can be accomplished by first writing a '1' to REG20<2> and then performing memory read cycles to all entries in the cache directory. For example, reading a 16KB block of contiguous memory with the flush bit set invalidates all entries for a 16KB direct mapped cache. A 16KB two-way set-associative cache requires a read to 8KB of contiguous memory.

Other cases requiring cache flushing include redefinition of cacheable areas and re-enabling the cache after disabling it. The following provides an example of flushing cache.

```
                .
                .
                .
        MOV     AX,0420         ;SETTING REG20<2>
        OUT     22,AL
        XCHG    AH,AL
        OUT     23,AL           ;ENABLING DIRECTORY FLUSH

:FLUSHING   MOV     BX,8000     ;SETTING 32KB FLUSHING AREA
        MOV     AX,[BX]         ;READING ONE WORD FROM AREA
        ADD     BX,02           ;INCREMENT NEXT WORD AREA
        JNZ     FLUSHING        ;END OF FLUSHING AREA

        MOV     AX,0020         ;SETTING REG20<2>
        OUT     22,AL
        XCHG    AH,AL
        OUT     23,AL           ;DISABLING DIRECTORY FLUSH

        MOV     AX,8020         ;SETTING REG20<7>
        OUT     22,AL
        XCHG    AH,AL
        OUT     23,AL           ;ENABLING CACHE OPERATION
                .
                .
                .
```

Direct SRAM Access

The 82C835 allows the contents of the external data SRAMs to be directly examined and modified when in this diagnostic mode. Normal memory read and write cycles access the SRAMs directly. The 82C835 provides the -READY for these cycles in zero wait states. During direct SRAM reads, the memory controller samples -READY and does not interfere with the cycle, similar to its response during a cache read hit. For direct SRAM writes, the memory controller must have a programmable mode to prevent it from initiating a write to memory until after it verifies that -READY did not occur in the first T2. The 82C836 contains such a mode. This diagnostic mode is disabled after a reset (default normal cache operation).

The starting memory address of the directly accessible SRAMs in this mode is user selectable. REG24H<4:0> contains a 5-bit value corresponding to the system address lines A<19:15> and determines the starting SRAM location in the memory map. For example, a value of '01000' in REG24H<4:0> corresponds to a starting SRAM address of 40000H.

When in direct mapped mode, a 16KB cache appears as main memory with a memory base address specified in register 24H. The address range begins at the base address and extends to the base + 3FFFH. Similarly, a 32KB cache range starts from the same base and extends to the base + 7FFFH.

For a 16KB two-way set-associative cache, accesses start at the base location specified in REG24H<4-0> with an offset range of 0-1FFFH for set 0, and an offset range of 2000H-3FFFH for set 1. A 32KB cache accesses the SRAM starting at the selected memory base plus an offset range of 0-3FFFH for set 0 and an offset range of 4000H-7FFFH for set 1. (All direct writes to SRAM must be 16-bits wide cycles.)

Directory Access

The internal directory of the 82C835 may be accessed with the following I/O sequence:

1. Load REG21H<7> with a '1' to enable directory access. Also, select the desired directory field by writing the appropriate value to REG21<6-3>.
2. Load REG21H<1-0> and REG22H with the directory index pointing to the desired entry.

The selected field can now be accessed through REG23H. An I/O read from REG23H reads the corresponding contents of the directory field and an I/O write to REG23H loads the value into the directory field.

Cache Type (Direct Mapped or Two-Way Set-Associative)

The cache type is software selectable. Direct map is the default mode, but since the cache is disabled after a reset, two-way set mode can be selected by software before the cache begins operation. Configuration REG24H<7> controls this option. Writing a '1' to this bit enables the 82C835 to operate as a two-way set-associative cache and writing a '0' selects a direct mapped organization.

The cache size is programmed by REG24H<5>. Writing a '1' to this bit indicates that a 32KB of external cache SRAM exists. Writing a '0' (default) specifies a 16KB cache.

Cacheable Areas

The 82C835 recognizes two types of cacheable areas: those defined by configuration registers, and those defined by the external non-cacheable area input -EXTNC. Non-cacheable regions must be selected BEFORE enabling the cache. Once an area is defined as cacheable and the cache enabled, changing that area to a non-cacheable region will not prevent hits resulting from accesses to that area from continuing to occur. Therefore, the cache should be flushed anytime an area is re-defined from cacheable to non-cacheable. When an area is defined to be non-cacheable, read misses to that area will not update the internal directory or external SRAMs. Write hits will never occur since a write hit only occurs after a read miss update cycle to that particular address has previously occurred. Chips configuration registers 28H-2DH and 2FH define cacheable regions.

RAM Write Protect

Configuration register 2EH allows the area between C0000H and FFFFFH to be designated as either read-only or readable and writeable. Each bit in the register corresponds to 32KB segment of memory with bit 0 referring to segment 0C0000H-0C7FFF.

AT Channel Memory Caching

The 82C835 is capable of caching AT bus memory as well as motherboard DRAM memory. For 16-bit memory read cycles, the data will be cached regardless of the source if the location is configured as cacheable. However, to guarantee caching of extended memory on the AT bus, 16-bits of data must always be presented to the CPU for read cycles. The 82C835, in conjunction with 82C836, support a feature to force 16-bit read cycles to AT bus memory.

To achieve these 16-bit cycles, -SBHE can be forced low by enabling REG24<6> with a logic '1' and loading REG25 (AT memory boundary) with a value designating the starting address of AT Bus Memory. The 8-bit value corresponds to the upper 8 bits of the AT address. For all CPU read cycles, the upper 8 bits of CPU address (A<23:16>) are compared with the value in REG25H. If the CPU address is equivalent or greater, the 82C835 assumes the memory resides on the AT bus. As an example, if REG25H contains the value '0001 0000B, all access at and above 0100000H are considered AT memory access.

With the feature enabled, signal -SBHE from the 82C835 and MODA<0> from the system controller are always asserted low during memory read cycles to the defined AT address memory space, effectively generating a 16-bit access to the AT bus and allowing the 82C835 to cache the data.

Note The Memory Boundary register (REG25H) should never be set below 1MB (less the 10H). Also, certain types of adapter cards must not be cached. These adapters include those which contain either memory-mapped I/O or multi-ported memory. Configuration registers are provided in the 82C835 to define "non-cacheable" memory address spaces.

2.8 Design Considerations

The following considerations should be observed when designing a system with the 82C835.

Clocks

Care should be taken to prevent excessive loading of the processor clock signal. At minimum, the 82C835 requires a duty cycle which meet the specifications for the CPU. A duty cycle of 50% is optimum for the cache controller. If the 82C836 is used as the source of PROCCLK, the duty cycle may be tuned by adjusting the duty cycle of the CXIN input to the 82C836.

Cache Size and Type

Small application programs very often show no performance difference between the direct mapped cache and the two-way set-associative cache. The difference in architectures becomes more apparent when running larger applications and multi-tasking programs.

Cache Data SRAM Speed Requirements

The following table shows the basic SRAM requirements for the two cache architectures. Note that since the chip enables of the SRAMs are typically gounded (always selected), the output enable time is a critical parameter. Unfortunately, SRAMs are marked according to -CE access times. Therefore, consult the SRAM vendor specifications to verify that a particular device meets the required tOE.

SRAM Speed, Maximum Output Enable Time Allowed

20 MHz Direct Mapped, 35ns; tOE max = 20ns

20 MHz Two Way Set, 25ns; tOE max = 12ns

DRAM Controller Impact on Performance

The write cycle performance of the DRAM controller plays a significant role in determining overall system performance with the cache enabled. Typically, the 82C835 will have a very high hit rate for read cycles. Once a high read hit rate is achieved, the percentage of read misses is small and therefore, for read cycles, the DRAM controller's performance contribution is small.

However, every write cycle is serviced by the DRAM controller regardless of whether a hit or a miss occurs. The 82C836 optimizes its write cycles when it is

programmed to work with a cache controller such as the 82C835. With this configuration, write cycles that are DRAM page hits will complete in zero wait states, write cycles that require a DRAM bank switch require 1 wait state, and write cycles that are DRAM page misses require three wait-states.

The size and number of DRAM banks configured for the 82C836 also impacts to the system performance. Multiple DRAM banks increase the number of pages which in turn increases the number of bank switch write cycles. These bank switch cycles complete faster than page misses. An increase of DRAM size to 1MB increases the page size and thereby increases the probability of page hit write. Page hit write cycles are completed by the 82C836 in zero wait states.

Cache Address Bus

To guarantee setup to the 82C835, the address signals A5-A14 must not be loaded beyond 65pF capacitance. These critical path signals select the directory index and limit the access time of the internal directory. Their speed is especially critical when operating in the two-way set-associative mode.

Cache Data Bus

The cache SRAM data bus should be connected to the local data bus. Since this bus is also shared with the CPU, the coprocessor, the system controller, and main memory, careful attention should be given to signal order to reduce signal trace delays.

External Non-cacheable Areas

For reliable operation, the -EXTNC pin must not become active in an area that has previously been declared cacheable until after the cache is flushed. Otherwise, the 82C835 will continue to respond to cache hits to those areas.

Future Revisions

Hidden refresh is supported in Revision ES1 of the 82C835. To utilize this feature in the future without modifications to the system, current designs should latch the cache address bus from the local address bus. The CALE signal from the 82C835 can be used to control the latches (2 x 74F373).

Hidden refresh will allow the system controller to initiate a refresh cycle to the local DRAMs without putting the processor in Hold. Simultaneously, the 82C835 will drive the refresh address on the SA bus. The CPU can continue cache read hit cycles during this time while the system memory controller and the AT bus interface of the 82C835 completes the refresh cycle.

2.9 Test Considerations

For the duration of PWRGOOD, all outputs from the 82C835 will float, except CRD01, -CRD1, -CWE0L, -CWE0H, -CWE1L, and -CWE1H.

Section 3

Configuration Registers

3.1 CHIPS Configuration Registers

The configuration and diagnostics registers listed in this section are accessed through I/O ports 22H and 23H. An indexing scheme is used to reduce the number of I/O addresses required to access all configuration registers. Each access (either read or write) to an internal register is executed by first writing its index into port 22. This index controls the multiplexers gating the appropriate register data accessible as port 23H. Every register data access to port 23H must be preceded by writing the register index value to port 22H, even if the same indexed register is being accessed.

All bits indicated as "reserved" must be written as zero and are undefined for read accesses (may vary from one read to the next).

Index 20H *Cache Control Register (READ/WRITE)*

Index	Bits	Values and Functions
20H	7	Cache enable bit.
		(0): Cache disabled.
		1 : Cache enabled.
	6	(Reserved)
	5	Disable bit for cache directory update on read misses.
		(0): Normal cache operation.
		1 : Disable cache directory update for read misses. A cache read miss will not cause a directory update or change the data in cache datas RAM. Instead, a normal DRAM read operation will be performed. A cache write hit will update the cache data RAM.
	4	Enable bit for direct data SRAM access.
		(0): Normal cache operation.
		Two Way Set Associative mode. Access SRAM directly for 16 KB cache, Set 0 at 00000-01FFFH, Set 1 at 02000-03FFFH, plus the offset value specified by register REG24<4:0>. For 32KB cache, Set 0 at 00000-03FFFH, Set 1 at 04000-07FFFH, plus the offset value specified by register REG24<4:0>. **Direct Mapped mode.** Access SRAM directly for 16 KB cache, at 00000-03FFFH, plus the offset value specified by register REG24<4:0>. For 32KB cache, at 00000-07FFFH, plus the offset value specified by register REG24<4:0>.
	3	Write pulse width for cache read-miss.
		(0): Write pulse deasserted at the end of cycle.
		1 : Write pulse deasserted one half of PROCCLK before the end of cycle.
	2	Flush cache directory.
		(0): Normal cache operation.
		1 : Enable cache directory flush. When this bit is enabled, any access to cache directory RAM causes the particular valid field (of both sets) selected by the index address field to become invalid.
	1	Duplicated ALT GATEA20 (READ ONLY). Represents the current state of the bit 1 of port 92H, i.e. ALT GATEA20.
	0	KBD GATEA20 (READ ONLY). Represents the current state of the KBD GATEA20 pin.

Index 21H *Directory RAM Control Register (READ/WRITE)*

Index	Bits	Values and Functions
21H	7	Enable directory access.
		(0): Disable cache directory access.
		1 : Enable cache directory to be accessed through 8 bit peripheral data bus (XD bus).
	6	S3- Bit 3 of pointer to various fields of cache directory.
	5	S2- Bit 2 of pointer to various fields of cache directory.
	4	S1- Bit 1 of pointer to various fields of cache directory.
	3	S0- Bit 0 of pointer to various fields of cache directory.

S3	S2	S1	S0	Selection
1	1	1	1	Write to all fields of the selected entry.
1	0	0	0	Access to LRU field.
0	1	1	1	Access to high byte of tag field of set 1. (A<23:21>)
0	1	1	0	Access to low byte of tag field of set 1. (A<20:13>)
0	1	0	1	Access to high byte of valid field of set 1.
0	1	0	0	Access to low byte of valid field of set 1.
0	0	1	1	Access to high byte of tag field of set 0. (A<23:21>)
0	0	1	0	Access to low byte of tag field of set 0. (A<20:13>)
0	0	0	1	Access to high byte of valid field of set 0.
(0	0	0	0)	Access to low byte of valid field of set 0.

	2	Reserved.
	1	Bit-9 of the high order address for directory RAM.
	0	Bit-8 of the high order address for directory RAM.

Index 22H *Low Bits of Directory Address Register (READ/WRITE)*

Index	Bits	Values and Functions
22H	7:0	Low order address bits for directory RAM. Together with REG21<1><0>, they form a 10-bit address for a maximum of 1024 entries.

Index 23H *Reference Location Register (READ/WRITE)*

Index	Bits	Values and Functions
23H	7:0	Used as a reference location to directory RAM access. In order to access the cache directory, following IO cycle sequences should be used:
		1. Program REG21<7>=1 to enable directory access and setup the apropriate bits of registers 21H for proper selection of field to be accessed.
		2. Load register 22H and 21H (bit 0 and 1) with the desired directory index.
		3. Following I/O read from register 23H will read the contents of the directory RAM, I/O write to register 23 will load the value into the directory RAM.

Index 24H *SRAM Configuration and Direct Access Address Register (READ/WRITE)*

Index	Bits	Values and Functions
24H	7	Two-way Set-associative cache enable.
		(0): Direct Mapped cache.
		1 : Two-way Set-associative cache.
	6	Force -SBHE pin low.
		(0): Do not force.
		1 : Force -SBHE pin low for memory addresses above the boundary set by the Memory Boundary Register (Index=25H).
	5	Size of cache memory.
		(0): 16 KB data cache.
		1 : 32 KB data cache.
	4:0	The highest 5 address bits, A19 through A15, for SRAM direct access.

Index 25H *Memory Boundary Register (READ/WRITE)*

Index	Bits	Values and Functions
25H	7:0	Upper 8 bits of AT-bus memory start address. (Default value=FFH) For the control of forcing -SBHE to a low and other internal controls. The value of this register must be set between 10H and FFH, inclusive.

Index 26H *Version Register (READ)*

Index	Bits	Values and Functions
26H	7:4	Family type. This field will identify the specific part out of a potentially pin-compatible family. The value for 82C835 with cache support will be 0H.
	3:0	Version level bit-3 through bit-0. Starting with 0H this field will track the revision level of the silicon.

Index 27H *Special Control Register (READ/WRITE)*

Index	Bits	Values and Functions
27H	7	Reserved

Index 28H *Cacheable Block Enable Register 1 (READ/WRITE)*

Index	Bits	Values and Functions
28H	7	Cache 0CA000H-0CBFFFH (808KB-816KB).
		(0): Disabled.
		1 : Enabled.
	6	Cache 0C8000H-0C9FFFH (800KB-808KB).
		(0): Disabled.
		1 : Enabled.
	5	Cache 0C6000H-0C7FFFH (792KB-800KB).
		(0): Disabled.
		1 : Enabled.
	4	Cache 0C4000H-0C5FFFH (784KB-792KB).
		(0): Disabled.
		1 : Enabled.
	3	Cache 0C2000H-0C3FFFH (776KB-784KB).
		(0): Disabled.
		1 : Enabled.
	2	Cache 0C0000H-0C1FFFH (768KB-776KB).
		(0): Disabled.
		1 : Enabled.
	1	Cache 0B0000H-0BFFFFH (704KB-768KB).
		(0): Disabled.
		1 : Enabled.
	0	Cache 0A0000H-0AFFFFH (640KB-704KB).
		(0): Disabled.
		1 : Enabled.

Index 29H *Cacheable Block Enable Register 2 (READ/WRITE)*

Index	Bits	Values and Functions
29H	7	Cache 0DA000H-0DBFFFH (872KB-880KB).
		(0): Disabled.
		1 : Enabled.
	6	Cache 0D8000H-0D9FFFH (864KB-872KB).
		(0): Disabled.
		1 : Enabled.
	5	Cache 0D6000H-0D7FFFH (856KB-864KB).
		(0): Disabled.
		1 : Enabled.
	4	Cache 0D4000H-0D5FFFH (848KB-856KB).
		(0): Disabled.
		1 : Enabled.
	3	Cache 0D2000H-0D3FFFH (840KB-848KB).
		(0): Disabled.
		1 : Enabled.
	2	Cache 0D0000H-0D1FFFH (832KB-840KB).
		(0): Disabled.
		1 : Enabled.
	1	Cache 0CE000H-0CFFFFH (824KB-832KB).
		(0): Disabled.
		1 : Enabled.
	0	Cache 0CC000H-0CDFFFH (816KB-824KB).
		(0): Disabled.
		1 : Enabled.

Index 2AH *Cacheable Block Enable Register 3 (READ/WRITE)*

Index	Bits	Values and Functions
2AH	7	Cache 280000H-2FFFFFH (2.5MB-3MB).
		(0): Disabled.
		1 : Enabled.
	6	Cache 200000H-27FFFFH (2MB-2.5MB).
		(0): Disabled.
		1 : Enabled.
	5	Cache 180000H-1FFFFFH (1.5MB-2MB).
		(0): Disabled.
		1 : Enabled.
	4	Cache 100000H-17FFFFH (1MB-1.5MB).
		(0): Disabled.
		1 : Enabled.
	3	Cache 0F0000H-0FFFFFH (960KB-1MB).
		(0): Disabled.
		1 : Enabled.
	2	Cache 0E0000H-0EFFFFH (896KB-960KB).
		(0): Disabled.
		1 : Enabled.
	1	Cache 0DE000H-0DFFFFH (888KB-896KB).
		(0): Disabled.
		1 : Enabled.
	0	Cache 0DC000H-0DDFFFH (880KB-888KB).
		(0): Disabled.
		1 : Enabled.

Index 2BH *Cacheable Block Enable Register 4 (READ/WRITE)*

Index	Bits	Values and Functions
2BH	7	Cache 680000H-6FFFFFH (6.5MB-7MB).
		(0): Disabled.
		1 : Enabled.
	6	Cache 600000H-67FFFFH (6MB-6.5MB).
		(0): Disabled.
		1 : Enabled.
	5	Cache 580000H-5FFFFFH (5.5MB-6MB).
		(0): Disabled.
		1 : Enabled.
	4	Cache 500000H-57FFFFH (5MB-5.5MB).
		(0): Disabled.
		1 : Enabled.
	3	Cache 480000H-4FFFFFH (4.5MB-5MB).
		(0): Disabled.
		1 : Enabled.
	2	Cache 400000H-47FFFFH (4MB-4.5MB).
		(0): Disabled.
		1 : Enabled.
	1	Cache 380000H-3FFFFFH (3.5MB-4MB).
		(0): Disabled.
		1 : Enabled.
	0	Cache 300000H-37FFFFH (3MB-3.5MB).
		(0): Disabled.
		1 : Enabled.

Index 2CH *Cacheable Block Enable Register 5 (READ/WRITE)*

Index	Bits	Values and Functions
2CH	7	Cache E00000H-EFFFFFH (14MB-15MB).
		(0): Disabled.
		1 : Enabled.
	6	Cache D00000H-DFFFFFH (13MB-14MB).
		(0): Disabled.
		1 : Enabled.
	5	Cache C00000H-CFFFFFH (12MB-13MB).
		(0): Disabled.
		1 : Enabled.
	4	Cache B00000H-BFFFFFH (11MB-12MB).
		(0): Disabled.
		1 : Enabled.
	3	Cache A00000H-AFFFFFH (10MB-11MB).
		(0): Disabled.
		1 : Enabled.
	2	Cache 900000H-9FFFFFH (9MB-10MB).
		(0): Disabled.
		1 : Enabled.
	1	Cache 800000H-8FFFFFH (8MB-9MB).
		(0): Disabled.
		1 : Enabled.
	0	Cache 700000H-7FFFFFH (7MB-8MB).
		(0): Disabled.
		1 : Enabled.

Index 2DH *Cacheable Block Enable Register 6 (READ/WRITE)*

Index	Bits	Values and Functions
2DH	7:3	Reserved.
	2	Cache FF0000H-FFFFFFH [(16MB-64KB)-16MB].
		(0): Disabled.
		1 : Enabled.
	1	Cache FE0000H-FEFFFFH [(16MB-128KB)-(16MB-64KB)].
		(0): Disabled.
		1 : Enabled.
	0	Cache F00000H-FDFFFFH [15MB-(16MB-128KB)].
		(0): Disabled.
		1 : Enabled.

Index 2EH — *RAM Write Protect Register (READ/WRITE)*

Index	Bits	Values and Functions
2EH	7	RAM 0F8000H-0FFFFFH (992KB-1MB).
		(0): Read and write.
		1 : Read only.
	6	RAM 0F0000H-0F7FFFH (960KB-992KB).
		(0): Read and write.
		1 : Read only.
	5	RAM 0E8000H-0EFFFFH (928KB-960KB).
		(0): Read and write.
		1 : Read only.
	4	RAM 0E0000H-0E7FFFH (896KB-928KB).
		(0): Read and write.
		1 : Read only.
	3	RAM 0D8000H-0DFFFFH (864KB-896KB).
		(0): Read and write.
		1 : Read only.
	2	RAM 0D0000H-0D7FFFH (832KB-864KB).
		(0): Read and write.
		1 : Read only.
	1	RAM 0C8000H-0CFFFFH (800KB-832KB).
		(0): Read and write.
		1 : Read only.
	0	RAM 0C0000H-0C7FFFH (768KB-800KB).
		(0): Read and write.
		1 : Read only.

Index 2FH *Cacheable Block Enable Register 7 (READ/WRITE)*

Index	Bits	Values and Functions
2FH	7	Cache 090000H-09FFFFH (576KB-640KB).
		(0): Disabled.
		1 : Enabled.
	6	Cache 080000H-08FFFFH (512KB-576KB).
		(0): Disabled.
		1 : Enabled.
	5	Cache 070000H-07FFFFH (448KB-512KB).
		(0): Disabled.
		1 : Enabled.
	4	Cache 060000H-06FFFFH (384KB-448KB).
		(0): Disabled.
		1 : Enabled.
	3	Cache 050000H-05FFFFH (320KB-384KB).
		(0): Disabled.
		1 : Enabled.
	2	Cache 040000H-04FFFFH (256KB-320KB).
		(0): Disabled.
		1 : Enabled.
	1	Cache 020000H-03FFFFH (128KB-256KB).
		(0): Disabled.
		1 : Enabled.
	0	Cache 000000H-01FFFFH (000KB-128KB).
		(0): Disabled.
		1 : Enabled.

3.2 OS/2 Optimization Control Register

Addr 092H *OS/2 Optimization Control Register (WRITE)*

Addr	Bits	Values and Functions
092H	7:2	Reserved.
	1	ALT GATEA20.
		(0): MODA20 pin is forced low if all other gating signals for A20 are also low.
		1 : The logical value of MODA20 pin is equal to that of A20 from CPU.
	0	(not implemented in 82C835; see 82C836)

Note In 82C836, this register is READ/WRITE.

Section 4

Pin Descriptions

4.1 Pin Assignments

Table 4-1. Pin Definitions

Pin Name	Type	Drive	Description
A1:19, A21:23	I/O	4mA	Local address bus. Outputs for -MASTER=0 and -REF=1.
A20	I		Local address bit-20.
-BHE	I/O	4mA	Byte high enable input from 80386sx/80286. Output for -MASTER=0 & -REF=1.
-BLE	I		Byte low enable or local address bit-0 (A0) input from 80386sx.
GATEA20	I		GATEA20 from the KBD controller.
MODA20	O	2mA	Modified A20. Enabled by -MASTER=0 & -REF=1.
MODA0	I/O	2mA	Modified A0. Outputs for -MASTER=0 & -REF=1.
-ADS	I		Address Strobe from 80386sx.
W/-R, D/-C	I		Status inputs from 80386sx.
M/-IO	I		Status input from 80386sx.
SA0:16	I/O	24mA	System address bus. Inputs for -MASTER=0 & -REF=1.
SA17:19	O	24mA	System address bus. Enabled by -MASTER=1.
LA17:23	I/O	24mA	System address bus (traditionally unlatched). Inputs for -MASTER=0 & -REF=1.
-SBHE	I/O	24mA	Byte high enable to/from bus. Input for -MASTER=0 & -REF=1.
HLDA	I		Processor hold acknowledge.
XD0:7	I/O	2mA	X-Bus Data.
-XIOR	I/O	2mA	X-Bus I/O read command. Output for -MASTER=0 & -REF=1.
-XIOW	I/O	2mA	X-Bus I/O write command. Output for -MASTER=0 & -REF=1.
-XMEMR	I/O	2mA	X-Bus Memory read command. Output for -MASTER=0 and -REF=1.
-XMEMW	I/Ot	2mA	X-Bus Memory write command. Output for -MASTER=0 and -REF=1.
-MREF	I/O	2mA	Memory refresh signal. Output for -MASTER=0.
-IOR	I/O	24mA	S-Bus I/O read command. Output for -MASTER=1 & -REF=1.
-IOW	I/O	24mA	S-Bus I/O write command. Output for -MASTER=1 & -REF=1.
-MEMR	I/O	24mA	S-Bus Memory read command. Input for -MASTER=0 & -REF=1.

Table 4-1. Pin Definitions (continued)

Pin Name	Type	Drive	Description
-MEMW	I/O	24mA	S-Bus Memory write command. Output for -MASTER=1 & -REF=1.
-SMEMR	O	24mA	S-Bus System memory read command.
-SMEMW	O	24mA	S-Bus System memory write command.
-MASTER	I		Alternate bus master request.
AEN	O	24mA	S-Bus address enable.
-REF	I/O	24mA	S-Bus memory refresh signal. Output for -MASTER=1.
PWRGOOD	I		Power Good input.
XRST	I		Bus reset input.
PROCCLK	I		Processor clock input.
-READY	I/O	8mA	Ready to processor and from SCAT/sx.
-CRD0	O	8mA	Set 0 SRAM output enable (both bytes).
-CRD1	O	8mA	Set 1 SRAM output enable (both bytes). Not used for direct mapped implementation.
-CWE0H	O	8mA	Set 0 SRAM write enable-high byte.
-CWE0L	O	8mA	Set 0 SRAM write enable-low byte.
-CWE1H	O	8mA	Set 1 SRAM write enable-high byte. Not used for direct mapped implementation.
-CWE1L	O	8mA	Set 1 SRAM write enable-low byte. Not used for direct mapped implementation.
PT386	I		Processor type strap 1=80386sx, 0=Reserved.
-EXTNC	I		External non-cacheable input.
CALE	O	4mA	Control signal for external cache address latches. When CALE is low, cache addresses are latched.
SYSCLK	O/Diagnostic	4mA	82C835's version of SYSCLK (386sx phase clock).
-READYO	O/Diagnostic	2mA	82C835's contribution to -READY. Indicates a cache write-hit for DMA and MASTER cycles.

4.2 Pin Totals and Summary

Signal total: 98

Reserved pins: 0

Vcc total: 7

Vss total: 15

PIN TOTAL: 120

4.3 Numerical Listing of Pin Assignments

Table 4-2. Numerical Pin Definitions

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	A23	31	-BLE(A0)	61	SA8	91	XRST
2	A22	32	-CWE1L	62	Vss	92	-MREF
3	A21	33	-CWE0L	63	SA7	93	-XIOW
4	A20	34	-CWE1H	64	Vcc	94	-XIOR
5	A19	35	-CWE0H	65	SA6	95	-XMEMW
6	A18	36	-EXTNC	66	SA5	96	-XMEMR
7	A17	37	Vss	67	Vss	97	MODA20
8	A16	38	AEN	68	SA4	98	XD7
9	A15	39	-SMEMW	69	SA3	99	XD6
10	A14	40	Vss	70	SA2	100	XD5
11	A13	41	-SMEMR	71	Vss	101	XD4
12	A12	42	-IOW	72	SA1	102	XD3
13	A11	43	-IOR	73	SA0	103	XD2
14	Vcc	44	Vcc	74	Vcc	104	Vcc
15	Vss	45	Vss	75	Vss	105	Vss
16	PROCCLK	46	SA19	76	-SBHE	106	XD1
17	PT386	47	SA18	77	LA23	107	XD0
18	A10	48	SA17	78	LA22	108	MODA0
19	A9	49	Vss	79	LA21	109	GATEA20
20	A8	50	SA16	80	Vss	110	PWRGOOD
21	A7	51	Vcc	81	LA20	111	-READYO
22	A6	52	SA15	82	LA19	112	-READY
23	A5	53	SA14	83	Vcc	113	-MASTER
24	A4	54	Vss	84	LA18	114	HLDA
25	A3	55	SA13	85	Vss	115	M/-IO
26	A2	56	SA12	86	LA17	116	-BHE
27	A1	57	SA11	87	-MEMW	117	D/-C
28	CALE	58	Vss	88	-MEMR	118	W/-R
29	-CRD1	59	SA10	89	Vss	119	-ADS
30	-CRD0	60	SA9	90	-REF	120	SYSCLK

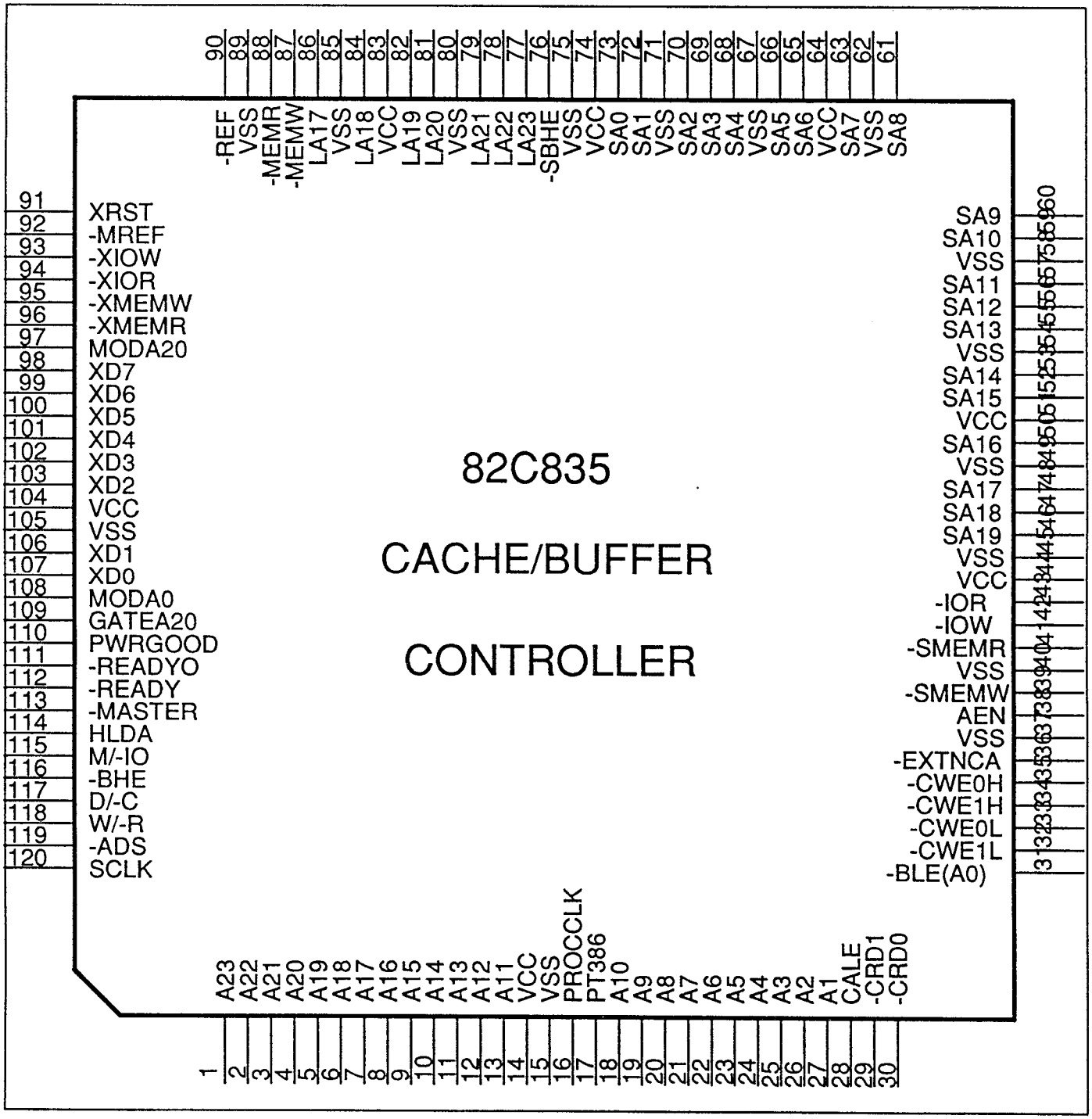
4.4 Alphabetical Listing of Pin Assignments

Table 4-3. Alphabetical Pin Definitions

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A1	27	-CWE0H	35	SA0	73	Vcc	104
A2	26	-CWE0L	33	SA1	72	Vss	15
A3	25	-CWE1H	34	SA2	70	Vss	37
A4	24	-CWE1L	32	SA3	69	Vss	40
A5	23	D/-C	117	SA4	68	Vss	45
A6	22	-EXTNC	36	SA5	66	Vss	49
A7	21	GATEA20	109	SA6	65	Vss	54
A8	20	HLDA	114	SA7	63	Vss	58
A9	19	-IOR	43	SA8	61	Vss	62
A10	18	-IOW	42	SA9	60	Vss	67
A11	13	LA17	86	SA10	59	Vss	71
A12	12	LA18	84	SA11	57	Vss	75
A13	11	LA19	82	SA12	56	Vss	80
A14	10	LA20	81	SA13	55	Vss	85
A15	9	LA21	79	SA14	53	Vss	89
A16	8	LA22	78	SA15	52	Vss	105
A17	7	LA23	77	SA16	50	W/-R	118
A18	6	-M/IO	115	SA17	48	XD0	107
A19	5	-MASTER	113	SA18	47	XD1	106
A20	4	-MEMR	88	SA19	46	XD2	103
A21	3	-MEMW	87	-SBHE	76	XD3	102
A22	2	MODA0	108	-SMEMR	41	XD4	101
A23	1	MODA20	97	-SMEMW	39	XD5	100
-ADS	119	-MREF	92	SYSCLK	120	XD6	99
AEN	38	PROCCLK	16	Vcc	14	XD7	98
-BHE	116	PT386	17	Vcc	44	-XIOR	94
-BLE(A0)	31	PWRGOOD	110	Vcc	51	-XIOW	93
CALE	28	-READY	112	Vcc	64	-XMEMR	96
-CRD0	30	-READYO	111	Vcc	74	-XMEMW	95
-CRD1	29	-REF	90	Vcc	83	XRST	91

4.5 Pin Diagram

Figure 4-1. 82C835 Cache Controller Pin Diagram



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Section 5

Physical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1. Physical Characteristics - Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	Vcc	-0.5	5.5	V
Input Voltage	V_{IN}	-0.5	5.5	V
Output Voltage	V_{OUT}	-0.5	5.5	V
Operating Temperature	Top	-25	85	°C
Storage Temperature	Tstg	-40	125	°C

Note Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. Exceeding the absolute maximum ratings can cause permanent damage to the device.

5.2 Operating Conditions

Table 5-2. Physical Characteristics - Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	Vcc	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

5.3 Capacitive Characteristics

Table 5-3. Physical Characteristics - Capacitive Characteristics

Parameter	Symbol	Min.	Max.	Units	Test Conditions
Input Capacitance	C_{IN}		10	pF	f_c= 1 MHz
I/O Capacitance	$C_{I/O}$		20	pF	Unmeasured pins grounded
Output Capacitance	C_{OUT}		20	pF	Unmeasured pins grounded

Section 6

DC/AC Characteristics

6.1 DC Characteristics

Table 6-1. *DC Characteristics of the 82C835*

Parameter	Symbol	Min.	Max.	Units
Input low voltage	V_{IL}		0.8	V
Input high voltage	V_{IH}	2.0		V
Output low voltage	V_{OL}†		0.4	V
Output high voltage	V_{OH}†	2.4		V
Input leakage current V_I = 0 to V_{CC}	I_{IL}	-10	20	µA
Output leakage current V_O = 0.45V to V_{CC}	I_{OL}	-10	20	µA
V_{CC} Supply current* C_{XIN} = 40 MHz	I_{CC}		100	mA

Note

*Application dependent.
†I_{OL} = 2mA, and I_{OH} = -2mA for MODA20, MODA0, XD0:7, -XIOR, -XIOW, -XMEMR, -XMEMW, -MREF, -READYO.
I_{OL} = 4mA, and I_{OH} = -4mA for A1:19, A21:23, -BHE, CALE, SYSCLK.
I_{OL} = 8mA, and I_{OH} = -8mA for -READY, -CRD0, -CRD1, -CWE0H, -CWE0L, -CWE1H, -CWE1L.
I_{OL} = 24mA, and I_{OH} = -24mA for SA0:16, SA17:19, LA17:23, -SBHE, -IOR, -IOW, -MEMR, -MEMW, -SMEMR, -SMEMW, AEN, -REF.

6.2 AC Characteristics

All timing parameters are specified under capacitive load of 50 pF and temperature of 70 degree C, unless otherwise stated. Unless otherwise specified, all the units discussed in the following tables are in nanoseconds. Also, the AC specifications mentioned in this document are subject to change.

Note that timing parameters are grouped into subsections according to the most common modes and cycle types to which they apply, but the parameters are not necessarily limited only to those cases. Unless otherwise noted, all referenced signals follow the stated functional relationship.

Legend

Direct	=	Cache programmed for Direct Mapped operation
2-Way	=	Cache programmed for 2-way set associative operation
CRMiss	=	Cache Read Miss
CRMiss - DWD	=	Cache Read Miss - Default Write Disable
CRMiss - EWD	=	Cache Read Miss - Early Write Disable
CWrite	=	Cache Write Hit (or Miss if appropriately programmed)
force -SBHE	=	82C835 programmed to force -SBHE low
DSA	=	Direct SRAM Access

Table 6-2. Clock Requirements

Symbol	Parameter	Min	Max
t01	Operating frequency		40 MHz
t02	PROCCLK period	25	
t03	PROCCLK high time @ 2V	10	
t05	PROCCLK low time @ 2V	10	
t07	PROCCLK fall time (3.7V to 0.8V)		8
t08	PROCCLK rise time (0.8V to 3.7V)		8

Table 6-3. Cache Control

Symbol	Parameter	Min	Max
t11	$CALE_L$ from $PROCCLK_H$		22
t12	$CALE_H$ from $PROCCLK_L$		21
t13	$CALE_H$ from CWEH - (CRMiss)	3	
t14	$-CRD_L$ from $PROCCLK_H$ - (Direct)		21
t15	$-CRD_H$ from $PROCCLK_H$ - (Direct)		15
t16	$-CRD_L$ from $PROCCLK_L$ - (2-Way)		13
t17	$-CRD_H$ from $PROCCLK_H$ - (2-Way)		14
t18	$-CWE_L$ from $PROCCLK_L$ - (CWrite)	0	
t19	$-CWE_H$ from $PROCCLK_H$ - (CWrite)	0	21
t20	$-CWE_L$ from $PROCCLK_H$ - (CRMiss)		21
t21	$-CWE_H$ from $PROCCLK_L$ - (CRMiss-EWD)	0	18
t22	$-CWE_H$ from $PROCCLK_H$ - (CRMiss-DWD)	0	13
t23	-CWE write pulse width - (CWrite)	25	
t24	$-CWE_L$ from $PROCCLK_H$ - (CWMiss)		25
t25	$-CWE_L$ from $PROCCLK_H$ - (DSA)		25
t26	$-CWE_H$ from $PROCCLK_H$ - (DSA)		23
t27	$-CRD_L$ from $PROCCLK_H$ - (DSA)		21
t28	$-CRD_H$ from $PROCCLK_H$ - (DSA)	6	21
t29a	$-READY_L$ delay from $PROCCLK_L$		22
t29b	$-READY_L$ delay from $PROCCLK_H$ - (DSA)		22
t30	$-READY_H$ delay from $PROCCLK_H$	4	25

Table 6-4. *Address/Control Requirements*

Symbol	Parameter	Min	Max
t31	A1-A4, A15-A23 setup to $PROCCLK_H$ - C_L=120 pF	20	
t32	A5-14 setup to $PROCCLK_H$ - C_L=65 pF	24	
t33	-BLE, -BHE setup to $PROCCLK_H$ - C_L-75 pF	20	
t34	A1-A23, -BLE, -BHE hold from $PROCCLK_H$	3	
t37	M/-IO, D/-C, W/R setup to $PROCCLK_H$	10	
t38	M/-IO, D/-C, W/-R hold from $PROCCLK_H$	3	
t39	-ADS setup to $PROCCLK_H$	10	
t40	-ADS hold from $PROCCLK_H$	3	
t41	XRST setup to $PROCCLK_H$	6	
t42	XRST hold from $PROCCLK_H$	3	
t43	-EXTNCA setup to $PROCCLK_H$	20	
t44	-EXTNCA hold from $PROCCLK_H$	3	
t45	-READY setup to PROCCLKH - (CRMiss-DWD)	10	
t46	-READY setup to PROCCLKL - (CRMiss-EWD)	10	
t47	-READY hold from PROCCLKH	3	

Table 6-5. *Address/Control Delays*

Symbol	Parameter	Min	Max
t51	SA<1-19> delay from A<1-19>	3	15
t52	SA<0> delay from MODA0		13
t53	SA<0-19> delay from $PROCCK_L$	3	15
t54	-SBHE delay from -BHE		25
t55	-SBHE delay from $PROCCLK_H$ (force -SBHE)		20
t56	LA<23-21, 19-17> delay from A<23-21, 19-17>		15
t57	LA<20> delay from A<20>		15
t58	-MEMR/-W delay from -XMEMR/-W		15
t59	-SMEMR/-W delay from -XMEMR/-W		15
t60	-IOR/-W delay from -XIOR/-W		15
t61	-REF delay from -MREF		18

Table 6-6. *Master Cycles*

Symbol	Parameter	Min	Max
t71	A<23-21, 19-17> delay from LA<23-21, 19-17>		13
t72	MODA20 delay from LA<20>		22
t73	-BHE delay from -SBHE		15
t74	-XMEMR/-W delay from -MEMR/-W	2	23
t75	-XIOR/-W delay from -IOR/-W	2	23
t76	-MREF delay from -REF		24

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Section 7

Timing Diagrams

Figure 7-1. *Supplemental AC Parameters*

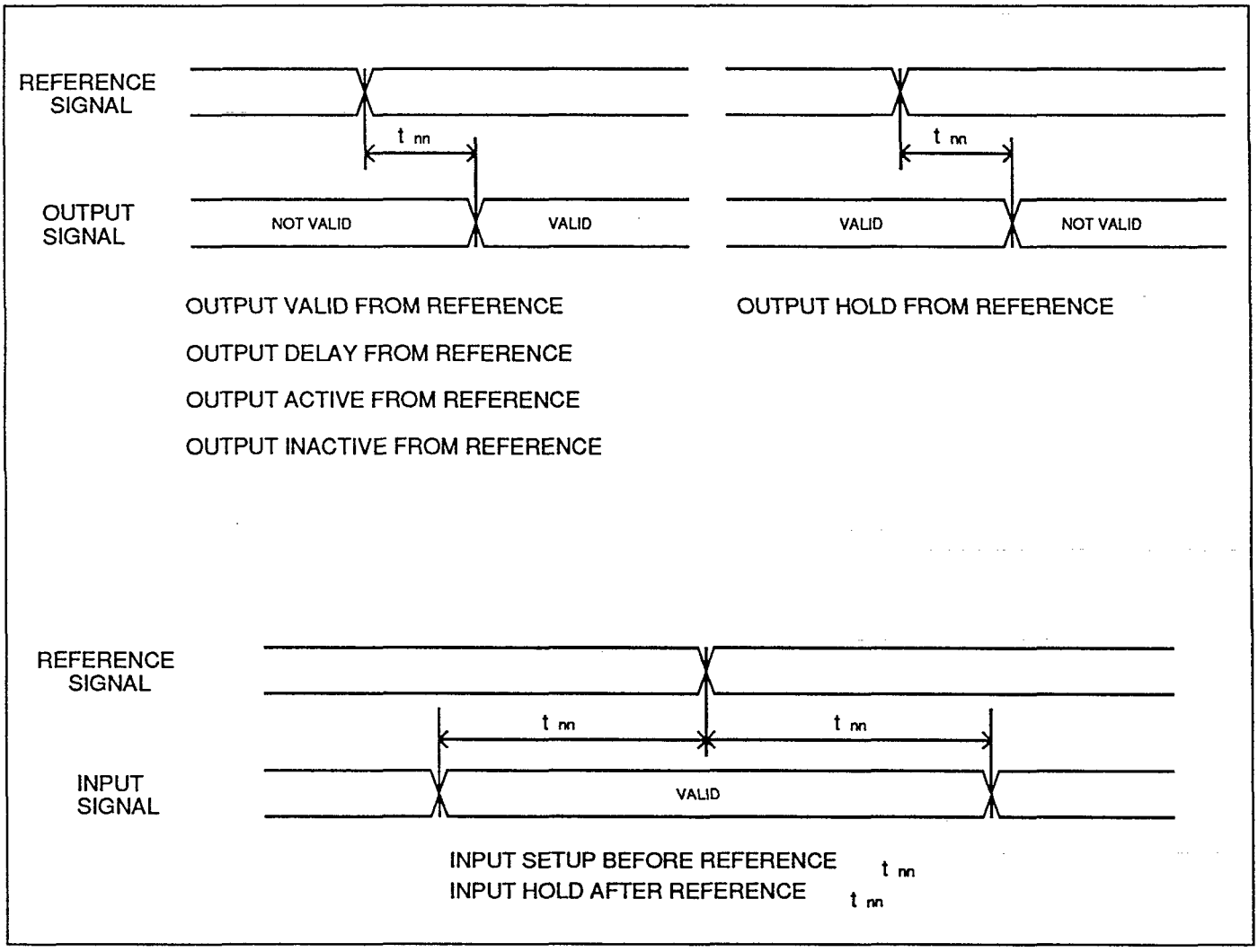


Figure 7-2. PROCCLK and AC Load Requirement

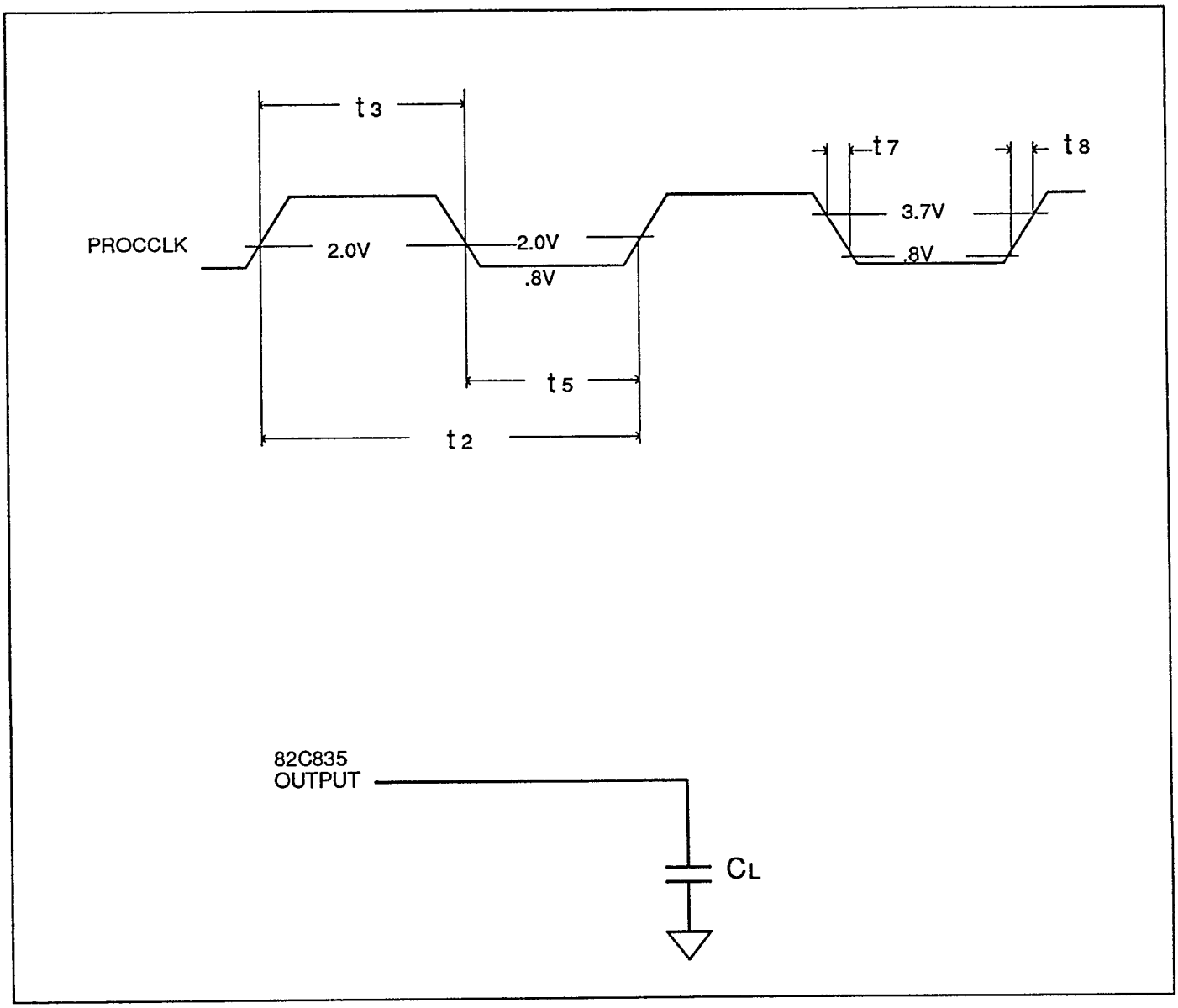


Figure 7-3. *CPU/82C835 Interface*

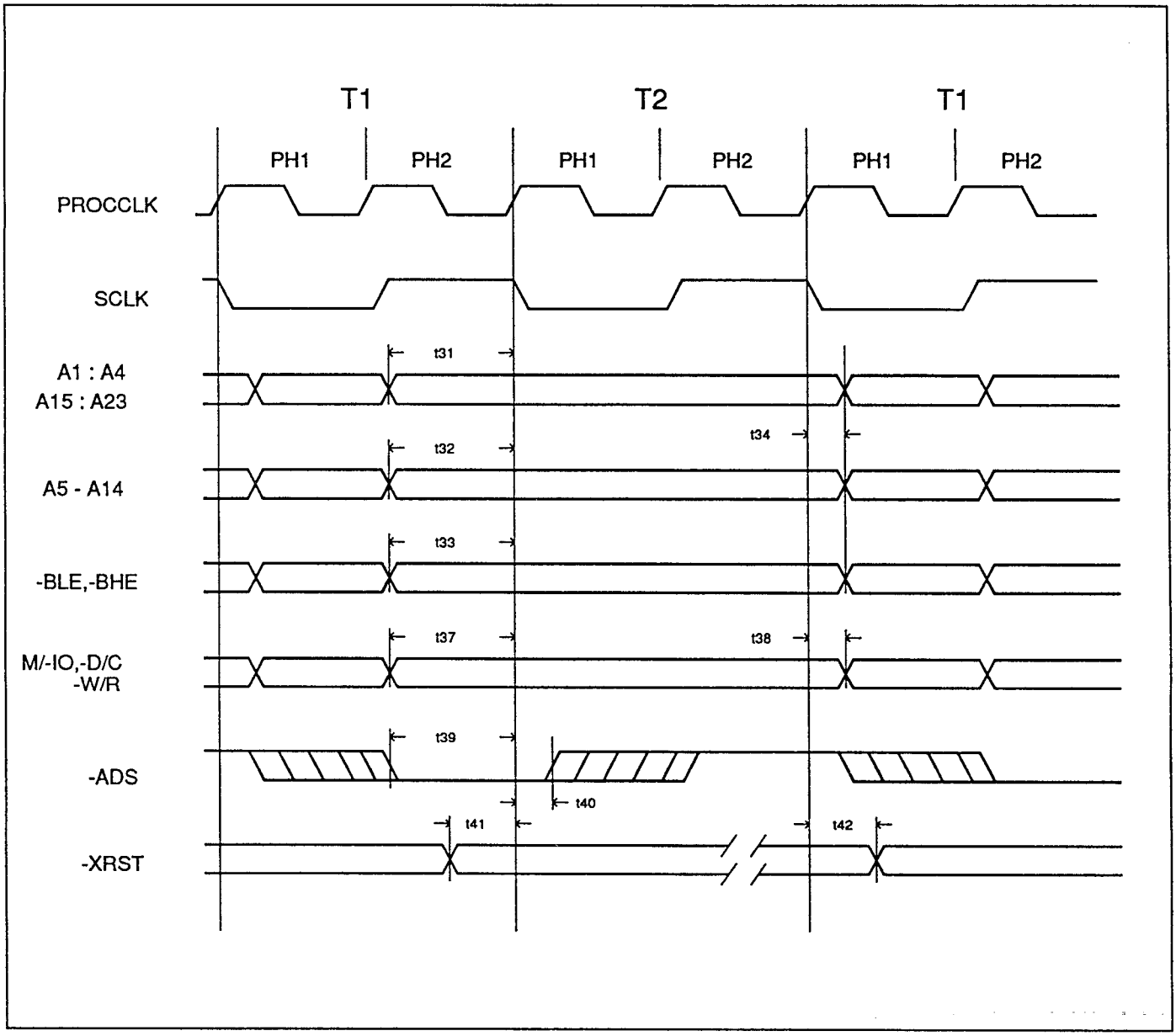


Figure 7-4. *Cache Read Hit*

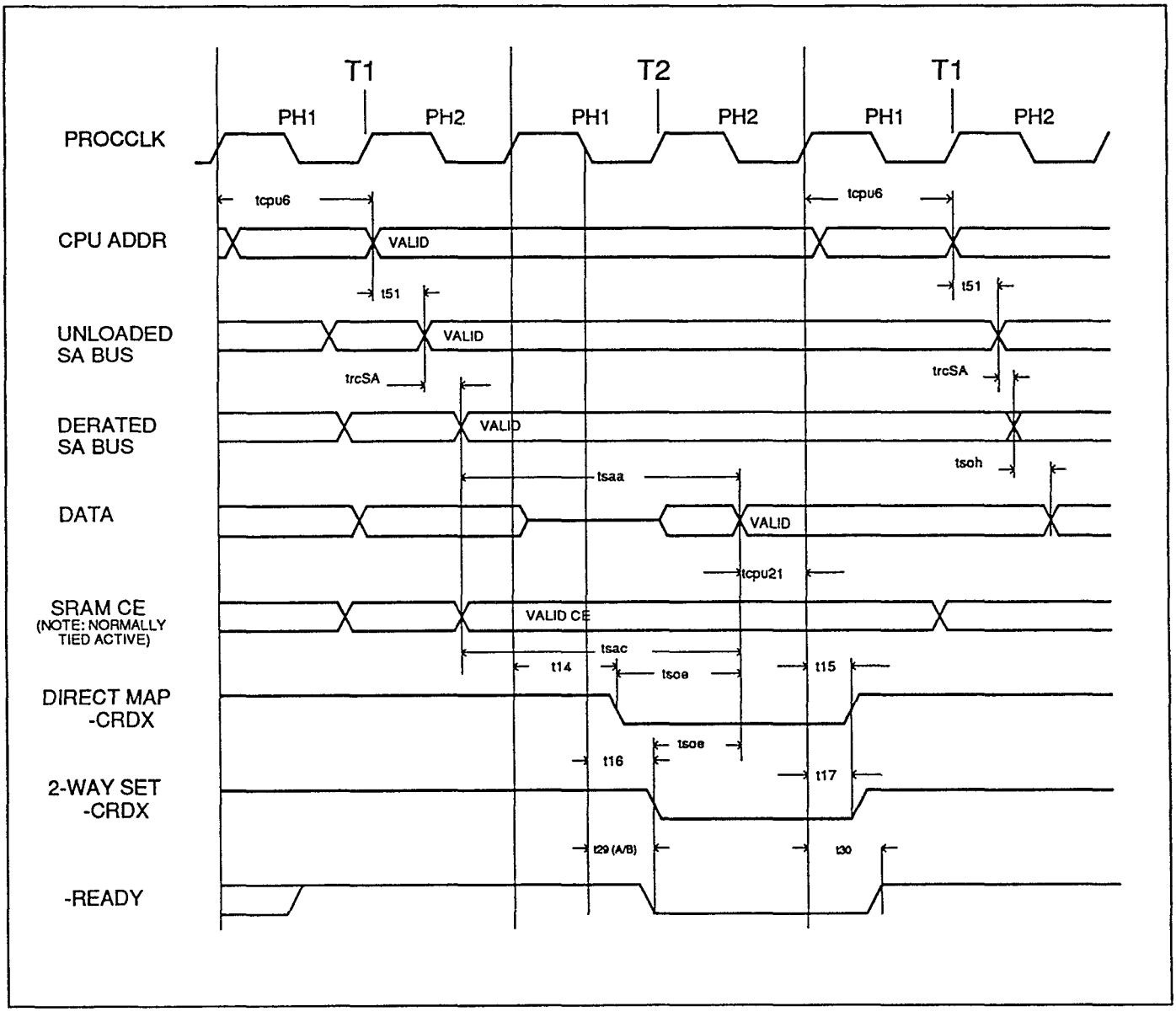


Figure 7-5. *Cache Write Hit*

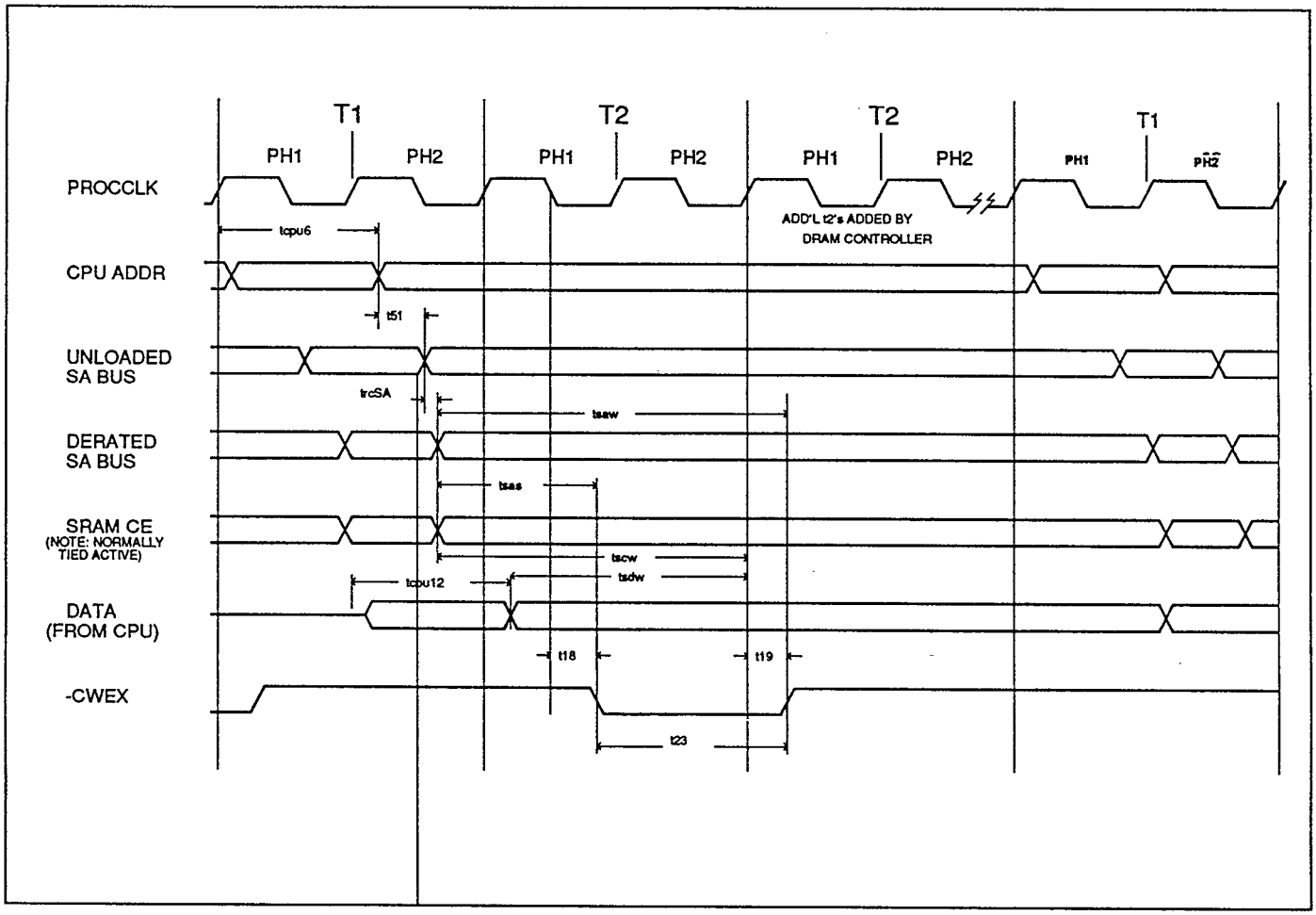


Figure 7-6. *Cache Read Miss*

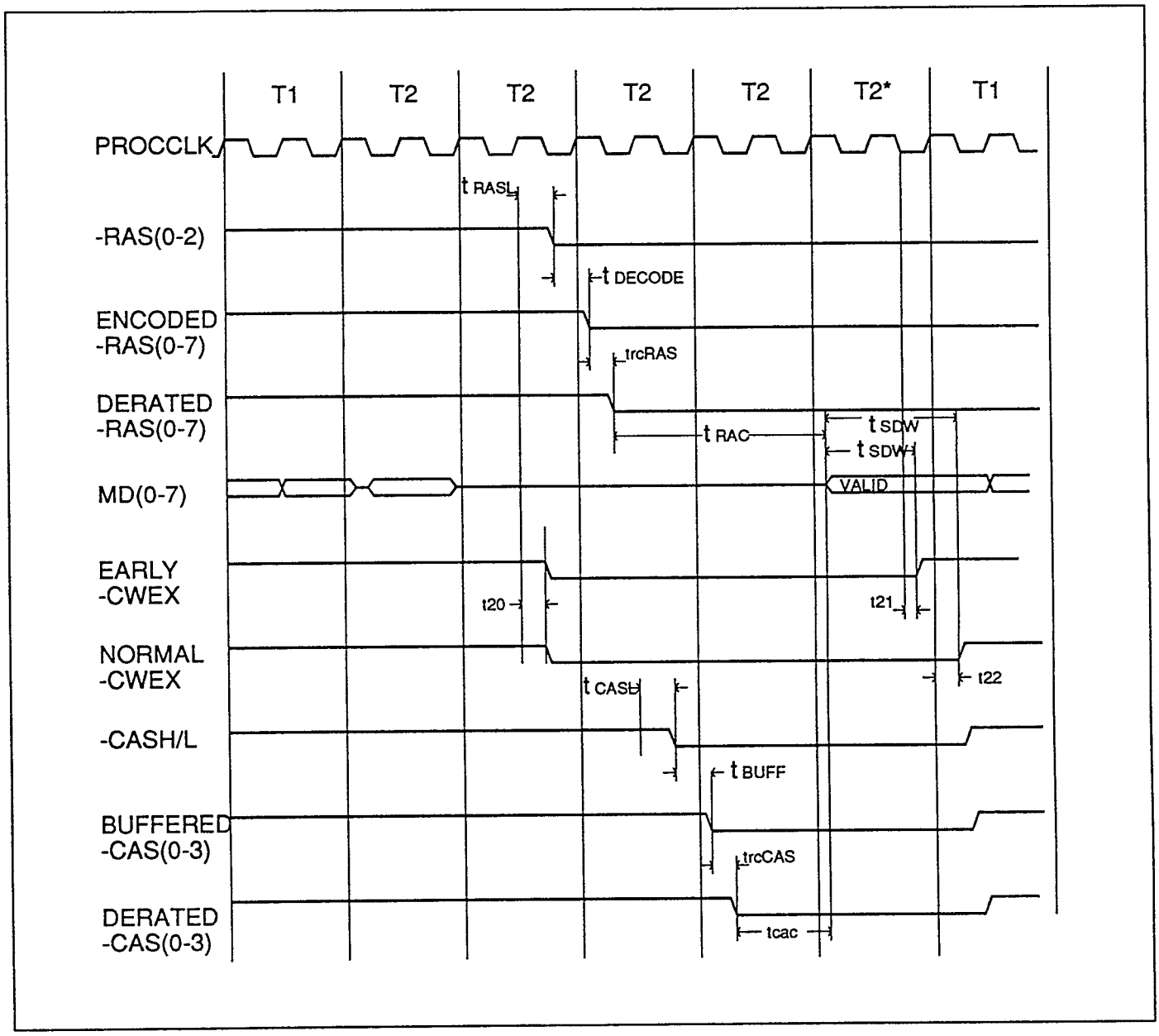


Figure 7-7. Cache Read Miss (Back-End Timing)

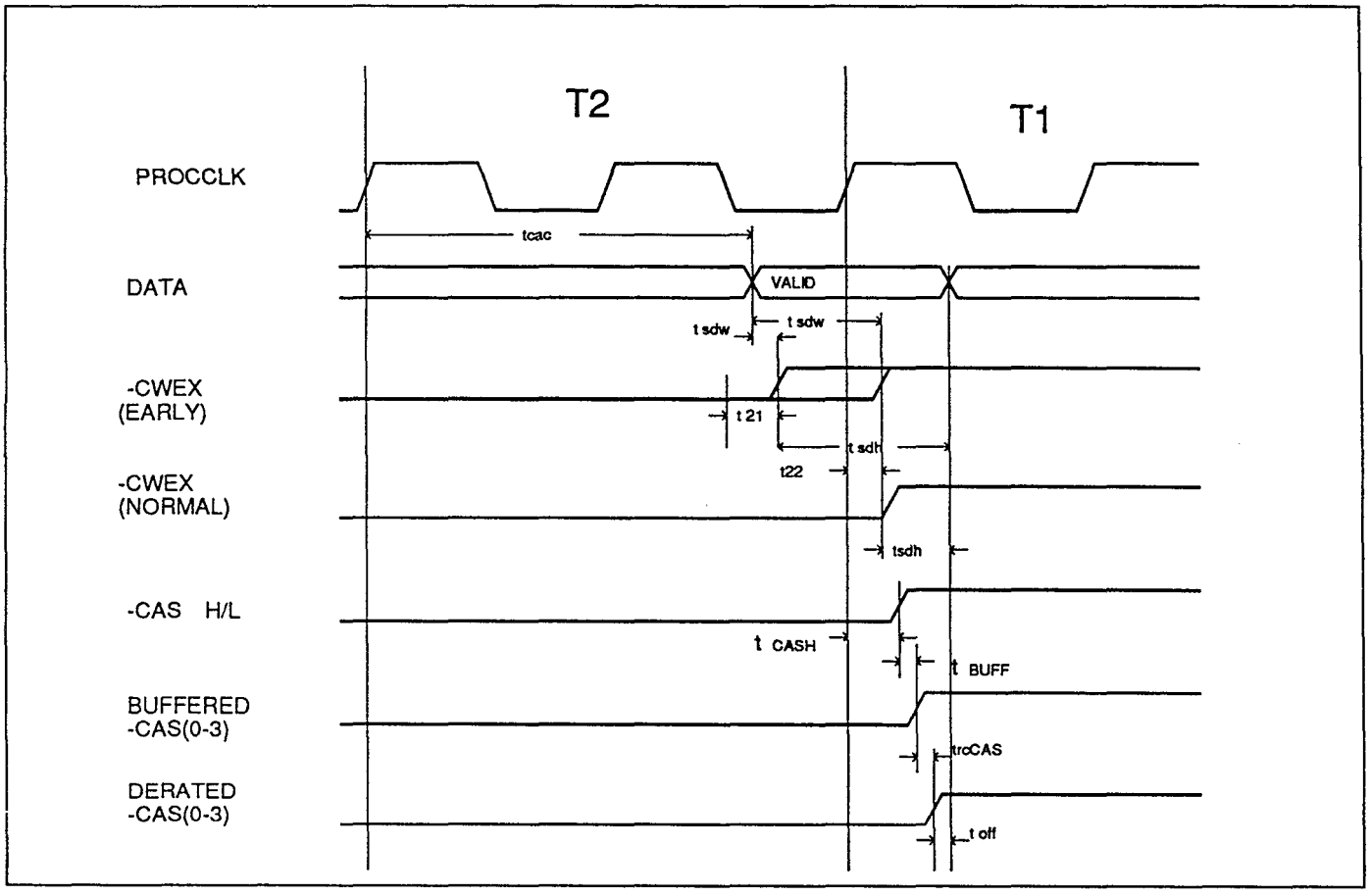


Figure 7-8. *CPU Write (After Cache Read Hit)*

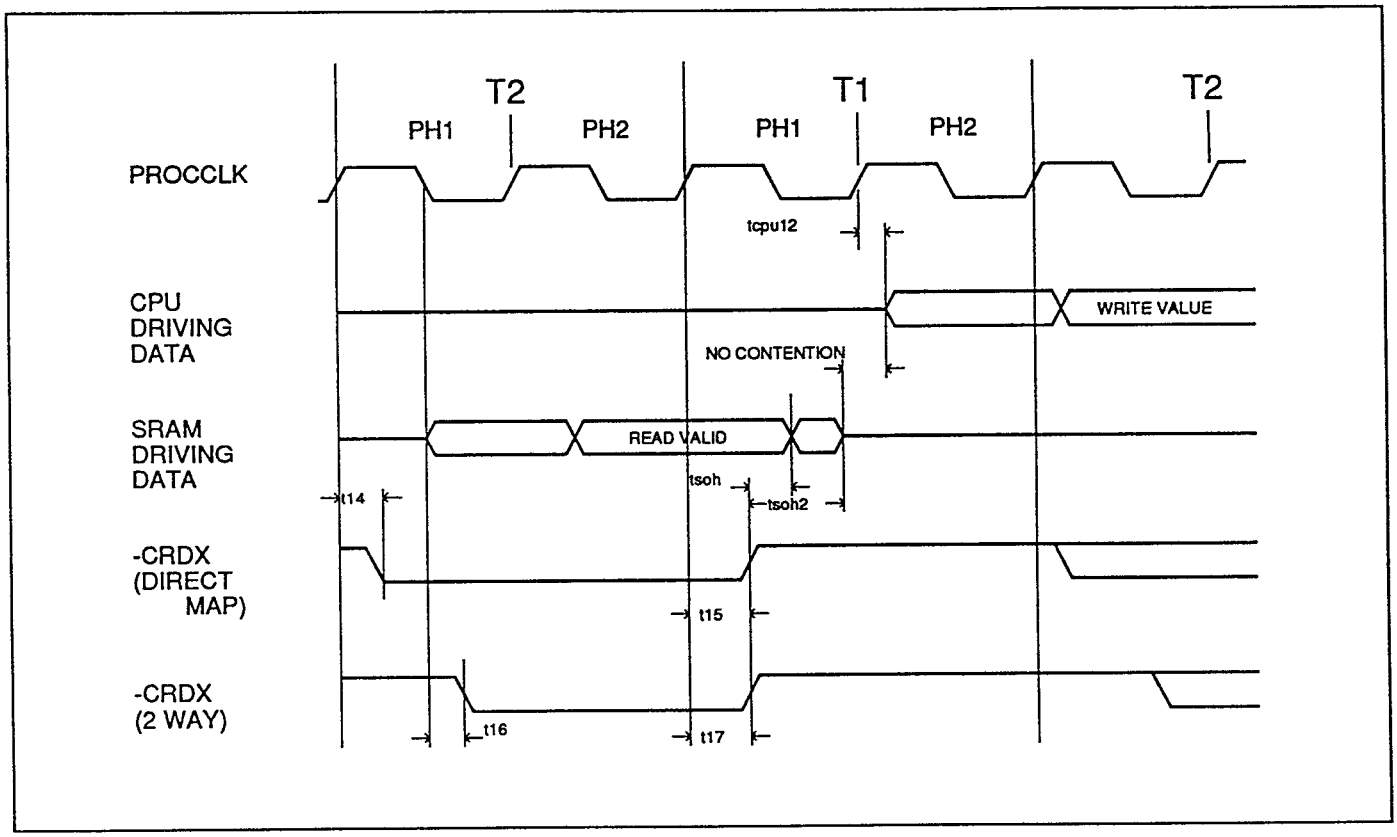
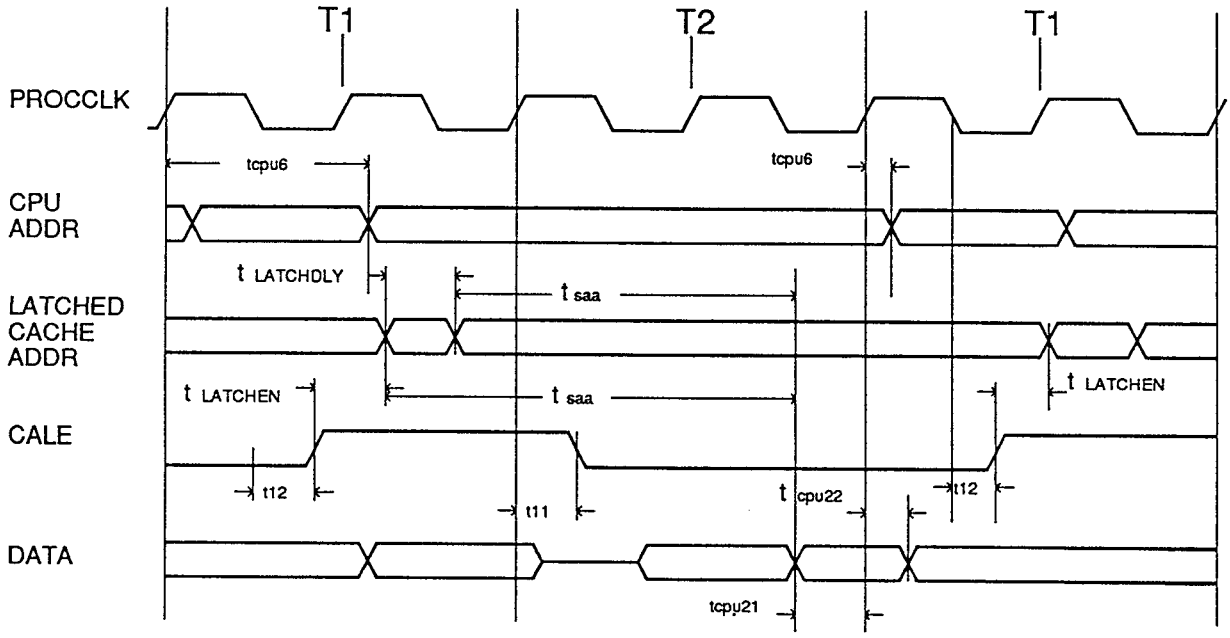


Figure 7-9. *CALE Timing*



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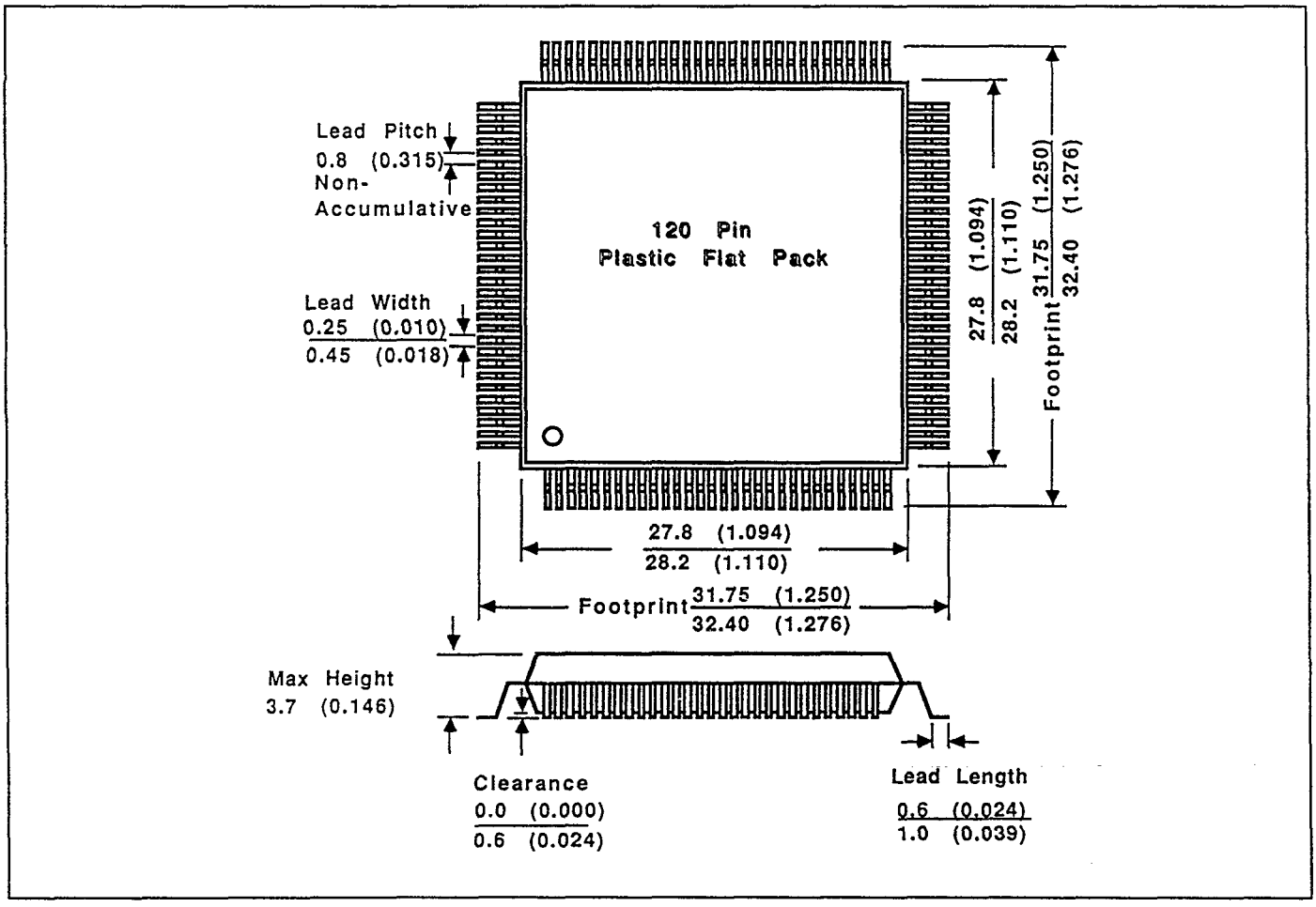
Section 8

Physical Dimensions

8.1 82C835 Cache Controller

Figure 8-1. 120-Pin Plastic Flat Package



Note 1 Package Body Size = 28 + 0.2/-0.4 (1.102 + 0.008/-0.016) (Swire)
Package Body Size = 28 ± 0.2 (1.102 ± 0.008) (All Other Package Vendors)

Note 2 Lead Length = 0.6 ± 0.3 (0.024 ± 0.012) (Package Vendor = Seiko)
Lead Length = 0.7 ± 0.2 (0.028 ± 0.008) (Package Vendor = Yamaha)
Lead Length = 0.8 ± 0.2 (0.031 ± 0.008) (All Other Package Vendors)

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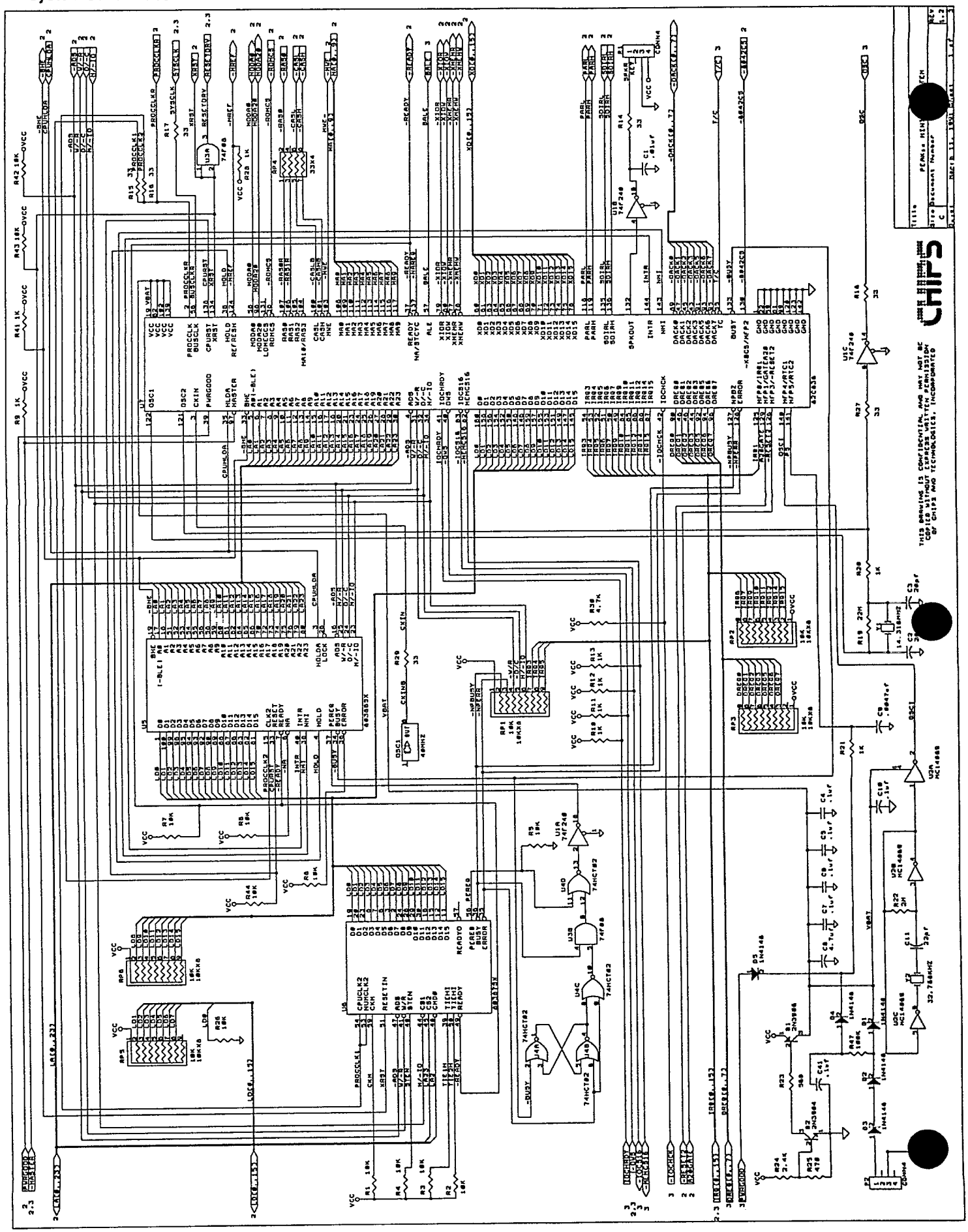
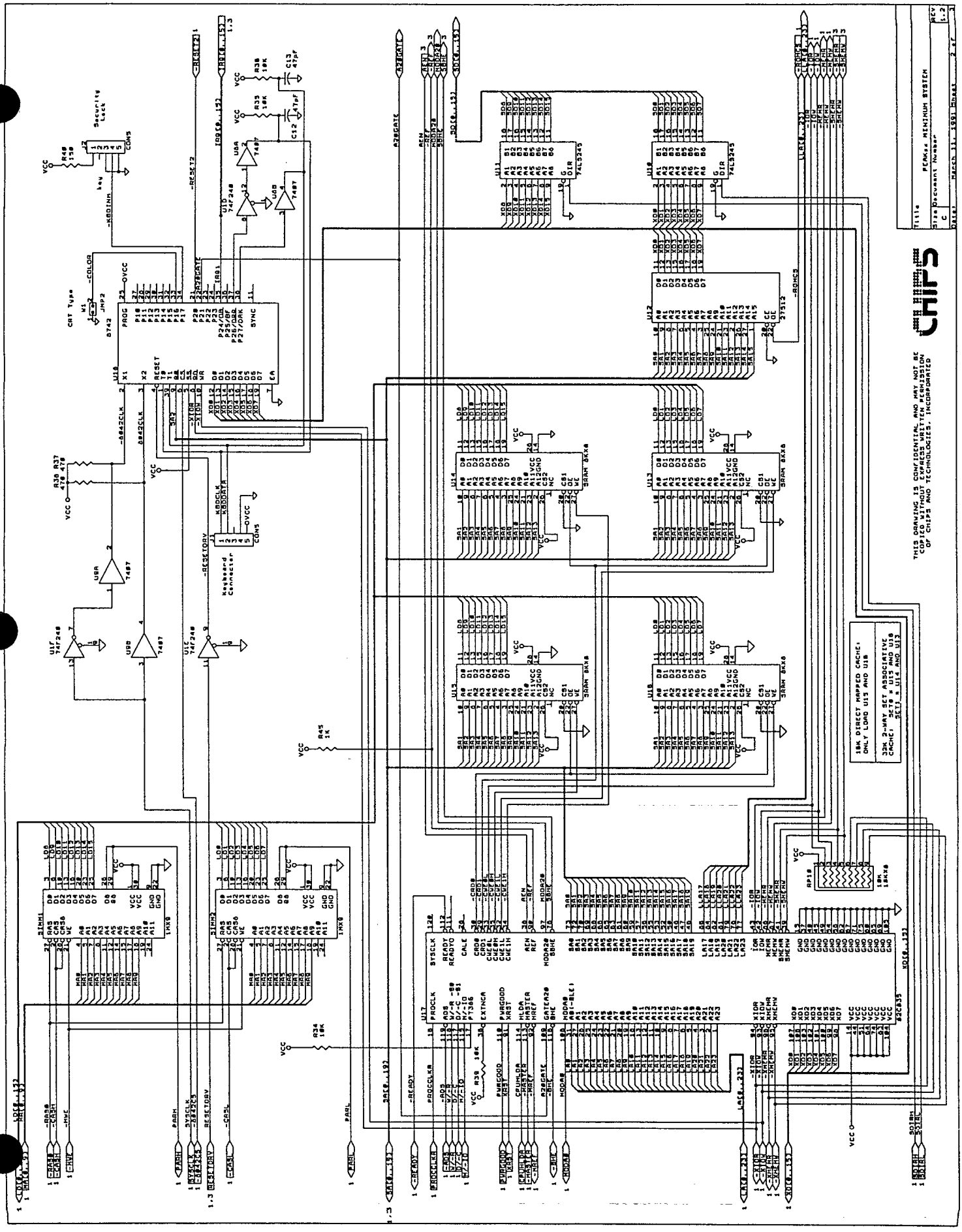
Appendix A

System Schematics

The following diagrams provide you with schematics of the Peak-sx minimum system.

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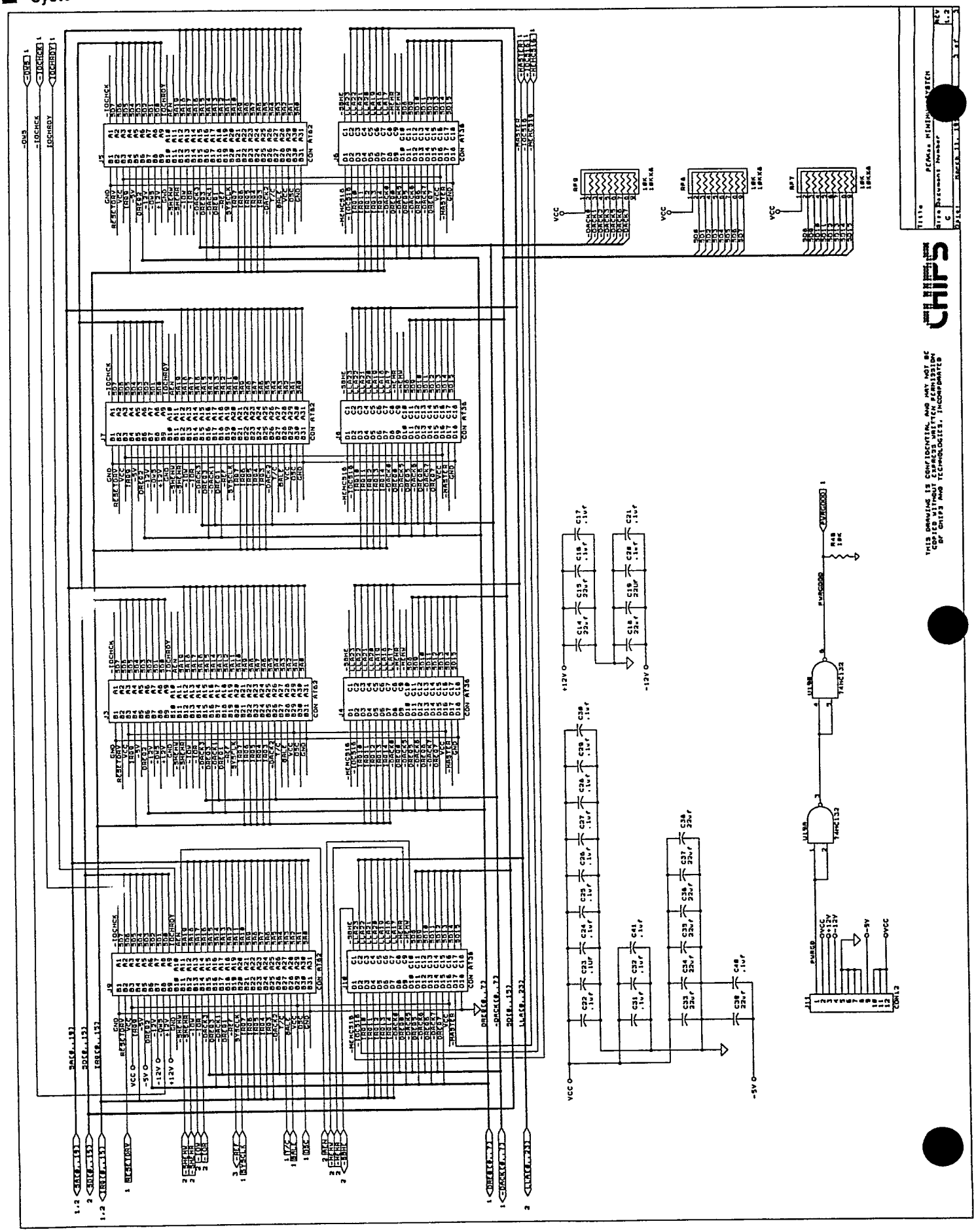
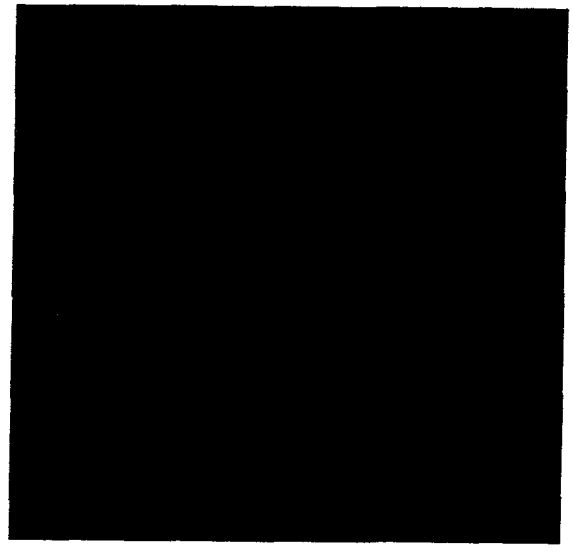
Title
PEMAX MINIMUM SYSTEM
Size C
Document Number
Date: March 11, 1991 Sheet 2 of 3
16K DIRECT MAPPED CACHE: ONLY LOAD U15 AND U16
32K 2-WAY SET ASSOCIATIVE CACHE: LOAD U15, U16, U14 AND U13





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