Pixel Semiconductor
A Cirrus Logic Company

CL-PX2080

Preliminary Data Book

FEATURES

- **Mixes graphics and video in real time**
- **Supports multiple, occluded video windows**
- **Pixel-clock rates up to 85 MHz**
  - — 1024 x 768 at 2^{24} colors, 76 Hz refresh rate
- **Extensive software support available — contact Cirrus Logic sales office for complete details**
- **Video inputs**
  - — RGB — 8:8:8, (1)5:5:5 (T), 5:6:5 RGB
  - — YUV — tagged or untagged 4:2:2
- **Graphics input format**
  - — Pseudocolor — 4- or 8-bit
  - — RGB — 5:6:5, 5:5:5, 8:8:8
- **Display functions:**
  - — Pseudocolor
  - — Display of true-color RGB data
  - — Interpolated, continuously variable zoom
  - — Hardware cursor controls
  - — Three graphics overlay controls: tagged chroma color key, graphics overlay color key, x/y window
- **Direct ISA/MCA bus interface**
- **Local bus interface**
- **Interlaced or non-interlaced output**

MediaDAC™

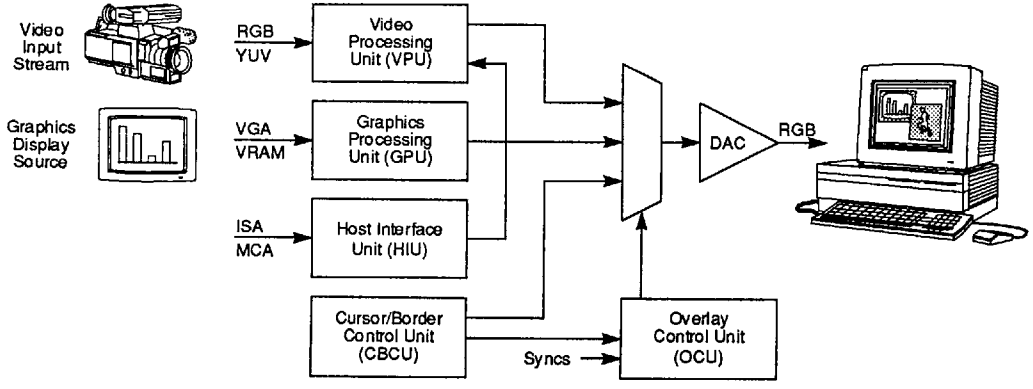
APPLICATIONS

- **Presentations**
- **Video Editing**
- **Video Authoring**
- **Video Teleconferencing**
- **Interactive Education**
- **Games**

OVERVIEW

The CL-PX2080 MediaDAC™ is a multiple-source digital-to-analog video converter. It mixes and manages two different input video data streams while converting the input data into the display subsystem format. It also converts color space and color resolution from the input to the output format in real time.

Simplified Functional Block Diagram



ARCHITECTURAL OVERVIEW

The MediaDAC inputs both video and graphics data. It converts the video data stream to its final output format, then mixes and/or overlays it with processed graphics data and cursor data.

The MediaDAC contains six functional blocks:

- Host Interface Unit (HIU)
- Video Processing Unit (VPU)
- Graphics Processing Unit (GPU)
- Cursor/Border Control Unit (CBCU)
- Overlay Control Unit (OCU)
- Monitor Interface Unit (MIU).

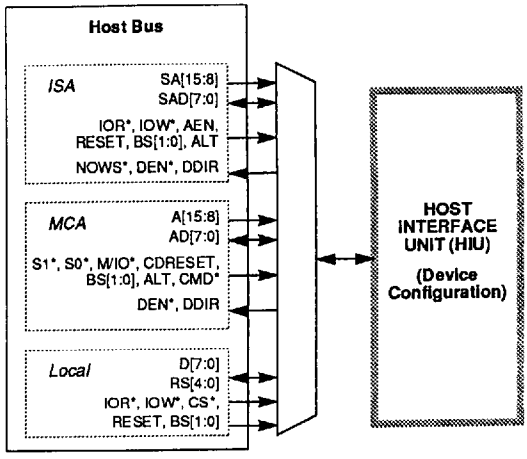
Host Interface Unit (HIU)

The HIU connects the MediaDAC™ directly to ISA and MCA buses, internally decoding a 16-bit address and responding as an 8-bit peripheral. (This interface eliminates most of the costly 'glue' circuitry common to PC expansion boards.) The HIU also interfaces with local hardware.

The HIU contains the bus interface and the configuration, control, and status registers.

Video Processing Unit (VPU)

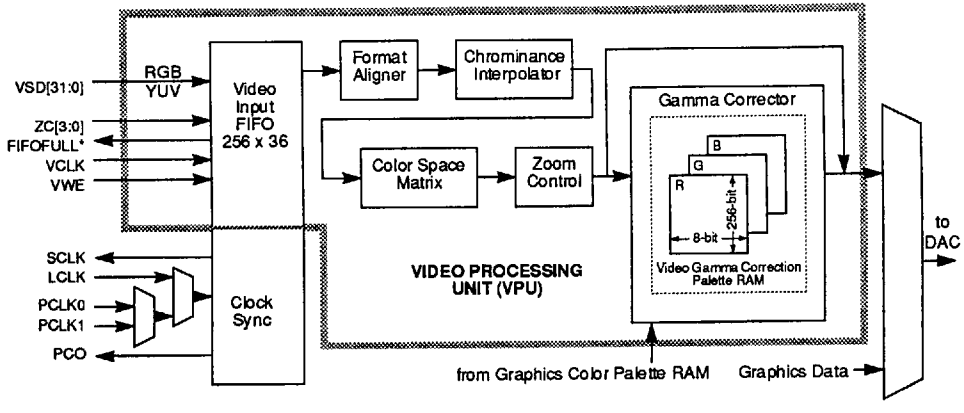
The VPU inputs digitized RBG and YUV video data in a wide range of formats. Its video processing functions are illustrated below.



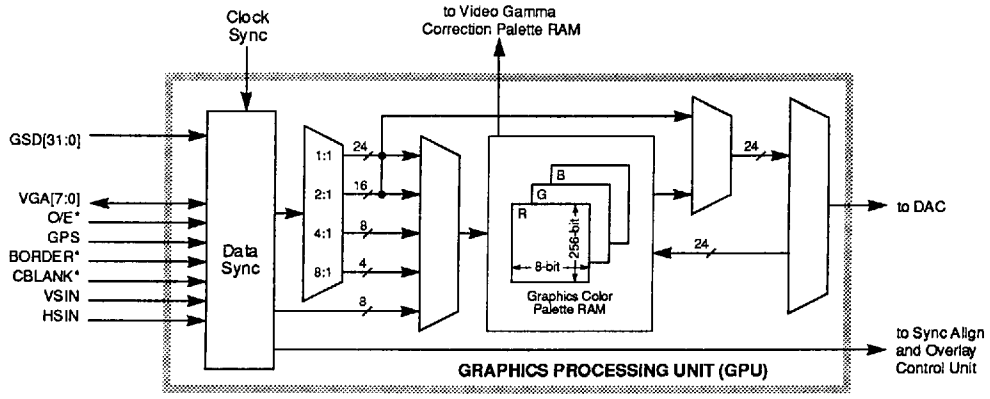
Host Bus Interface

VPU Features:

- 36-bit input data path (VSD[31:0], ZC[3:0])
- internal 256 x 36-bit input FIFO that supports:
  - — 24-bit RGB data (up to 40 million pixels)
  - — 16-bit RGB or YCbCr data (up to 85 million pixels)
- continuously variable zoom (up to 256x)
- format alignment
- chrominance interpolation
- YUV-to-RGB color-space conversion
- programmable gamma-correction/removal lookup table.



Video Processing Functions



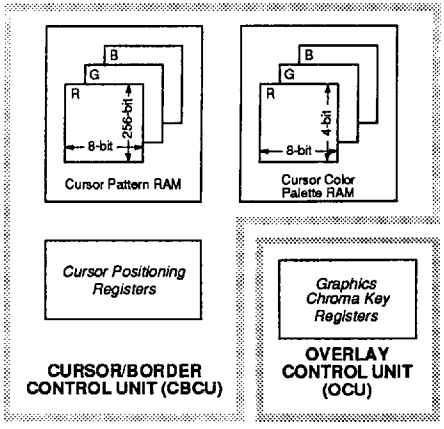
Graphics Processing Functions

Graphics Processing Unit (GPU)

The GPU accepts graphics data through either of two paths — VGA or VRAM — as shown above. As a result, PC graphics subsystems based on the MediaDAC can maintain compatibility with both types of systems.

GPU Features:

- VGA interface (VGA[7:0]):
  - — 8-bit VGA serial data port
  - — supports a large, existing installed base of systems and VGA-specific software.
- VRAM interface (GSD[31:0]):
  - — 32-bit high-resolution VRAM serial data port; supports a variety of architectures
  - — supports the next generation of higher-performance and higher-resolution products
  - — efficient pixel mapping within graphics-data word
- true-color (CLUT bypass) option



Cursor/Overlay Control Functions

Overlay Control Unit (OCU)

The OCU contains the Graphics Chroma Key registers. Its variety of operations allows the combination of video and graphics images.

Every graphics pixel is either opaque (its color information is displayed on the screen) or transparent (its color information is not displayed; instead, the color information of the video pixel behind it is displayed). The OCU determines which graphics pixels are transparent.

The MediaDAC has 256 possible overlay combinations based on the video-pixel tag bit, the graphics-pixel overlay color, and the XY window of the video data.

Cursor/Border Control Unit (CBCU)

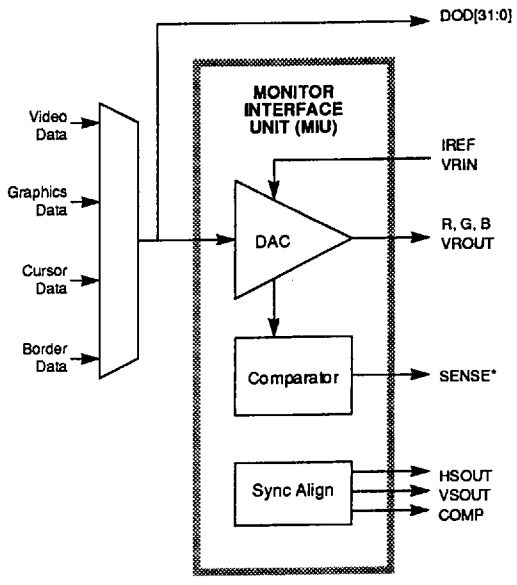
The MediaDAC implements an on-chip, three-color, user-definable 32 x 32 x 2 hardware cursor that works in both interlaced and non-interlaced systems. The color, pattern, and position of this hardware cursor is controlled by the CBCU. The CBCU also specifies the characteristics of the screen window borders.

Monitor Interface Unit (MIU)

The MIU contains three subunits, as illustrated:

- three video-speed, 8-bit digital-to-analog converters,
- internal comparators to provide the sense function, and
- sync alignment logic.

During power-down mode, the DACs are turned off and the RAM enters a low-power, data-retaining standby mode. The processor can read from or write to the RAM while the pixel clock is running. The RAM automatically enables during processor read/write cycles, then returns to a standby condition when processor access is completed.



RGB Monitor Interface

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CONVENTIONS, ABBREVIATIONS, AND TRADEMARKS

CONVENTIONS

GCKc	Register names that contain lowercase variables represent groups of registers with similar functions. For example, GCKc represents *all* of the Graphics Chroma Key registers — GCKR (Graphics Chroma Key Red), GCKG (Graphics Chroma Key Green), and GCKB (Graphics Chroma Key Blue). In this data book, the following register variables are used:		
	b (byte)	=	L (Low) or H (High)
	c (color space)	=	Y, U, V, R, G, or B

ABBREVIATIONS, ACRONYMS, and MNEMONICS

CCIR	Consultative Committee of International Radio	MCA	Micro Channel Architecture
CLUT	Color LookUp Table	MSB	Most Significant Byte
CMOS	Complementary Metal Oxide Silicon	MSb	Most Significant bit
CPU	Central Processing Unit	MUX	MUltipleX
CRT	Cathode Ray Tube	PQFP	Plastic Quad Flat Pack
DAC	Digital-to-Analog Converter	RGB	Red, Green, Blue
FIFO	First In, First Out	RAM	Random Access Memory
ISA	Industry Standard Architecture	RAMDAC	Random Access Memory Digital-to-Analog Converter
LSB	Least Significant Byte	TTL	Transistor/Transistor Logic
LSb	Least Significant bit	VGA	Video Graphics Architecture
LUT	LookUp Table	VRAM	Video dynamic Random Access Memory

TRADEMARKS

MediaDAC is a trademark of Pixel Semiconductor, Inc.

HiCOLOR™ is a trademark of Sierra Semiconductor.

1. PIN INFORMATION

The CL-PX2080 MediaDAC is available in a 160-lead Plastic Quad Flat Pack (PQFP) surface-mount package. It can be configured for ISA, MCA, and local hardware configurations, as shown in Figure 1-1.

NOTE: (*) denotes active-low signals.

1.1 Pin Diagram

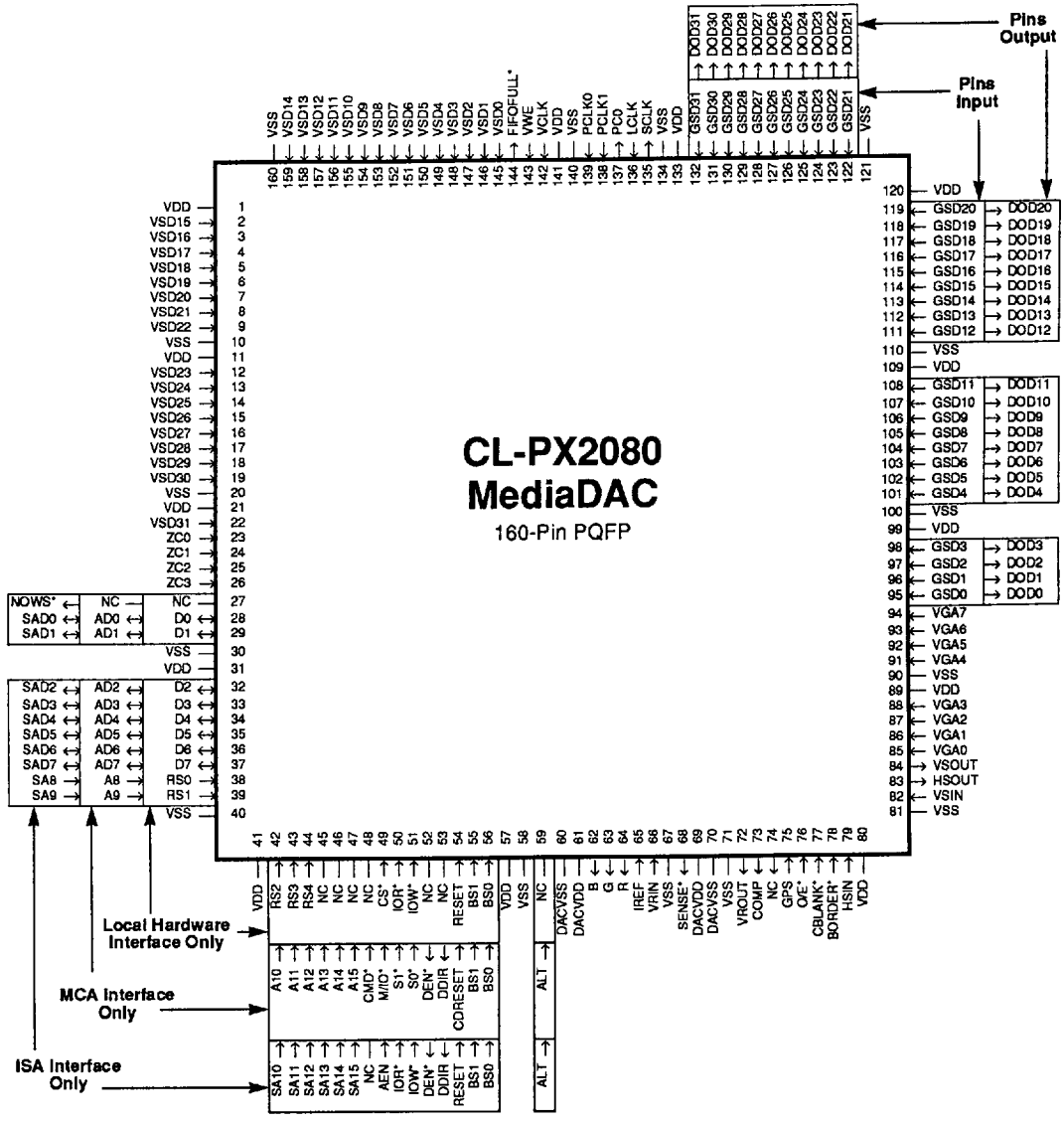


Figure 1-1. MediaDAC Pin Diagram

1.2 MediaDAC Functional Signal Groups

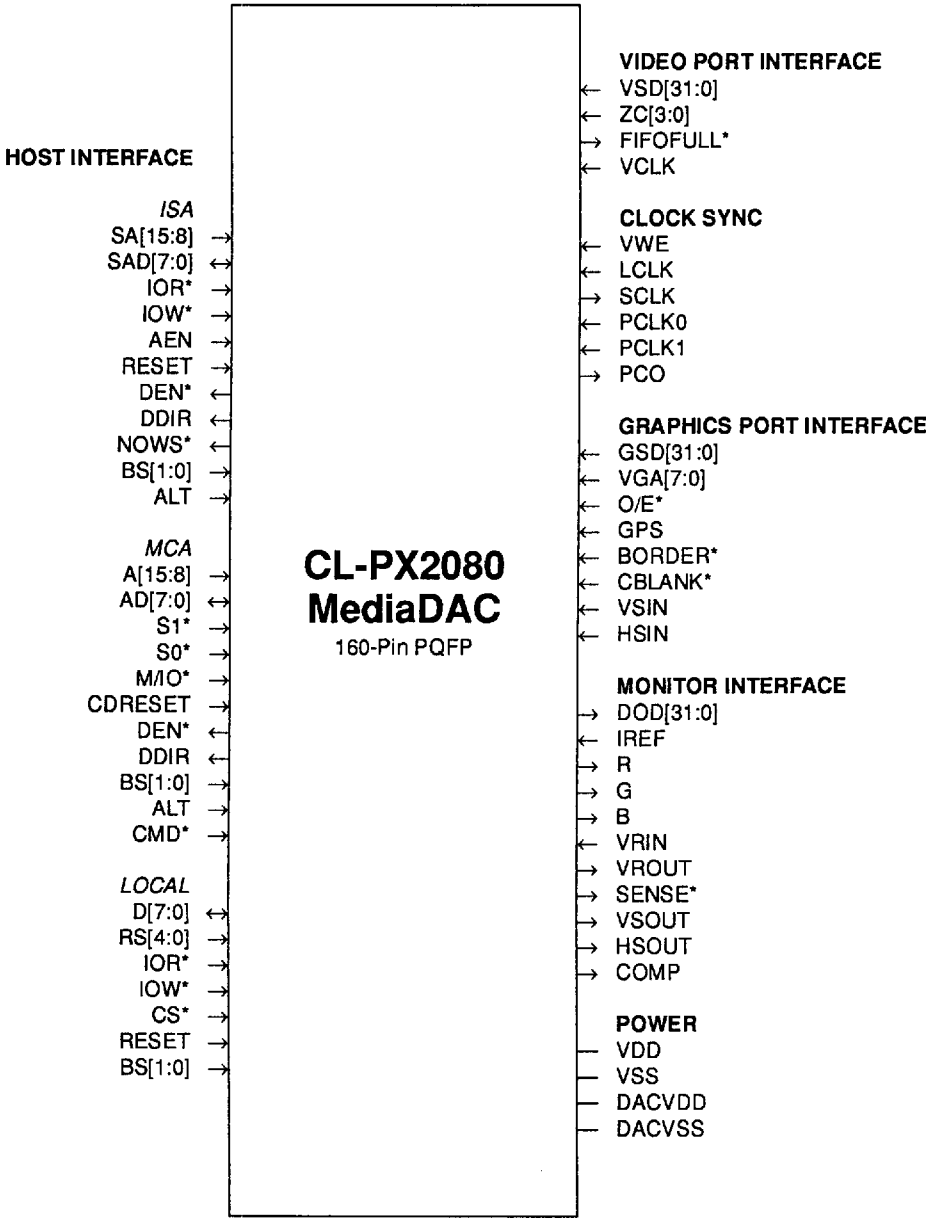


Figure 1-2. MediaDAC Functional Signal Group

1.3 Pin Assignment Table

The following conventions are used in the pin assignment table:

(*)	= active-low signal	TTL	= standard TTL input threshold and TTL output levels
I	= input	CMOS	= standard CMOS input threshold and CMOS output levels
O	= output	3S	= three-state TTL drive capability
AN	= analog signal	OD	= open drain, TTL inputs
PU	= internal pull-up	8	=
PD	= internal pull-down	12	= 12-mA sink and 4-mA source drive capability
PWR	= power	24	= 24-mA sink and 8-mA source drive capability

NAME			PIN	TYPE	CELL	FUNCTION
HOST INTERFACE						
ISA	**MCA**	**LOCAL**				
SA[15:8]	A[15:8]		47:42, 39:38	I	TTL	Address Bus — High Byte
SAD[7:0]	AD[7:0]		37:32, 29:28	I/O	3S, 8	Address and Data Bus — Low Byte
—	—	D[7:0]	37:32, 29:28	I/O	3S, 8	Data Bus
		NC	47:45	N/A	N/A	No Connect
		RS[4:0]	44:42, 39:38	I	PD, TTL	Register Select
IOR*	—	IOR*	50	I	TTL	I/O Read
—	S1*	—	50	I	TTL	Status 1
IOW*		IOW*	51	I	TTL	I/O Write
—	S0*	—	51	I	TTL	Status 0
AEN	—	—	49	I	TTL	Address Enable
—	M/IO*	—	49	I	TTL	Memory or I/O Cycle
—	—	CS*	49	I	TTL	Chip Select
RESET	CDRESET	RESET	54	I	TTL	Reset
DEN*	DEN*		52	O	OD, TTL, 8	Data Buffer Enable
—	—	NC	52	N/A	N/A	No Connect
DDIR	DDIR	—	53	O	OD, TTL, 8	Data Buffer Direction
—	—	NC	53	N/A	N/A	No Connect
NOWS*	—	—	27	O	OD, TTL, 24	No Wait State
—	NC	NC	27	N/A	N/A	No Connect
BS[1:0]	BS[1:0]	BS[1:0]	55:56	I	TTL	Bus Select
ALT	ALT	—	59	I	TTL	BIR alternate address
—	—	NC	59	N/A	N/A	No Connect
NC	—	NC	48	N/A	N/A	No Connect
—	CMD*	—	48	I	TTL	Command

NAME	PIN	TYPE	CELL	FUNCTION
VIDEO PORT INTERFACE				
VSD[31:0]	22, 19:12, 9:2, 159:145	I	PU, TTL, 8	Video Source Data
ZC[3:0]	26:23	I	TTL	Zoom Control Code
FIFOFULL*	144	O	TTL, 8	FIFO Full
VCLK	142	I	TTL	Video Data Clock
VWE	143	I	TTL	Video FIFO Write Enable
CLOCK SYNC				
LCLK	136	I	TTL	Latch Clock Input
SCLK	135	O	TTL, 12	VRAM Shift Clock Output
PCLK0	139	I	TTL	Pixel Input Clock 0
PCLK1	138	I	TTL	Pixel Input Clock 1
PCO	137	O	TTL, 12	Pixel Clock Output
GRAPHICS PORT INTERFACE				
GSD[31:0]	132:122, 119:111, 108:101, 98:95	I	PU, 3S, 8	Graphics Source Data (VRAM) (shares pins with DOD[31:0])
VGA[7:0]	94:91, 88:85	I	PU, TTL	VGA Graphics Source Data
O/E*	76	I	TTL	Odd/Even Field Input
GPS	75	I	TTL	Graphics Port Select
BORDER*	78	I	TTL	Active Display Border
CBLANK*	77	I	TTL	Composite Blank Input
VSIN	82	I	TTL	Vertical Sync Input
HSIN	79	I	TTL	Horizontal Sync Input
MONITOR INTERFACE				
DOD[31:0]	132:122,119:111,108:101, 98:95	O	PU, 3S, 8	Display Output Data
IREF	65	I	AN	Current Reference
R	64	O	AN	Analog Red
G	63	O	AN	Analog Green
B	62	O	AN	Analog Blue
VRIN	66	I	AN	Voltage Reference In
VROUT	72	O	AN	Voltage Reference Out
SENSE*	68	O	TTL, 8	Monitor Sense
VSOUT	84	O	TTL, 8	Vertical Sync Output
HSOUT	83	O	TTL, 8	Horizontal Sync Output
COMP	73	O		Compensation
POWER				
VDD	1, 11, 21, 31, 41, 57, 80, 89, 99, 109, 120, 133, 141		PWR	+5 VDC for Digital Logic and Interface Buffers
VSS	10, 20, 30, 40, 58, 67, 71, 81, 90, 100, 110, 121, 134, 140, 160		PWR	Ground for Digital Logic and Interface Buffers
DACVDD	61, 69		PWR	+5 VDC for DAC
DACVSS	60, 70		PWR	Ground for DAC

2. DETAILED SIGNAL DESCRIPTIONS

2.1 Host Interface — ISA

Signal	Pin	Type	Cell	Function
SA[15:8]	47:42, 39:38	I	TTL	**Address Bus — High Byte:** Specifies the resource to be accessed during an I/O or memory cycle.
SAD[7:0]	37:32, 29:28	I/O	3S, 8	**Address and Data Bus — Low Byte:** Bidirectional, multiplexed address/data bus that transfers video data and operation status and commands between the host system and the MediaDAC.
IOR*	50	I	TTL	**I/O Read:** 0 Specifies an I/O read cycle.
IOW*	51	I	TTL	**I/O Write:** 0 Specifies an I/O write cycle.
AEN	49	I	TTL	**Address Enable:** 0 I/O cycle in progress. 1 DMA cycle in progress.
RESET	54	I	TTL	**Reset:** 1 Stops all MediaDAC activity and resets the hardware.
DEN*	52	O	OD, TTL, 8	**Data Buffer Enable:** 0 Enables the host data bus buffer.
DDIR	53	O	OD, TTL, 8	**Data Buffer Direction:** Specifies the direction of data flow on SAD[7:0]. 0 The host system is reading data from SAD[7:0]. 1 The host system is writing data to SAD[7:0].
NOWS*	27	O	OD, TTL, 24	**No Wait State:** Instructs the host system to run a zero-wait-state cycle. The default ISA bus cycle is one wait state.
BS[1:0]	55:56	I	TTL	**Bus Select:** Specifies MediaDAC bus mode. 00 ISA 01 MCA 10 Local hardware 11 Reserved
ALT	59	I	TTL	**BIR alternate address:** Selects ISA address range for BIR access. 0 Primary ISA address range. 1 Secondary ISA address range.
NC	48	N/A	N/A	**No Connect:** (must be left floating).

2.2 Host Interface — MCA

Signal	Pin	Type	Cell	Function
A[15:8]	47:42, 39:38	I	TTL	**Address Bus — High Byte:** Specifies the resource to be accessed during an I/O or memory cycle.
AD[7:0]	37:32, 29:28	I/O	3S, 8	**Address and Data Bus — Low Byte:** Bidirectional, multiplexed data bus that transfers video data and operation status and commands between host system and the MediaDAC.
S1*	50	I	TTL	**Status 1:** Specifies current bus cycle (used with M/IO* and S0*).
S0*	51	I	TTL	**Status 0:** Specifies current bus cycle (used with M/IO* and S1*).
M/IO*	49	I	TTL	**Memory or I/O Cycle:** Specifies current bus cycle (used with S0* and S1*): **M/IO* S0* S1*** 0 0 0 Reserved 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Inactive 1 0 0 Reserved 1 0 1 Memory Write 1 1 0 Memory Read 1 1 1 Inactive
CDRESET	54	I	TTL	**Reset:** 1 Stops all MediaDAC activity and resets the hardware.
DEN*	52	O	OD, TTL, 8	**Data Buffer Enable:** 0 Enables the host data bus buffer.
DDIR	53	O	OD, TTL, 8	**Data Buffer Direction:** Specifies the direction of data flow on AD[7:0]. 0 The host system is reading data from AD[7:0]. 1 The host system is writing data to AD[7:0].
BS[1:0]	55:56	I	TTL	**Bus Select:** Specifies MediaDAC bus mode. 00 ISA 01 MCA 10 Local hardware 11 Reserved
ALT	59	I	TTL	**BIR alternate address:** Selects ISA address range for BIR access. 0 Primary ISA address range. 1 Secondary ISA address range.
CMD*	48	I	TTL	**Command:** 0 (write cycle) valid data is on bus AD[7:0] (read cycle) MediaDAC should place valid data on the bus
NC	27	N/A	N/A	**No Connect:** (must be left floating).

2.3 Host Interface — Local Hardware

Signal	Pin	Type	Cell	Function
D[7:0]	37:32, 29:28	I/O	3S, 8	**Data Bus:** Bidirectional data bus that accesses the internal control registers.
RS[4:0]	44:42, 39:38	I	PD, TTL	**Register Select:** Specifies the internal register to be accessed during a MediaDAC I/O cycle.
IOR*	50	I	TTL	**I/O Read:** 0 Specifies an I/O read cycle.
IOW*	51	I	TTL	**I/O Write:** 0 Specifies an I/O write cycle.
CS*	49	I	TTL	**Chip Select:** 0 The host system is accessing the MediaDAC.
RESET	54	I	TTL	**Reset:** 1 Stops all MediaDAC activity and resets the hardware.
BS[1:0]	55:56	I	TTL	**Bus Select:** Specifies MediaDAC bus mode. 00 ISA 01 MCA 10 Local hardware 11 Reserved
NC	59, 53:52, 48, 47:45, 27	N/A	N/A	**No Connect:** (must be left floating).

2.4 Video Port Interface

Signal	Pin	Type	Cell	Function
VSD[31:0]	22, 19:12, 9:2, 159:145	I	PU, TTL, 8	**Video Source Data:** Port through which video data enters the MediaDAC. The MediaDAC supports the following data formats (tagged and untagged): 16-bit YUV (4:2:2), 16-bit RGB (5:6:5), 24-bit RGB (8:8:8). VCLK transfers 16-bit modes as two pixels per pixel word.
ZC[3:0]	26:23	I	TTL	**Zoom Control Code:** (used with the CL-PX2070 DVP) Specifies several options for interpolation and alignment of the input video stream on VSD[31:0]. (Refer to the zoom code table in the *System Reference Manual*.)
FIFOFULL*	144	O	TTL, 8	**FIFO Full:** 0 Notifies the external video source that the 256-deep, double-pixel FIFO is within 8 pixels of a full condition.

2.4 Video Port Interface *(cont.)*

Signal	Pin	Type	Cell	Function
VCLK	142	I	TTL	**Video Data Clock:** On rising edge, clocks VSD[31:0] and ZC[3:0] data into the MediaDAC input video FIFO; generated by the source video processor when VWE = 1.
VWE	143	I	TTL	**Video FIFO Write Enable:** 0 Writes are disabled. 1 Data is written on the rising edge of VCLK.

2.5 Clock Sync

Signal	Pin	Type	Cell	Function
LCLK	136	I	TTL	**Latch Clock Input:** On rising edge, latches GSD[31:0] or VGA[7:0], and CBLANK*, HSIN, VSIN, GPS, and BORDER*. When the input data multiplexing rate is *x*:1, LCLK must equal PCLKn ÷ *x*. (*x*:1 = operating mode; *x* = 8, 4, 2, or 1.) **NOTE:** To avoid metastability, LCLK must maintain setup and hold requirements to SCLK.
SCLK	135	O	TTL, 12	**VRAM Shift Clock Output:** SCLK = PCLKn ÷ *x*. (*x*:1 = operating mode; *x* = 8, 4, 2, or 1.)
PCLK0	139	I	TTL	**Pixel Input Clock 0:** VGA input clock; enabled when register CSC, bit CS = 0.
PCLK1	138	I	TTL	**Pixel Input Clock 1:** High-speed GSD[31:0] input clock used during multiplexed operation of the 32-bit VRAM serial pixel port; Enabled when register CSC, bit CS = 1.
PCO	137	O	TTL, 12	**Pixel Clock Output:** Buffered output of PCLKn.

2.6 Graphics Port Interface

Signal	Pin	Type	Cell	Function
GSD[31:0]	132:122, 119:111, 108:101, 98:95	I	PU, 3S, 8	**Graphics Source Data (VRAM):** 32-bit VRAM serial data port that accepts data at 4, 8, 16, and 24 bits per pixel. Shares pins with output signals DOD[31:0].
VGA[7:0]	94:91, 88:85	I	PU, TTL	**VGA Graphics Source Data:** Enabled when register CSC, bit DPS = 00 (or DPS = 01 with pin GPS = 0). Latched on the rising edge of LCLK. All unused bits must be connected to VSS.

2.6 Graphics Port Interface *(cont.)*

Signal	Pin	Type	Cell	Function
O/E*	76	I	TTL	**Odd/Even Field Input:** Ensures proper operation of the cursor controller in interlaced mode (not used in non-interlaced mode). O/E* should be changed only during vertical blanking.
GPS	75	I	TTL	**Graphics Port Select:** Specifies GSD[31:0] or VGA[7:0] as the graphics port. In cobination with GFC_GPF, GPS defines condition PORTSEL (See BORDER* and register GFC definition). 0 VGA[7:0] is the graphic port. 1 GSD[31:0] is the graphic port.
BORDER*	78	I	TTL	**Active Display Border:** Used with CBLANK* and GPS to specify whether the DAC outputs are blanked or contain cursor, pixel, or border color (BORDER* = 1 when a display border is not used). CBLANK* BORDER* PORTSEL 0 X X Blanked area 1 0 0 VGA data 1 0 1 Overscan (border) 1 1 0 VGA data, cursor data 1 1 1 GSD data, cursor data
CBLANK*	77	I	TTL	**Composite Blank Input:** Applies a color value of '0' to the DAC inputs to produce black at the DAC outputs. The cursor position counters are referenced to CBLANK*.
VSIN	82	I	TTL	**Vertical Sync Input:** Generates a vertical sync pulse once per frame in non-interlaced mode, and once per field in interlaced mode. (Polarity-programmable.)
HSIN	79	I	TTL	**Horizontal Sync Input:** Generates a horizontal sync pulse every line. (Polarity-programmable.)

2.7 Monitor Interface

Signal	Pin	Type	Cell	Function
DOD[31:0]	132:122, 119:111, 108:101, 98:95	O	PU, 3S, 8	**Display Output Data:** (shares pins with input signals GSD[31:0]) Enabled when register CSC, bit DPS = 01, and outputs graphics data as follows: • GSD[23:16] = R[7:0] • GSD[26] = Window Active • GSD[15:8] = G[7:0] • GSD[25] = VSOUT • GSD[7:0] = B[7:0] • GSD[24] = HSOUT DOD[31:0] is latched on the rising edge of LCLK. All unused bits must be connected to VSS. DOD[31:0] will not run at maximum frequency.
IREF	65	I	AN	**Current Reference:** 8.8-mA reference current for the DAC.

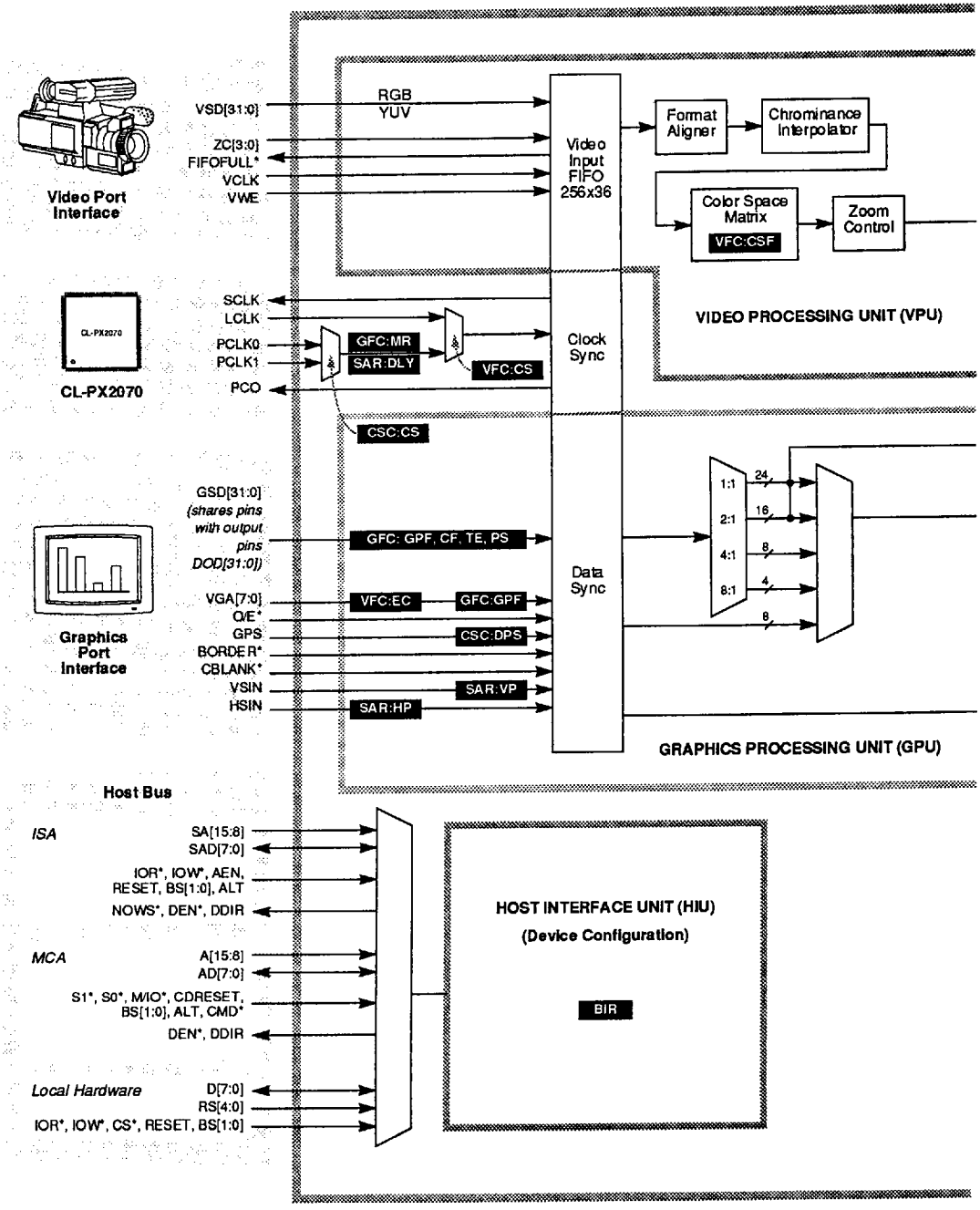
2.7 Monitor Interface *(cont.)*

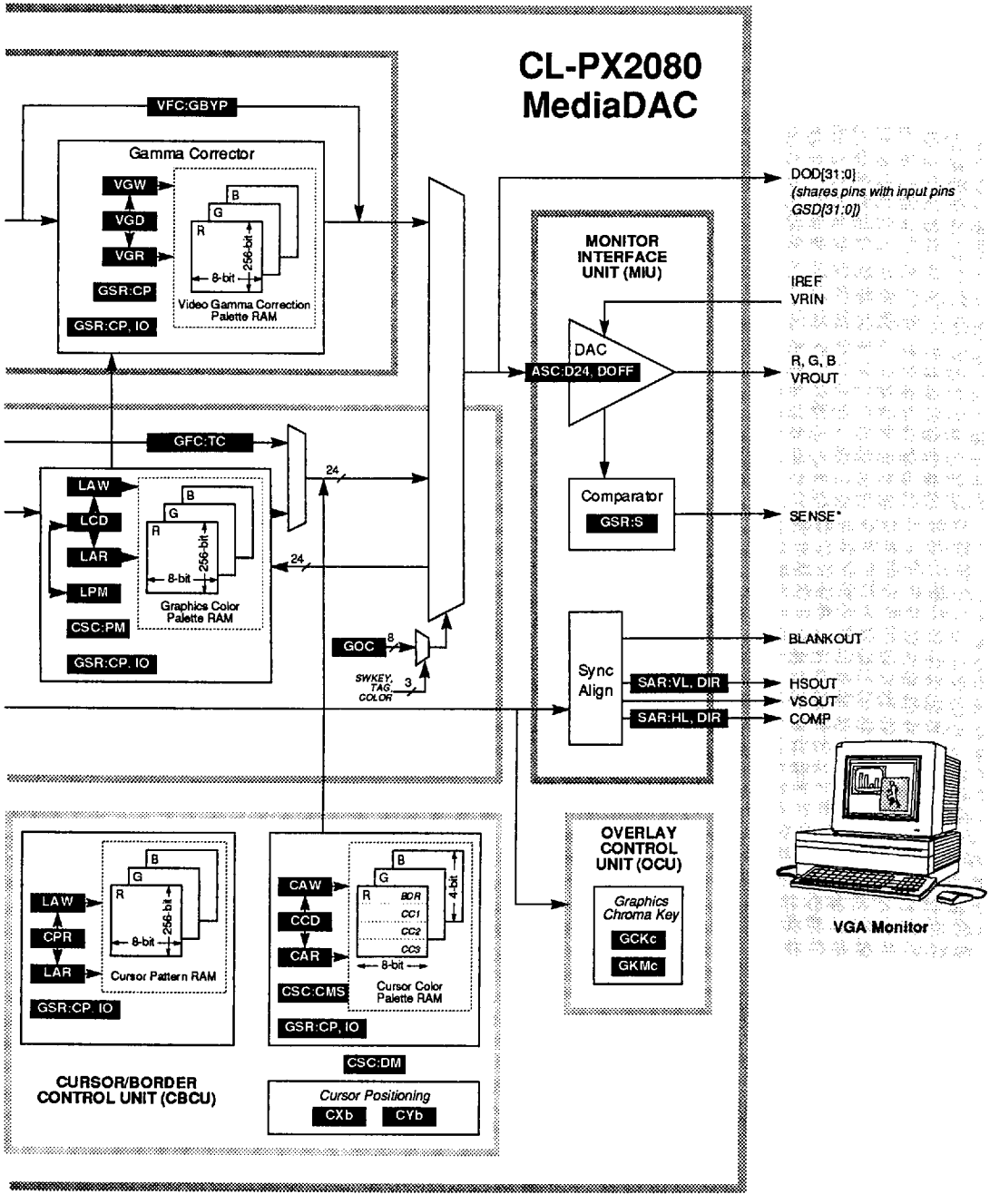
Signal	Pin	Type	Cell	Function
R	64	O	AN	**Analog Red:** The analog red channel from the 8-bit DAC.
G	63	O	AN	**Analog Green:** The analog green channel from the 8-bit DAC.
B	62	O	AN	**Analog Blue:** The analog blue channel from the 8-bit DAC.
VRIN	66	I	AN	**Voltage Reference In:** 1.23V reference voltage for the DAC.
VROUT	72	O	AN	**Voltage Reference Out:**
SENSE*	68	O	TTL, 8	**Monitor Sense:** A logical OR of the comparator outputs. Three level-detecting comparators individually monitor the red, green, and blue DAC outputs. A maximum analog DAC output level generates a high-level comparator output. A minimum analog level produces a low-level comparator output.
VSOUT	84	O	TTL, 8	**Vertical Sync Output:** Delay of HSIN. (Polarity-programmable.)
HSOUT	83	O	TTL, 8	**Horizontal Sync Output:** Delay of HSIN or a composite sync generated from HSIN and VSIN, as determined by register SAR. (Polarity-programmable.)
COMP	73	O	AN	**Compensation:** For best image quality, connect COMP to DACVDD (pin 69) with minimum length PC-board wiring through a series 0.1 µf capacitor. This stabilizes an internal reference voltage, minimizes inductive parasitics, and allows maximum benefit of the external capacitor.

2.8 Power

Signal	Pin	Type	Function
VDD	1, 11, 21, 31, 41, 57, 80, 89, 99, 109, 120, 133, 141	PWR	**+5 VDC for Digital Logic and Interface Buffers:** Each pin must be connected directly to the VDD plane.
VSS	10, 20, 30, 40, 58, 67, 71, 81, 90, 100, 110, 121, 134, 140, 160	PWR	**Ground for Digital Logic and Interface Buffers:** Each pin must be connected directly to the ground plane.
DACVDD	61, 69	PWR	**+5 VDC for DAC:** Each pin must be decoupled from digital VDD with a ferrite bead or inductor.
DACVSS	60, 70	PWR	**Ground for DAC:** Each pin must be connected to the analog ground plane.

3. FUNCTIONAL DESCRIPTION




CL-PX2080
MediaDAC
VFC:GBYP
Gamma Corrector
VGW
VGD
VGR
GSR:CP
GSR:CP, IO
B
G
R
256-bit
8-bit
Video Gamma Correction Palette RAM
GFC:TC
24
LAW
LCD
LAR
LPM
CSC:PM
GSR:CP, IO
Graphics Color Palette RAM
GOC
8
SWKEY, TAG, COLOR
3
MONITOR INTERFACE UNIT (MIU)
DAC
ASC:D24, DOFF
Comparator
GSR:S
Sync Align
SAR:VL, DIR
SAR:HL, DIR
DOD[31:0]
(shares pins with input pins GSD[31:0])
IREF
VRIN
R, G, B
VROUT
SENSE*
BLANKOUT
HSOUT
VSOUT
COMP
VGA Monitor
CPR
Cursor Pattern RAM
CURSOR/BORDER CONTROL UNIT (CBCU)
CAW
CCD
CAR
CSC:CMS
BDR
CC1
CC2
CC3
4-bit
Cursor Color Palette RAM
CSC:DIM
Cursor Positioning
CXb
CYb
OVERLAY CONTROL UNIT (OCU)
Graphics Chroma Key
GCKc
GKMc

4. REGISTERS

This section describes the internal registers that control MediaDAC operations.

NOTE: In order to maintain compatibility with future Pixel Semiconductor products, all reserved register bits must be written as '0'. Data values in reserved register locations are not guaranteed on readback.

Register names containing lowercase variables represent groups of registers with similar functions. Refer to the *Conventions* table on p. 7 for a list of MediaDAC register variables.

Table 4-1. MediaDAC Control Registers

Register Definition		Local	ISA / MCA			Ref. Pg.	Bit Definitions							
		RS [4:0]	Pri. Adr. BIR[5]=0	Sec. Adr. BIR[5]=1	BIR [2:0]		7	6	5	4	3	2	1	0
Memory Access Addressing and Indexing														
BIR	Block Index Register	N/A	0x27CE ALT=0 (BIR[5] N/A)	0x029E ALT=1 (BIR[5] N/A)	N/A	p. 22	IE	RE	SE	RO	RSVD	BLK		
Graphics Color Palette RAM Registers														
LAW	LUT Address Write	00h	0x03C8* 0x27CC†	N/A* 0x029C†	N/A* 000†	p. 23	WA[1]							
							P[2]	WA[2]						
LCD	LUT Color Data	01h	0x03C9* 0x27CD†	N/A* 0x029D†	N/A* 000†	p. 24	D							
LPM	LUT Pixel Mask	02h	0x03C6* 0x27CA†	N/A* 0x029A†	N/A* 000†	p. 24	M							
LAR	LUT Address Read	03h	0x03C7* 0x27CB†	N/A* 0x029B†	N/A* 000†	p. 25	RA[1]							
							P[2]	RA[2]						
Cursor Color Palette RAM Registers / Analog Setup Registers														
CAW	Cursor Address Write	04h	0x27CC	0x029C	001	p. 26	RSVD							WA
CCD	Cursor Color Data	05h	0x27CD	0x029D	001	p. 26	D							
ASC	Analog Setup Control	06h	0x27CA	0x029A	001	p. 27	RSVD	COFF	BPE	BS	GS	RS	D24	DOFF
CAR	Cursor Address Read	07h	0x27CB	0x029B	001	p. 28	RSVD							RA
Graphic and Cursor Setup Registers														
GFC	Graphics Format Control	08h	0x27CC	0x029C	010	p. 28	RSVD	GPF		TC	CF	MR	TE	PS
CSC	Cursor Setup Control	09h	0x27CD	0x029D	010	p. 30	SD	DPS		CS	DM	PM	CMS	
GSR	Graphics Status Register	0Ah	0x27CA	0x029A	010	p. 31	REV				S	IO	CP	
CPR	Cursor Address Read	0Bh	0x27CB	0x029B	010	p. 32	D							

NOTE: * = VGA Modes 0 and 1 only. † = VGA Mode 2 only. [1] = Function 1 — Palette Color Selection [2] = Function 2 — Cursor Color Selection

Table 4-1. MediaDAC Control Registers *(cont.)*

Register Definition		Local	ISA / MCA			Ref.	Bit Definitions							
		RS [4:0]	Pri. Adr. *BIR[5]=0*	Sec. Adr. *BIR[5]=1*	BIR [2:0]	Pg.	7	6	5	4	3	2	1	0
Cursor Positioning Registers														
CXb	*Cursor X Position Registers*													
CXL	Cursor X Position, LSB	0Ch	0x27CC	0x029C	011	p. 32	X							
CXH	Cursor X Position, MSB	0Dh	0x27CD	0x029D	011	p. 32	RSVD				X			
CYb	*Graphics Status Registers*													
CXL	Cursor Y Position, LSB	0Eh	0x27CA	0x029A	011	p. 33	Y							
CYH	Cursor Y Position, MSB	0Fh	0x27CB	0x029B	011	p. 33	RSVD				Y			
Video, Graphics, and Sync Control Registers														
VFC	Video Format Control	10h	0x27CC	0x029C	100	p. 34	EC	CS	CM	GBYP	CSF			
GOC	Graphics Overlay Opcode	11h	0x27CD	0x029D	100	p. 35	T7	T6	T5	T4	T3	T2	T1	T0
SAR	Sync Alignment Register	12h	0x27CA	0x029A	100	p. 36	RSVD			VL	DIR	DLY		
TEST	Test Register	13h	0x27CB	0x029B	100	p. 36	GT	CCT	RSVD	PO	SO*	WO	RSVD	BCE
Video Gamma Correction Palette RAM Registers														
VGW	Video Gamma Address Write	14h	0x27CC	0x029C	101	p. 37	WA							
VGD	Video Gamma Data	15h	0x27CD	0x029D	101	p. 38	D							
RSV2	Reserved 2	16h	0x27CA	0x029A	101	p. 38	RSVD							
VGR	Video Gamma Address Read	17h	0x27CB	0x029B	101	p. 39	RA							
Graphics Chroma Key Registers														
GCKc	*Graphics Chroma Key Registers*													
GCKR	GCK Red	18h	0x27CC	0x029C	110	p. 40	CKR							
GCKG	GCK Green	19h	0x27CD	0x029D	110	p. 40	CKG							
GCKB	GCK Blue	1Ah	0x27CA	0x029A	110	p. 40	CKB							
RSV3	Reserved 3	1Bh	0x27CB	0x029B	110	p. 40	RSVD							
GKMc	*Graphics Chroma Key Mask*													
GKMR	GCK Mask Red	1Ch	0x27CC	0x029C	111	p. 41	MR							
GKMG	GCK Mask Green	1Dh	0x27CD	0x029D	111	p. 41	MG							
GKMB	GCK Mask Blue	1Eh	0x27CA	0x029A	111	p. 41	MB							
RSV4	Reserved 4	1Fh	0x27CB	0x029B	111	p. 41	RSVD							

4.1 Memory Access Addressing and Indexing

4.1.1 BIR: Block Index Register

ISA/MCA	Primary I/O Address (ALT = 0)	0x27CE
	Secondary I/O Address (ALT = 1)	0x029E
	BIR[2:0]	N/A
Local Hardware Interface	Direct Address (RS[4:0])	N/A

BIR specifies the access modes for all MediaDAC control registers.

7	6	5	4	3	2	1	0
IE	RE	SE	RO	RSVD	BLK		

Bit #	Access	Reset	Description
7	R/W	0	IE Index Enable. Specifies direct (local hardware interface) or indexed addressing (ISA/MCA) for MediaDAC registers. 0 Direct addressing; RS[4:0] overrides BIR[2:0] 1 Indexed addressing; I/O address specified by bit SE
6	R/W	0	RE Read Access Enable. Enables read/write access of VGA-compatible registers, as shown below. 0 Write-only access 1 Read/write access
5	R/W	0	SE Secondary Enable. Specifies I/O address for MediaDAC registers. 0 Primary I/O address selected 1 Secondary I/O address selected
4	R/W	0	RO LUT Address Read (LAR) Override. Enables LAR at I/O address 0x03C7 (VGA modes 0 and 1 only). 0 LAR disabled 1 LAR enabled
3	R/W	0	RSVD Reserved (read as '0').
2:0	R/W	0	BLK Block Select. Specifies which block of registers is to be read and written at 16-bit I/O addresses 0x27CA, 0x27CB, 0x27CC, and 0x27CD.

VGA Mode	*IE*	*RE*	*RO*	*LPM*	*LAR*	*LAW*	*LCD*
0	0	0	x	Write only			
1a	0	1	0	R/W	W-only	R/W	R/W
1b	0	1	1	R/W			
2	1	x	x	R/W			

BLK	*Registers*	*27CA*	*27CB*	*27CC*	*27CD*
000	Graphics Color Palette RAM	LPM	LAR	LAW	LCD
001	Cursor Color Palette RAM / Analog Setup	ASC	CAR	CAW	CCD
010	Graphic and Cursor Setup	GSR	CPR	GFC	CSC
011	Cursor Positioning	CYL	CYH	CXL	CXH
100	Video, Graphics, and Sync Control	SAR	TEST	VFC	GOC
101	Video Gamma Correction Palette RAM	RSV2	VGR	VGW	VGD
110	Graphics Chroma Key	GCKB	RSV3	GCKR	GCKG
111	Graphics Chroma Key Mask	GKMB	RSV4	GKMR	GKMG

4.2 Graphics Color Palette RAM Registers

The Graphics Color Palette RAM is a 256 x 24-bit color LUT that can be modified using data register LCD and write and read registers LAW and LAR.

NOTE: Register BIR, bit BLK must be set to '000' to access the Graphics Color Palette RAM registers.

4.2.1 LAW: LUT Address Write

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x03C8	0x27CC
	Secondary I/O Address (BIR[5]=1)	N/A	0x029C
	BIR[2:0]	N/A	000
Local Hardware Interface	Direct Address (RS[4:0])	00h	

Write register LAW has two functions:

- it addresses the Graphics Color Palette RAM when the host system writes 24- or 18-bit color data through register LCD, and
- it addresses the Cursor Pattern RAM when the host system writes cursor pattern data through register CPR.

LAW addresses each of the 256 bytes of the Graphics Color Palette RAM three times (R, G, and B write cycles), then automatically increments by one to specify the next byte of RAM to be written. During/Cursor Pattern RAM access, LAW increments after each access.

7	6	5	4	3	2	1	0
WA							
P	WA						

Bit #	Access	Reset	Description	
Palette Color Selection				
7:0	R/W	0h	WA	Write Address for Graphics Color Palette RAM.
Cursor Pattern Selection				
7	R/W	0	P	Plane of Cursor Pattern RAM Data to be addressed. 0 Plane 0 1 Plane 1
6:0	R/W	0h	WA	Write Address for Cursor Pattern RAM Data. **NOTE:** Byte 0 is located in the upper left corner of plane 0.

4.2.2 LCD: LUT Color Data

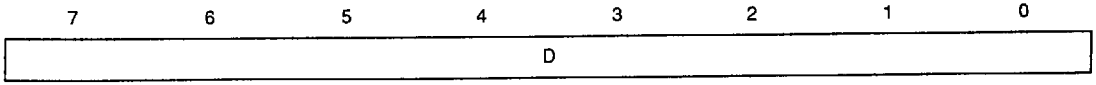
ISA/MCA	Primary I/O Address (BIR[5]=0)	0x03C9	0x27CD
	Secondary I/O Address (BIR[5]=1)	N/A	0x029D
	BIR[2:0]	N/A	000
Local Hardware Interface	Direct Address (RS[4:0])	01h	

Register LCD is an 8-bit-wide port from the host system to the Graphics Color Palette RAM. The host system writes data to the Graphics Color Palette RAM through LCD using address register LAW, and reads data from the Graphics Color Palette RAM through LCD using address register LAR.

LAW/LAR must address LCD three times (R, G, and B read/write cycles) for each of the 256 bytes of the Graphics Color Palette RAM:

- During the first I/O operation, LAW/LAR writes/reads the red component of the palette color;
- the second I/O operation writes/reads the green component; and
- the third I/O operation writes/reads the blue component.

After each RGB cycle, LAW/LAR automatically increments by one to specify the next byte of the Graphics Color Palette RAM to be written/read.



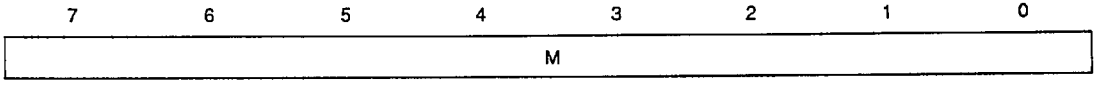
Bit #	Access	Reset	Description
7:0	R/W	0h	D — Data for Graphics Color Palette RAM. **NOTE:** For 18-bit color (specified by register ASC, bit D24),bits 5:0 are shifted to register bits 7:2, and bits 1:0 are padded with '0's.

4.2.3 LPM: LUT Pixel Mask

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x03C6	0x27CA
	Secondary I/O Address (BIR[5]=1)	N/A	0x029A
	BIR[2:0]	N/A	000
Local Hardware Interface	Direct Address (RS[4:0])	02h	

NOTE: *(*) = VGA Mode 0, 1; (†) = VGA Mode 2*

The graphics pixel data used to look up color information in the Graphics Color Palette can be masked before the lookup occurs. LPM masks the address. The graphics pixel is logically ANDed with the LPM data, and the result is used to address the Graphics Color Palette.



Bit #	Access	Reset	Description	
7:0	R/W	FFh	M	Data for Graphics Color Palette RAM Pixel Mask.

4.2.4 LAR: LUT Address Read

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x03C7	0x27CB
	Secondary I/O Address (BIR[5]=1)	N/A	0x029B
	BIR[2:0]	N/A	000
Local Hardware Interface	Direct Address (RS[4:0])	03h	

Read register LAR has two functions:

- it addresses the Graphics Color Palette RAM when the host system reads 24- or 18-bit color data through register LCD, and
- it addresses the Cursor Pattern RAM when the host system reads cursor pattern data through register CPR.

LAR addresses each of the 256 bytes of the Graphics Color Palette RAM three times (R, G, and B read cycles), then automatically increments by one to specify the next byte of RAM to be read. During/Cursor Pattern RAM access, LAR increments after each access.

7	6	5	4	3	2	1	0
RA							
P	RA						

Bit #	Access	Reset	Description	
Palette Color Selection				
7:0	R/W	0h	RA	Read Address for Graphics Color Palette RAM.
Cursor Pattern Selection				
7	R/W	0	P	Plane of Cursor Pattern RAM Data to be addressed. 0 Plane 0 1 Plane 1
6:0	R/W	0h	RA	Read Address for Cursor Pattern RAM Data. **NOTE:** Byte 0 is located in the upper left corner of plane 0.

4.3 Cursor Color Pallette RAM Registers / Analog Setup Registers

The Cursor Color Palette RAM is a 4 x 24-bit color LUT. It comprises four internal registers — Border (BDR), Cursor Color 1 (CC1), Cursor Color 2 (CC2), and Cursor Color 3 (CC3) — that are addressed using data register CCD and write and read registers CAW and CAR. Refer to the *System Reference Manual* for more detailed information.

NOTE: Register BIR, bit BLK must be set to '001' to access the Cursor Color Palette RAM / Analog Setup registers.

4.3.1 CAW: Cursor Address Write

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CC
	Secondary I/O Address (BIR[5]=1)	0x029C
	BIR[2:0]	001
Local Hardware Interface	Direct Address (RS[4:0])	04h

Write register CAW addresses the Cursor Color Palette RAM when the host system writes 24-bit cursor or border color data through register CCD.

NOTE: The Cursor Color Palette RAM is a 4 x 24-bit color LUT. Its four internal registers include: Border (BDR), Cursor Color 1 (CC1), Cursor Color 2 (CC2), and Cursor Color 3 (CC3).

CAW addresses each of the four registers of the Cursor Color Palette RAM three times (R, G, and B write cycles), then automatically increments by one to specify the next register to be written.

7	6	5	4	3	2	1	0
RSVD						WA	

Bit #	Access	Reset	Description	
7:2	R/W	0h	RSVD	Reserved (write as '0').
1:0	R/W	00	WA	Write Address for Cursor Color Palette RAM.

4.3.2 CCD: Cursor Color Data

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CD
	Secondary I/O Address (BIR[5]=1)	0x029D
	BIR[2:0]	001
Local Hardware Interface	Direct Address (RS[4:0])	05h

Register CCD is an 8-bit-wide port from the host system to the Cursor Color Palette RAM. The host system writes data to the Cursor Color Palette RAM through CCD using address register CAW, and reads data from the Cursor Color Palette RAM through CCD using address register CAR.

CAW/CAR must address LCD three times (R, G, and B read/write cycles) for each of the four bytes of the Cursor Color Palette RAM (internal registers BDR, CC1, CC2, and CC3). During the first I/O operation, CAW/CAR writes/reads the red component of the palette color; the second I/O operation writes/reads the green component; and the third I/O operation writes/reads the blue. After each RGB cycle, CAW/CAR automatically increments by one to specify the next byte of the Cursor Color Palette RAM to be written/read.

7	6	5	4	3	2	1	0
D							

Bit #	Access	Reset	Description	
7	R/W	0	D	Data for Cursor Color Palette RAM. **NOTE:** For 18-bit color (specified by register ASC, bit D24), bits 5:0 are shifted to 7:2, and bits 1:0 are padded with '0's.

4.3.3 ASC: Analog Setup Control

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CA
	Secondary I/O Address (BIR[5]=1)	0x029A
	BIR[2:0]	001
Local Hardware Interface	Direct Address (RS[4:0])	06h

Register ASC sets up the DAC and analog output for the MediaDAC.

NOTE: All I/O registers and the Cursor Color Data can be R/W accessed when the internal clock is off. The Cursor Pattern RAM and Palette maintain their integrity. Reads from register CSC or any I/O register do not affect the state of the internal clock.

7	6	5	4	3	2	1	0
RSVD	COFF	BPE	BS	GS	RS	D24	DOFF

Bit #	Access	Reset	Description	
7	R/W	0	RSVD	Reserved (write as '0').
6	R/W	0	COFF	Clock Off. 0 Normal clocking 1 Powers down the MediaDAC; forces all clocks high when DOFF also = 1, internal clock forced high.
5	R/W	0	BPE	Blank Pedestal Enable.
4	R/W	0	BS	Blue Sync.
3	R/W	0	GS	Green Sync.
2	R/W	0	RS	Red Sync.
1	R/W	0	D24	Specifies DAC data as 18- or 24-bit. 0 18-bit DAC 1 24-bit DAC
0	R/W	0	DOFF	DAC Off. 0 Normal operation 1 Disables DAC output when COFF also = 1, internal clock forced high.

4.3.4 CAR: Cursor Address Read

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CB
	Secondary I/O Address (BIR[5]=1)	0x029B
	BIR[2:0]	001
Local Hardware Interface	Direct Address (RS[4:0])	07h

Read register CAR addresses the Cursor Color Palette RAM when the host system reads 24-bit cursor or border color data through register CCD.

NOTE: The Cursor Color Palette RAM is a 4 x 24-bit color LUT. Its four internal registers include: Border (BDR), Cursor Color 1 (CC1), Cursor Color 2 (CC2), and Cursor Color 3 (CC3).

CAR addresses each of the four registers of the Cursor Color Palette RAM three times (R, G, and B read cycles), then automatically increments by one to specify the next register to be read.

7	6	5	4	3	2	1	0
RSVD						RA	

Bit #	Access	Reset	Description	
7:2	R/W	0h	RSVD	Reserved (write as '0').
1:0	R/W	00	RA	Read Address for Cursor Color Palette RAM.

4.4 Graphic and Cursor Setup Registers

NOTE: Register BIR, bit BLK must be set to '010' to access the Graphic and Cursor Setup registers.

4.4.1 GFC: Graphics Format Control

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CC
	Secondary I/O Address (BIR[5]=1)	0x029C
	BIR[2:0]	010
Local Hardware Interface	Direct Address (RS[4:0])	08h

Register GFC sets up the graphics interface timing and color format controls.

7	6	5	4	3	2	1	0
RSVD	GPF		TC	CF	MR	TE	PS

Bit #	Access	Reset	Description
7	R/W	0	RSVD — Reserved (write as '0').
6:5	R/W	00	GPF — Graphics Port Format. Specifies data type for GSD[31:0]/VGA[7:0], and works with PORTSEL and bit MR to specify SCLK. 00 24-bit pixel 8:8:8 RGB data (PCLKn:LCLK = 1:1) When PORTSEL = 1, SCLK = PCLKn 01 16-bit pixel data (mux ratios set by bit TE) When PORTSEL = 1 and MR = 0, SCLK = PCLKn/2 When PORTSEL = 1 and MR = 1, SCLK = PCLKn 10 Four 8-bit pixels (PCLKn:LCLK = 4:1) When PORTSEL = 1, SCLK = PCLKn/4 11 Eight 4-bit pixels (PCLKn:LCLK = 8:1) When PORTSEL = 1, SCLK = PCLKn/8 XX When PORTSEL = 0, SCLK = PCLKn
4	R/W	0	TC — True Color Graphics Color Palette RAM bypass. 0 Pixel data is pseudocolor When PORTSEL = 1, GSD[31:0] data addresses palette 1 Pixel data is true color When PORTSEL = 1, GSD[31:0] data bypasses palette X When PORTSEL = 0, VGA[7:0] data addresses palette
3	R/W	0	CF — Color Format. Selects GSD[31:0] RGB color format. 0 5:5:5 1 5:6:5
2	R/W	0	MR — Multiplexing Rate. Controls 16-bit graphics port data multiplexing rate 0 PCLKn:LCLK ratio = 2:1 (two-pixel bus) 1 PCLKn:LCLK ratio = 1:1 (one-pixel bus)
1	R/W	0	TE — Tag Enable. Specifies pixel selector for 5:5:5 RGB graphics data. 0 Bit PS is pixel selector 1 5:5:5 RGB graphics data; GSD31 is video pixel selector
0	R/W	0	PS — Pixel Selector. Selects graphics pixel for 5:6:5 and 5:5:5 RGB 1:1 mux data. 0 Graphics pixel 0 (graphics data on port GSD[15:0]) 1 Graphics pixel 1 (graphics data on port GSD[31:16])

GPS	CSC[6:5]	Port Selected		PORTSEL
0	00	VGA[7:0]	(ignore GPS)	0
0	01	VGA[7:0]	(based on GPS)	0
0	10	GSD[31:0]	(ignore GPS)	1
0	11	VGA[7:0]	(ignore GPS)	0
1	00	VGA[7:0]	(ignore GPS)	0
1	01	GSD[31:0]	(based on GPS)	1
1	10	GSD[31:0]	(ignore GPS)	1
1	11	VGA[7:0]	(ignore GPS)	0

4.4.2 CSC: Cursor Setup Control

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CD
	Secondary I/O Address (BIR[5]=1)	0x029D
	BIR[2:0]	010
Local Hardware Interface	Direct Address (RS[4:0])	09h

Register CSC sets cursor modes and controls Graphics Color Palette RAM indexing for 16-bit graphics data modes and clock selections.

7	6	5	4	3	2	1	0
SD	DPS		CS	DM	PM	CMS	

Bit #	Access	Reset	Description	
7	R/W	0	SD	SCLK Disable. Enables or disables signal SCLK. 0 SCLK enabled 1 SCLK disabled
6:5	R/W	00	DPS	Data Port Select. 00 GSD[31:0] disabled (VGA[7:0] always selected) 01 GSD[31:0] enabled (VGA[7:0] or Serial Graphics port) 10 GSD[31:0] disabled (Serial Graphics port always selected) 11 GSD[31:0] disabled (Serial Graphics port is output, VGA input)
4	R/W	0	CS	Clock Select. Selects pixel clock PCLK0 or PCLK1. 0 PCLK0 1 PCLK1
3	R/W	0	DM	Display Mode. Specifies progressive-scan or interlaced display. 0 Progressive-scan 1 Interlaced scan
2	R/W	0	PM	Palette Mapping for 16-bit graphics data to 18-bit DAC. 0 Color components mapped to MSb's of Graphics Color Palette 1 Color components mapped to LSb's of Graphics Color Palette **NOTE:** All unused bits are padded with '0's.
1:0	R/W	00	CMS	Cursor Mode Select. Specifies cursor format. 00 Cursor disabled 01 Three-color cursor 10 Two-color cursor with highlighting 11 Two-color cursor

4.4.3 GSR: Graphics Status Register

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CA
	Secondary I/O Address (BIR[5]=1)	0x029A
	BIR[2:0]	010
Local Hardware Interface	Direct Address (RS[4:0])	0Ah

Register GSR is a read-only, modulo-3 counter that sets up and monitors the MediaDAC revisions and I/O cycles.

7	6	5	4	3	2	1	0
REV				S	IO	CP	

Bit #	Access	Reset	Description	
7:4	R	0h	REV	MediaDAC revision level.
3	R	0	S	Sense bit status. 0 All analog outputs are below the 335-mV level 1 One or more analog outputs have exceeded the 335-mV level
2	R	0	IO	I/O read/write access status. 0 LAW, CAW, or VGW has been specified (I/O write) 1 LAR, CAR, or VGR has been specified (I/O read)
1:0	R	00	CP	Color Pointer. Specifies color component for host to access on next I/O cycle to a palette. 00 Red 01 Green 10 Blue

4.4.4 CPR: Cursor Pattern RAM Data

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CB
	Secondary I/O Address (BIR[5]=1)	0x029B
	BIR[2:0]	010
Local Hardware Interface	Direct Address (RS[4:0])	0Bh

Register CPR is an 8-bit-wide port from the host system to the Cursor Pattern RAM.

NOTE: The Cursor Pattern RAM is a 256-byte memory array comprising two 32 x 32-bit (128-byte) planes. It can be modified using data register CPR, and write and read registers LAW and LAR. Refer to the *System Reference Manual* for more detailed information.

The host system writes data to the Cursor Pattern RAM through CPR using address register LAW, and reads data from the Cursor Pattern RAM through CPR using address register LAR.

After each RGB cycle, LAW/LAR automatically increments by one to specify the next byte of the Cursor Pattern RAM to be written/read.

7	6	5	4	3	2	1	0
D							

Bit #	Access	Reset	Description	
7:0	R/W	0h	D	Data for Cursor Color Palette RAM.

4.5 Cursor Positioning Registers

NOTE: Register BIR, bit BLK must be set to '011' to access the Cursor Positioning registers.

4.5.1 CXb: Cursor X Position

		CXL	*CXH*
ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CC	0x27CD
	Secondary I/O Address (BIR[5]=1)	0x029C	0x029D
	BIR[2:0]	011	011
Local Hardware Interface	Direct Address (RS[4:0])	0Ch	0Dh

Registers CXb specify the X position of the bottom right corner of the cursor.

NOTE: During reset, when CXL and CXH are set to 0h, the cursor is positioned in the upper-left corner, off-screen. When CXL = 20h and CXH = 0h, the left column of cursor pixels are positioned at the left column of display-screen pixels.

7	6	5	4	3	2	1	0
X							
RSVD				X			

Bit #	Access	Reset	Description	
CXL: Cursor X Position, LSB				
7:0	R/W	0	X	Cursor X position, Low Byte.
CXH: Cursor X Position, MSB				
7:4	R/W	0	RSVD	Reserved (read as '0').
3:0	R/W	0	X	Cursor X position, High Byte.

4.5.2 CYb: Cursor Y Position

		CYL	*CYH*
ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CA	0x27CB
	Secondary I/O Address (BIR[5]=1)	0x029A	0x029B
	BIR[2:0]	011	011
Local Hardware Interface	Direct Address (RS[4:0])	0Eh	0Fh

Registers CYb specify the Y position of the bottom-right corner of the cursor relative to the top of the display screen.

NOTE: During reset, when CYL and CYH are set to 0h, the cursor is positioned in the upper-left corner, off-screen. When CYL = 20h and CYH = 0h, the top row of cursor pixels is positioned at the top row of display screen pixels.

7	6	5	4	3	2	1	0
Y							
RSVD				Y			

Bit #	Access	Reset	Description	
CYL: Cursor Y Position, LSB				
7:0	R/W	0	Y	Cursor Y position, Low Byte.
CYH: Cursor Y Position, MSB				
7:4	R/W	0	RSVD	Reserved (read as '0').
3:0	R/W	0	Y	Cursor Y position, High Byte.

4.6 Video, Graphics, and Sync Control Registers

NOTE: Register BIR, bit BLK must be set to '100' to access the Video, Graphics, and Sync Control registers.

4.6.1 VFC: Video Format Control

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CC
	Secondary I/O Address (BIR[5]=1)	0x029C
	BIR[2:0]	100
Local Hardware Interface	Direct Address (RS[4:0])	10h

Register VFC sets up the video port interface timing and color format controls.

7	6	5	4	3	2	1	0
EC	CS	CM	GBYP	CSF			

Bit #	Access	Reset	Description	
7	R/W	0	EC	Extended Color mode for VGA data. 0 Normal mode 1 Extended color mode
6	R/W	0	CS	Clock Select for graphics data. 0 LCLK 1 PCLKn (specified by register CSC, bit CS)
5	R/W	0	CM	Clock Mode. 0 Clock Mode 1 1 Clock Mode 2 (2x PCLKn)
4	R/W	0	GBYP	Gamma Correction Bypass. 0 Gamma enabled 1 Gamma disabled
3:0	R/W	0h	CSF	Color Space Format. Specifies color space format of VSD[31:0]. 0000 YUV 4:2:2, non-tagged 0001 Y(U:T)(V:T) 4:(2):(2); LSb of U and V are tag data 1000 RGB 5:6:5 1010 RGB 5:5:5 1011 TRGB 1:5:5:5 (MSb = tag data) 1110 RGB 8:8:8, non-tagged 1111 TRGB 1:8:8:8 (bit 31= tag bit) XXXX All other bit configurations are reserved

Bits 7:5 define EC modes as follows:

	EC	CS	CM
ECMODE1	1	0	0
ECMODE2	1	1	1

4.6.2 GOC: Graphics Overlay Opcode

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CD
	Secondary I/O Address (BIR[5]=1)	0x029D
	BIR[2:0]	100
Local Hardware Interface	Direct Address (RS[4:0])	11h

GOC is an 8-bit value that inputs to an 8:1 multiplexer. Three select signals determine which of the eight bits become the transparency control for each pixel time:

- SWKEY = 1 when MediaDAC signals ZC[3:0] = 1100b;
- TAG = 1 when input data is tagged (tagged formats only);
- COLOR = 1 when data color matches contents of GCKc.

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0

Bit #	Access	Reset	Description	
7	R/W	0h	T7	111*
6	R/W	0h	T6	110*
5	R/W	0h	T5	101*
4	R/W	0h	T4	100*
3	R/W	0h	T3	011*
2	R/W	0h	T2	010*
1	R/W	0h	T1	001*
0	R/W	0h	T0	000*

(For all bits 7:0) Transparency controls.
1 video pixel enabled; graphics transparent
0 graphics pixel opaque; video pixel not visible

*Bit outputs from the multiplexer and becomes the transparency control for the current pixel time when SWKEY:TAG:COLOR = this value.

4.6.3 SAR: Sync Alignment Register

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CA
	Secondary I/O Address (BIR[5]=1)	0x029A
	BIR[2:0]	100
Local Hardware Interface	Direct Address (RS[4:0])	12h

Register SAR programs outgoing sync signals to match the monitor, both in polarity and PCLKn delay, relative to the DAC outputs and internal pixel pipeline. SAR also sets the output sync signals VSOUT and HSOUT to align with the DAC RGB outputs in PCLKn time units.

7	6	5	4	3	2	1	0
RSVD			VL	DIR	DLY		

Bit #	Access	Reset	Description	
7:5	R/W	0h	RSVD	Reserved (read as '0').
4	R/W	0	VL	Horizontal and vertical sync output polarity in LCD mode. 0 HSOUT (GSD24), VSOUT (GSD25) = active low () 1 HSOUT, VSOUT = active high
3	R/W	0	DIR	Delay direction of HSOUT, VSOUT relative to R, G, B. 0 Sync signals behind DAC outputs 1 Sync signals ahead of DAC outputs
2:0	R/W	000	DLY	PCLKn delay. 000 No delay 111 7 PCLKn difference

4.6.4 TEST: Test Register

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CB
	Secondary I/O Address (BIR[5]=1)	0x029B
	BIR[2:0]	100
Local Hardware Interface	Direct Address (RS[4:0])	13h

7	6	5	4	3	2	1	0
GT	CCT	RSVD	PO	SO*	WO	RSVD	BCE

Bit #	Access	Reset	Description	
7	R/W	0	GT	Graphics Test. Graphics data (GSD[31:0] or VGA[7:0]) is output to VSD[31:0].
6	R/W	0	CCT	Cursor Counter Test. Also bypasses cursor memory.
5	R/W	0	RSVD	Reserved (write as '0').
4	R/W	0	PO	PCLKn off.
3	R/W	0	SO*	Sense off.
2	R/W	0	WO	COMP off.
1	R/W	0	RSVD	Reserved (write as '0').
0	R/W	0	BCE	Border Counter Enable. Generates border internally to MediaDAC.

4.7 Video Gamma Correction Palette RAM Registers

The Video Gamma Correction Palette RAM is a 256 x 24-bit color LUT that maps non-linear video pixel data to linear color data. It can be modified using data register VGD and write and read registers VGW and VGR, as explained in the following sections. (See the *System Reference Manual* for a more detailed explanation.)

NOTE: Register BIR, bit BLK must be set to '101' to access the Video Gamma Correction Palette registers.

4.7.1 VGW: Video Gamma Address Write

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CC
	Secondary I/O Address (BIR[5]=1)	0x029C
	BIR[2:0]	101
Local Hardware Interface	Direct Address (RS[4:0])	14h

Write register VGW addresses the Video Gamma Correction Palette RAM when the host system writes 24-bit color data through register VGD.

VGW addresses each of the 256 bytes of the Video Gamma Correction Palette RAM three times (R, G, and B write cycles), then automatically increments by one to specify the next byte of RAM to be written.

7	6	5	4	3	2	1	0
WA							

Bit #	Access	Reset	Description	
7:0	R/W	0h	WA	Write Address for Video Gamma Correction Palette RAM.

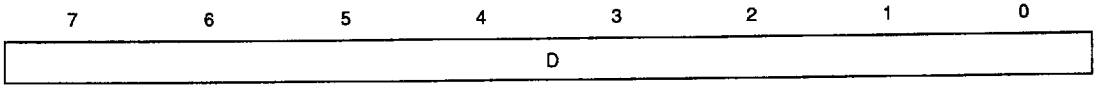
4.7.2 VGD: Video Gamma Data

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CD
	Secondary I/O Address (BIR[5]=1)	0x029D
	BIR[2:0]	101
Local Hardware Interface	Direct Address (RS[4:0])	15h

Register VGD is an 8-bit-wide port from the host system to the Video Gamma Correction Palette RAM. The host system writes data to the Video Gamma Correction Palette RAM through VGD using address register VGW, and reads data from the Video Gamma Correction Palette RAM through VGD using address register VGR.

VGW/VGR must address VGD three times (R, G, and B read/write cycles) for each of the 256 bytes of the Video Gamma Correction Palette RAM. During the first I/O operation, VGW/VGR writes/reads the red component of the palette color; the second I/O operation writes/reads the green component; and the third I/O operation writes/reads the blue.

After each RGB cycle, VGW/VGR automatically increments by one to specify the next byte of the Video Gamma Correction Palette RAM to be written/read.



Bit #	Access	Reset	Description	
7:0	R/W	0	D	Video Gamma Correction Palette RAM Data. **NOTE:** For 18-bit color (specified by register ASC, bit D24), bits 1:0 are padded with '0's before loading into the Video Gamma Correction Palette RAM.

4.7.3 RSV2: Reserved 2

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CA
	Secondary I/O Address (BIR[5]=1)	0x029A
	BIR[2:0]	101
Local Hardware Interface	Direct Address (RS[4:0])	16h

Register RSV2 is reserved.

4.7.4 VGR: Video Gamma Address Read

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CB
	Secondary I/O Address (BIR[5]=1)	0x029B
	BIR[2:0]	101
Local Hardware Interface	Direct Address (RS[4:0])	17h

Read register VGR addresses the Video Gamma Correction Palette RAM when the host system reads 24-bit color data through register VGD.

VGR addresses each of the 256 bytes of the Video Gamma Correction Palette RAM three times (R, G, and B write cycles), then automatically increments by one to specify the next byte of RAM to be read.

7	6	5	4	3	2	1	0
RA							

Bit #	Access	Reset	Description	
7:0	R/W	0h	RA	Read Address for Video Gamma Correction Palette RAM.

4.8 Graphics Chroma Key Registers

NOTE: Register BIR, bit BLK must be set to '110' to access the Graphics Chroma Key registers, and must be set to '111' to access the Graphics Chroma Key Mask registers.

4.8.1 GCKc: Graphics Chroma Key

		GCKR	*GCKG*	*GCKB*
ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CC	0x27CD	0x27CA
	Secondary I/O Address (BIR[5]=1)	0x029C	0x029D	0x029A
	BIR[2:0]	110	110	110
Local Hardware Interface	Direct Address (RS[4:0])	18h	19h	1Ah

Registers GCKR, GCKG, and GCKB control the Graphics Chroma Key function.

- When graphics data inputs on VGA[7:0], the data in registers GCKc is compared against four adjacent graphics pixels. GCKR is compared to the least-significant pixel.
- When graphics data inputs on GSD[31:0], the data in registers GCKc is used as specified by the PCLKn:SCLK ratio.

7	6	5	4	3	2	1	0
CKR							
CKG							
CKB							

Bit #	Access	Reset	Description	
GCKR: GCK Red				
7:0	R/W	0	CKR	Chroma Key Red Data.
GCKG: GCK Green				
7:0	R/W	0	CKG	Chroma Key Green Data.
GCKB: GCK Blue				
7:0	R/W	0	CKB	Chroma Key Blue Data.

4.8.2 RSV3: Reserved 3

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CB
	Secondary I/O Address (BIR[5]=1)	0x029B
	BIR[2:0]	110
Local Hardware Interface	Direct Address (RS[4:0])	1Bh

Register RSV3 is reserved.

4.8.3 GKMc: Graphics Chroma Key Mask

		GKMR	*GKMG*	*GKMB*
ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CC	0x27CD	0x27CA
	Secondary I/O Address (BIR[5]=1)	0x029C	0x029D	0x029A
	BIR[2:0]	111	111	111
Local Hardware Interface	Direct Address (RS[4:0])	1Ch	1Dh	1Eh

Registers GKMR, GKMG, and GKMB control the Graphics Chroma Key Mask function.

- When graphics data inputs on VGA[7:0], the data in registers GKMc is ANDed with four adjacent graphics pixels. GKMR is compared to the least-significant pixel.
- When graphics data inputs on GSD[31:0], the data in registers GKMc is used as specified by the PCLKn:SCLK ratio.

7	6	5	4	3	2	1	0
MR							
MG							
MB							

Bit #	Access	Reset		Description
GKMR: GCK Mask Red				
7:0	R/W	1	MR	Graphics Key Mask Red Data.
GKMG: GCK Mask Green				
7:0	R/W	1	MG	Graphics Key Mask Green Data.
GKMB: GCK Mask Blue				
7:0	R/W	1	MB	Graphics Key Mask Blue Data.

4.8.4 RSV4: Reserved 4

ISA/MCA	Primary I/O Address (BIR[5]=0)	0x27CB
	Secondary I/O Address (BIR[5]=1)	0x029B
	BIR[2:0]	111
Local Hardware Interface	Direct Address (RS[4:0])	1Fh

Register RSV4 is reserved.

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the MediaDAC. Stresses above those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Ambient temperature under bias ..... 0° to + 70° C

Storage temperature ..... -65° to +150° C

Voltage on any pin with respect to ground ..... GND -0.5 to V_{CC} + 0.5V

Power supply voltage 7V

Lead temperature (10 seconds) ..... 300° C

5.2 DC Specifications (Digital)

Symbol	Parameter	MIN	MAX	Conditions
V_{DD}	Power Supply Voltage	4.75 V	5.25 V	Normal Operation
V_{IL}	Input Low Voltage	0 V	0.8 V	
V_{IH}	Input High Voltage	2.0 V	V_{DD} + 0.8 V	
V_{OL}	Output Low Voltage		0.4 V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4 V		I_{OH} = 400 µA
V_{ILC}	Input Low Voltage CMOS		0.8 V	
V_{IHC}	Input High Voltage CMOS	3.0 V		
V_{OLC}	Output Low Voltage CMOS		0.4 V	I_{OLC} = 3.2 mA
V_{OHC}	Output High Voltage CMOS	3.5 V		I_{OHC} = -200 µA
I_{DD}	Digital Supply Current		N/A (mA)	V_{DD} Nominal
I_{DDT}	Total Supply Current		N/A (mA)	Note 1
I_L	Input Leakage	-10 µA	10 µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Input Capacitance		10 pF	
C_{OUT}	Output Capacitance		10 pF	

NOTE: 1) I_{DDT} is the sum of I_{DD} + $DACI_{DD}$ + $CLKI_{DD}$; it must be < 200 mA (package constraint).
2) DACVSS must not exceed V_{DD}.

5.3 DC Specifications (RAMDAC)

(V_{DD} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Conditions
DACVDD	Power Supply Voltage	4.75 V	5.25 V	Normal Operation
$DACI_{DD}$	DAC Supply Current		85 mA	Note 4

NOTE: 1) I_{REF} outside the specified limits may cause the analog outputs to become invalid.
2) The dotclock must be stable for a period of 100 µs after power-up before proper DAC operation is guaranteed.
3) See the IREF description in the *System Reference Manual*.
4) $DACI_{DD}$ is specified with the three analog outputs (R,G,B) each loaded with 37.5 ohms.

5.4 DAC Characteristics

(V_{DD} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Conditions
R	Resolution	8 bits		
I_{Omax}	Output Current		-27 mA	V_O < 1 V
Co	Output Capacitance		12 pF	
t_D	Analog Output Delay		TBD	Notes 1, 2, 3
t_R	Analog Output Rise/Fall time		TBD	Notes 2, 3, 4
t_S	Analog Output Settling time		TBD	Notes 2, 3, 5
t_{SK}	Analog Output Skew		TBD	Notes 2, 3, 6
FT	Clock and Data Feedthrough		TBD	Notes 2, 3, 6
DT	DAC-to-DAC Variability		± 3%	Notes 6, 7
GI	Glitch Impulse		TBD	Notes 2, 3, 6
DNL	Differential Nonlinearity		± ½ lsb	

NOTE: 1) t_D is measured from the 50% point of VDCLK to 50% point of full-scale transition.
2) Load is 37.5 ohms and 30 pF per analog output.
3) I_{REF} = -8.8 mA.
4) t_R is measured from 10% to 90% full scale.
5) t_S is measured from 50% point of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the midpoint of the distribution of the three DACs measured at full-scale deflection.

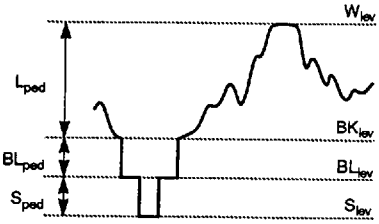
5.5 Analog Video Output Signals

Table 5-1. Analog Output Operating Conditions

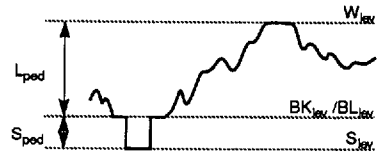
Symbol	Parameter	A	B	C	D	E
		Load Conditions				
		RS343			IBM PS/2™ 6-bit/DAC mode	
W_{lev}	White Level	26.7 mA* 1.0 V	25.3 mA* 0.95 V	17.6 mA* 0.66 V	14.0 mA* 0.70 V	14.0 mA* 0.70 V
BK_{lev}	Black Level	9.04 mA* 0.95 V	7.59 mA* 0.28 V	0 mA* 0 V	0 mA* 0 V	0 mA* 0 V
BL_{lev}	Blank Level	7.59 mA* 0.28 V	7.59 mA* 0.28 V	—	—	—
S_{lev}	Sync Level	0 mA* 0 V	0 mA* 0 V	—	—	—
I_{ref}	Reference Current	TBD	TBD	TBD	TBD	TBD
R_{set}†	Reference Current Resistor Value	720 Ω	720 Ω	1.5 kΩ	1.87 kΩ	1.82 kΩ
L_{ped}	Luminance Pedestal	92.5 IRE	100 IRE	100 IRE	100 IRE	100 IRE
BL_{ped}	Blank Pedestal	7.5 IRE	—	—	—	—
S_{ped}	Sync Pedestal	40 IRE	40 IRE	—	—	—
	LSB Size	69 µA*	69 µA*	69 µA*	55 µA*	222 µA*

† Recommended values.

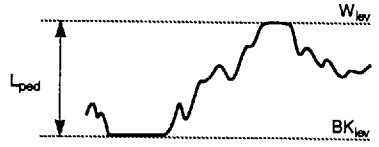
* Per test conditions as defined in Figure TBD with respect to reference current.



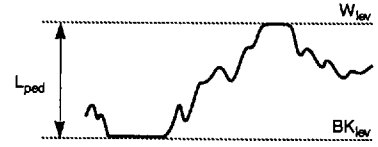
A) Composite Video Signal



B) Composite Video Signal with 0 IRE Setup

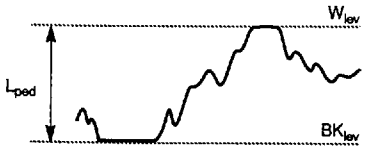


C) Blanked Video Signal with 0 IRE Setup



D) Blanked Video Signal with 0 IRE Setup and IBM PS/2 Levels

(V_{DD} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)



E) Blanked Video Signal with 0 IRE Setup and IBM PS/2 Levels (6-bit-DAC mode)

Figure 5-1. MediaDAC Analog Video Output Signals

5.6 AC Characteristics/Timing Information

This section includes system timing requirements for the MediaDAC. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0° to 70° C, and V_{DD} varying from 4.75 to 5.25 VDC.

NOTE: 1) All timings assume a load of 50 pF.
2) TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.

5.6.1 Index of Timing Information

5.6.2 ISA Bus Timing

Table 5-2. ISA Bus Timing

Ref.	Parameter		MIN	MAX
t_1	Setup	Valid address to IOR*/IOW* active	25 ns	
t_2	Delay	IOR*/IOW* active to DEN* active, DDIR change		20 ns
t_3	Delay	IOR* active to data output low Z	5 ns	25 ns
t_4	Delay	IOR* active to data out valid		40 ns
t_5	Pulse width	IOR*/IOW*	50 ns	
t_6	Delay	IOR*/IOW* inactive to DEN* inactive, DDIR changing		20 ns
t_7		IOR* inactive to Three-State delay		15 ns
t_8	Hold	Address from IOR*/IOW* active	0 ns	
t_9	Setup	Data valid to IOW* inactive	20 ns	
t_{10}	Hold	IOW* inactive to data invalid	0 ns	
t_{11}	Delay	IOW* inactive to next IOW* or IOR* active	50 ns	
t_{12}	Setup	AEN rising edge to IOW* or IOR* active	10 ns	
t_{13}	Delay	IOW* or IOR* inactive to AEN falling edge	10 ns	

NOTE: The low-byte address-buffer enable must be qualified by IOR* to avoid data contention. Also, AEN must be low during cycle.

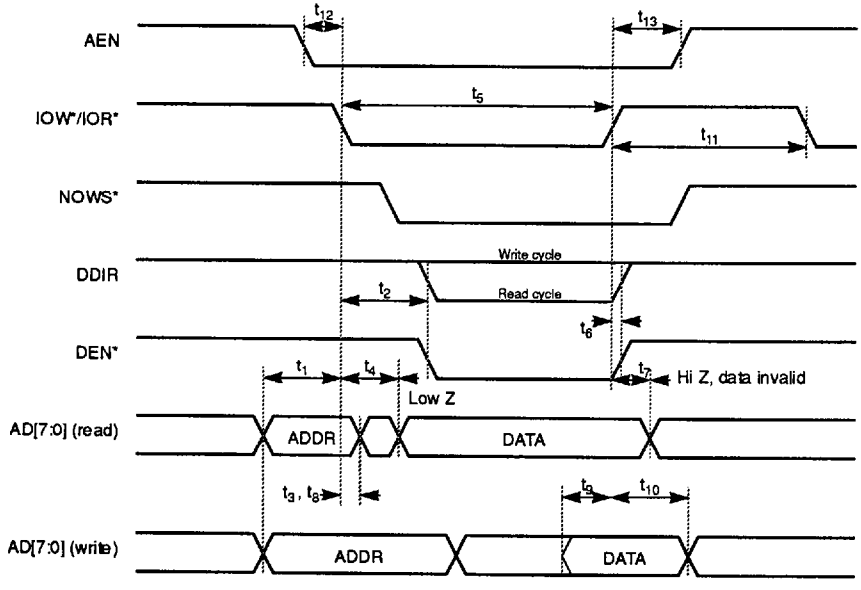


Figure 5-2. ISA Bus Timing

5.6.3 MCA Bus Timing

Table 5-3. CMD* Timing

Ref.	Parameter		MIN	MAX
t_1	Setup	address valid to CMD* active	25 ns	
t_2	Delay	CMD* active to DEN* active		20 ns
t_{3a}	Hold	address valid from CMD* active	0 ns	
t_{3b}	Delay	CMD* active to data output low Z	5 ns	25 ns
t_4	Delay	CMD* active to read data valid		40 ns
t_5	Pulse width	CMD*	50 ns	
t_6	Delay	CMD* inactive to data invalid, high Z		15 ns
t_7	Setup	write data valid to CMD* inactive	20 ns	
t_8	Hold	write data valid to CMD* inactive	0 ns	
t_9	Delay	CMD* inactive to next CMD* active	50 ns	
t_{10}	Setup	status valid to CMD* active	25 ns	
t_{11}	Hold	CMD* active to status invalid	5 ns	
t_{12}	Delay	CMD* inactive to DEN* inactive, DDIR change		20 ns

NOTE: See Write Cycle and Read Cycle diagrams for data timing with respect to CMD*.

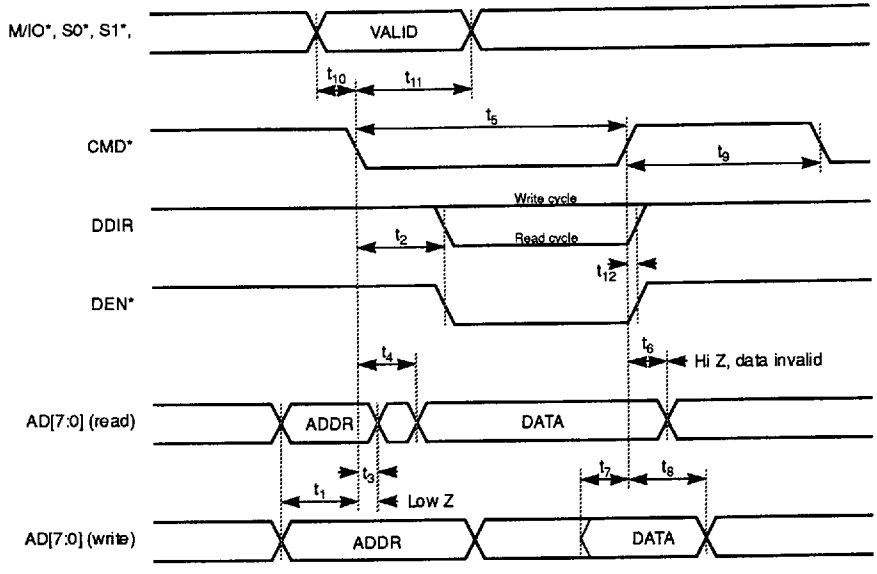


Figure 5-3. CMD* Timing (MCA Bus)

5.6.4 Local Hardware Interface Timing

Table 5-4. Local Hardware Interface — I/O Timing

Ref.	Parameter		MIN	MAX
t_1	Setup	Valid address to IOR*/IOW* active	25 ns	
t_2	Delay	IOR*/IOW* active to DEN* active, DDIR change		20 ns
t_3	Delay	IOR* active to data out low Z	5 ns	25 ns
t_4	Delay	IOR* active to data out valid		40 ns
t_5	Pulse width	IOR*/IOW*	50 ns	
t_6	Delay	IOR*/IOW* inactive to DEN* inactive, DDIR changing		20 ns
t_7	Delay	IOR* inactive to data Hi Z		15 ns
t_8	Hold	from IOR*/IOW* active to Address invalid	0 ns	
t_9	Setup	data valid to IOW* inactive	20 ns	
t_{10}	Hold	IOW* inactive to data invalid	0 ns	
t_{11}	Delay	IOW* inactive to next IOW* or IOR* active	50 ns	
t_{12}	Setup	CS* falling edge to IOW* or IOR* active	10 ns	
t_{13}	Delay	IOW* or IOR* inactive to CS* inactive	10 ns	

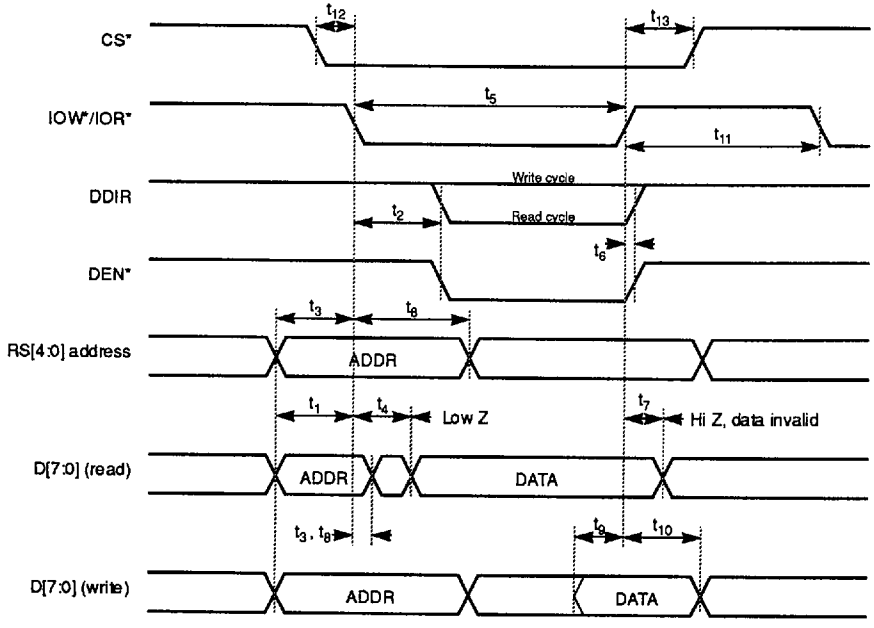


Figure 5-4. I/O Timing (Local Hardware Interface Bus)

5.6.5 Clocks as Inputs

Ref.	Parameter		85 MHz MIN	85 MHz MAX
t_1	Rise Time	PCLKn		3 ns
		LCLK		3 ns
		SCLK		3 ns
t_2	Fall Time	PCLKn		3 ns
		LCLK		3 ns
		SCLK		3 ns
t_3	High Period	PCLKn	4 ns	
		LCLK	4 ns	
		SCLK	10 ns	
t_4	Low Period[a]	PCLKn	4 ns	
		LCLK	4 ns	
		SCLK	10 ns	
t_5	Cycle Time	PCLKn	11:5 ns	
		LCLK	11:5 ns	
		SCLK	25 ns	

NOTE: LCLK and SCLK cycle and pulse width times are multiplied by 2, 4, and 8 in 2:1, 4:1, and 8:1 multiplexing modes, respectively.

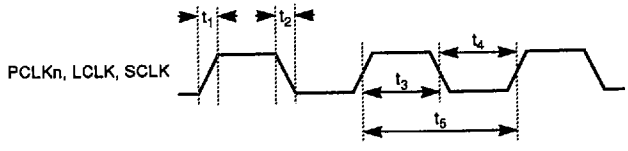


Figure 5-5. PCLKn, LCLK, and SCLK as Inputs (LCLK = 1:1 Mux Rate)

5.6.6 Sync, RGB, and GSD[23:0] Output Timing from PCLKn

Ref.	Parameter		MIN	MAX
t_1	Delay	PCLKn rise to R,G,B output		30 ns
t_2		R, G, B output rise/fall	3 ns	
t_3		R, G, B output full-scale settling time		15 ns
t_4	Delay	PCLKn rise to VSOUT, HSOUT output	2 ns	10 ns
t_5	Delay	PCLKn rise to GSD[23:0] output	2 ns	10 ns
	Delay	R, G, B output to SENSE* output		1 µs

NOTE: 1) Output delay is measured from the 50% point of the rising edge of PCLKn to the 50% point of full-scale transition.
2) Settling time is measured from the 50% point of full-scale transition to the output remaining within +/- 1 LSB.
3) Output rise/fall time is measured between the 10% and 90% points of full-scale transition.
4) In 1:1 multiplexing mode, RGB data is clocked out directly from LCLK, and synchronizing with SCLK and PCLKn is unnecessary and bypassed. All timing PCLKn references in the table above apply to LCLK when in 1:1 multiplexing mode.

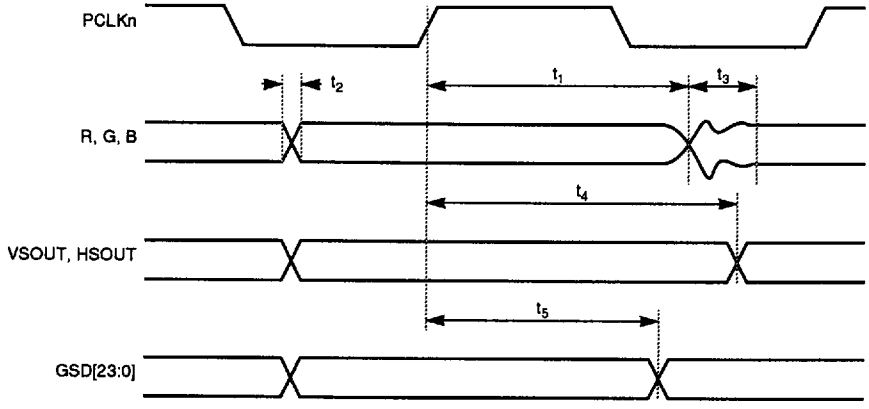


Figure 5-6. Sync, RGB, and GSD[23:0] Output Timing from PCLKn

5.6.7 Graphics Port Input Timing

Ref.	Parameter		MIN	MAX
t_1	Hold	SCLK rise to LCLK rise synchronizer	0 ns	
t_2	Delay	PCLKn rise to SCLK output 1:1 mode 2:1, 4:1, 8:1 mode		 10 ns 15 ns
t_3	Setup	Graphics data, control to LCLK rise	1 ns	
t_4	Hold	Graphics data, control to LCLK rise	5 ns	

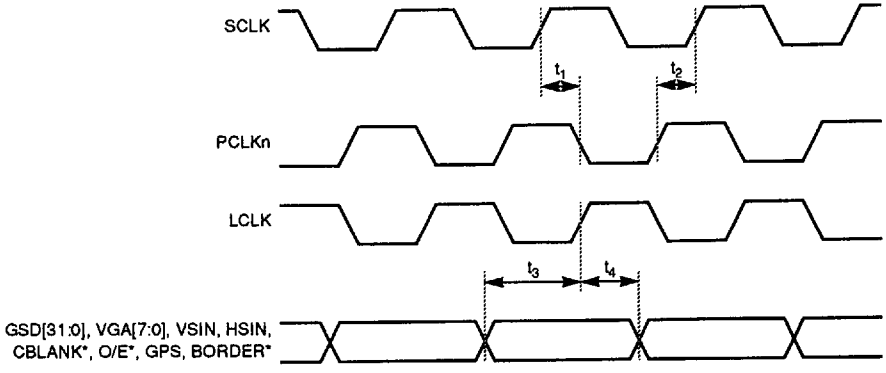


Figure 5-7. Graphics Port Input Timing

5.6.8 VGA Port Interface Timing, EC Mode 1

Ref.	Parameter		MIN	MAX
t_1	Setup	MSB data valid to falling edge PCLKn	1 ns	
t_2	Hold	LCLK falling edge to MSB data	5 ns	
t_3	Setup	LSB data and graphics controls valid to rising edge PCLKn	1 ns	
t_4	Hold	LCLK rising edge to LSB data, graphics controls invalid	5 ns	
t_5	Pulse Width	LCLK low	12 ns	
t_6	Pulse Width	LCLK high	12 ns	
t_7	Period	LCLK	30 ns	
t_8	Delay	LCLK rising edge to RGB output		30 ns
t_9	Delay	valid data to full-scale RGB output		15 ns
t_{10}	Delay	RGB out to SENSE* valid	0 µs	1 µs
t_{11}	Delay	Pipeline		32 PCLKn cycles

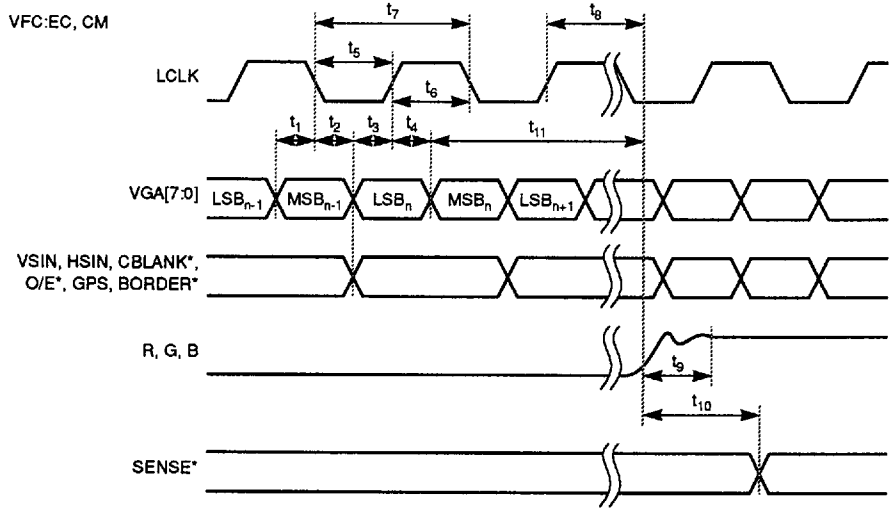
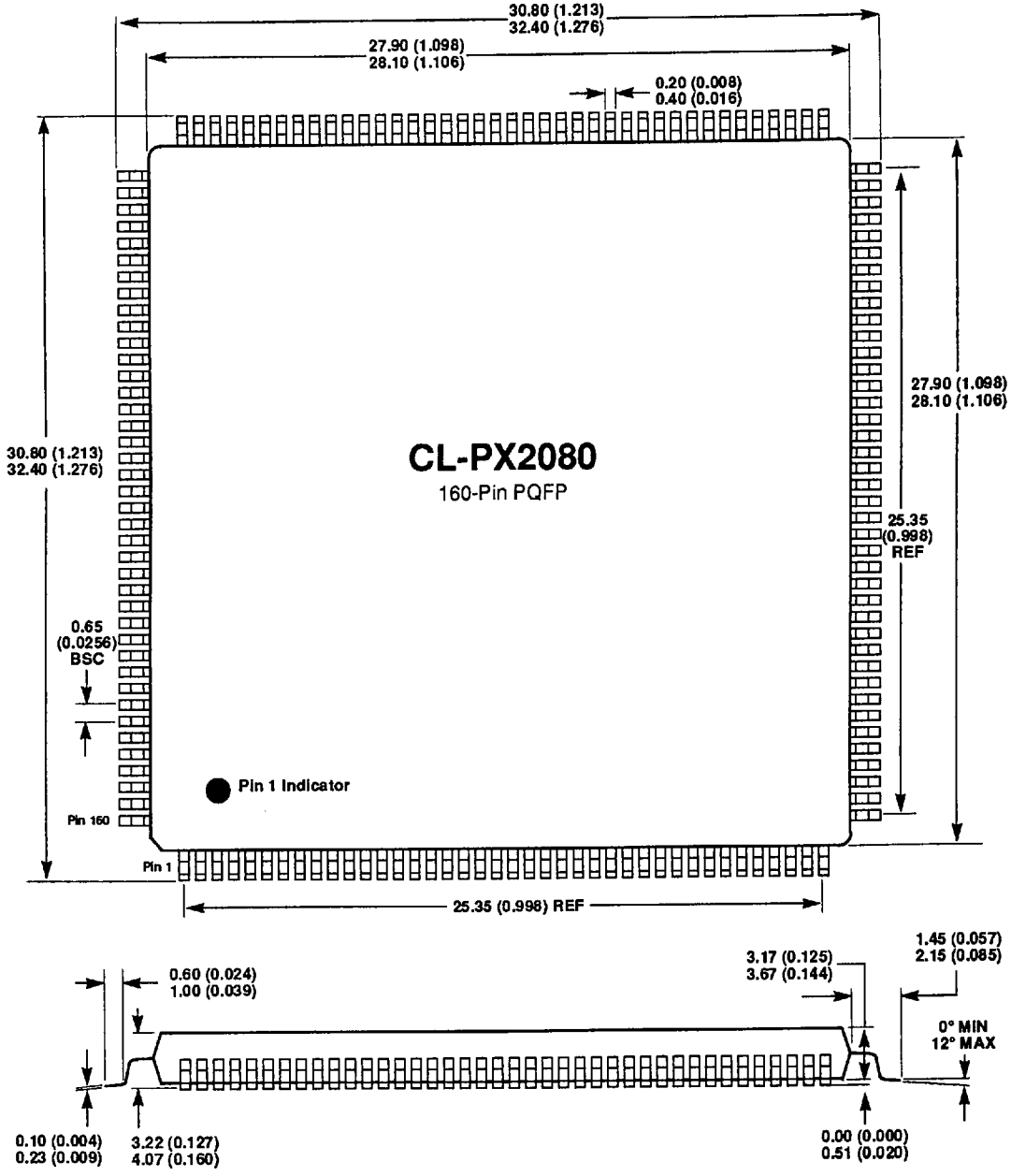


Figure 5-8. VGA Port Interface Timing, EC Mode 1 (16-Bit)

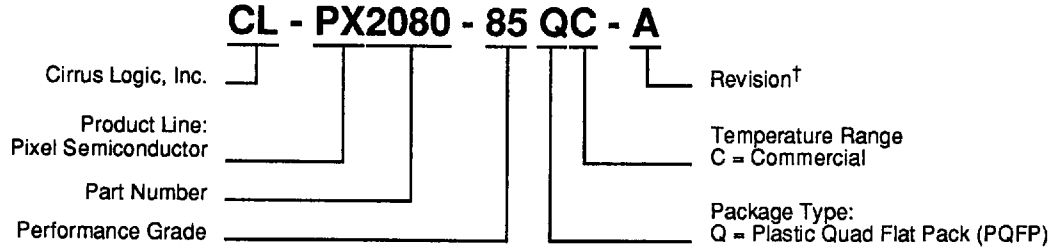
6. PACKAGE DIMENSIONS — 160-Lead PQFP



NOTE: Dimensions are in millimeters (inches).

7. ORDERING INFORMATION

When ordering the CL-PX2080 MediaDAC™, use the following format:



† Contact Cirrus Logic, Inc., for up-to-date information on revisions.

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