EDSON

Advance Information

EL2010
MICRO CHANNEL
MEMORY BOARD CHIPSET

- COMPLETE MICRO CHANNEL MEMORY CARD IN 2 CHIP SET
- UP TO 16 MEGABYTES OF MEMORY
- FULL SET OF MICRO CHANNEL POS REGISTERS
- COMPLETE TRAM (TRANSLATION RAM) SUPPORT
- MEMORY FULLY SOFTWARE RELOCATABLE
- MIX 256K AND 1 MEG RAM
- 2 SERIAL PORTS SOFTWARE ASSIGNABLE AS COM2 THROUGH COM8
- 1 PARALLEL PORT SOFTWARE ASSIGNABLE AS LPT2 OR LPT3
- PARALLEL PORT SOFTWARE CONFIGURABLE AS PS/2 "EXTENDED"
- AUTOMATIC GENERATION OF 2 WAIT STATES FOR I/O
- OPTIONAL ON-BOARD ROM SOFTWARE RELOCATABLE
- 2 BUILT-IN IBM-AUTHORIZED BOARD ID CODES
- OPTIONAL EXTERNAL ID CODES
- PARITY CHECK

INTRODUCTION

The EL2010, in a compact 2 CMOS chip set, provides all PS/2 Micro Channel interface and memory control necessary for a 16-bit Micro Channel memory expansion board. The chips support up to 16 Megabytes of memory and allow a mix of 256k and 1 Meg DRAM chips.

In addition to memory control, the chips provide decoding for 1 parallel and 2 serial ports. The I/O ports can be enabled, disabled and reassigned under software control with the POS registers (Serial ports can be COM2 - COM8 and Parallel port can be LPT2 or LPT3). Parallel port interrupts are automatically redirected to the proper channel when the software selects LPT2 or LPT3. Also, parallel port interrupts are converted from PC/AT-style pulse to PS/2-style levels.

Optional on-board ROM can be enabled, disabled and reassigned under software control with the POS registers. ROM can be located in one of 7 address ranges from C4000h to DC000h

The EL2010 provides 2 selectable IBM authorized board ID codes or can be configured to enable external ID buffers.

The EL2010 uses a unique two-chip architecture to enhance performance and reliability. The two chips contain identical circuitry, performing complementary functions. In this booklet, the two functions will be referred to as *Chip 1* and *Chip 2*. The two chips share the job of running the memory board while verifying the proper operation of the other.

Chip 1 performs Memory address multiplexing, Translation RAM (TRAM) control (reading and writing), and address comparison for I/O and on-board ROM.

Chip 2 is responsible for timing and control signals. Control signals include memory strobes, Parity control and check, data buffer enables, Micro Channel status feedback and I/O strobes.

Both chips contain a full complement of POS registers and both are written when the processor sets up the card. To avoid conflict, only one responds to any read of POS registers. *Chip 1* responds to reads of POS registers 3, 4, 6 and 7. *Chip 2* responds to POS registers 0, 1, 2, and 5.

Because both chips fully monitor the Micro Channel bus status, both chips know, at all times, what operation the other chip is performing. Because both chips independently recognize the command, they can each begin performing their part of the task simultaneously. The resulting lack of delay for inter-chip communication allows the EL2010 to keep up with the highest speed processor.

The dual-chip architecture increases system reliability. Because each chip knows the processor request, it also knows what its partner chip will be doing. Any requests of one chip by the other is checked before action is taken. This redundant checking helps eliminate soft errors often found in noisy system environments.

PROGRAMMING

Programming note: TRAM (Translation RAM) is only written or read when POS register #3 (POS-3) is written or read. POS-4 bits 0, 1 and 2 contain three additional TRAM data bits. When POS-3 is written, the contents of POS-3 and POS-4 (bits 0-2) are all written to the TRAM. When POS-3 is read, the additional TRAM data bits are also read and stored in POS-4 for later reading. Reading POS-4 does not read the TRAM, but will return the bits stored in POS-4 by the previous TRAM read cycle. Writing POS-4 does not write to TRAM, but stores data to be written on the next POS-3 write.

TRAM Data bits are written and read through POS registers 3 and 4 in the following pattern:

	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
POS-3 bit:				7	6	5	4	3	2	1	0
POS-4 bit:	2	1	0								

TRAM Address bits are written through POS registers 6 and 7 in the following pattern:

	TA9	TA8	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
POS-6 bit:			7	6	5	4	3	2	1	0
POS-7 bit:	1	0								

To Read a TRAM entry:

- Write address LSB to POS-6
- Write two most significant address bits to POS-7 bits 0 and 1.
- Read POS-3
- Read POS-4
- Mask and use data bits 0, 1 and 2 of POS-4.

To write a TRAM entry:

- Write address LSB to POS-6
- Write two most significant address bits to POS-7 bits 0 and 1.
- Read POS-4.
- Mask and update data bits 0, 1 and 2 of POS-4.
- Write POS-4
- Write POS-3

MEMORY BOARD POS REGISTER USE

Reg 2, Bits 1-7 Not used. Readable and writable.

Reg 5, Bit 0 Not used. Readable and writable.

Reg 3, TRAM data read, write. Bit 7 indicates valid if "1".

Reg 4, Bits 2,1,0 TRAM data bits 10, 9 and 8 respectively.

	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
POS-3 bit:				7	6	5	4	3	2	1	0
POS-4 bit:	2	1	0								

Reg 4 Bits 7-4: Serial port assignment for 2 Serial Ports

bit#:	7	6	5	4	Serial A	Serial B
	0	0	0	0	disabled	disabled
	0	0	0	1	Serial 8	disabled
	0	0	1	0	Serial 2	disabled
	0	0	1	1	Serial 3	disabled
	0	1	0	0	Serial 4	disabled
	0	1	0	1	Serial 5	disabled
	0	1	1	0	Serial 6	disabled
	0	1	1	1	Serial 7	disabled
	1	0	0	0	reserved	reserved
	1	0	0	1	Serial 8	disabled
	1	0	1	0	Serial 2	Serial 3
	1	0	1	1	Serial 3	Serial 4
	1	1	0	0	Serial 4	Serial 5
	1	1	0	1	Serial 5	Serial 6
	1	1	1	0	Serial 6	Serial 7
	1	1	1	1	Serial 7	Serial 8

Reg 4 Bit 3: ROM Address selection.
Reg 5 Bits 2,1: ROM Address selection.

POS reg. bit#: 4	5 3	5 2	1	ROM Address Range
	0	0	0	disabled
	0	0	1	C4000 - C5FFF
	0	1	0	C8000 - C9FFF
	0	1	1	CC000 - CDFFF
	1	0	0	D0000 - D2FFF
	1	0	1	D4000 - D5FFF
	1	1	0	D8000 - D9FFF
	1	1	1	DC000 - DDFFF

Reg 5 Bit 5,4,3: Parallel port assignment.

bit#: 5	4	3	Parallel port
0	0	0	Disabled
0	0	1	Parallel-2
0	1	0	Parallel-3
0	1	1	Parallel-2-Extended
1	0	0	Parallel-3 Extended
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Reg 6: Bits 7-0 Respectively TRAM address bits 7-0.

Reg 7 bits 1,0: Respectively TRAM address bits 9,8.

	TA9	TA8	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
POS-6 bit:			7	6	5	4	3	2	1	0
POS-7 bit:	1	0								

Reg 7 bits 7-2: not used.

EL2010 SIGNALS

The two EL2010 chips have some common signals and each has some unique signals. The following section details the Signals of the EL2010 when configured as Chip1 and Chip 2.

Pin assignments for EL2010 configured as Chip 1 are shown in Pin Diagrams 1A, 1B and 1C. Pin Diagrams 2A, 2B and 2C show Pin Diagrams for the EL2010 when configured as Chip 2.

The EL2010 is packaged in an 84 pin plastic Leaded Chip Carrier (PLCC), also referred to as J-Lead. The package can be surface mounted or socketed. Pin Diagram A shows a top view of the PLCC package. Pin diagrams B and C show the pin placement when the PLCC is in a socket.

Terminals labeled as no-connection (NC) should not be connected to any signal; these may be active signals used for manufacture testing -- connection may damage the device.

The signals common to both chips fall into two categories, Micro Channel Signals and Inter-EL2010 communication signals. In addition to the common Micro Channel signals, Each chip has some Micro Channel signals that the other does not have.

- **Micro Channel Signals**
- **Inter-EL2010 Communication**

CHIP 1 signals are sorted into four groups:

- **Micro Channel Signals**
- **I/O control Signals**
- **Memory Address Signals**
- **Translation RAM Signals**

Chip 2 signals are sorted into seven groups:

- **Micro Channel Signals**
- **Data Buffer Control Signals**
- **EL2010 Setup Signals**
- **Parity Control Signals**
- **I/O Control, ROM Control and External ID**
- **Memory Control and Timing Signals**
- **Translation RAM (TRAM) Signals**

MICRO CHANNEL SIGNALS

ADL- (Input) Active Low

Micro Channel status signal to indicate address portion of a bus cycle.

CD-SETUP- (Input) Active Low

Micro Channel status signal indicating that a POS register read or write cycle is being performed.

CMD- (Input) Active Low

Micro Channel status signal indicates Command portion of a bus cycle.

D0-D7 (Bi-directional)

Micro Channel Data signals.

MADE24 (Input)

Micro Channel status signal asserted high when channel address is an unextended value equal or less than 16M.

REFRESH- (Input)

Micro Channel status signal asserted for memory refresh cycles.

MIO (Input)
S0- (Input)
S1- (Input)

Micro Channel status signals indicating Bus Cycle:

	MIO	S0-	S1-
I/O Write	0	0	1
I/O Read	0	1	0
Memory Write	1	0	1
Memory Read	1	1	0

INTER-EL2010 COMMUNICATION

BK2 (Bi-Directional)

During reset, Chip 2 drives BK2 to send setup data to Chip 1. After Reset, Chip 1 drives BK2 and Chip 2 monitors BK2 to detect when the parallel port is addressed.

MUX (Chip 1 Input, Chip 2 Output)

MUX is a multi-use signal. During reset, MUX is used to clock serial setup data into Chip 1. Setup data is read on the rising edge of MUX.

After reset, MUX signals multiplexer timing for RAS and CAS. MUX is high for RAS and falls for CAS.

During POS register #3 read/write operations, MUX is asserted low to switch TRAM address (TA0-TA9) from normal values of A14-A23 to (in order) POS-6 bits 0-7 and POS-7 bits 0 and 1. On POS register #3 read operations, TRAM data (TD0-TD10) is sampled on rising edge of MUX.

RESET (Chip 1 Input, Chip 2 Output) Active High

Reset is asserted high to indicate a reset. During reset, MUX and BK2 are used to shift setup information into Chip 1.

ROM-I/O-SEL (Chip 1 Output, Chip 2 Input) Active High

This signal allows Chip 1 to communicate one of two conditions to Chip 2:

1) A memory read access to the memory range for which ROM is configured and enabled is occurring.

2) An I/O access to an enabled I/O port is occurring.

CHIP 1 MICRO CHANNEL SIGNALS

A0-A23 (Input)

Micro Channel Address signals. Chip 1 receives all 24 address pins while Chip 2 receives only A0, A1 and A2.

MADE24 (Input) Active High

Micro Channel status signal asserted high when channel address is an unextended value equal or less than 16M.

CHIP 1 I/O CONTROL

BK0 (Output)
BK1 (Output)
BK2 (Bi-Directional)

During memory operations these assert the latched memory bank number. During I/O operations, BK0 is latched low when Serial-A is selected. BK1 is latched low when Serial-B is addressed. BK2 is latched low when the Parallel Port is addressed. During POS register setup operations, BK2-BK0 contain latched address bits A2-A0 respectively. During ROM accesses, BK0-BK2 contain latched addresses A10-A12 respectively.

For memory operations BK2-BK0 buffer TRAM Data (TD) to select memory banks in the following pattern.

	TD10 BK2	TD9 BK1	TD8 BK0
Bank 0	0	0	0
Bank 1	0	0	1
Bank 2	0	1	0
Bank 3	0	1	1
Bank 4	1	0	0
Bank 5	1	0	1
Bank 6	1	1	0
Bank 7	1	1	1

For I/O operations BK2-BK0 act as active low chip selects. Figure 2 shows use of BK0 for serial port-A UART select.

	BK2	BK1	BK0
SERIAL-A	1	1	0
SERIAL-B	1	0	1
PARALLEL	0	1	1

For ROM operations BK2-BK0 assert latched address bits A12, A11, and A10 respectively. ROM usage is shown in Figure 3.

During POS register setup operations, BK2-BK0 assert latched address bits A2, A1, and A0 respectively.

During reset, BK2 becomes an input pin to receive setup data from chip 2.

CHIP 1 MEMORY ADDRESS SIGNALS

MA0-MA9 (Outputs)

Memory address bits. Multiplexed for RAS, CAS, and Refresh. During I/O and ROM operations, MA0-MA9 assert latched Micro Channel addresses A0-A9. These pins should be buffered as shown in Figure 1.

Memory Address Multiplexing:

	RAS	CAS	Refresh, I/O, ROM
MA0	A 1	A10	A 0
MA1	A 2	A11	A 1
MA2	A 3	A12	A 2
MA3	A 4	A13	A 3
MA4	A 5	TD-0	A 4
MA5	A 6	TD-1	A 5
MA6	A 7	TD-2	A 6
MA7	A 8	TD-3	A 7
MA8	A 9	TD-4	A 8
MA9	TD-6	TD-5	A 9

Note: TD-x indicates TRAM Data bit #x.

CHIP 1 TRANSLATION RAM SIGNALS

The EL2010 provides all signals necessary to address read and write TRAM. Figure 1 shows connection of TRAM (U7 and U8) to the EL2010.

TA0-TA9: (Output)

Translation RAM address pins.

TRAM Address bits are written through POS registers 6 and 7 in the following pattern:

	TA9	TA8	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
POS-6 bit:			7	6	5	4	3	2	1	0
POS-7 bit:	1	0								

TD0-TD10: (Bi-directional)

Translation RAM (TRAM) data signals. TD7 is memory valid bit (1 = valid). TRAM data bits are used as follows:

TD0: Multiplexed Memory Address (See MA0-MA9)
TD1: Multiplexed Memory Address (See MA0-MA9)
TD2: Multiplexed Memory Address (See MA0-MA9)
TD3: Multiplexed Memory Address (See MA0-MA9)
TD4: Multiplexed Memory Address (See MA0-MA9)
TD5: Multiplexed Memory Address (See MA0-MA9)
TD6: Multiplexed Memory Address (See MA0-MA9)
TD7: Memory Valid Bit (1 = Valid)
TD8: Memory Bank Select BK0
TD9: Memory Bank Select BK1
TD10: Memory Bank Select BK2

TRAM Data bits are written and read through POS registers 3 and 4 in the following pattern:

	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
POS-3 bit:				7	6	5	4	3	2	1	0
POS-4 bit:	2	1	0								

TWE: (Input) Active Low

TWE is asserted low by Chip 2 to write data into TRAM. When TWE is low, Chip 1 asserts POS Reg. 3 bits 0-7 and POS reg. 4 bits 0-2 on TRAM data bits TD0-TD10, respectively.

CHIP 2 MICRO CHANNEL SIGNALS

The EL2010 receives Micro Channel status and generates response signals. EL2010 outputs do not have the drive necessary to meet Micro Channel requirements, and should be fully buffered as shown in Figure 1.

A0, A1, A2, (Inputs)

Micro Channel Address signals.

14-MHZ (Input)

Micro Channel clock signal at video frequency. Used to time I/O wait-states.

CD-SFDBK- (Output) Active Low

Micro Channel status signal asserted to acknowledge receipt of an address of this card used for RAM, ROM or I/O.

CD-CHRDY (Output) Active High

Micro Channel status signal indicates that card is ready and current cycle can end. CD-CHRDY is de-asserted (Low) to insert wait-states.

CD-DS-16- (Output) Active Low

Micro Channel status signal indicates a 16-bit transfer. Asserted for RAM cycles.

CHCK (Output) Active High

Signals NMI as result of Parity error. Connect to open collector buffer to drive Micro Channel. Can be cleared by writing to POS register 5, a Channel Reset (CHRESET), or a memory write operation to this board.

CHRESET (Input) Active High

Micro Channel reset signal.

SBHE- (Input) Active Low

Micro Channel Address signal indicating that upper byte of data (D8-D15) is being used for the current bus cycle.

CHIP 2 DATA BUFFER CONTROL

BUF-DIR-WRT (Output) Active High

Controls direction of Micro Channel data buffers. BUF-DIR-WRT is high to write data to the memory card, and low to read data from the memory card.

BUF-ENBL-L- (Output) Active Low
BUF-ENBL-H- (Output) Active Low

Active low enable for the Micro Channel data buffers for low and high data bytes respectively. POS register 2, bit 0 which controls CARD-DIS (Card Disable) is factored into these signals to tri-state buffers when card is disabled.

CARD-DIS (Output)

CARD-DIS is asserted (high) when bit 0 of POS register 2 is "0". This high condition indicates that the card is disabled and no buffers should drive the bus except for POS register setup operations. CARD-DIS be used to tri-state card buffers not already controlled by BUF-ENBL-L-, BUF-ENBL-H-, CS-ROM-, ID-LO- or ID-HI-. On Micro Channel reset, POS register 2 is cleared resulting in an initial condition where CARD-DIS is asserted.

CHIP 2 EL2010 SETUP SIGNALS

The EL2010 can be configured with I/O and ROM capabilities enabled or disabled. If enabled, then the POS registers must contain the proper codes to configure the I/O or ROM. Software may also disable the features by virtue of the contents of the POS registers.

If the features are disabled by grounding these pins, then software cannot enable these features and the corresponding POS registers can be written and read without effect.

Only Chip 2 has inputs to configure these features. The information is relayed to Chip 1 during reset. Having only one setup source eliminates errors due to conflicting configurations.

ID-SEL0 (Input) Selects Board ID
ID-SEL1 (Input) Selects Board ID

	ID-SEL1	ID-SEL0
RESERVED	1	1
EDSUN-1 = 7048	1	0
EDSUN-2 = 7049	0	1
EXTERNAL	0	0

IO-ENBL (Input) Active High

When IO-ENBL is high, the EL2010 will decode IO addresses as controlled by POS register contents. If IO-ENBL is low, no I/O decode will occur and the register contents are ignored.

ROM-ENBL (Input) Active High

When ROM-ENBL is high, the EL2010 will decode ROM addresses as controlled by POS-4 bit 3 and POS-5 bits 2 and 1. If ROM-ENBL is low, no ROM decode will occur and the POS register contents are ignored.

CHIP 2 PARITY CONTROL

The EL2010 fully supports parity generation and checking for the lower data byte (D0-D7) and the upper data byte (D8-D15). When the system accesses a word, both parity bits are generated or checked. If the system is accessing a byte, only the corresponding parity bit is generated or checked.

The EL2010 contains internal circuitry to check the lower data byte and controls an external parity chip (74F280) for the upper data byte. Figure 4 shows a schematic using the parity circuit. This same configuration is used in the full memory board shown in Figure 1.

In Figure 4, the buffered upper byte of data (D8-D15) is connected to the D0-D7 inputs of the 74F280. D8, the ninth data input, is connected to PARITY-H-OUT (from the EL2010) and to the Q output of the DRAM which stores the parity bit. The EL2010 automatically asserts "0" during memory write cycles to drive the D8 bit; this generates "even" parity. During memory read cycles, the EL2010 tri-states PARITY-H-OUT allowing the DRAM to drive D8 of the 74F280.

During memory write cycles, the "even" output of the F280 is stored in the DRAM ("1" if the number of 1's in the data is even). The "odd" output of the F280 becomes PARITY-H-IN returned to the EL2010. The "odd" output of the F280 will be "0" only if there is an error.

Parity for the lower data byte is completely generated and checked internally by the EL2010. As shown in Figure 4, PARITY-L-OUT is connected to the "D" input of the DRAM and PARITY-L-IN is connected to the "Q" output of the DRAM. If the "D" and "Q" signals of the DRAM are separate as shown in Figure 4, PARITY-L-OUT may be buffered.

If the "D" and "Q" signals of the DRAM are connected (as found in some SIMM modules) PARITY-L-OUT should not be buffered, and both PARITY-L-OUT and PARITY-L-IN should be connected to the combined "D-Q" signal -- PARITY-L-OUT is tri-stated by the EL2010 during memory read operations, and will not conflict with the DRAM output.

To disable the internal generation/checking of the lower data byte, the INT-PARITY signal should be de-asserted (low). One would disable internal parity for special error checking such as an ECC. If INT-PARITY is low, PARITY-L-OUT and PARITY-L-IN behave exactly the same as PARITY-H-OUT and PARITY-H-IN and can be used with an external parity chip in the same way.

If no parity is desired, then external parity should be selected and both PARITY-H-IN and PARITY-L-IN should be tied high, indicating "no error."

PARITY-L-IN and PARITY-H-IN are sampled during memory reads to the board on the trailing edge of CAS- (rising edge). If an error is detected then CHCK (channel check) is asserted and bit 7 of POS register 5 is set to "0". The channel check indication in POS register 5 can be cleared 3 ways: a write to POS register 5 of any value, a write to memory on the board, or a full channel reset (CHRESET).

INT-PARITY (Input)

Selects internal parity generation/check for lower data byte if "1". Selects external parity generation/check if "0".

PARITY-L-IN (Input)
PARITY-H-IN (Input)

Parity bits checked during memory read operations. If Parity is internal, then PARITY-IN-L is read from DRAM. If Parity is External, PARITY-IN-L is parity compare result (0 = error). In External or Internal mode, PARITY-IN-H is parity result of checker chip (0 = error).

PARITY-L-OUT (Output)
PARITY-H-OUT (Output)

Parity bits asserted during memory write operations. PARITY-H-OUT is asserted as LOW during memory write. Tri-stated otherwise.

During memory write operations, PARITY-L-OUT asserts even parity if INT-PARITY is high, or "0" if INT-PARITY is low. Tri-stated during read operations.

CHIP 2 I/O, ROM and ID SIGNALS

CS-ROM- (Output) Active Low

When CS-ROM- is low, ROM is enabled and a memory read is in progress for an address in the selected 8k ROM address range. CS-ROM- is low for the entire CMD- low cycle and can be used to drive CS or OE on a ROM chip as shown in Figure 3.

ID-LOW- (Output) Active Low
ID-HI- (Output) Active Low

Board ID High byte and Board ID Low byte read strobes. These signals can be used as chip output enables for buffers or registers to assert an External ID as shown in Figure 6.These strobes become active when CMD- is active during a Setup I/O read of POS registers 1 and 0 (I/O addresses 0101h and 0100h) respectively -- but only if the EL2010 is configured for External ID. External ID is selected with ID-SEL1=0 and ID-SEL0=0. If an internal ID is selected, the EL2010 will provide the ID to the Micro Channel without external components.

IOR- (Output) Active Low

I/O Read strobe. This is active during Command period of an I/O access to an enabled I/O port. Actual selection of one of the three possible I/O devices is done by signals BK0, BK1 and BK2 of Chip 1.

IOW- (Output) Active Low

I/O Write strobe. This active during the Command period of an I/O access to an enabled I/O port. Actual selection of one of the three possible I/O devices is done by signals BK0, BK1 and BK2 of Chip 1.

PAR-2-INT-OUT (Output) Active High
PAR-3-INT-OUT (Output) Active High

These active low PS/2-style level interrupt are asserted when a low pulse is received on PARAL-INT-IN-. If the parallel port is configured as parallel port 2, PAR-2-INT-OUT- is asserted. Similarly, if the parallel port is configured as parallel port 3 then PAR-3-INT-OUT- is asserted. Configuration is performed in software by writing POS registers.

These interrupt signals go low when PARAL-INT-IN- goes low, and remain low until PARAL-INT-IN- goes high and the processor reads the Parallel Port Status register.

PAR-EXT-MODE (Output) Active High

This active high output signals that the parallel port has been configured for extended PS/2 functionality. This signal is asserted whenever POS register 5 bits 5, 4 and 3 have values selecting an extended function parallel port. The EL2010 chipset is not affected by this selection, but passes the information to external parallel port circuitry.

PARAL-INT-IN- (Input) Active Low

This active low input signals that the parallel port requests an interrupt. This input can be a PS/2-style level or PC/AT-style pulse interrupt. It will be latched and converted to a level before being asserted as PAR-2-INT-OUT or PAR-3-INT-OUT by the EL2010.

CHIP 2 MEMORY CONTROL AND TIMING SIGNALS

CAS- (Output) Active Low

Memory Column Address Strobe. CAS0- through CAS7- strobe memory banks 0 through 7 respectively. The EL2010 has only 1 CAS signal. The necessary CAS signals (one per memory bank) must be generated externally by a decoder (typically a 74F138) as shown in Figure 5. The bank select signals BK0, BK1 and BK2 are used as the selector inputs to the 74F138 and the EL2010 CAS- signal is used as the enable to generate CAS0- through CAS7-.

CYCLE1 (Output) Active High
CYCLE2 (Output) Active High

Signals the second cycle of the delay circuitry as shown in Timing Diagram 1. These are provided to assist miscellaneous external circuitry. They are not used in typical applications.

RAS0- (Output) Active Low
RAS1- (Output) Active Low
RAS2- (Output) Active Low
RAS3- (Output) Active Low

Memory Row Address Strobes. During a memory cycle, one of the RAS signals will be asserted to strobe the Row Address into the RAM. Each RAS signal is used for two of the eight possible 16-bit memory banks in the following pattern:

Memory Bank 0: RAS0-
Memory Bank 1: RAS1-
Memory Bank 2: RAS2-
Memory Bank 3: RAS3-
Memory Bank 4: RAS0-
Memory Bank 5: RAS1-
Memory Bank 6: RAS2-
Memory Bank 7: RAS3-

During a refresh cycle, all four RAS signals are asserted. They are asserted in a staggered pattern to avoid the power surge required to refresh the entire memory board at once, as shown in timing diagram 12.

DELAY-DRV- (Output) Active Low

This signal is the start of a timing cycle and should be connected to the input of a 5-tap delay line. The delay should be 20ns to 30ns per tap.

TIME0- (Input) Active Low
TIME1- (Input) Active Low
TIME2- (Input) Active Low
TIME3- (Input) Active Low
TIME4- (Input) Active Low
TIME5- (Input) Active Low

These signals are used to time the memory address multiplexers, RAS-, CAS-, WE- and TWE- strobes. TIME0- should be connected to the input of a 5 tap delay line (or connected to DELAY-DRV-) to monitor the timing pulse outside the EL2010 chip. This external monitor allows the EL2010 to compensate for board-level capacitance effects. The relationship of the timing signals is shown in Timing Diagram 1.

TIME1- through TIME5- should be connected, in order, to the 5 outputs of a 5-tap delay line. The delay should be 20ns to 30ns per tap. Time1- should be connected to the first tap (total delay from TIME0- to TIME1- of 20ns to 30ns) and Time5- should be connected to the last tap (total delay from TIME0- to TIME5- of 100ns to 150ns).

WE0- (Output) Active Low
WE1- (Output) Active Low

Memory Write Enables. WE1- is used to write the upper data byte (D8-D15). WE0- is used to write the lower data byte (D0-D7).

CHIP 2 TRANSLATION RAM SIGNALS

Chip 2 monitors TD7 (valid bit) and generates the TRAM write signal TWE-. Figure 1 shows the connections between TRAM (U7 and U8) and Chip 2 (U2).

TWE- (Output) Active Low

Signal is asserted (low) to write data into TRAM.

TD7 (Input)

TD7 is the TRAM valid bit (1 = valid). Chip 2 monitors this signal to determine if the current memory cycle contains a valid board memory address.

ELECTRICAL SPECIFICATIONS

The EL2010 has an operating temperature range from 0 to 70 degrees Celsius and supply voltage range of 4.5 and 5.5 volts. Power dissipation is only 200 mW; no heat sink is required.

Packaged in a 84-pin plastic leaded chip-carrier (PLCC), the EL2010 can be socketed or surface-mounted.

Inputs are TTL compatible, implemented in CMOS (Complementary Metal Oxide Semiconductor). Outputs are TTL compatible and are capable of driving 10 LS-TTL loads.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias .....0 to 70 degrees Celsius
Storage Temperature .....-40 to 125 degrees Celsius
Power Dissipation .....200 mW
DC Supply (Vcc) .....-0.3 to +7 V
Input Voltage .....-0.3 V to Vcc +0.3 V

This is a stress rating only; functional operation of the device at these or other conditions beyond those described in the operational specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

D.C. CHARACTERISTICS

(Temp. = 0 to 70 degrees Celsius, Vcc = 4.5 to 5.5 Volts)

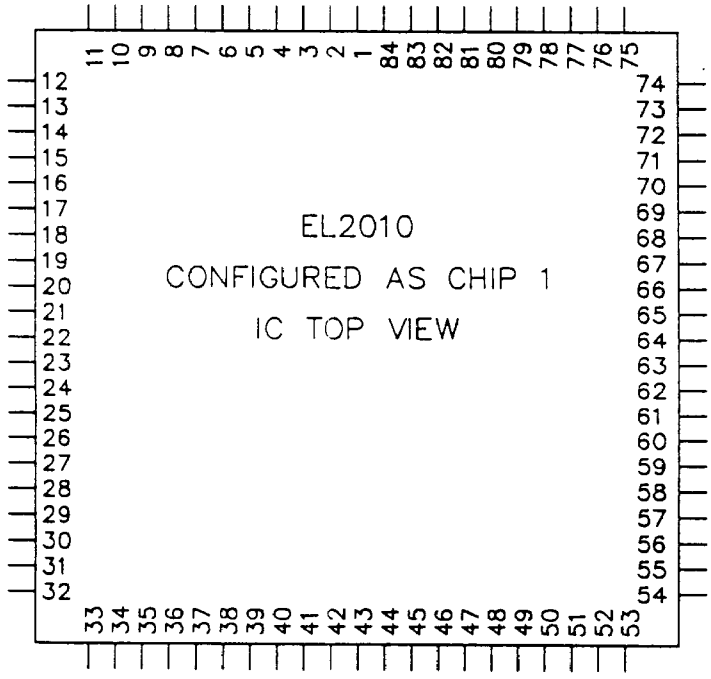
Symbol	Parameter	Min	Max	Units	Test Condition
Vil	Input LOW Voltage		0.8	V	
Vih	Input HIGH Voltage	2.0		V	
Iol	Output LOW Current	4.0		mA	Vol = 0.5 V
Ioh	Output HIGH Current	4.0		mA	Voh = 2.4 V
Iin	Input Leakage		10.0	uA	Vi = 0 to Vcc
Ioz	Tri-state Leakage		10.0	uA	Vo = 0 to Vcc
Cin	Input Capacitance		5.0	pF	
Iccq	Quiescent Current		20.0	uA	

A.C. CHARACTERISTICS

(Temp. = 0 to 70 degrees Celsius, Vcc = 4.5 to 5.5 Volts, Load Capacitance = 25pf)

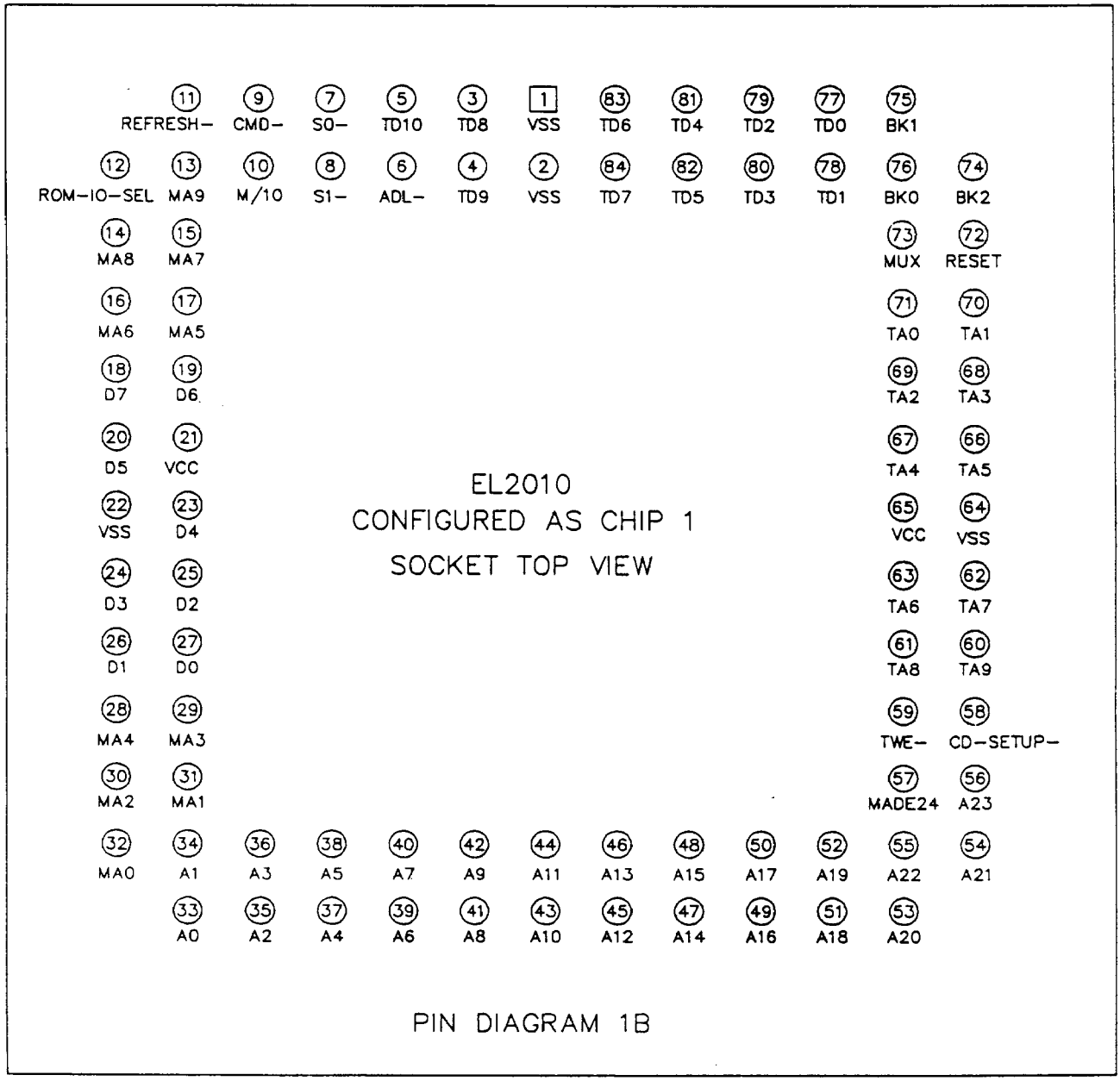
Symbol	Parameter	Min	Max	Units
t1	MA0-MA9 to TA0-TA9	2	13	ns
t2	ADL to MA0-MA9	5	27	ns
t3	A0-A23 to MA0-MA9	2	20	ns
t4	MUX to MA0-MA9	3	20	ns
t5	TD0-TD10 to BK0-BK2 (MEM)	4	20	ns
t6	ADL to BK0-BK2 (MEM)	6	25	ns
t7	A0-A23 to BK0-BK2 (I/O)	5	25	ns
t8	A0-A23 to ROM-IO-SEL	5	30	ns
t9	TWE Fall to TD0-TD10 Driven	5	25	ns
t10	TWE Rise to TD0-TD10 HI-Z	3	15	ns
t11	ADL Fall to DELAY-DRV- Fall	4	15	ns
t12	TIME1 Fall to RAS- Fall	5	20	ns
t13	TIME2 Fall to MUX Fall	5	25	ns
t14	TIME2 Fall to WE- Fall	5	25	ns
t15	TIME5 Fall to CAS- Fall (Write)	5	25	ns
t16	TIME4 Fall to CAS- Fall (Read)	5	20	ns
t17	TD7 to CD-SFDBK	3	15	ns
t18	TD7 to CD-DS-16	3	13	ns
t19	TD7 to CD-CHRDY	4	17	ns
t20	CMD Fall to CD-CHRDY Rise	5	20	ns
t21	D0-D7 to PARITY-L-OUT	5	22	ns
t22	PARITY-L-IN- to CAS- Rise (setup)		15	ns
t23	CMD to CS-ROM-	5	20	ns
t24	CMD Fall to IOR-,IOW- Fall	5	20	ns
t25	CMD Rise to IOR-,IOW- Rise	5	15	ns
t26	CMD Fall to BUF-ENBL-L,H Fall	5	25	ns
t27	CMD Rise to BUF-ENBL-L,H Rise	5	25	ns
t28	ROM-IO-SEL to CD-SFDBK Fall	5	15	ns
t29	ROM-IO-SEL to CD-CHRDY Fall	5	22	ns

Symbol	Parameter	Min	Max	Units
t30	REFRESH TIME1 Fall TO RAS0 Fall	5	20	ns
t31	REFRESH RAS0 Fall TO RAS1 Fall	5	15	ns
t31	REFRESH RAS1 Fall TO RAS2 Fall	5	15	ns
t31	REFRESH RAS2 Fall TO RAS3 Fall	5	15	ns

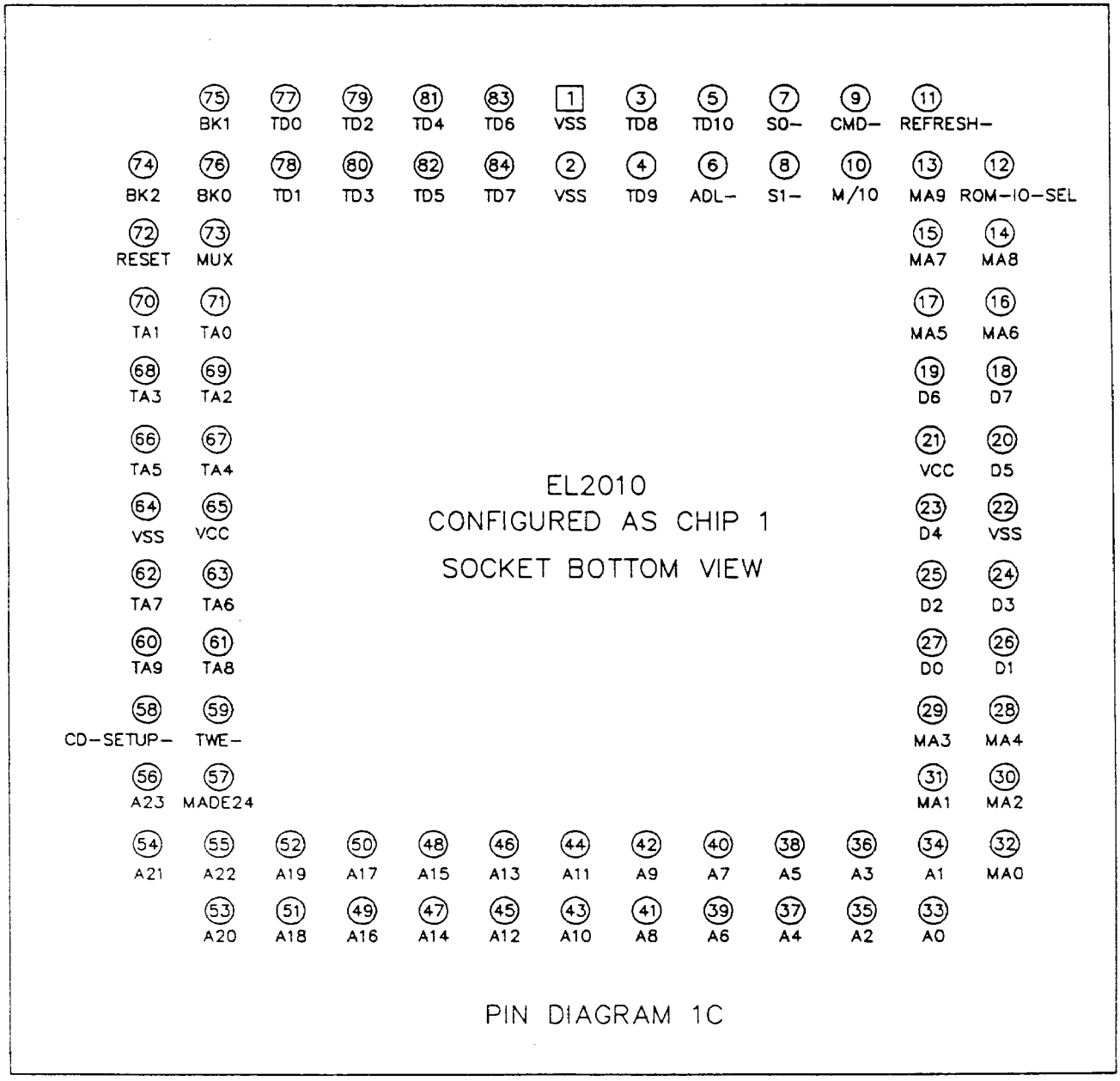


PIN DIAGRAM 1A

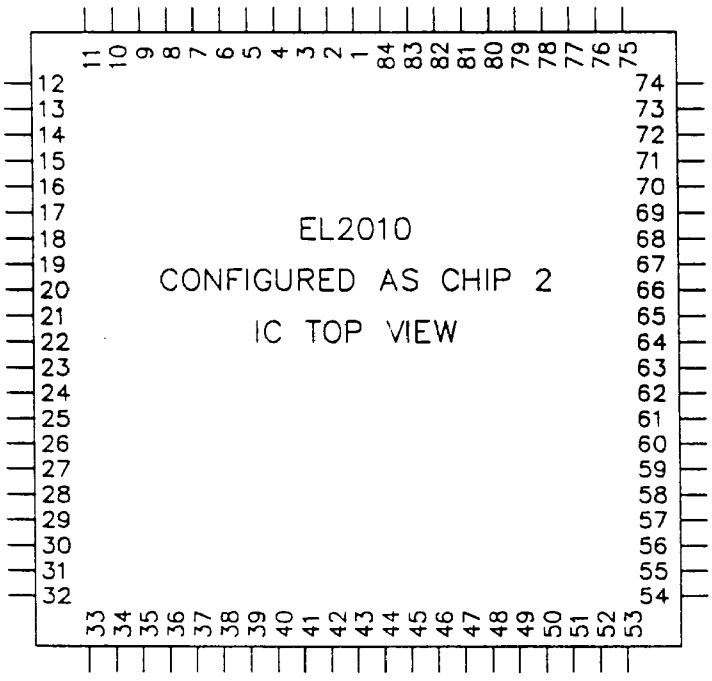
PIN	SIGNAL	PIN	SIGNAL
1.	VSS	43.	A10
2.	VSS	44.	A11
3.	TD8	45.	A12
4.	TD9	46.	A13
5.	TD10	47.	A14
6.	ADL–	48.	A15
7.	S0–	49.	A16
8.	S1–	50.	A17
9.	CMD–	51.	A18
10.	M/IO	52.	A19
11.	REFRESH–	53.	A20
12.	ROM–IO–SEL	54.	A21
13.	MA9	55.	A22
14.	MA8	56.	A23
15.	MA7	57.	MADE24
16.	MA6	58.	CD–SETUP–
17.	MA5	59.	TWE–
18.	D7	60.	TA9
19.	D6	61.	TA8
20.	D5	62.	TA7
21.	VCC	63.	TA6
22.	VSS	64.	VSS
23.	D4	65.	VCC
24.	D3	66.	TA5
25.	D2	67.	TA4
26.	D1	68.	TA3
27.	D0	69.	TA2
28.	MA4	70.	TA1
29.	MA3	71.	TA0
30.	MA2	72.	RESET
31.	MA1	73.	MUX
32.	MA0	74.	BK2
33.	A0	75.	BK1
34.	A1	76.	BK0
35.	A2	77.	TD0
36.	A3	78.	TD1
37.	A4	79.	TD2
38.	A5	80.	TD3
39.	A6	81.	TD4
40.	A7	82.	TD5
41.	A8	83.	TD6
42.	A9	84.	TD7



PIN DIAGRAM 1B



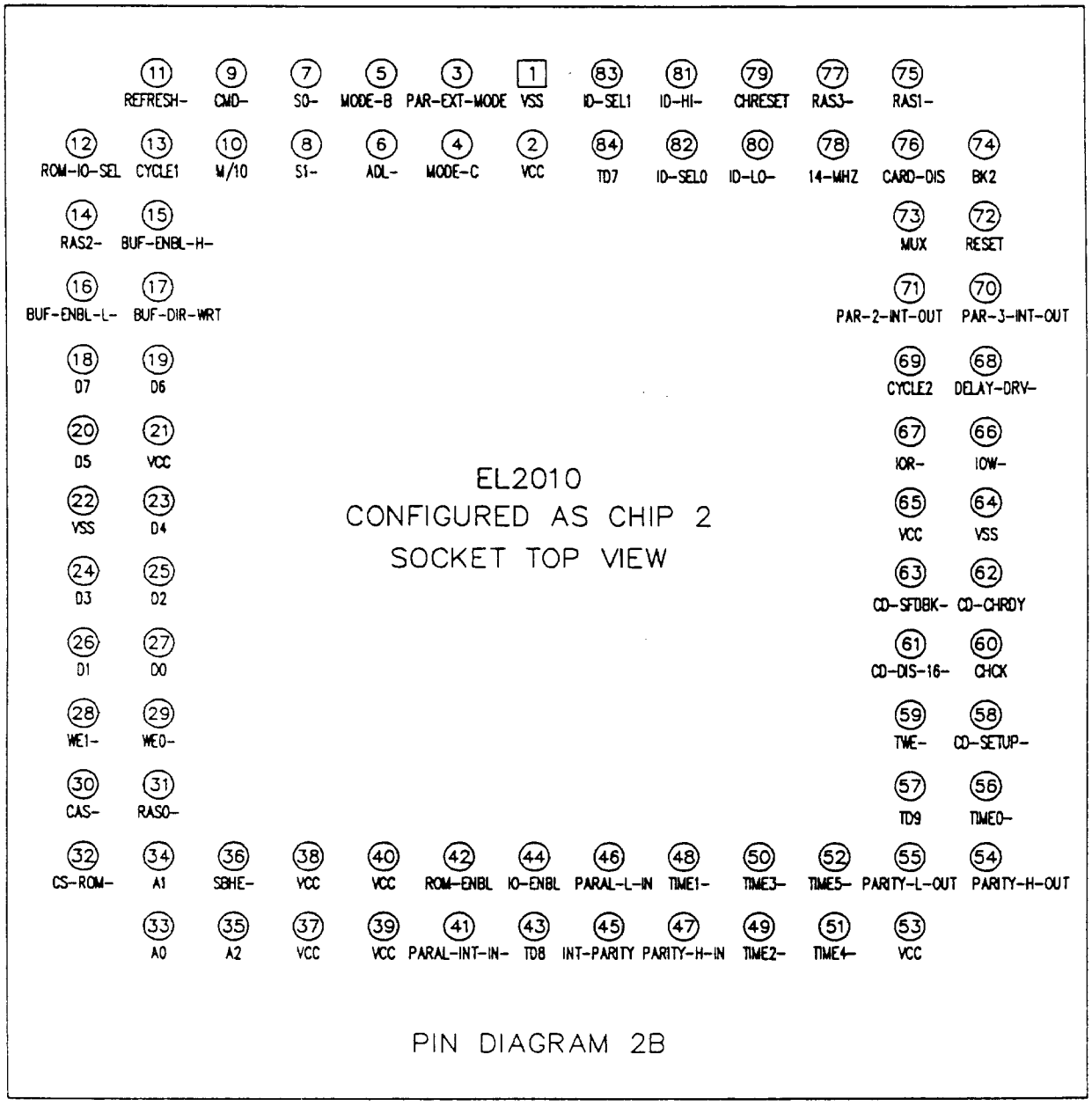
PIN DIAGRAM 1C



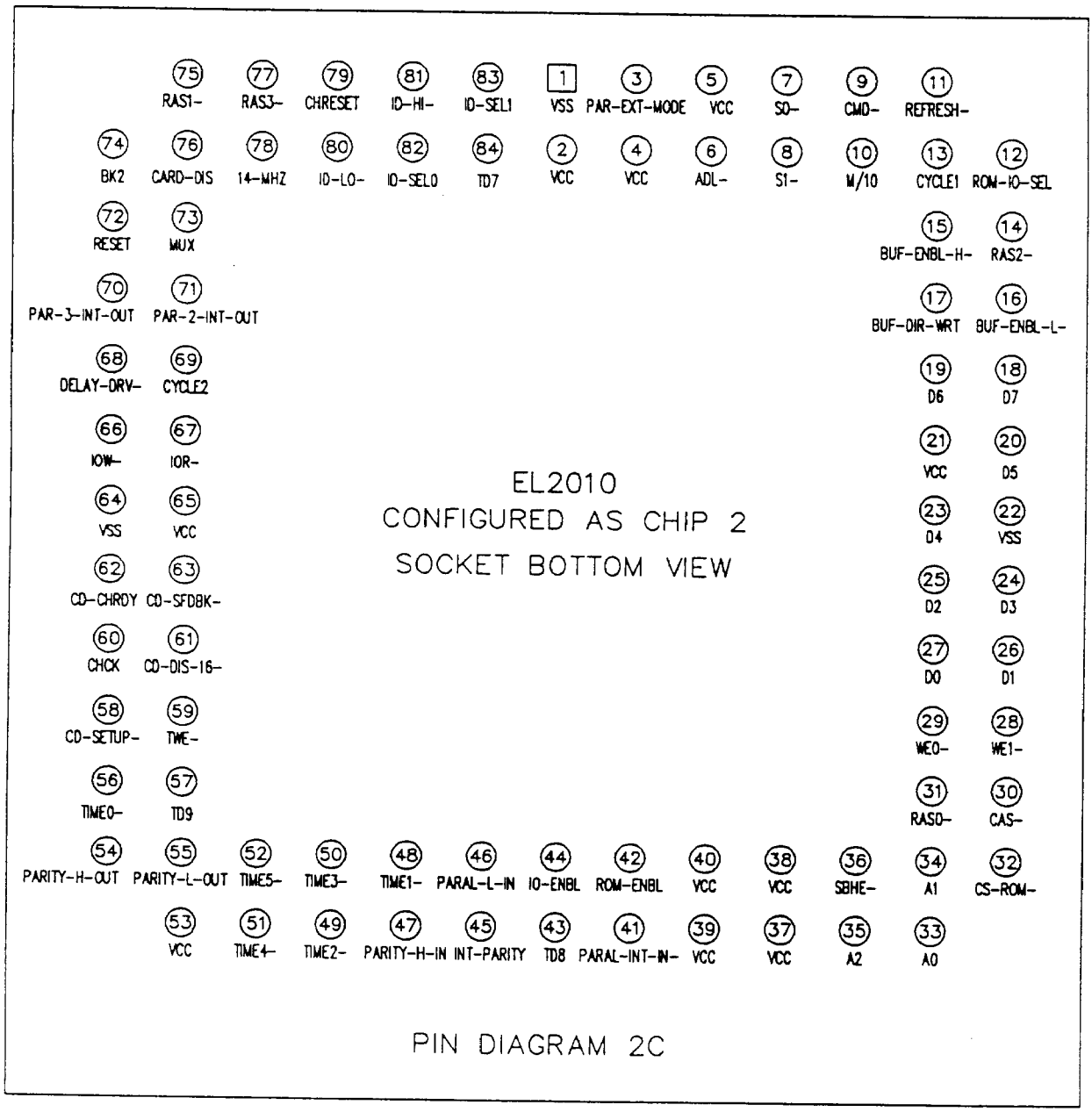
PIN DIAGRAM 2A

PIN SIGNAL

1.	VSS	43.	TD8
2.	VCC	44.	IO-ENBL
3.	PAR-EXT-MODE	45.	INT-PARITY-
4.	VCC	46.	PARAL-L-IN
5.	VCC	47.	PARAL-H-IN
6.	ADL-	48.	TIME1-
7.	S0-	49.	TIME2-
8.	S1-	50.	TIME3-
9.	CMD-	51.	TIME4-
10.	MIO	52.	TIME5-
11.	REFRESH	53.	VCC
12.	ROM-IO-SEL	54.	PARITY-H-OUT
13.	CYE1	55.	PARITY-L-OUT
14.	RAS2-	56.	TIME0
15.	BUF-ENBL-H-	57.	TD9
16.	BUF-ENBL-L-	58.	CD-SETUP-
17.	BUF-DIR-WRT	59.	TWE-
18.	D7	60.	CHCK
19.	D6	61.	CD-DS-16
20.	D5	62.	CD-CHRDY
21.	VCC	63.	CD-SFDBK-
22.	VSS	64.	VSS
23.	D4	65.	VCC
24.	D3	66.	IOW-
25.	D2	67.	IOR-
26.	D1	68.	DELAY-DRV-
27.	D0	69.	CYCLE2
28.	WE1-	70.	PAR-3-INT-OUT
20.	WE0-	71.	PAR-2-INT-OUT
30.	CAS-	72.	RESET
31.	RAS0-	73.	MUX
32.	CS-ROM-	74.	BK2
33.	A0	75.	RAS1-
34.	A1	76.	CARD-DIS
35.	A2	77.	RAS3-
36.	SBHE-	78.	14-MHZ
37.	VCC	79.	CHRESET
38.	VCC	80.	ID-LO-
39.	VCC	81.	ID-HI-
40.	VCC	82.	ID-SEL0
41.	PARAL-INT-IN-	83.	ID-SEL1
42.	ROM-ENBL	84.	TD7



PIN DIAGRAM 2B



PIN DIAGRAM 2C

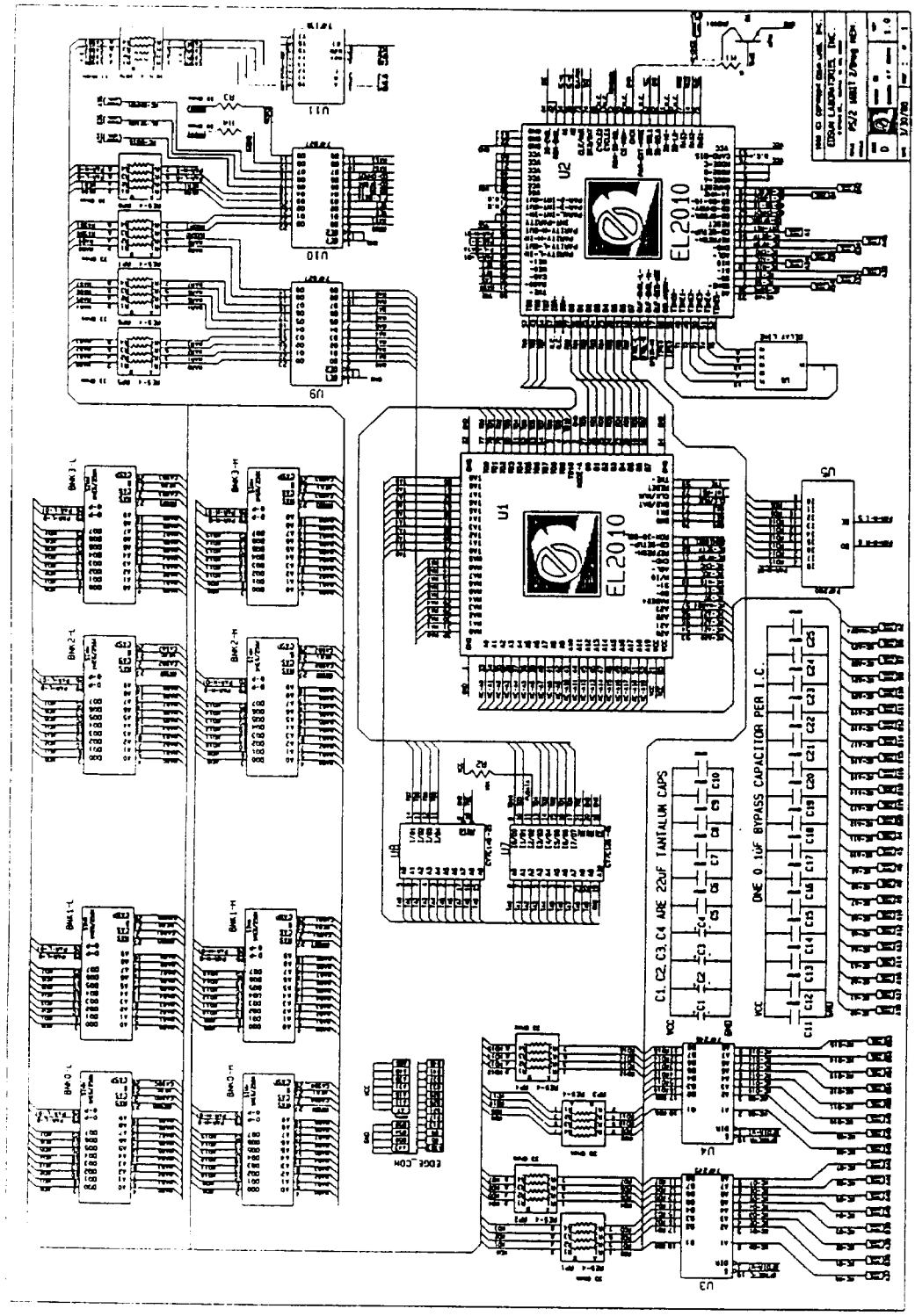


FIGURE 1
8 MEG MEMORY BOARD

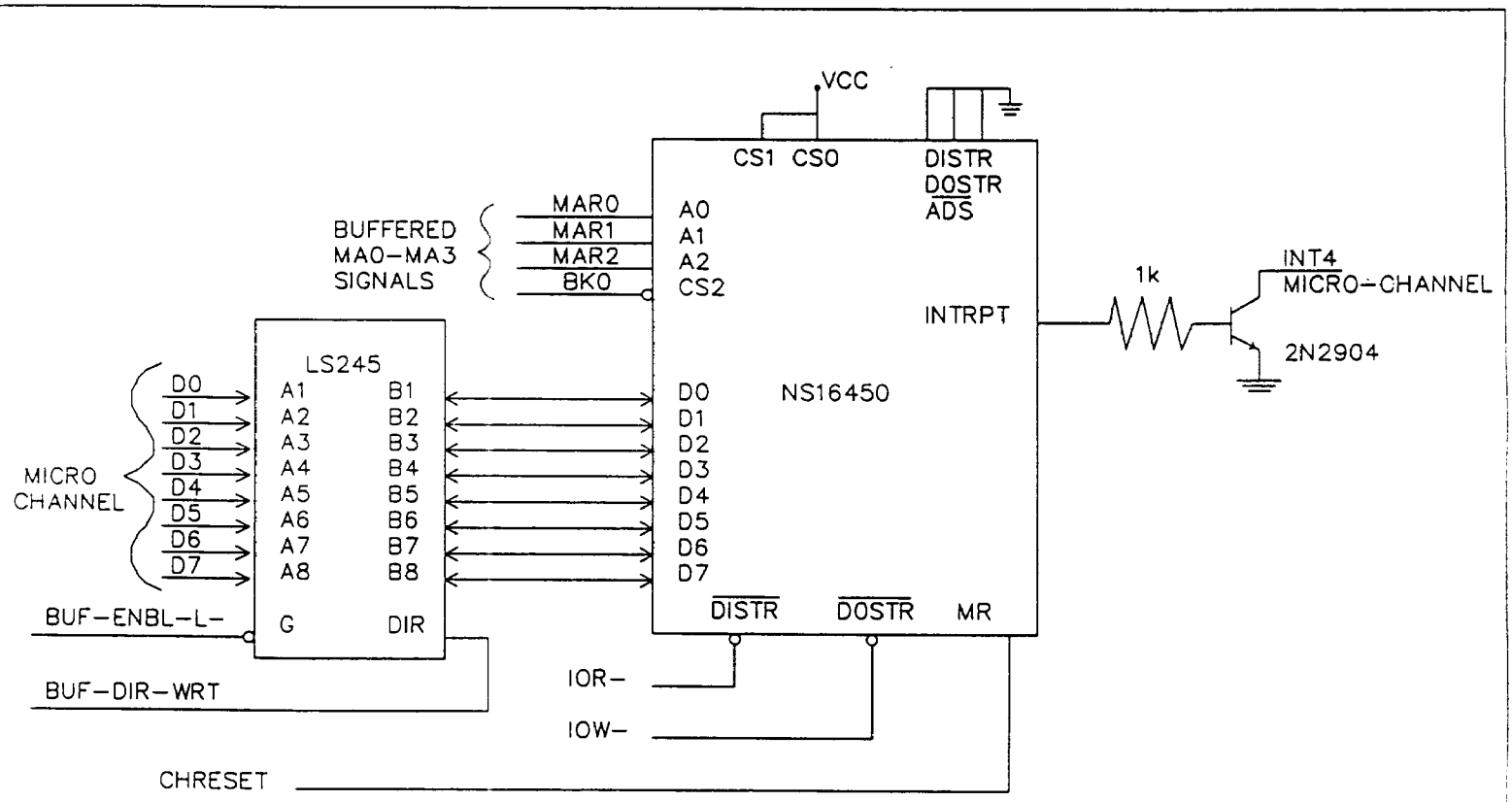


FIGURE 2
UART CONNECTION

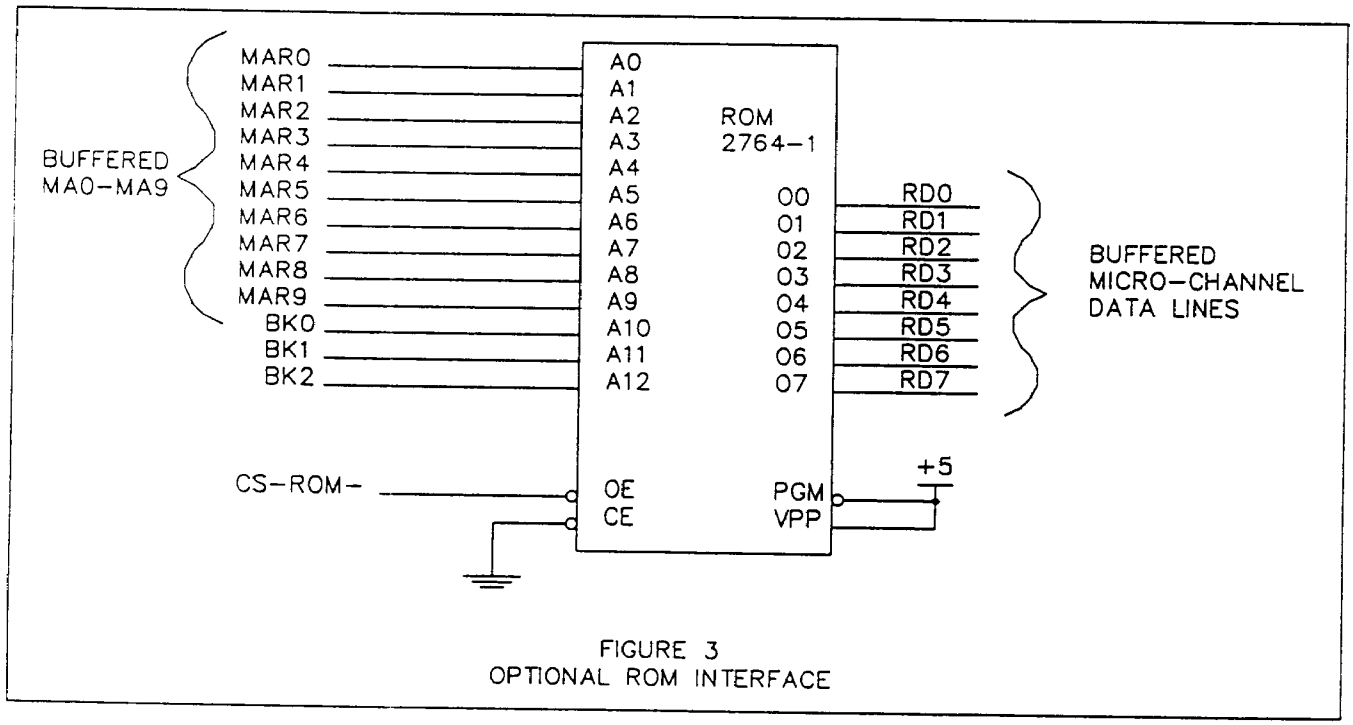


FIGURE 3
OPTIONAL ROM INTERFACE

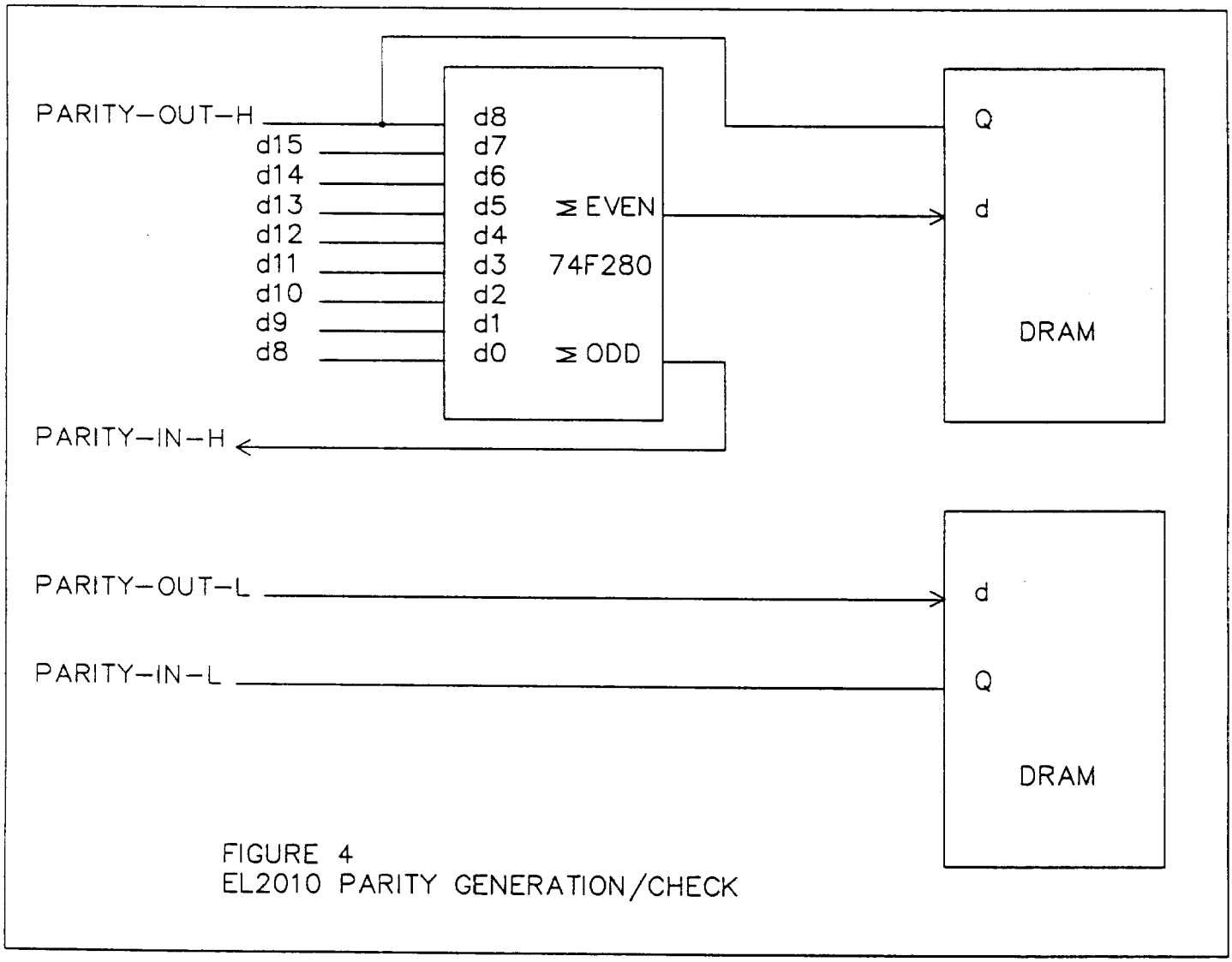


FIGURE 4
EL2010 PARITY GENERATION/CHECK

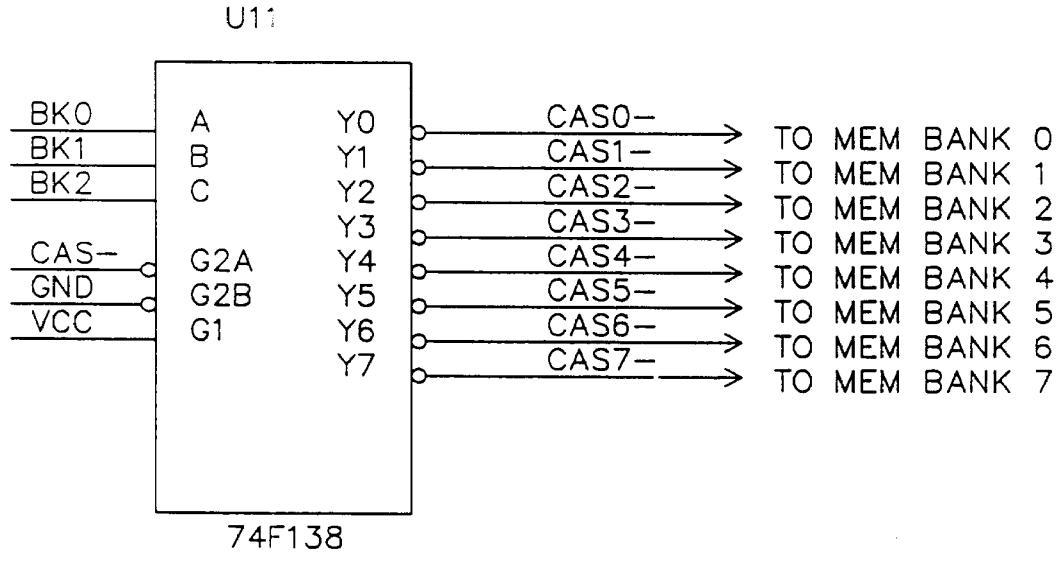


FIGURE 5
GENERATION OF CAS FOR MEMORY BANKS

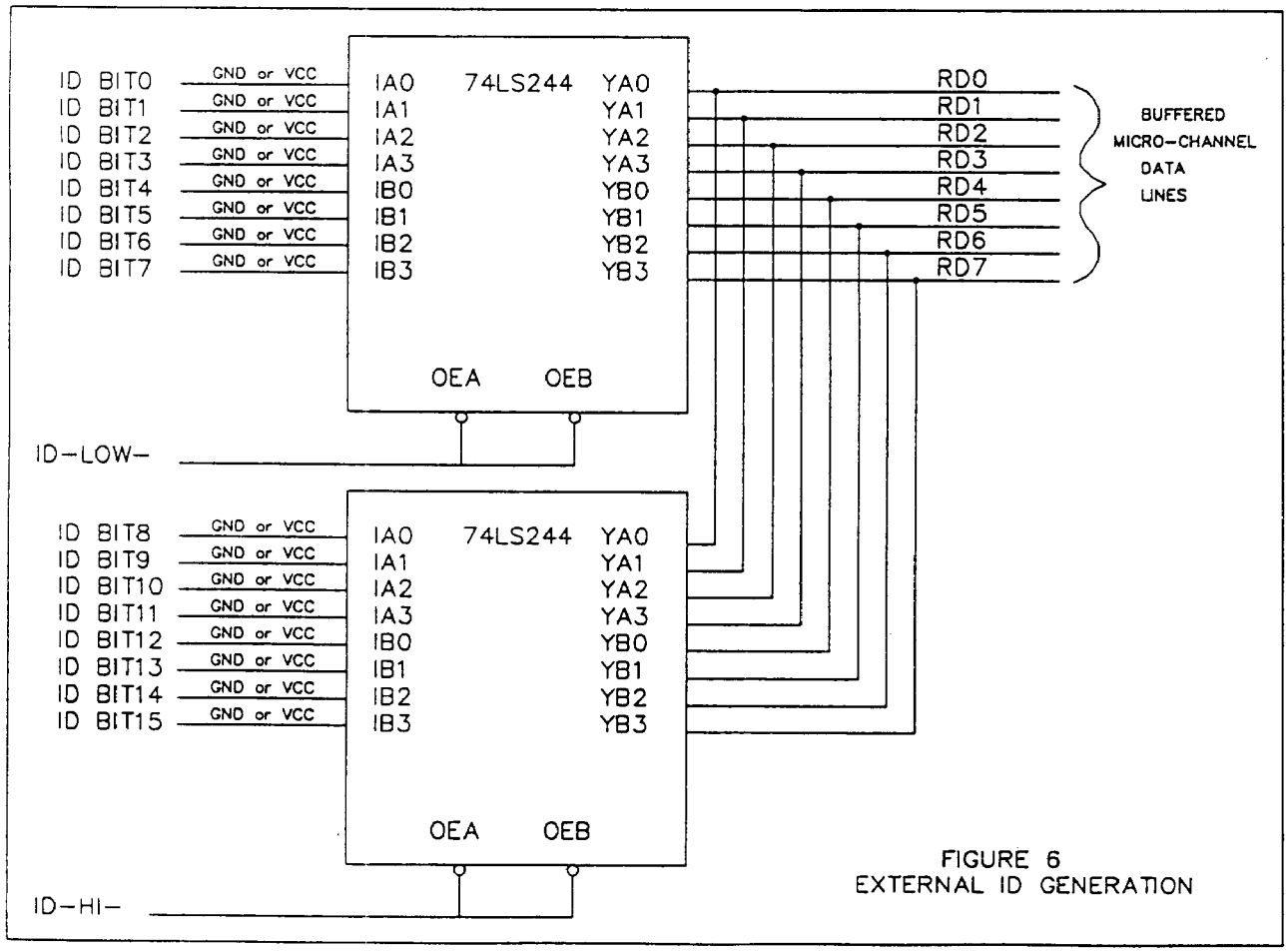
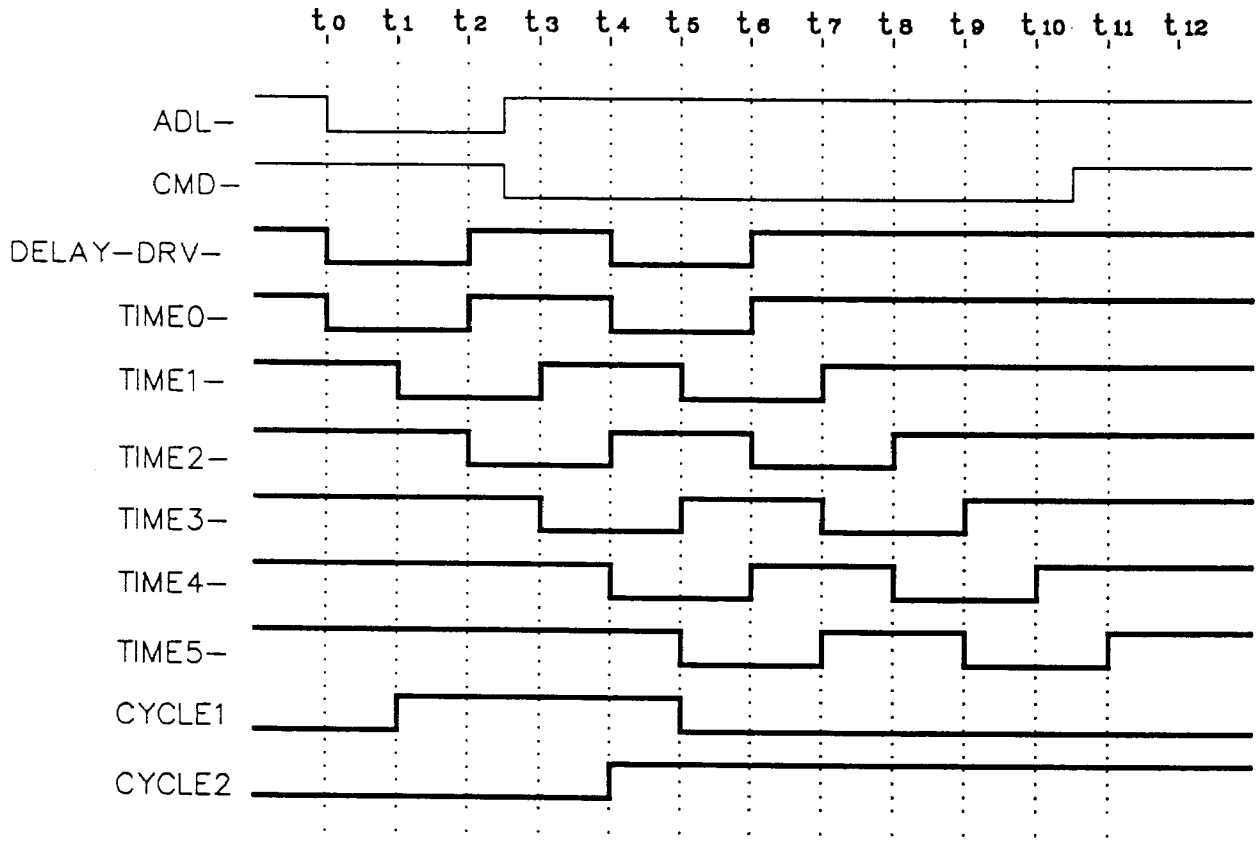
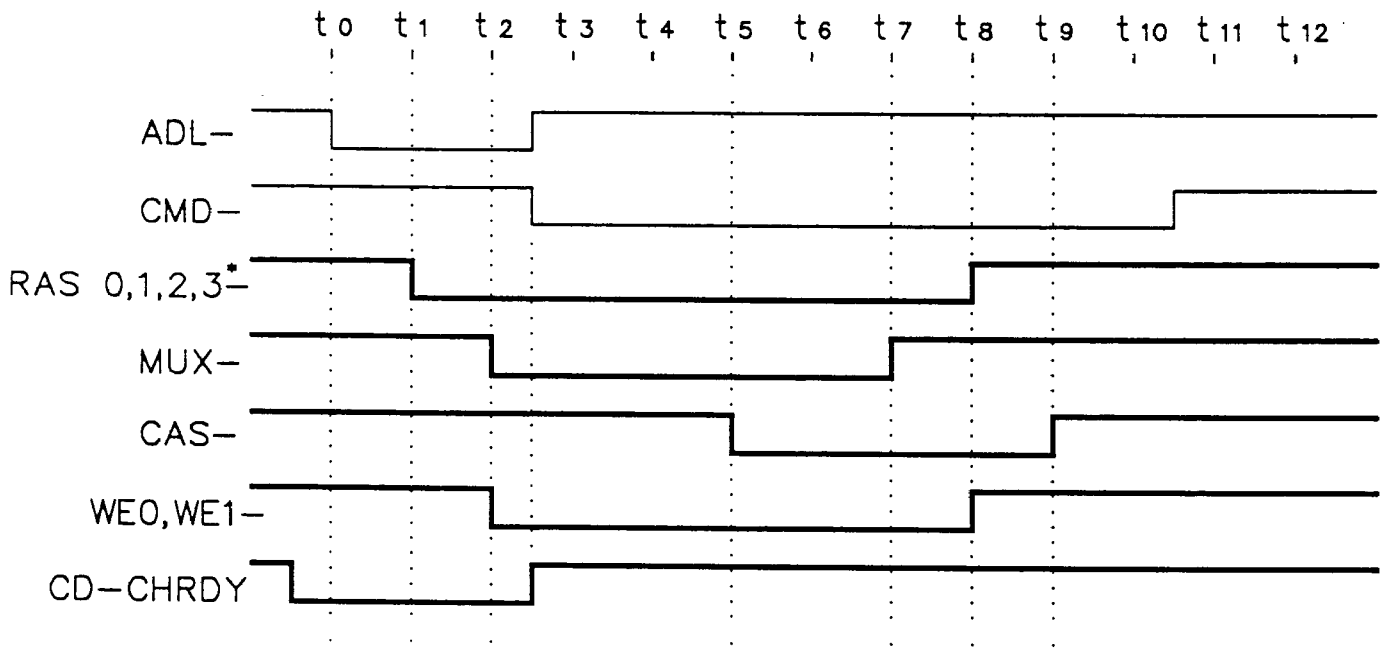


FIGURE 6
EXTERNAL ID GENERATION

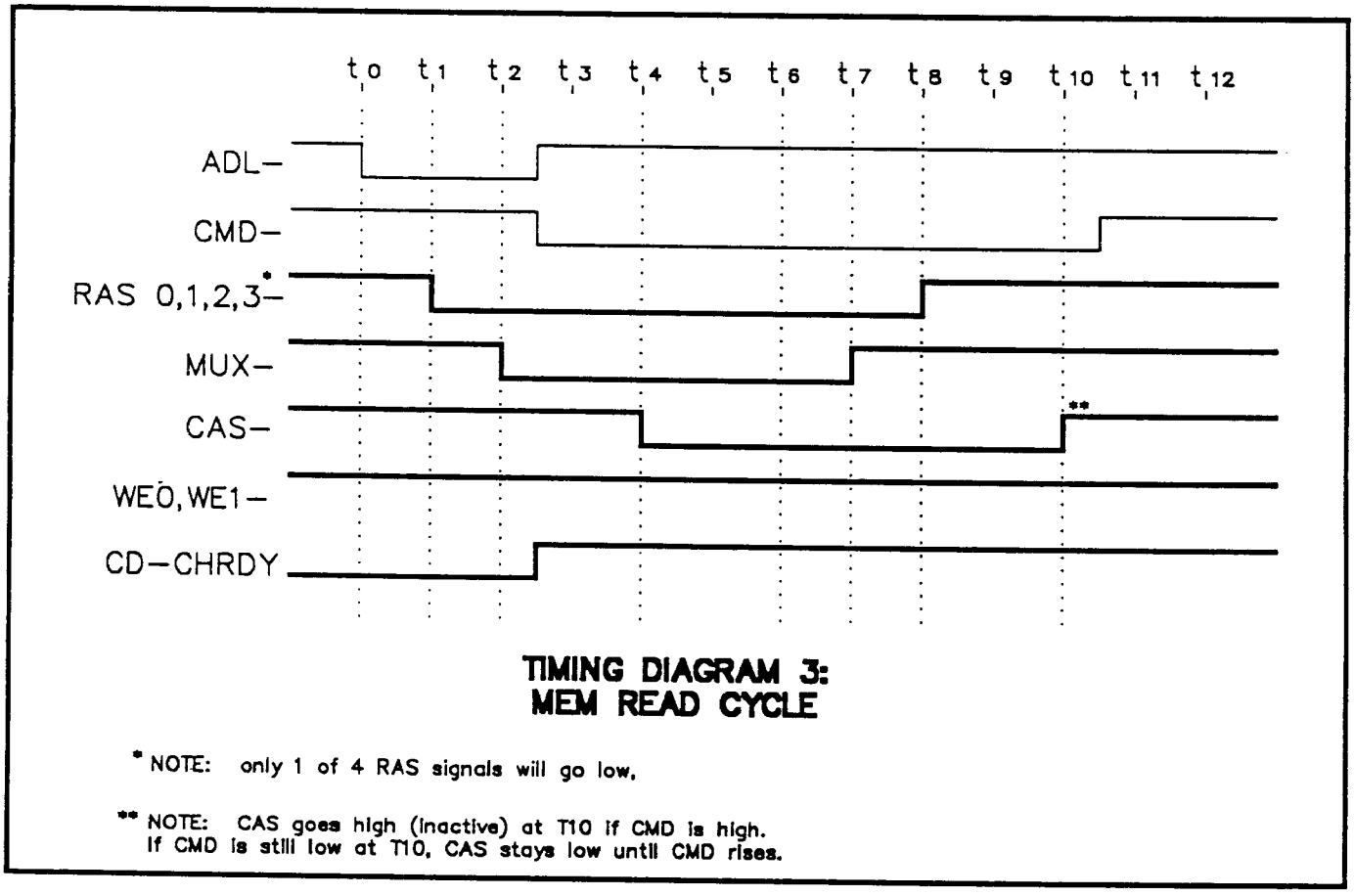


TIMING DIAGRAM 1:
EL2010 MASTER TIMING SEQUENCE



TIMING DIAGRAM 2:
MEM WRITE CYCLE

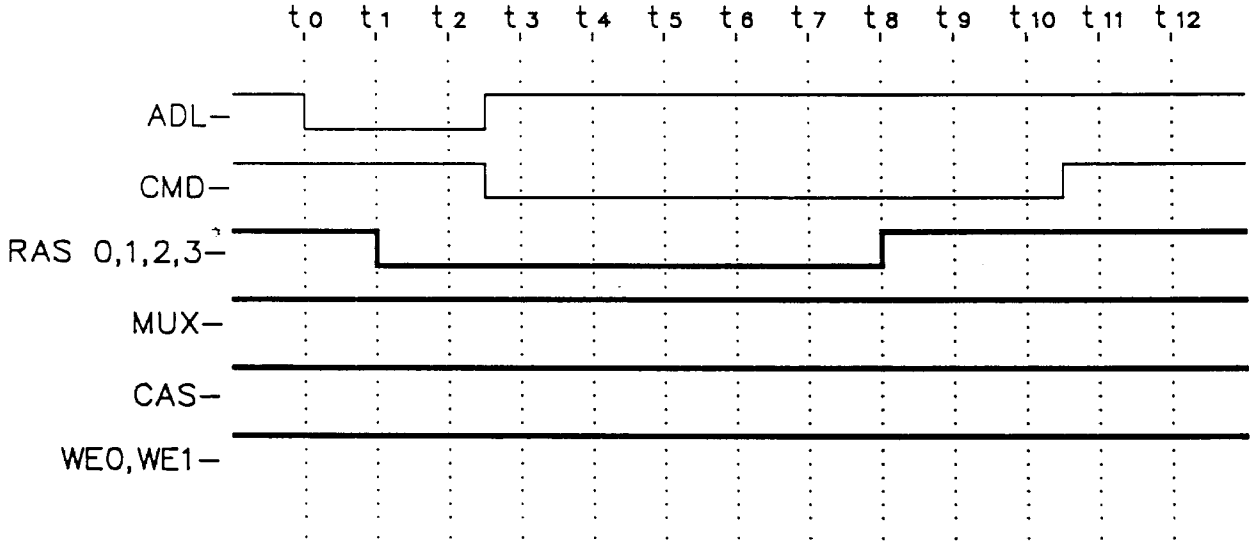
*NOTE: Only 1 of 4 RAS signals will go low.



TIMING DIAGRAM 3:
MEM READ CYCLE

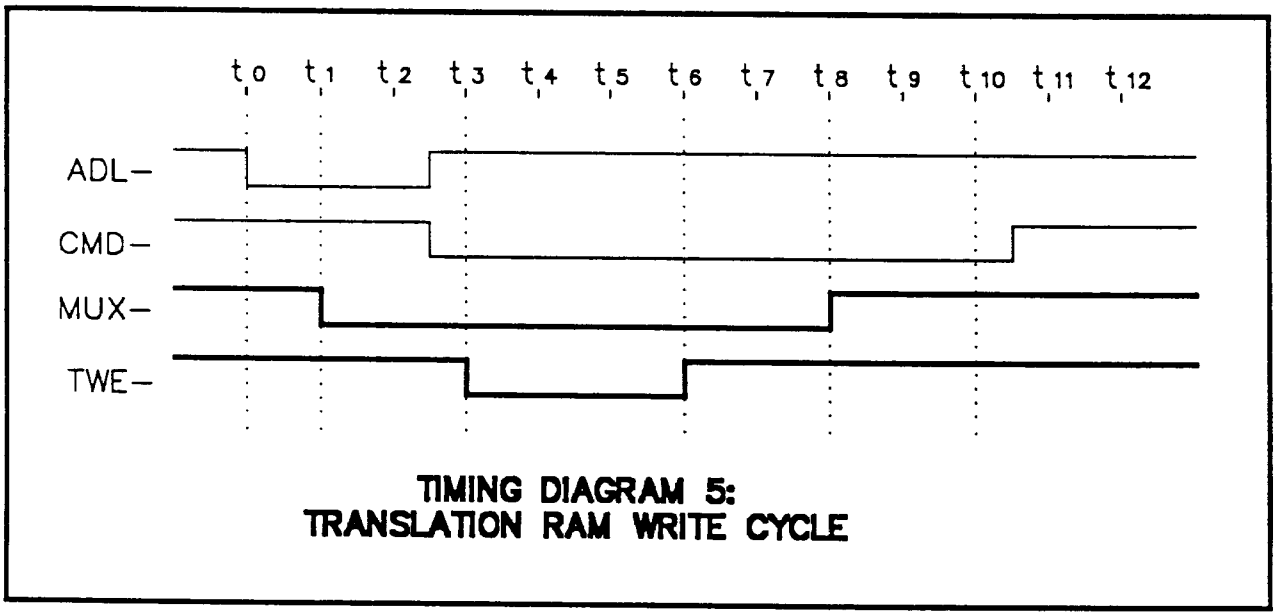
* NOTE: only 1 of 4 RAS signals will go low.

** NOTE: CAS goes high (inactive) at T10 if CMD is high. If CMD is still low at T10, CAS stays low until CMD rises.

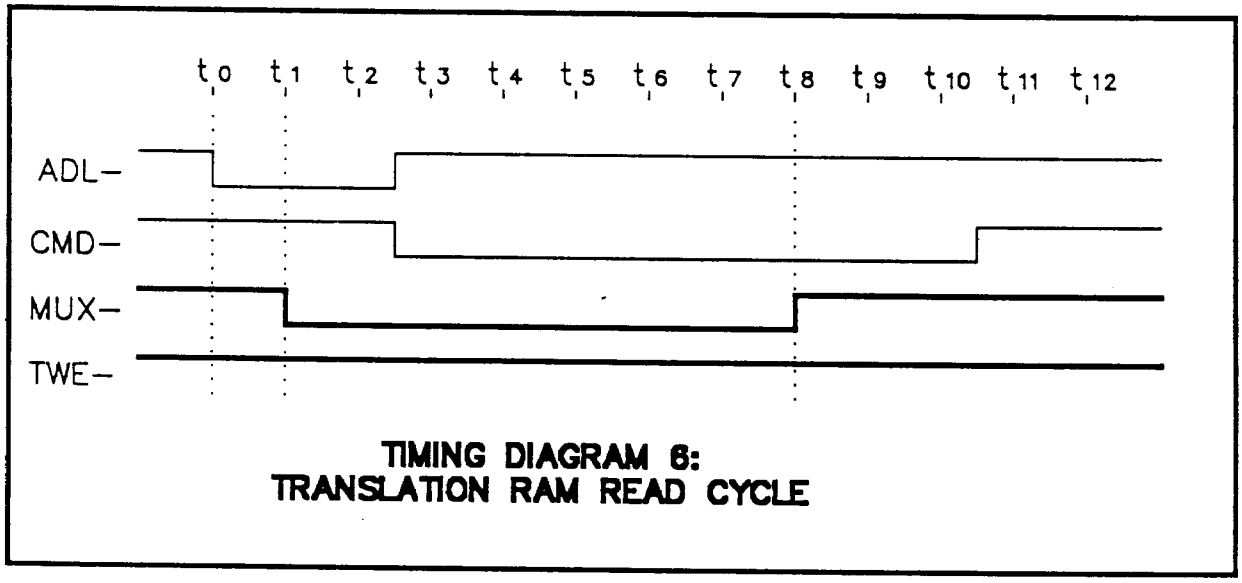


TIMING DIAGRAM 4:
REFRESH CYCLE

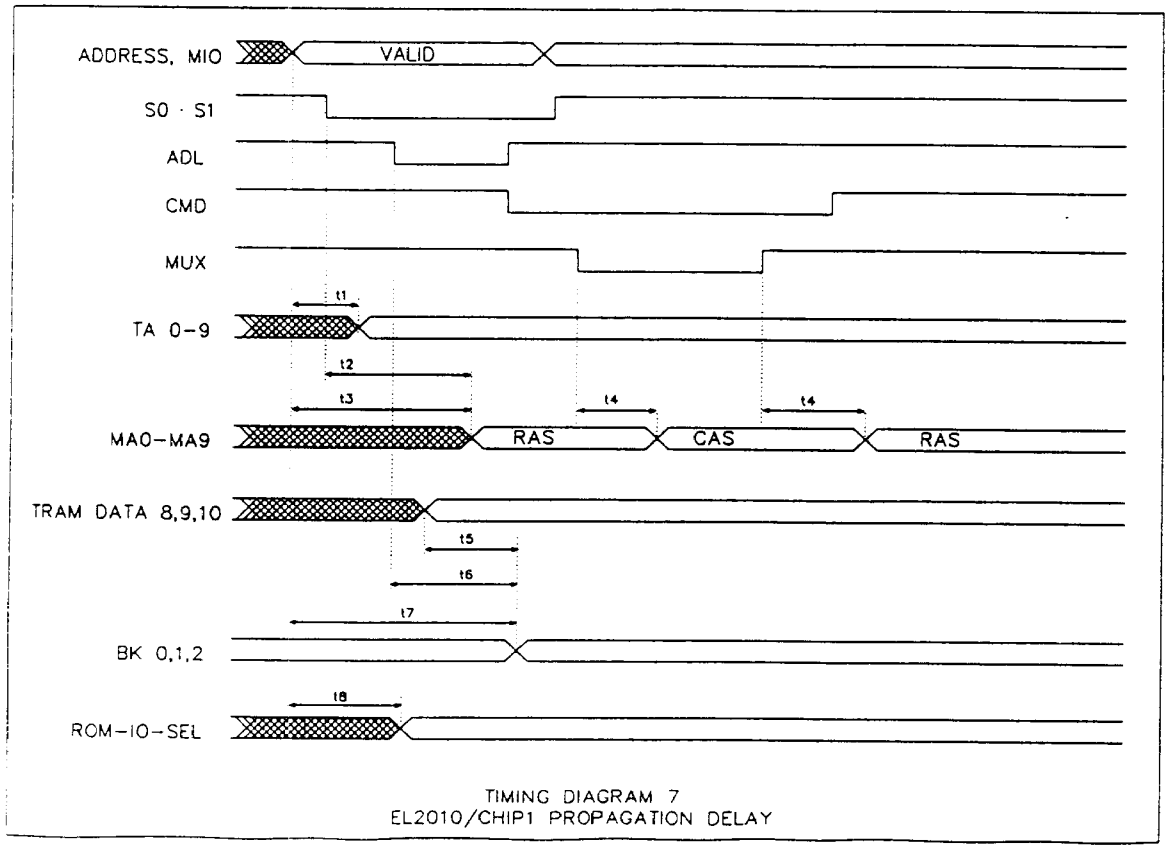
*NOTE: During REFRESH all 4 RAS signals go low.



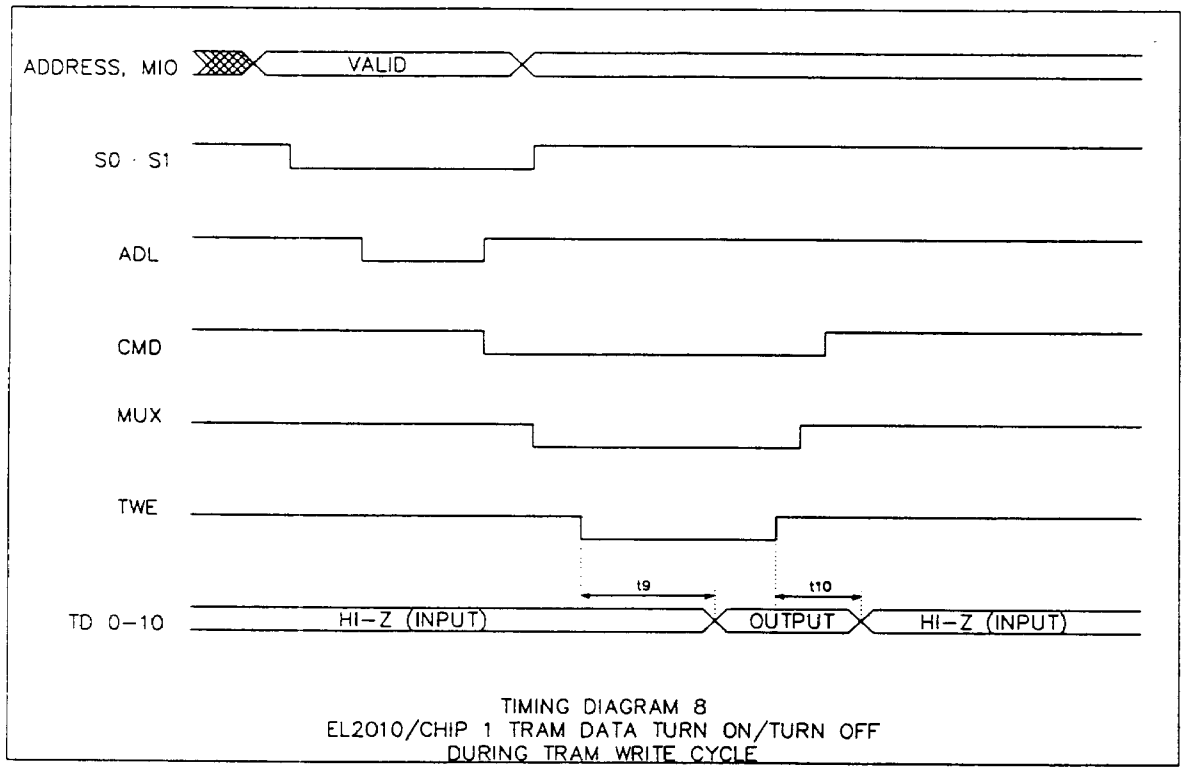
TIMING DIAGRAM 5:
TRANSLATION RAM WRITE CYCLE



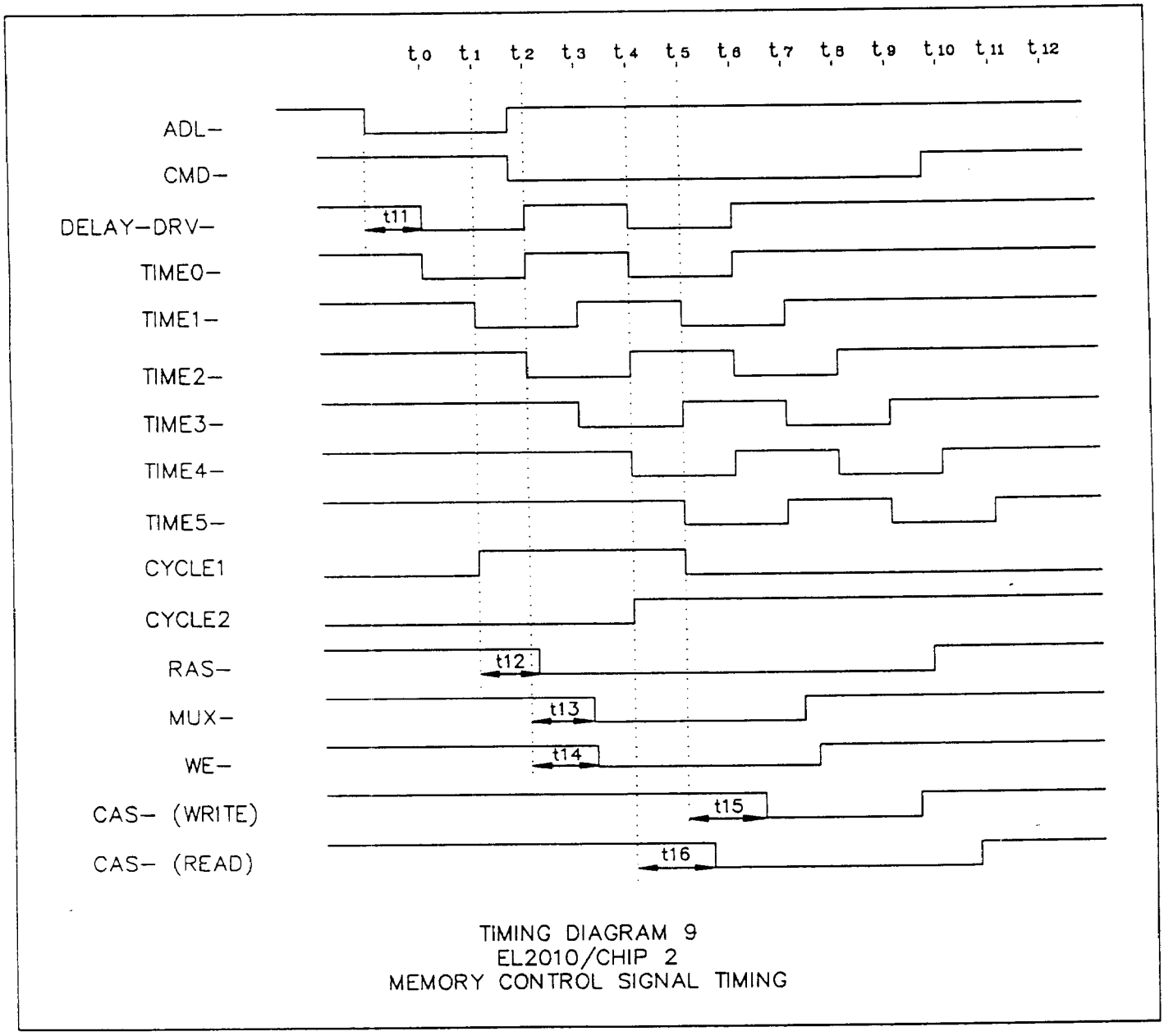
TIMING DIAGRAM 6:
TRANSLATION RAM READ CYCLE



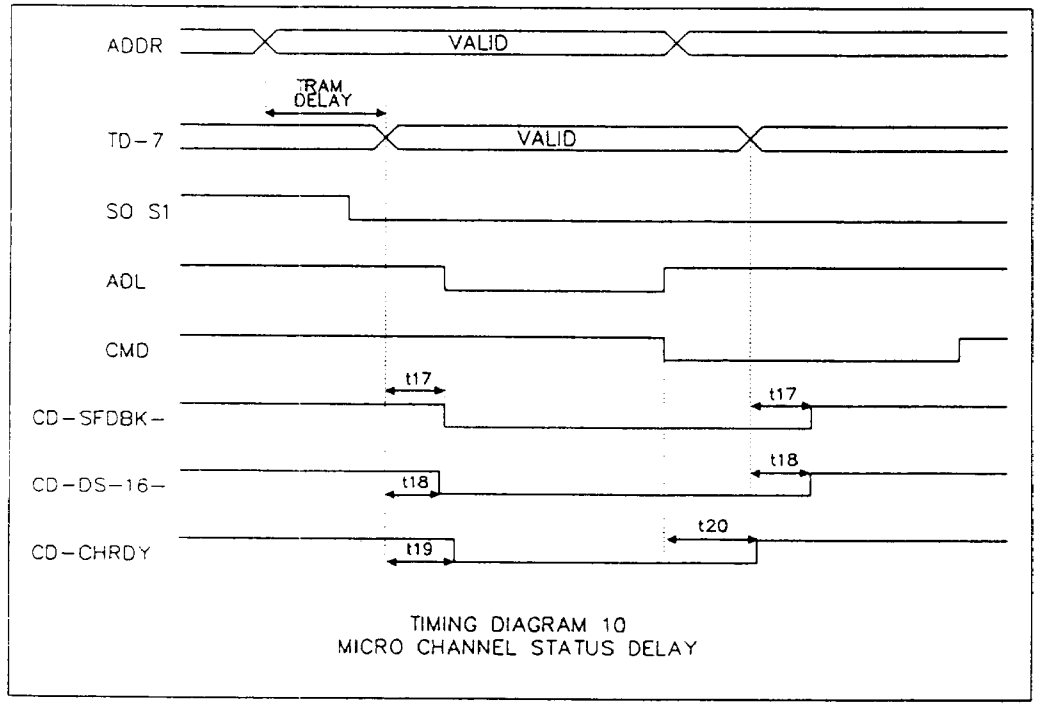
TIMING DIAGRAM 7
EL2010/CHIP1 PROPAGATION DELAY



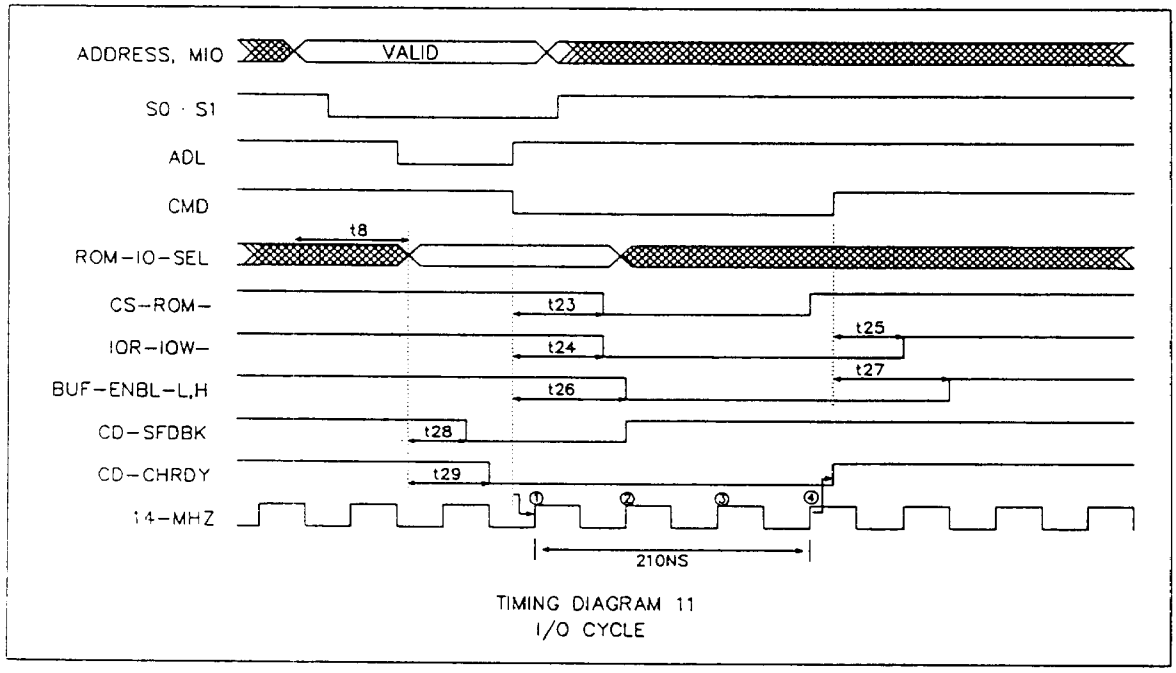
TIMING DIAGRAM 8
EL2010/CHIP 1 TRAM DATA TURN ON/TURN OFF
DURING TRAM WRITE CYCLE



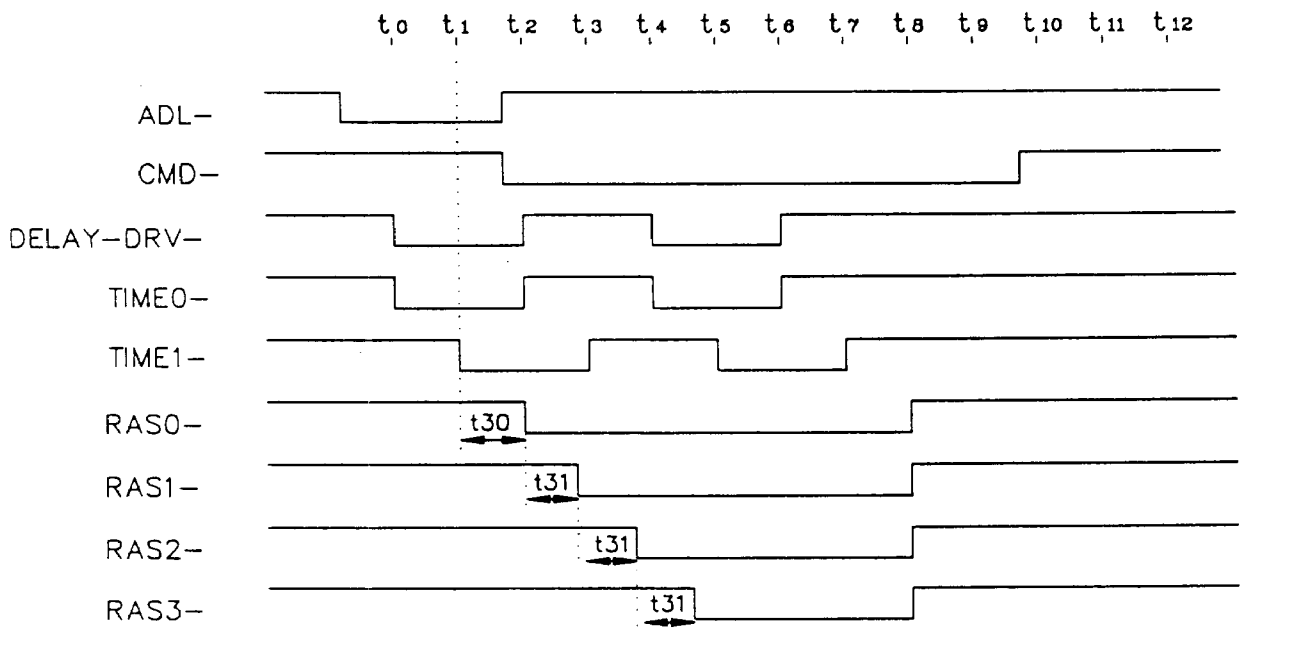
TIMING DIAGRAM 9
EL2010/CHIP 2
MEMORY CONTROL SIGNAL TIMING



TIMING DIAGRAM 10
MICRO CHANNEL STATUS DELAY



TIMING DIAGRAM 11
I/O CYCLE



TIMING DIAGRAM 12
CHIP 2 REFRESH TIMING CYCLE

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