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EMULEX MICRO DEVICES
FAST ARCHITECTURE SCSI CHIP
FAS216/226/236 *

FEATURES

- ❑ For Host Applications and 16-bit Peripheral Applications
- ❑ Supports ANSI X3T9.2 SCSI Standard, with SCSI-2 Fast Timing Requirements
- ❑ Asynchronous Data Transfer up to 7 MB/sec
- ❑ Synchronous Data Transfers up to 5 MB/sec and 10 MB/sec FAST
  - – Programmable Synchronous Transfer Period
  - – Programmable Synchronous Transfer Offsets up to 15 Bytes
- ❑ 24-Bit Transfer Counter
- ❑ Functions as Initiator or Target
- ❑ Up to 20 MB/sec DMA Burst Transfer Rate (10 Megatransfers Per Second)
- ❑ Pipelined Command Structure
- ❑ 16 Byte Data FIFO Between the DMA and SCSI Channels
- ❑ Implements SCSI Sequences without Microprocessor Intervention
- ❑ Parity Pass-Through on FIFO Data
- ❑ Part Unique ID Code
- ❑ On-Chip 48 mA Single-Ended SCSI Transceivers
- ❑ Interrupts Microprocessor Only When Service is Required
- ❑ Packaging
  - – 216 - 84 PLCC
  - – 226 - 84 PLCC
  - – 236 - 100 PQFP

* *FAS216 will refer to FAS226 and FAS236 except as noted*

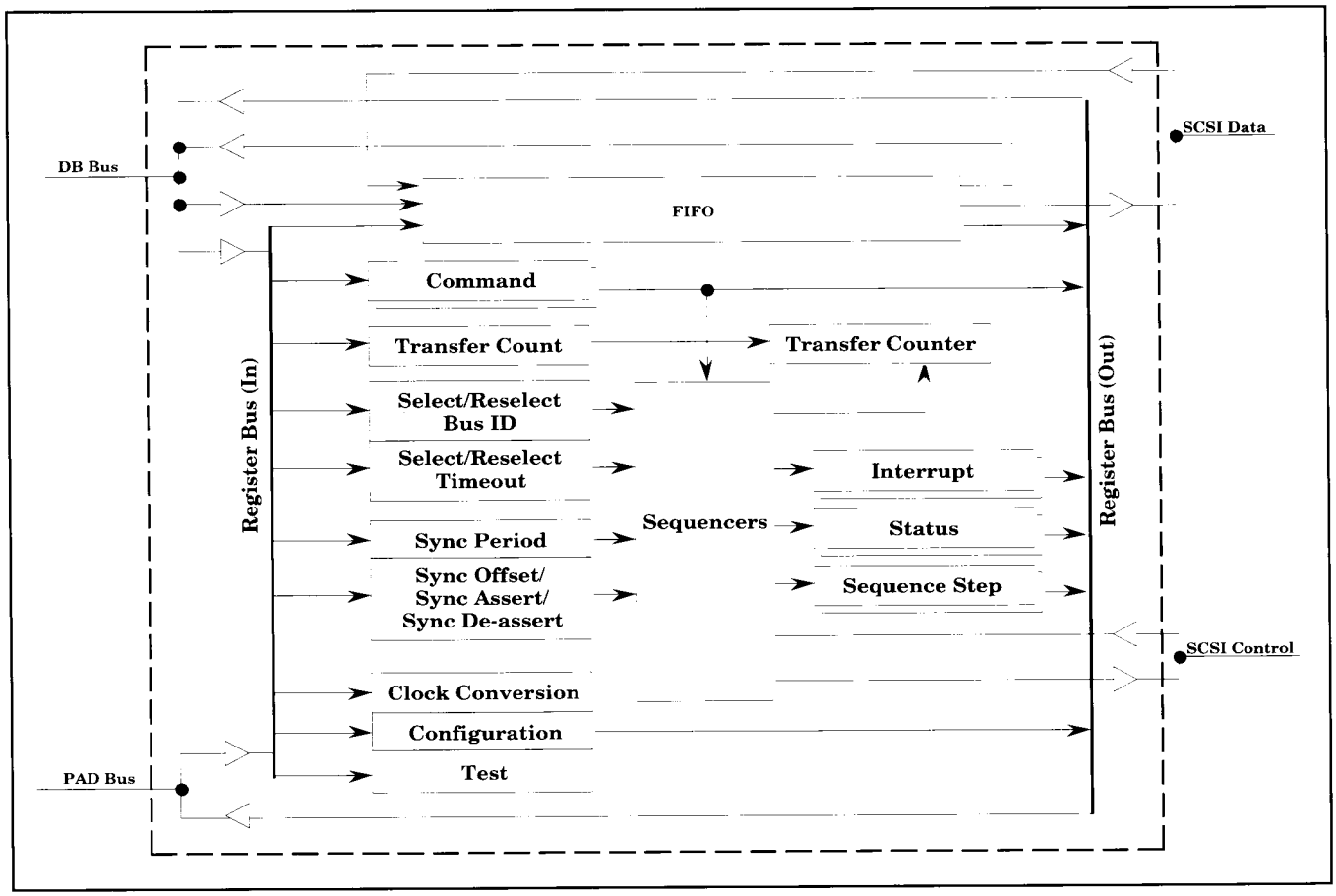


Figure 1. FAS216 Block Diagram Mode 2/3

PRODUCT DESCRIPTION

The FAS216, FAS226, and FAS236 are new additions to the Emulex SCSI Processor (ESP) chip family with features designed to facilitate SCSI-2 support. The major new feature of the FAS chip is its ability to transfer synchronous data at 10 Mbytes per second. The current 5 Mbytes per second transfer rate is also supported on-chip by setting a register. Asynchronous transfers up to 7 Mbytes per second are supported as well.

Of the three versions of the chip, the FAS216 supports single-ended operations; the FAS226 supports differential only; and the FAS236 supports both single-ended and differential operations. Since the FAS216 operates in both the Initiator and Target roles, it can be used in both host and peripheral applications. The chip performs such functions as bus arbitration, selection of a target, or reselection of an initiator. The FAS216 also handles message, command, status, and data transfers between the SCSI Bus and its internal FIFO or a buffer memory.

The chip maximizes protocol efficiency by utilizing a first-in, first-out command pipeline and combination commands to minimize host intervention. The FAS216 also maximizes transfer rates by sustaining asynchronous data rates up to 7 MB/sec and, in the FAST SCSI mode, synchronous data rates up to 10 MB/sec.

The FAS216 controller systems support three main busses: the 8-bit SCSI Bus, the 8-bit or 16-bit Data Bus (DB), and the 8-bit Processor Address (PAD) bus. This versatile split-bus architecture separates the two high traffic information flows of the system, providing maximum efficiency and throughput. Figure 1 shows the internal architecture of the FAS216.

The FAS216 replaces existing SCSI interface circuitry which typically consists of discrete devices, external drivers, and a low performance SCSI interface chip. It contains a fast DMA interface, a 16-byte FIFO, and fast asynchronous and synchronous data interfaces to the SCSI Bus, including drivers.

The FAS216 has been optimized for interaction with the controller processor. Common SCSI bus sequences that would typically require significant amounts of time have been reduced to single commands. The commands are:

Sequence	Description
Selection	Arbitration, target selection, transmission of optional 1- or 3-byte message followed by multiple-byte command
Reselection	Arbitration, initiator reselection, and transmission of a 1-byte message
Bus-initiated Selection	Transmission of selection bus ID, a 1-byte Identify or null message, a 2-byte Queue Tag Message (if SCSI-2 mode), followed by Command Phase bytes.
Bus-initiated Reselection	Reselection detection and receipt of a 1-byte message.
Target Command Complete	Transmission of a status byte and a 1-byte message.
Target Disconnect Sequence	Transmission of two 1-byte messages followed by disconnection from the SCSI bus
Initiator Command Complete	Receipt of a status byte and a 1-byte message

SYSTEM ORGANIZATION

The FAS216 chip provides the host with a complete SCSI interface. An 8-bit microprocessor bus (PAD) provides access to all internal registers and an 18-bit DMA bus (DB) provides a path for DMA transfers through the FIFO.

The versatile architecture supports various microprocessor and DMA bus configurations such as the following:

- Microprocessor interface via the PAD bus or the DB bus
- PAD bus selectable as data-only bus or as a multiplexed address and data bus
- DB bus selectable for 8-bit transfers, 16-bit transfers with byte control

FAS216 bus configuration is selected by pulling the MODE1 and MODE0 signals up or down, as shown in Table 1.

Mode No.	Mode 1	Mode 0	Register Addr	Register Data	Register
0	0	0	A3-0	DB Bus	Single-bus, 8-bit DMA
1	0	1	A3-0	DB Bus	Single-bus, 16-bit DMA
2	1	0	PAD3-0	PAD Bus	Split-bus, 16-bit DMA, byte control option
3	1	1	PAD3-0	PAD Bus	Split-bus, 16-bit DMA

Table 1. Bus Configuration

PROCESSOR INTERFACE

The processor can interface to the FAS216 using either the PAD bus or the DB bus. Both interfaces allow the processor to read and write to all chip registers, including the FIFO. The PAD bus allows the processor interface to the chip registers independent of DMA activity on the DB bus. All register accesses are 8-bits wide.

DMA INTERFACE

The FAS216 DMA logic transfers data to and from a buffer over the DB bus, which may be configured as either 8-bit or 16-bit.* If byte control mode is enabled, an external DMA controller can control how the bytes are placed on the bus.

* *Each byte on the bus has its own parity.*

SIGNALS

The FAS216 acts as the interface between the microprocessor and the SCSI Bus, in either the target or initiator mode. Refer to Figure 2 (FAS216/226 Functional Signal Grouping) and Figure 3 (FAS236 Functional Signal Grouping) which show which pins interface with the microprocessor and which interface with the SCSI Bus.

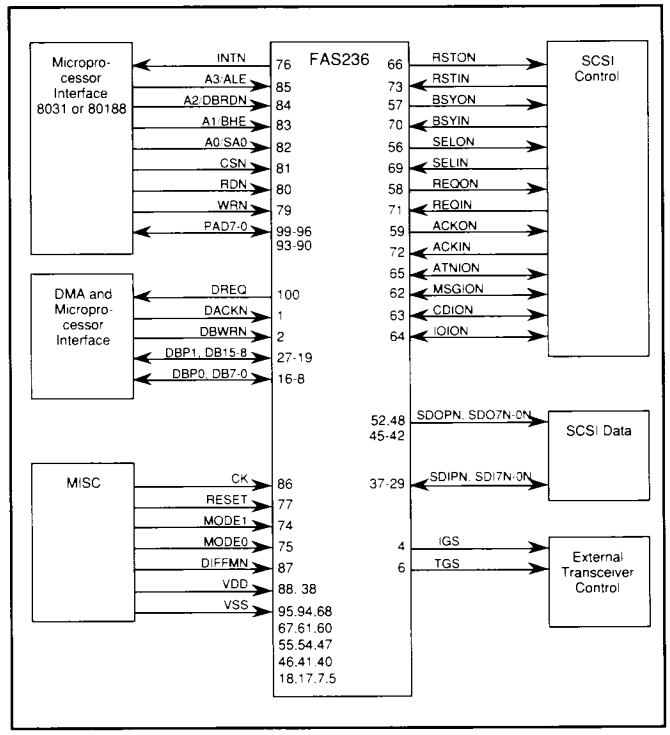


Figure 2. FAS236 Functional Signal Grouping

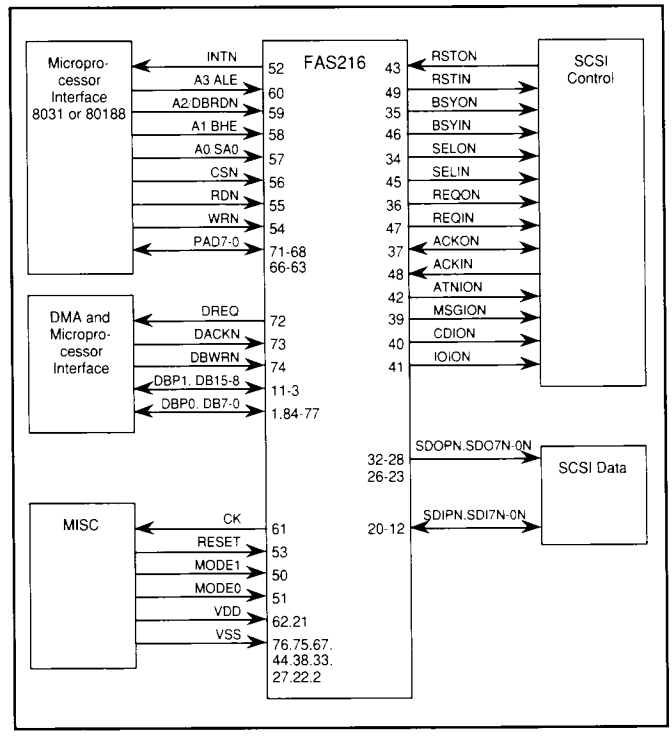


Figure 3. FAS216/226 Functional Signal Grouping

PACKAGING

The FAS216 and FAS226 chips are available in an 84-pin PLCC for surface or socket mounting. The FAS236 is available in a 100-pin plastic quad flat pack (PQFP).

PIN DESCRIPTION

Figure 4 shows the signal names with each pin of the FAS216/226 84-pin PLCC. The diagram is viewed from the top of the chip, with the pins facing away from the reader. The pins for the FAS216 and 226 are identical, with the exception of pins 75 and 76. Pins 75 and 76 in FAS216 are VSS; in the FAS226, pin 75 is IGS and pin 76 is TGS.

Figure 5 shows the signal name associated with each pin of the FAS236 100-pin PQFP. The diagram is viewed from the top of the chip, with the pins facing away from the reader.

REGISTERS

The FAS216 registers are used by the microprocessor to control the operation of the SCSI bus. Through these registers, the microprocessor can configure, command, monitor, and pass through the chip to the SCSI bus. These registers are listed in Table 2.

FAS216 FEATURES/BENEFITS

Features:	Benefits:
❑ Low SCSI Bus overhead	❑ Allows sharing of the SCSI Bus with more peripherals, more efficient bus utilization, fast delivery of information to host
❑ Fast synchronous SCSI data transfers (10 MB/sec)	❑ Can transfer data twice as fast as normal SCSI
❑ SCSI-2 command support	❑ Allows the option of utilizing new SCSI commands
❑ SCSI-2 feature selectability	❑ Backward-compatible with existing chips, so SCSI-2 features can be selected when necessary
❑ Parity pass-through	❑ Maintains data integrity all the way through the chip directly into the buffer
❑ Separate microprocessor and DMA busses	❑ During data transfer, the microprocessor has instant access to status and has the ability to execute commands
❑ 16-bit DMA Channel	❑ High-speed information flow can be handled with the split-bus architecture to provide maximum efficiency and throughput

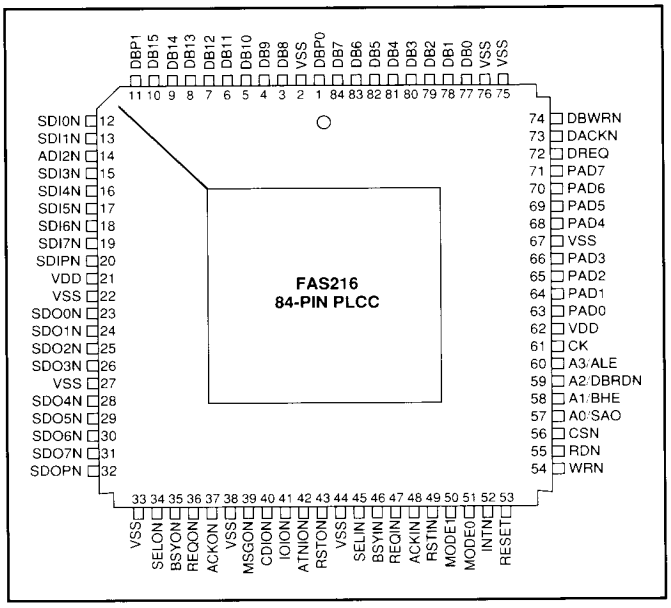


Figure 4. FAS216 84-Pin PLCC Designations

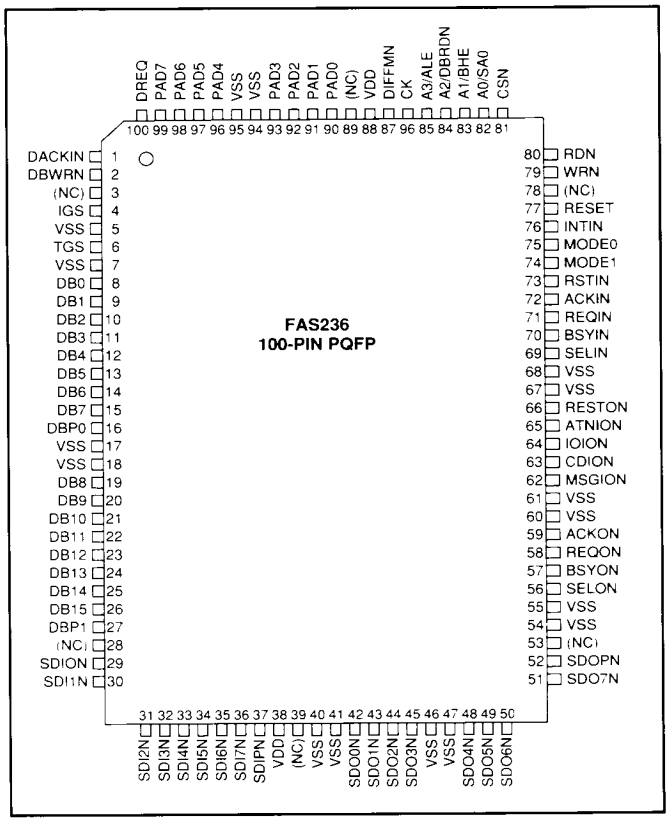


Figure 5. FAS236 100-Pin PQFP Designations

FAS216 Address (BFxx or FExx)	Register Name	Type	FAS216 Address (BFxx or FExx)	Register Name	Type
00	Transfer Counter Low	R	07	FIFO Flags	R
	Transfer Count Low	W		Synchronous Offset	W
01	Transfer Counter Mid	R	08	Configuration #1	R/W
	Transfer Count Mid	W	09	Clock Conversion	W
02	FIFO	R/W		Factor	
03	Command	R/W	0A	Test	W
04	Status	R	0B	Configuration #2	R/W
	Select/Reselect Bus ID	W	0C	Configuration #3	R/W
05	Interrupt	R	0E	Transfer Counter High	R
	Select/Reselect Timeout	W		Transfer Count High	W
06	Sequence Step	R	0F	FIFO Bottom	W
	Synch Transfer Period	W			

Table 2. FAS216 Registers

AC TIMING

The following figures and table values that accompany them are illustrative of the FAS216 chip timing characteristics. For more information, see the *FAS216/226/236 Technical Manual*, VLSI51007-00 .

Register Interface Timing (In ns)

#	Symbol	Description	Min	Max	Note
1	^{T}RASC	Address Setup to CSN	0		1
2	^{T}RAHC	Address Hold from CSN	30		1
3	^{T}RALSA	Address Setup to ALE	10		2
4	^{T}RALHA	Address Hold from ALE	10		2
5	^{T}RALD	ALE Pulse Width	20		2
6	^{T}RALSC	ALE to CSN	10		2
7	^{T}RALHC	ALE from CSN	50		2
8	^{T}RCCY	CSN High to CSN Low	30		

Read Cycle

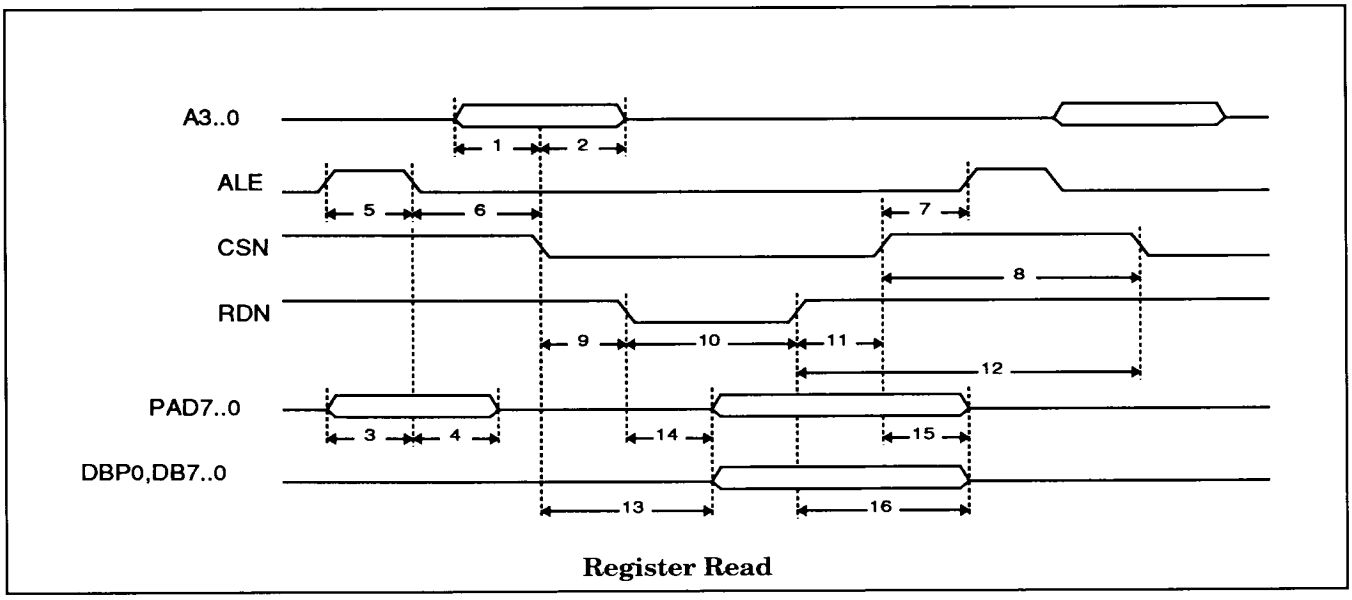
#	Symbol	Description	Min	Max	Note
9	^{T}RCSR	CSN Low to RDN Low	0		
10	^{T}RRD	RDN Pulse Width	30		
11	^{T}RCHR1	RDN High to CSN High	0		
12	^{T}RCHR2	RDN High to CSN Low	40		
13	^{T}RDC	CNS Low to Data		65	3
14	^{T}RDR	RDN Low to Data		30	3
15	^{T}RDHC	CSN High to Data Release	2	30	4
16	^{T}RDHR	RDN High to Data Release	2	30	4

Write Cycle

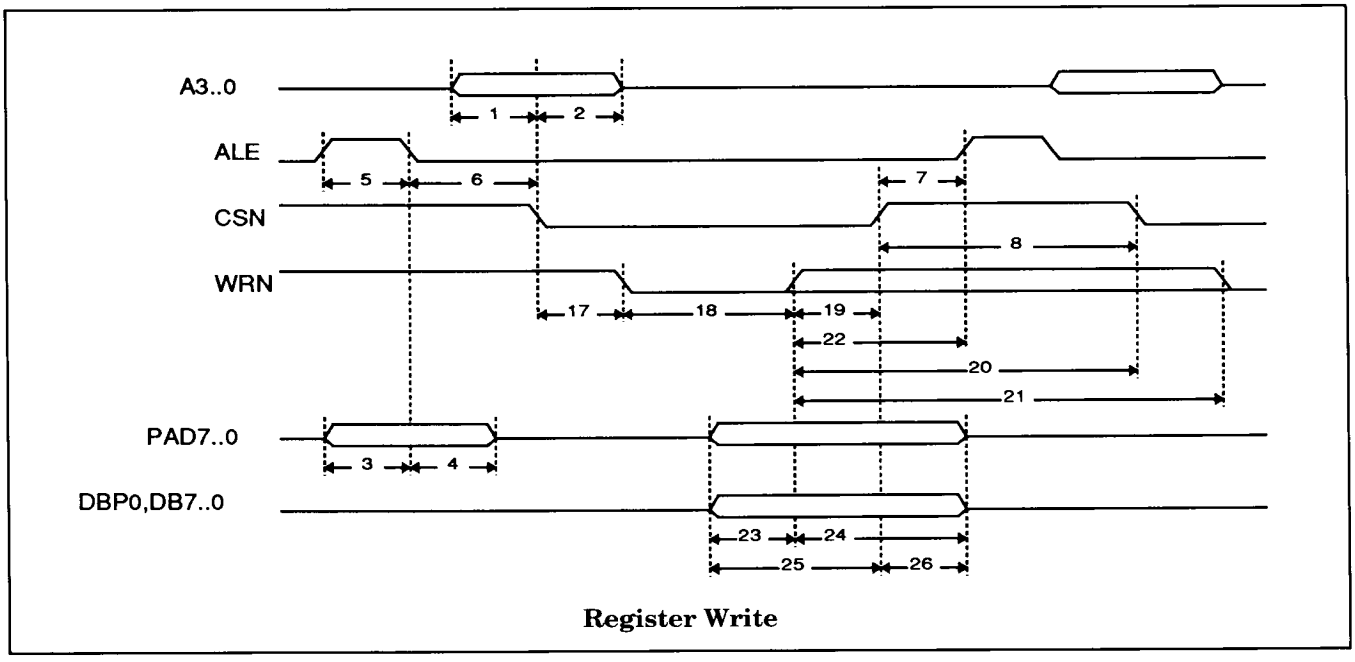
#	Symbol	Description	Min	Max	Note
17	^{T}CSW	CSN Low to WRN Low	0		5,6
18	^{T}RWR	WRN Pulse Width	30		6
19	^{T}RCHW	WRN High to CSN High	0		5,6
20	^{T}RWH	WRN High to CSN Low	30		6
21	^{T}RWCY	WRN High to WRN Low	40		6
22	^{T}RAHW	WRN High to ALE	50		2,6
23	^{T}RDW	Data Setup to WRN High	15		6,7
24	^{T}RDHW	Data Hold from WRN High	0		6,8
25	^{T}RDWC	Data Setup to CSN High	10		7
26	^{T}RDHWC	Data Hold from CSN High	30		8

Notes:

1. Bus Configuration modes #0, #1, and #3 only.
2. Bus configuration mode #2 only (multiplexed address and data mode).
3. Both ^{T}RDC and ^{T}RDR specifications must be met.
4. RDN edges may precede or follow CSN edges.
5. WRN edges may precede or follow CSN edges.
6. In Bus Configuration modes #0 and #1, WRN must be tied to DBWRN.
7. Either ^{T}RDW or ^{T}RDWC specification must met.
8. Either ^{T}RDHW or ^{T}RDHWC specification must met.



Register Read



Register Write

Figure 6. Register Access

DMA Interface Timing (In ns)

#	Symbol	Description	Min	Max	Note
1	^{T}DARL	DACKN Low to DREQ Low		30	1
2	^{T}DRH	DACKN High to DREQ High		30	2
3	^{T}DACY	DACKN High to DACKN Low	12		
4	^{T}ACK	DACKN Pulse Width	45		
5	^{T}ACP0	DACKN Low to DACKN Low	95		
6	^{T}ACP1	DACKN High to DACKN High	^{T}CS +25		12

Read Cycle

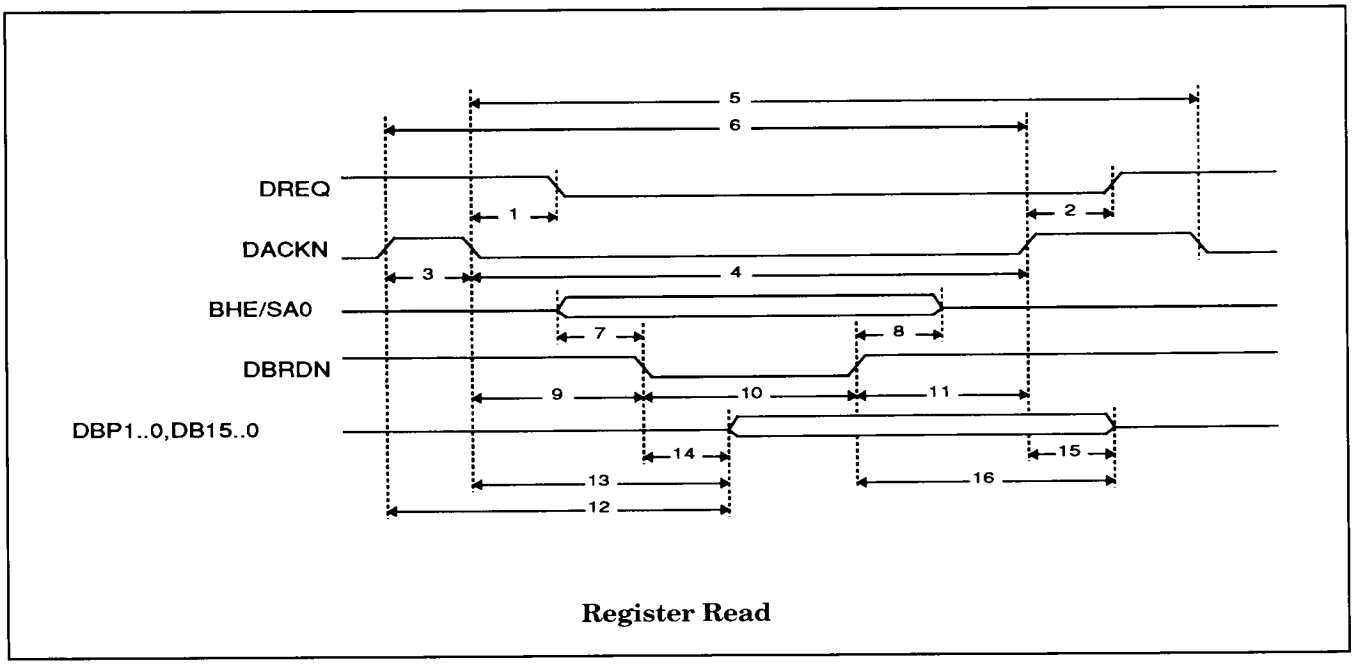
#	Symbol	Description	Min	Max	Note
7	^{T}DBSSR	BHE/SA0 Setup to DBRDN Low	20		3,4
8	^{T}DBSHR	BHE/SA0 Hold from DBRDN High	20		3,4
9	^{T}DAR	DACKN Low to DBRDN Low	0		3,6
10	^{T}DRD	DBRDN Pulse Width	35		3
11	^{T}DRA	DBRDN High to DACKN High	0		3,7
12	^{T}DDAH	DACKN High to Data	45		5
13	^{T}DDAL	DACKN Low to Data	30		5
14	^{T}DDRL	DBRDN Low to Data	35		3,5
15	^{T}DADR	DACKN High to Data Release	2	25	
16	^{T}DRDR	DBRDN High to Data Release	2	35	3

Write Cycle

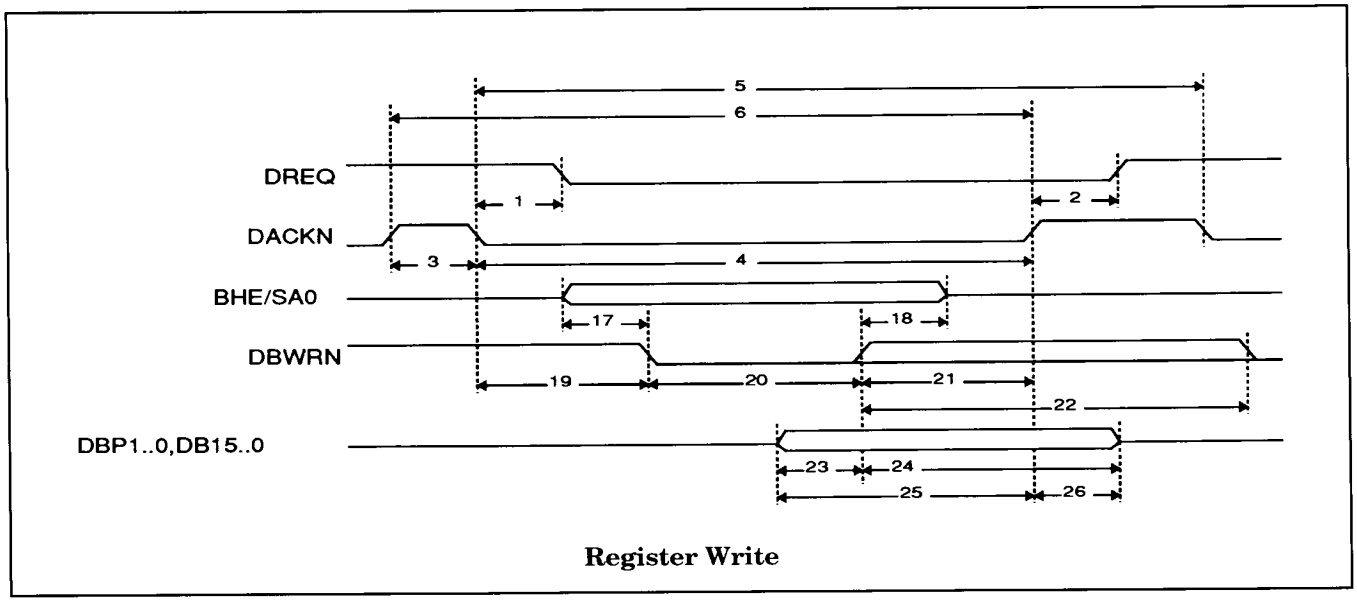
#	Symbol	Description	Min	Max	Note
17	^{T}DBSSW	BHE/SA0 Setup to DBWRN Low	20		3,4
18	^{T}DBSHW	BHE/SA0 Hold from DBWRN High	20		3,4
19	^{T}DAW	DACKN Low to DBWRN Low	0		8
20	^{T}DWR	DBWRN Pulse Width	30		
21	^{T}DWA	DBWRN High to DACKN High	0		9
22	^{T}DWCY	DBWRN High to DBWRN Low	25		
23	^{T}DDW	Data Setup to DBWRN High	15		10
24	^{T}DHW	Data Hold from DBWRN High	0		11
25	^{T}DDWA	Data Setup to DACKN High	10		10
26	^{T}DHWA	Data Hold from DACKN High	10		11

Notes:

1. Negation pending.
2. Assertion pending.
3. Bus configuration mode #2 only.
4. Byte control mode only.
5. ^{T}DDAH and ^{T}DDAL specifications must be met.
6. DBRDN low may precede DACKN low.
7. DBRDN low may follow DACKN high.
8. DBWRN low may precede DACKN low.
9. DBWRN low may follow DACKN high.
10. Either ^{T}DDW or ^{T}DDWA specification must be met.
11. Either ^{T}DHW or ^{T}DHWA specification must be met.
12. Synchronous transfers only.



Register Read



Register Write

Figure 7. DMA Access

Alternate DMA Interface Timing (In ns)

#	Symbol	Description	Min	Max	Note
1	^{T}DARL	DACKN Low to DREQ Low		30	1,10
2	^{T}DRH	DAKCN High to DREQ High		30	2
3	^{T}DACY	DACKN High to DACKN Low	60		
4	^{T}ACK	DACKN Pulse Width	70		

Read Cycle

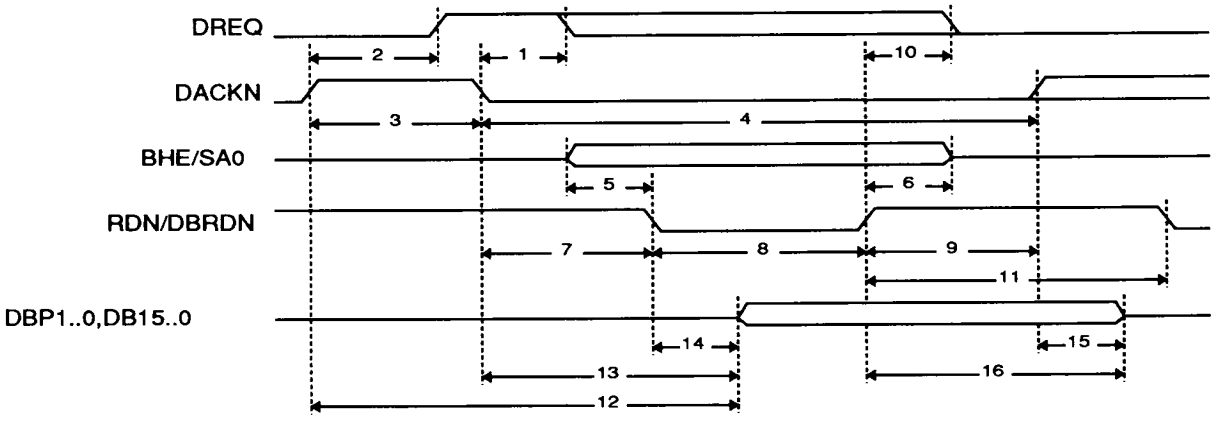
#	Symbol	Description	Min	Max	Note
5	^{T}DBSSR	BHE/SA0 Setup to RDN/DBRDN Low	20		3,4
6	^{T}DBSHR	BHE/SA0 Hold from RDN/DBRDN High	20		3,4
7	^{T}DAR	DACKN Low to RDN/DBRDN Low	0		6,12
8	^{T}DRD	RDN/DBRDN Pulse Width	70		12
9	^{T}DRA	RDN/DBRDN High to DACKN High	0		7,12
10	^{T}DRRL	RDN/DBRDN High to DREQ Low	90		1,11,12
11	^{T}DRACY	RDN/DBRDN High to RDN/DBRDN Low	60		11, 12
12	^{T}DDAH	DACKN High to Data	45		5
13	^{T}DDAL	DACKN Low to Data	35		5
14	^{T}DDRL	RDN/DBRDN Low to Data	55		5,12
15	^{T}DADR	DACKN High to Data Release		25	
16	^{T}DRDR	RDN/DBRDN High to Data Release		45	12

Write Cycle

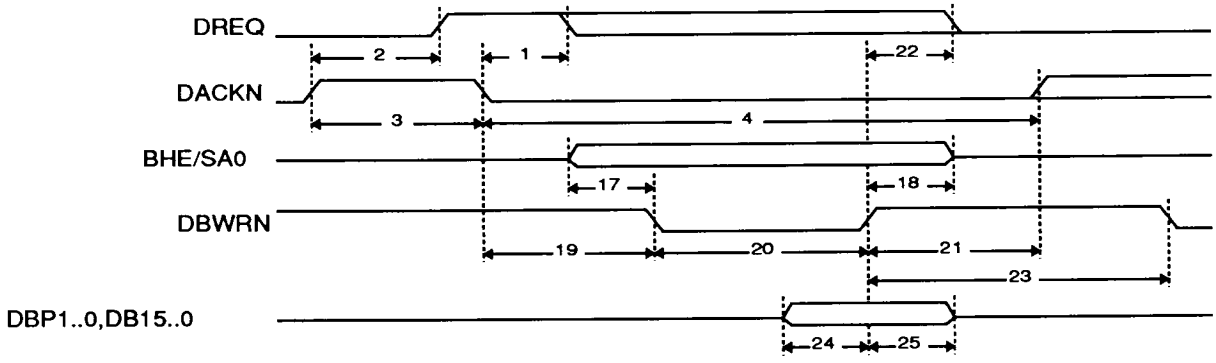
#	Symbol	Description	Min	Max	Note
17	^{T}DBSSW	BHE/SA0 Setup to DBWRN Low	20		3,4
18	^{T}DBSHW	BHE/SA0 Hold from DBWRN High	20		3,4
19	^{T}DAW	DACKN Low to DBWRN Low	0		8
20	^{T}DWR	DBWRN Pulse Width	70		
21	^{T}DWA	DBWRN High to DACKN High	0		9
22	^{T}DWRL	DBWRN High to DREQ Low	90		11
23	^{T}DWCY	DBWRN High to DBWRN Low	60		11
24	^{T}DDW	Data Setup to DBWRN High	15		
25	^{T}DHW	Data Hold from DBWRN High	0		

Notes:

1. Negation pending.
2. Assertion pending.
3. Bus configuration mode #2 only.
4. Byte control mode only.
5. ^{T}DDAH and ^{T}DDAL specifications must be met.
6. RDN/DBRDN low may precede DACKN low.
7. RDN/DBRDN high may follow DACKN high.
8. DBWRN low may precede DACKN low.
9. DBWRN high may follow DACKN high.
10. Single DMA transfers only.
11. Multiple DMA transfers only.
12. The DMA Read line is defined as RDN in Bus Configuration Modes #0 and #1, and as DBRDN in Bus Configuration Mode #2. In Bus Configuration Mode #3 there is no DMA read line, and DACKN must toggle for each DMA read cycle.



Register Read



Register Write

Figure 8. Alternate DMA Access

SCSI Asynchronous Timing

SINGLE-ENDED MODE[1]

#	Symbol	Description	Min	Max	Note
1	T_{AAR01}	ACKINLow to REQON High		50	
2	T_{AAR02}	ACKIN High to REQON Low		45	3,6
3	T_{ARA01}	REQIN High to ACKON High		50	
4	T_{ARA02}	REQIN Low To ACKON Low		50	4,6

Output Cycle

#	Symbol	Description	Min	Max	Note
5	T_{ARDSO}	Data Setup to REQON Low	60		
5	T_{AADSO}	Data Setup to ACKON Low	60		
6	T_{ARHDO}	Data Hold from REQIN High	5		5
6	T_{AAHDO}	Data Hold from ACKIN Low	5		5

DIFFERENTIAL MODE[2]

#	Symbol	Description	Min	Max	Note
1	T_{AAR01}	ACKIN Low to REQON High		30	
2	T_{AAR02}	ACKIN High to REQON Low		30	3,6
3	T_{ARA01}	REQIN High to ACKON High		25	
4	T_{ARA02}	REQIN Low to ACKON Low		30	4,6

Output Cycle

#	Symbol	Description	Min	Max	Note
5	T_{ARDSO}	Data Setup to REQON Low	70		
5	T_{AADSO}	Data Setup to ACKON Low	70		
6	T_{ARHDO}	Data Hold from REQIN High	5		5
6	T_{AAHDO}	Data Hold from ACKIN Low	5		5

Input Cycle

#	Symbol	Description	Min	Max	Note
7	T_{ARDSI}	Data Setup to REQIN Low	0		
7	T_{AADSI}	Data Setup to ACKIN Low	0		
8	T_{ARHDI}	Data Hold from REQIN Low		18	
8	T_{AAHDI}	Data Hold from ACKIN Low		18	

Notes:

1. 200pF loading, data out on lines SDOPN, SDO7N-0N.
2. Data out on lines SDIPN, SDI7N-0N.
3. T_{ARDSO} specification must also be met (output cycle only).
4. T_{AADSO} specification must also be met (output cycle only).
5. FIFO is not empty.
6. FIFO is not full (input cycle only).

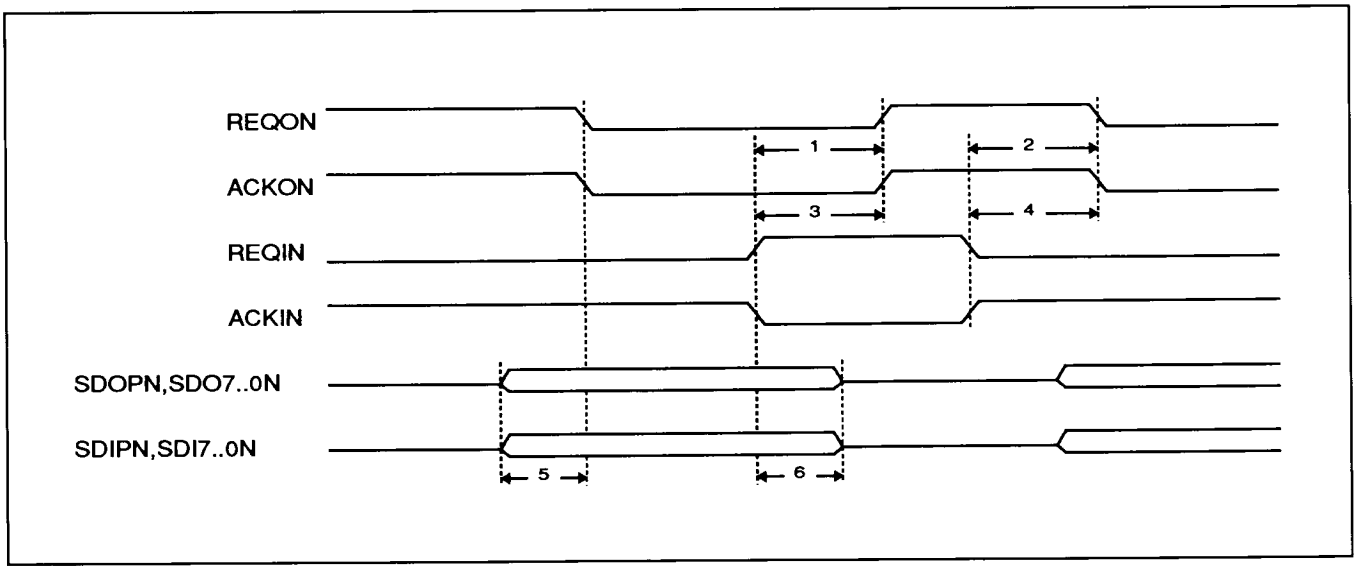


Figure 9. SCSI Asynchronous Timing

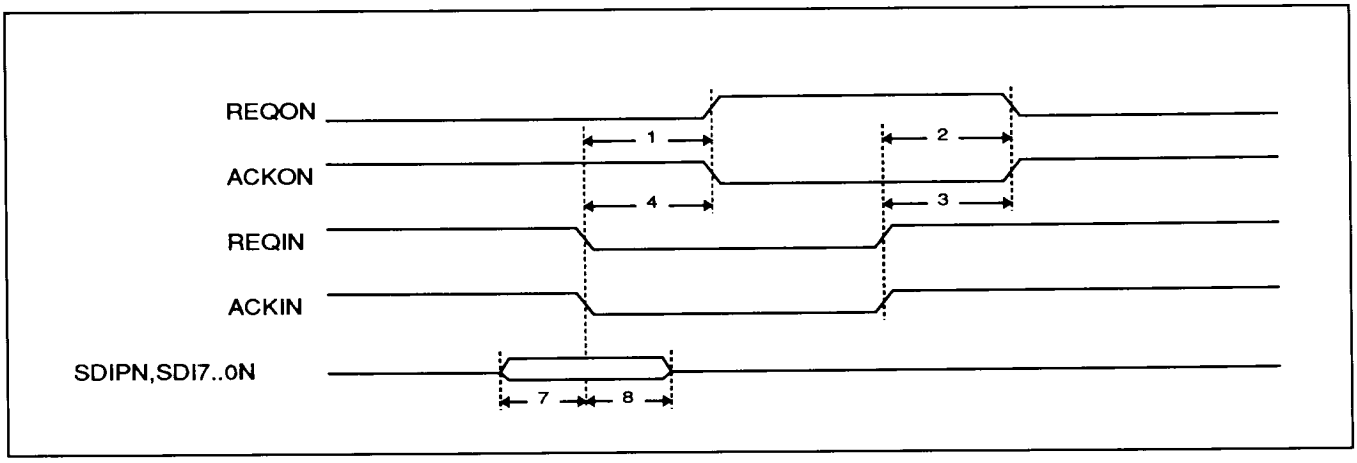


Figure 10. SCSI Asynchronous Input

SCSI Synchronous Timing (In ns)

OUTPUT CYCLE
Normal SCSI, Single-Ended Mode[1]

#	Symbol	Description	Min	Max
1	^{T}SASTO	REQON/ACKON Assertion Period	90	
2	^{T}SNEGO	REQON/ACKON Negation Period	90	
3	^{T}SDSO	Data Setup to REQON Low/ACKON Low	55	
4	^{T}SHIDO	Data Hold from REQON Low/ACKON Low	100	

Normal SCSI, Differential Mode[2]

#	Symbol	Description	Min	Max
1	^{T}SASTO	REQON/ACKON Assertion Period	96	
2	^{T}SNEGO	REQON/ACKON Negation Period	96	
3	^{T}SDSO	Data Setup to REQON Low/ACKON Low	65	
4	^{T}SHDO	Data Hold from REQON Low/ACKON Low	110	

FAST SCSI, Single-Ended Mode[3]

#	Symbol	Description	Min	Max
1	^{T}SASTO	REQON/ACKON Assertion Period	30	
2	^{T}SNEGO	REQON/ACKON Negation Period	30	
3	^{T}SDSO	Data Setup to REQON Low/ACKON Low	25	
4	^{T}SHDO	Data Hold from REQON Low/ACKON Low	35	

FAST SCSI, Differential Mode[4]

#	Symbol	Description	Min	Max
1	^{T}ASTO	REQON/ACKON Assertion Period	40	
2	^{T}SNEGO	REQON/ACKON Negation Period	40	
3	^{T}SDSO	Data Setup to REQON Low/ACKON Low	35	
4	^{T}SHDO	Data Hold from REQON Low/ACKON Low	45	

INPUT CYCLE

#	Symbol	Description	Min	Max
5	^{T}SRASTI	REQIN Assertion Period	27	
6	^{T}SRNEGI	REQIN Negation Period	20	
7	^{T}SAASTI	ACKIN Assertion Period	20	
8	^{T}SANEGI	ACKIN Negation Period	20	
9	^{T}SDSI	Data Setup to REQIN Low/ACKIN Low	5	
10	^{T}SHDI	Data Hold from REQIN Low/ACKIN Low	15	

Notes:

1. 5MBytes/sec max., data out on lines SDOPN, SDO7N-0N
2. 5MBytes/sec max., data out on lines SDIPN, SDI7N-0N
3. 10MBytes/sec max., data out on lines SDOPN, SDO7N-0N
4. 10MBytes/sec max., data out on lines SDIPN, SDI7N-0

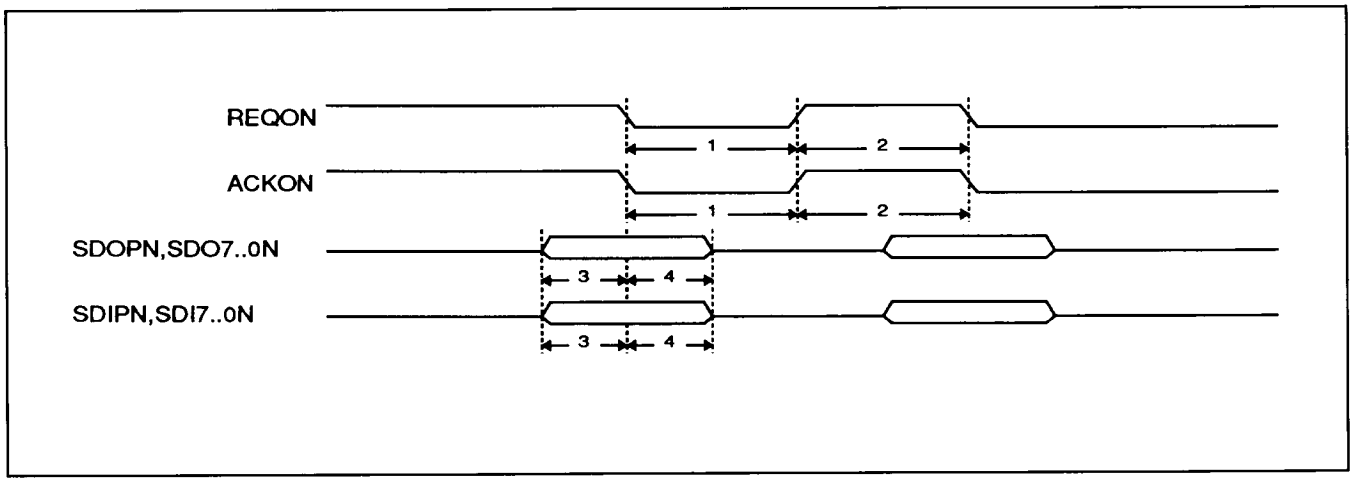


Figure 11. SCSI Synchronous Output

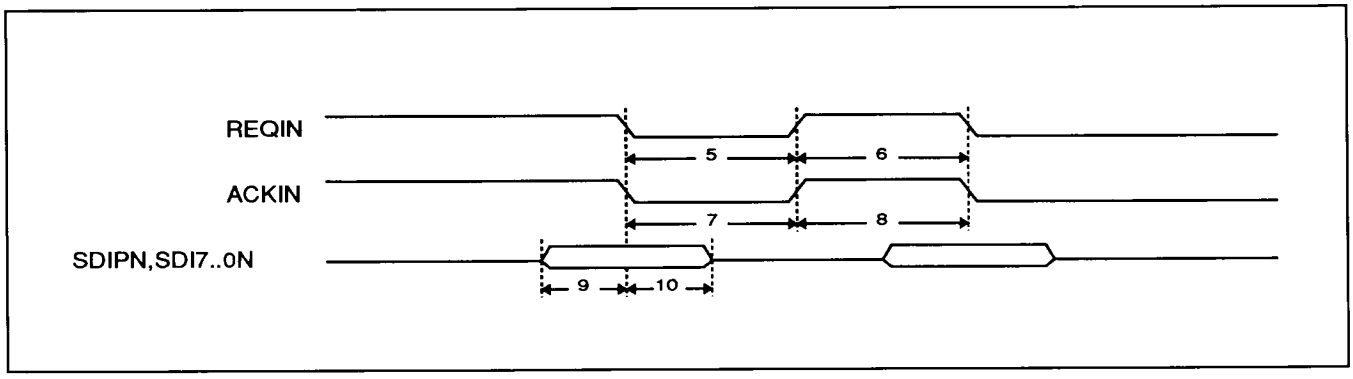


Figure 12. SCSI Synchronous Input

NOTES:

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  Specifications Subject To Change Without Notice FAS200/100A (6/91)