MB86950

ETHERSTAR™ ETHERNET CONTROLLER

FUJITSU

DATA SHEET

DECEMBER 1989

FEATURES

- IEEE 802.3 CSMA/CD Ethernet/Thin-Ethernet and StarLAN™ compatibility
- Configurable for 8-bit or 16-bit data path widths
- Unique buffer management architecture arbitrates all dedicated SRAM or DRAM memory data accesses and automatically allocates buffer memory area for incoming data frames
- Allows simultaneous transfer of data frames to/from host system and transmission/reception of data frames to/from the LAN media
- Allows automatic retransmission of data packets during collisions, thus saving bus bandwidth
- Keeps track of all buffer memory area pointers internally in hardware to reduce software overhead
- Supports data transfers at up to 3.3 Mbytes or Mwords per second to the host system
- Addresses 8, 16, 32, or 64 Kbytes of dedicated SRAM or DRAM buffer memory. Dedicated buffer memory architecture allows data packet reception without using bus bandwidth
- Supports DMA transfers
- Available in 84-pin plastic J-bend PLCC or 80-pin plastic quad flat pack
- Dual metal, CMOS technology
- 25 mA typical ICC current
- EtherStar evaluation board with Ethernet/Thin-wire Ethernet and StarLAN connections available

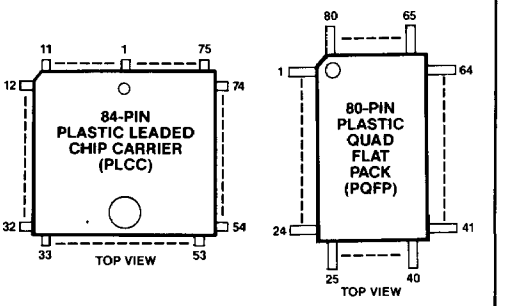
GENERAL DESCRIPTION

The MB86950 EtherStar is a highly integrated, local area network controller that supports both IEEE 802.3 CSMA/CD 10Mbps Ethernet and 1Mbps StarLAN protocols. Configurable for 8- or 16-bit wide bus interfaces, it links a host system bus to the local area network (LAN) transceiver or drivers in cost sensitive network applications such as personal computers, terminals, workstations, and other resource-sharing controllers with the minimum amount of controlling software and host system-EtherStar interaction. Its design enables the controller to be connected directly on the main system bus without contention with the host CPU for the bus. Also, there is no need for a dedicated local CPU to handle data transfers.

EtherStar arbitrates access to a dedicated DRAM or SRAM buffer memory of up to 64 Kbytes in size. The transfer of data frames to/from the host system and the transmission/reception of data frames to/from the network media can occur simultaneously. EtherStar supports transfers to/from the system using programmed I/O or DMA. EtherStar integrates a data link controller (DLC), a 1Mbps Manchester encoder/decoder, a dynamic memory controller (DMC), and a buffer manager to arbitrate simultaneous access to the buffer memory by the host system CPU and the data frames from the LAN media. The DLC block provides for automatic generation and stripping of the 64-bit preamble, 32-bit CRC generation/checking, serial and parallel data conversions, automatic retransmission, contention resolution by binary exponential backoff, and address recognition for 10Mbps Ethernet and 1Mbps StarLAN supporting IEEE 802.3 CSMA/CD specifications.

PIN CONFIGURATION

Top View



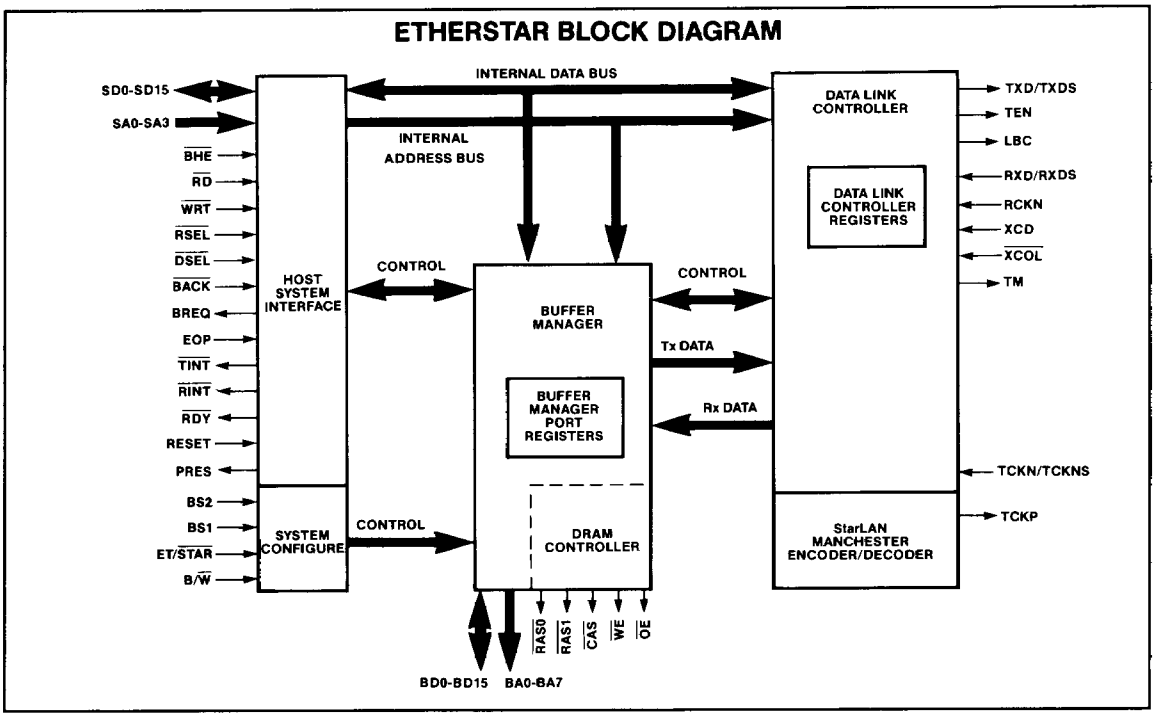
PIN ASSIGNMENTS — PQFP

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	ET/STAR	28	DSEL	55	BA1
2	B/W	29	EOP	56	BA2
3	BS0	30	SA3	57	BA3
4	BS1	31	SA2	58	BA4
5	TEN	32	TM	59	BA5
6	LBC	33	VCC1	60	BA6
7	XCD	34	SA1	61	BA7
8	XCOL	35	SA0	62	OE
9	TXD/TXDS	36	BHE	63	BD0
10	TCKP	37	RD	64	BD1
11	TCKN/TCKNS	38	WRT	65	BD2
12	GND1	39	BACK	66	BD3
13	RCKN	40	BREQ	67	BD4
14	RXD/RXDS	41	SD8	68	BD5
15	RESET	42	SD9	69	BD6
16	SD7	43	SD10	70	BD7
17	SD6	44	SD11	71	BD8
18	SD5	45	SD12	72	PRES
19	SD4	46	SD13	73	VCC2
20	SD3	47	SD14	74	BD9
21	SD2	48	SD15	75	BD10
22	SD1	49	WE	76	BD11
23	SD0	50	RAS0	77	BD12
24	RDY	51	RAS1	78	BD13
25	TINT	52	GND2	79	BD14
26	RINT	53	CAS	80	BD15
27	RSEL	54	BA0		

PIN ASSIGNMENTS — PLCC

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GND1	29	BACK	57	BD3
2	RCKN	30	BREQ	58	BD4
3	RXD/RXDS	31	SD8	59	BD5
4	RESET	32	SD9	60	BD6
5	SD7	33	SD10	61	BD7
6	SD6	34	SD11	62	BD8
7	SD5	35	SD12	63	VCC2
8	SD4	36	SD13	64	GND4
9	SD3	37	SD14	65	PRES
10	SD2	38	SD15	66	BD9
11	SD1	39	WE	67	BD10
12	SD0	40	RAS0	68	BD11
13	RDY	41	RAS1	69	BD12
14	TINT	42	NC	70	BD13
15	RINT	43	GND3	71	BD14
16	RSEL	44	CAS	72	BD15
17	DSEL	45	BA0	73	ET/STAR
18	EOP	46	BA1	74	B/W
19	SA3	47	BA2	75	BS0
20	SA2	48	BA3	76	BS1
21	VCC1	49	BA4	77	TEN
22	GND2	50	BA5	78	LBC
23	TM	51	BA6	79	XCD
24	SA1	52	BA7	80	XCOL
25	SA0	53	OE	81	TXD/TXDS
26	BHE	54	BD0	82	TCKP
27	RD	55	BD1	83	TCKN/TCKNS
28	WRT	56	BD2	84	NC

ETHERSTAR BLOCK DIAGRAM



PIN DESCRIPTIONS

Device Configuration Pins

PIN NO. PLCC	PIN NO. PQFP	SYMBOL	TYPE	DESCRIPTION
73	1	ET/$\overline{\text{STAR}}$	I	**NETWORK CONFIGURATION:** Configures EtherStar for Ethernet (ET/$\overline{\text{STAR}}$ = 1) or StarLAN (ET/$\overline{\text{STAR}}$ = 0).
74	2	B/$\overline{\text{W}}$	I	**BYTE/$\overline{\text{WORD}}$ SELECT:** B/$\overline{\text{W}}$ = 1 configures EtherStar for an 8-bit data bus, B/$\overline{\text{W}}$ = 0 configures EtherStar to a 16-bit data bus.
75,76	3,4	BS1, BS0	I	**BUFFER SIZE SELECT LINES:** These inputs, together with B/$\overline{\text{W}}$, determine the size of the buffer memory supported by EtherStar. For word transfers, $\overline{\text{BHE}}$ should be asserted. Refer to the $\overline{\text{BHE}}$ signal description for more details.

BS1	BS0	B/$\overline{\text{W}}$ = 1	B/$\overline{\text{W}}$ = 0
0	0	8KB	4KW
0	1	16KB	8KW
1	0	32KB	16KW
1	1	64KB	32KW

Network Interface Pins

PIN NO. PLCC	PIN NO. PQFP	SYMBOL	TYPE	DESCRIPTION
77	5	TEN	O	**TRANSMIT ENABLE:** This pin becomes active when the first bit of the outgoing packet is valid and is held stable during transmission of data from the TXD/TXDS pin. This pin goes low after the last bit of the packet is clocked out. The TEN pin interfaces directly with the TEN pin of the Ethernet encoder/decoder, such as Fujitsu's MB502A, in Ethernet configuration only.
78	6	LBC	O	**LOOPBACK CONTROL:** When LBC = 1, indicates that EtherStar is in the loopback mode. In Ethernet configurations, this pin connects to LBC on the encoder/ decoder, and instructs it not to send data to the Ethernet medium but to send the original data packet back to EtherStar for validation. In StarLAN configurations, this also occurs but loopback occurs on-chip.
79	7	XCD	I	**CARRIER DETECT:** This signal is provided by the encoder/decoder. It indicates the presence of a carrier on the network media.
80	8	$\overline{\text{XCOL}}$	I	**COLLISION DETECT:** This active low input indicates that a collision has been detected on the network media. Signal is provided by the encoder/decoder for Ethernet configurations or as an optional pin for StarLAN configurations.
81	9	TXD/TXDS	O	**TRANSMIT DATA (Ethernet)/TRANSMIT DATA (StarLAN):** This pin is a dual function pin. In an Ethernet configuration, (ET/$\overline{\text{STAR}}$ = 1), TXD/TXDS is the serial data output to the encoder/decoder. In a StarLAN configuration (ET/$\overline{\text{STAR}}$ = 0), TXD/TXDS transmits Manchester encoded data to an RS422 type transceiver.
82	10	TCKP	O	**CRYSTAL OUTPUT:** This is the 10MHz output pin required if a crystal is used. It is available for StarLAN configurations only. The multiplexed pin TCKN/TCKNS is used as the OSCIN input in conjunction with the TCKP signal pin if a crystal is used.

PIN DESCRIPTIONS

Network Interface Pins (Continued)

PIN NO. PLCC	PIN NO. PQFP	SYMBOL	TYPE	DESCRIPTION
83	11	TCKN/TCKNS	I	**TRANSMIT CLOCK (Ethernet)/StarLAN CLOCK/(StarLAN):** This pin is a dual function pin. In an Ethernet configuration, (ET/$\overline{STAR}$ = 1), TCKN/TCKNS is the input clock. Typically this clock is 10MHz and is generated by the external encoder/decoder. In a StarLAN configuration (ET/$\overline{STAR}$ = 0), TCKN/TCKNS is a 10MHz clock required by the on-chip Manchester encoder/decoder.
2	13	RCKN	I	**RECEIVE DATA CLOCK:** This is the 10MHz synchronous receive data clock signal supplied by the encoder/decoder. Not used in StarLAN configurations.
3	14	RXD/RXDS	I	**RECEIVE DATA (Ethernet)/RECEIVE DATA (StarLAN):** This pin is a dual function pin. In an Ethernet configuration, RXD/RXDS is the serial data input line from the external encoder/decoder. In a StarLAN configuration, RXD/RXDS is the input line that receives the asynchronous 1MHz Manchester encoded data from the LAN network.

System Interface Pins

PIN NO. PLCC	PIN NO. PQFP	SYMBOL	TYPE	DESCRIPTION
4	15	RESET	I	**HARDWARE RESET:** Active high. A minimum pulse of 2 microseconds in duration is required. This pin resets EtherStar's internal pointers and registers to the appropriate state.
5-12 31-38	16-23 41-48	SD7-SD0 SD8-SD15	I/O	**SYSTEM DATA BUS:** All data, command and status transfers between the host system and EtherStar take place over this bidirectional, 3-state, bus. The direction of the transfer is controlled by $\overline{RD}$ and $\overline{WRT}$. The type of transaction which is occurring is controlled by $\overline{RSEL}$, $\overline{DSEL}$, and $\overline{BACK}$. The portion of the data bus over which the transaction occurs is controlled by B/$\overline{W}$, $\overline{BHE}$, and SA0.
13	24	$\overline{RDY}$	O	**READY:** Active Low. This output is asserted to indicate to the host system that EtherStar is ready to complete the requested read or write operation. It will also be asserted if the device is unable to respond to the request for a read or write within 2.4 microseconds. In that case, EtherStar will also assert $\overline{RINT}$ and the bus read error status bit (DLCR2, bit 6) or $\overline{TINT}$ and the bus write error status bit (DLCR0, bit 0).
14	25	$\overline{TINT}$	O	**TRANSMIT INTERRUPT:** Active low. Indicates that EtherStar requires host system attention after successful transmission of a packet or if an error occurs during transmission. This interrupt is maskable and can be cleared by writing to DLCR1.
15	26	$\overline{RINT}$	O	**RECEIVE INTERRUPT:** Active low. Indicates that EtherStar requires host system attention after successful reception of a packet or during reception should any error conditions occur. This signal is maskable and can be cleared by writing to DLCR3.

PIN DESCRIPTIONS

System Interface Pins (Continued)

<table>
<tr><th colspan="2">PIN NO.</th><th rowspan="2">SYMBOL</th><th rowspan="2">TYPE</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>PLCC</th><th>PQFP</th></tr>
<tr><td>16</td><td>27</td><td>$\overline{RSEL}$</td><td>I</td><td>REGISTER SELECT: Active low. Enables read/write operations between the 16 data link control registers (DLCR0-15) and the host system.</td></tr>
<tr><td>17</td><td>28</td><td>$\overline{DSEL}$</td><td>I</td><td>DATA SELECT: Active low. Enables read/write operation between the host system and EtherStar's buffer memory port (BMPR0) and buffer manager registers (BMPR2-4).</td></tr>
<tr><td>18</td><td>29</td><td>EOP</td><td>I</td><td>END OF PROCESS: Indicates that an entire packet has been transferred between the buffer memory and the host system. When the DMA controller asserts EOP, further assertions of EtherStar's bus request output, BREQ, will be discontinued.</td></tr>
<tr><td>19, 20
24, 25</td><td>30,31
34, 35</td><td>SA3, SA2
SA1, SA0</td><td>I</td><td>SYSTEM ADDRESS LINES: Specify which of the internal registers or ports of EtherStar is selected for read/write operations.</td></tr>
<tr><td>23</td><td>32</td><td>TM</td><td>O</td><td>TEST MODE: The signal on this pin is the complement of the value of the TM bit (DLCR4, bit 2). It is used to control external functions.</td></tr>
<tr><td>26</td><td>36</td><td>$\overline{BHE}$</td><td>I</td><td>BYTE HIGH ENABLE: Active low. This pin is the byte/word control line. It is used only when EtherStar is configured for a 16-bit data bus (B/$\overline{W}$ = 0). It allows word, upper byte only or lower byte only transfers. The address select pin SA0 is used with $\overline{BHE}$ for byte or word transfers as follows:
<table>
<tr><th>B/$\overline{W}$</th><th>$\overline{BHE}$</th><th>SA0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Word transfer (BMPR0, BMPR2-3, 4 only)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (SD15-SD8)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (SD7-SD0)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Byte (SD7-SD0)</td></tr>
</table></td></tr>
<tr><td>27</td><td>37</td><td>$\overline{RD}$</td><td>I</td><td>READ: Active low input which specifies that the current transfer between EtherStar and the host system is a read from one of EtherStar's internal registers or its data port.</td></tr>
<tr><td>28</td><td>38</td><td>$\overline{WRT}$</td><td>I</td><td>WRITE: Active low input which specifies that the current transfer between EtherStar and the host system is a write to one of EtherStar's internal registers or its data port.</td></tr>
<tr><td>29</td><td>39</td><td>$\overline{BACK}$</td><td>I</td><td>BUS ACKNOWLEDGE: Active low. Indicates that the DMA controller is ready to transfer data between the host system and EtherStar's buffer memory.</td></tr>
<tr><td>30</td><td>40</td><td>BREQ</td><td>O</td><td>BUS REQUEST: Issued to the DMA controller to indicate that EtherStar has data available to be read in its receive buffer, or is ready to accept data into its transmit buffer.</td></tr>
<tr><td>65</td><td>72</td><td>PRES</td><td>O</td><td>PACKET RESET: This signal pin follows the RMT RST bit (DLCR2, bit 4) that indicates a complete special data packet with the data length field 0900H has been received. This is intended to be used as a hardware control function from other nodes in the network.</td></tr>
</table>

PIN DESCRIPTIONS

Buffer Memory Control Pins

PIN NO. PLCC	PIN NO. PQFP	SYMBOL	TYPE	DESCRIPTION
39	49	$\overline{WE}$	O	**WRITE ENABLE:** Active low. This output enables the DRAM memory buffer for write operations.
40 41	50 51	$\overline{RAS0}$, $\overline{RAS1}$	O	**ROW ADDRESS STROBES:** Active low. Outputs to the DRAM buffer memory.
44	53	$\overline{CAS}$	O	**COLUMN ADDRESS STROBE:** Active low. DRAM buffer memory column address strobe.
45-52	54-61	BA0-BA7	O	**BUFFER MEMORY ADDRESS:** These eight lines can address 64 Kbytes of DRAM buffer memory.
53	62	$\overline{OE}$	O	**OUTPUT ENABLE:** Active low. Used to enable the buffer memory during read operations.
54-62 66-72	63-71 74-80	BD0-BD8 BD9-BD15	I/O	**BUFFER MEMORY DATA:** Data lines between the DRAM buffer memory and EtherStar. This 3-state data bus is configurable for an 8-bit or 16-bit data size by the B/$\overline{W}$ input.

Device Power Pins

PIN NO. PLCC	PIN NO. PQFP	SYMBOL	TYPE	DESCRIPTION
1 22 43 64	12 52 — —	GND1 GND2 GND3 GND4		**SYSTEM GROUND**
21 63	33 73	VCC1 VCC2		**POWER SUPPLY:** A nominal +5V DC supply is required.

ORDERING CODE

PACKAGE STYLE	PACKAGE CODE	V_{CC} = +5V ±5%, T_A = 0 to +70°C
80-Pin Plastic Quad Flat Pack	FPT-80P-M01 #37.69	MB86950BPF-G
84-Pin Plastic Leaded Chip Carrier	LCC-84P-M01 #185	MB86950BPD-G

For package outlines
see old data sheet,
ISS# 5495, pg. 23-24

SYSTEM CONFIGURATION

A typical system configuration for the MB86950 EtherStar is shown in figure 1. On the host side, EtherStar interfaces to the system bus to obtain configuration information for its internal control registers, to provide receive and transmit status information from its internal status registers, to move data packets to be transmitted from the host memory to EtherStar's dedicated buffer memory, and to deliver received data packets from the dedicated buffer memory to the host system. The network side connection depends on the protocol mode of operation. For Ethernet mode, EtherStar connects to the LAN media via an external Manchester encoder/decoder (such as Fujitsu's MB502A) and an Ethernet transceiver. In StarLAN mode, the encoding/decoding function is performed internally, and EtherStar attaches to the LAN media via appropriate RS422 drivers and receivers.

BUFFER MEMORY

As described above, the MB86950 uses a dedicated buffer memory for intermediate storage of data frames to be transmitted and of data frames received from the network. The BS0 and BS1 input pins configure EtherStar to operate with 8, 16, 32 or 64 Kbytes of buffer. This memory is partitioned into two separate address spaces: the first four Kbytes are reserved for transmit buffers, while the remainder of the memory is used for a receive buffer (see figure 2).

EtherStar supports both programmed I/O and DMA transfers between the buffer memory and the host system. The host accesses the buffer memory by reading from or writing to EtherStar's buffer memory port register, designated BMPR0. The $\overline{RDY}$ signal synchronizes these transfers to accommodate other internal buffer access requests.

Access to the transmit and receive buffers is completely managed by EtherStar. As required, it updates its internal pointers to these buffers for the tasks of transmission, retransmission, reception, rejection of bad frames, and data transfers to and from the host. Thus, the host is relieved of these buffer management functions, making EtherStar extremely easy to operate and reducing firmware requirements substantially.

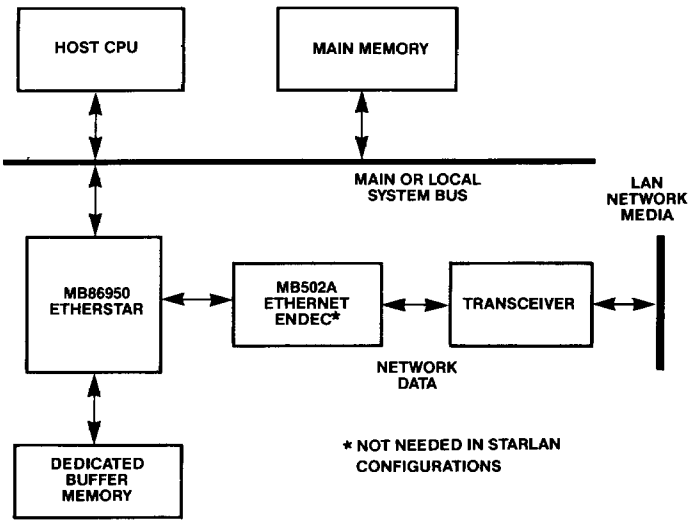


Figure 1. Typical System Configuration

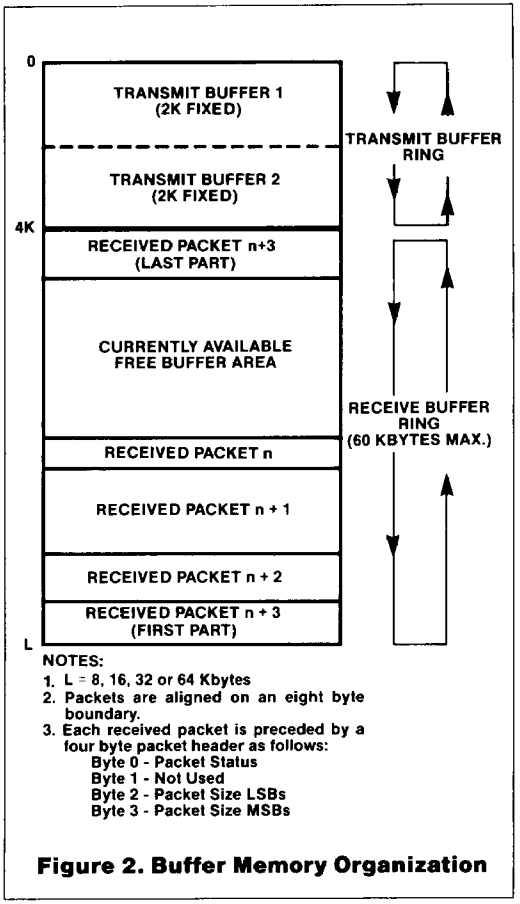


Figure 2. Buffer Memory Organization

TRANSMIT BUFFER

The transmit buffer space is divided to form a ring structure of two transmit buffers, each two Kbytes in length. These function in a 'ping-pong' manner to permit one of the buffers to be loaded by the host while the contents of a previously loaded data frame are being transmitted to the network.

Internal pointers, managed by EtherStar, control which of the two buffers is selected for access by the host and which byte/word of that buffer is written to. At reset, the pointers are initialized to point to the beginning of one of the transmit buffers. Each time the host writes data to the buffer via BMPR0, an internal pointer is advanced to the next memory location within the transmit buffer. Once a data byte/word is written it cannot be read, and the internal pointer cannot be reversed.

When the host has completed loading an outbound data packet into the buffer by successive writes to BMPR0, it initiates transmission of that data packet to the network by writing the length of the outbound packet to the packet length register within EtherStar. The internal pointers are then automatically set to point to the beginning of the second transmit buffer; that buffer is then available to be loaded with the next outbound packet. When the contents of the first data buffer are successfully transmitted, it again becomes available for use by the host.

RECEIVE BUFFER

Buffer memory from 4K through the end of memory is used for receiving packets from the network. This portion of the buffer is not partitioned into fixed length buffers, but is dynamically allocated as packets are received. Each received packet is preceded by a four byte header which provides packet status and the length of that data packet. All receive buffers are aligned on an eight byte boundary and are linked by internal pointers to form a ring structure.

A status bit in one of EtherStar's internal registers informs the host when one or more packets are resident in the receive buffer memory and available to be read. The host retrieves these packets from the buffer memory by successive reads of BMPR0. Once a data byte/word is read from the buffer memory, internal pointers are advanced and that memory becomes available for reception of new packets.

If EtherStar detects a bad incoming packet (CRC error, etc.), it releases the buffer space in which that packet is contained and resets its internal pointers so as to use that space for the next incoming packet. If an incoming packet requires more space than remains available in the buffer, that packet is automatically rejected.

MB86950 FUNCTIONAL DESCRIPTION

As illustrated in the block diagram, the MB86950 consists of five major functional blocks: system interface, buffer manager, DRAM controller, data link controller, and StarLAN encoder/decoder. The operation of these blocks is described below.

SYSTEM INTERFACE

The system interface block provides the connection between EtherStar and the host CPU. EtherStar supports both 8- and 16-bit bus architectures and byte or word transfers. It may be operated in I/O-mapped, memory mapped, or DMA modes. Two interrupt outputs, $\overline{TINT}$ and $\overline{RINT}$, are provided which may be programmed by the user to alert the host CPU of transmitter and receiver status conditions requiring host intervention.

Two sets of user accessible registers are contained within EtherStar: the data link control register set and the buffer memory port register set. Address decoding circuits within the system interface block select the appropriate register within the MB86950 for read and write transactions. All registers are accessible as bytes. Additionally, when the interface is configured for word mode (B/$\overline{W}$ = 0), the registers in the BMPR set can be accessed as bytes or as words.

BUFFER MANAGER

The buffer manager automatically arbitrates, prioritizes and services requests for access to the buffer memory from the data link controller, the refresh timer within the DRAM controller, and the host system, in that order. It updates all buffer memory pointers, allocates memory space for incoming data packets, and controls pertinent bits within the status registers.

The arbitration mechanism interleaves the buffer memory accesses without loss of data, so that operation appears to be 'simultaneous': data can be written to or read from the buffer memory by the host via BMPR0 while data frames are retrieved for transmission and/or provided for storage by the data link controller. Thus, the buffer manager supports all the cases of 'simultaneous' access to the buffer memory, as conveyed in figure 3 and as follows:

1. The host can transfer a packet to a transmit buffer while data from the network is stored in a receive buffer.
2. The host can retrieve a packet from a receive buffer while data from a transmit buffer is obtained by the data link controller.
3. The data link controller can obtain data from a transmit buffer while the host loads the next packet into the second transmit buffer.
4. The data from the network is stored in a receive buffer while the host reads the data in another receive buffer.
5. The host retrieves a packet from a receive buffer while the network side stores data in a different receive buffer and obtains data from a transmit buffer (e.g., in loopback or broadcast address modes).
6. The host delivers a packet to a transmit buffer while the network side obtains data from the second transmit buffer and stores data in a receive buffer (e.g., in loopback or broadcast address modes).

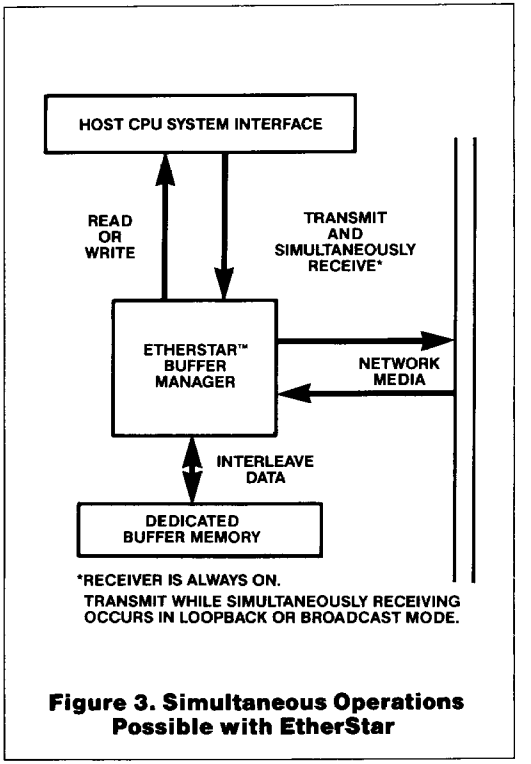


Figure 3. Simultaneous Operations Possible with EtherStar

DRAM CONTROLLER

The DRAM controller provides address multiplexing, timing and automatic refreshing for a DRAM dedicated buffer memory. In 8-bit bus mode (B/$\overline{W}$ = 1) EtherStar supports a memory of up to 64Kx8. In 16-bit bus mode (B/$\overline{W}$ = 0), a memory of up to 32Kx16 can be used.

DATA LINK CONTROLLER

The data link controller (DLC) fully implements the IEEE 802.3 CSMA/CD specification for 10Mbit/sec Ethernet and 1M bit/sec StarLAN. It assembles data packets for transmission and disassembles received data packets. The DLC provides for automatic generation and stripping of the 64-bit preamble, 32-bit CRC generation and checking, contention resolution by binary exponential backoff, several modes of address recognition, and serial/parallel and parallel/serial conversions.

Receiver

The receiver includes a receive state machine, serial to parallel converter, preamble recognition circuitry, address comparison logic for the various modes of address recognition, CRC checker and a FIFO.

The receiver state machine provides sequencing of events for the receiver, including idle, address recognition, data, CRC check and hold. It detects various receive error conditions and sets appropriate bits within the DLC registers.

A six byte receive data FIFO provides a small elastic buffer for synchronization with the buffer manager timing, and to hold data in the event that the buffer manager is servicing another buffer memory access request.

All received bytes are delayed by four bytes so that the last four bytes of the packet can be trapped and checked for correct CRC. These CRC bytes are not transferred to the receive buffer.

During reception, packets are automatically rejected if space in the receive buffer is insufficient to hold the entire received frame or if certain error conditions are detected. Status bits in the receive status register are set to indicate these occurrences.

Transmitter

Circuits within the transmitter include a transmitter state machine, a FIFO, preamble generator, CRC generator, parallel to serial converter, backoff generator and a time domain reflectometer (TDR) counter.

The transmitter state machine provides sequencing of events for the transmitter, including idle, preamble, data, CRC, interframe gap, jam and backoff. It detects various transmit error conditions and sets appropriate bits within the DLC registers.

The two-byte FIFO provides a small amount of elastic buffering that the buffer manager can load with data to be transmitted. The CRC generator produces the standard Ethernet 32-bit CRC that is appended to the end of the packet data field.

A 17-bit pseudo-random number generator provides for the backoff function. This is clocked at the bit rate so that distances between stations become part of the randomizing function. It is sampled at the time of collision and counted down at the slot-time rate (512 bits) defined in the Ethernet specification, which provides a binary exponential backoff from collisions.

The TDR function is provided by a 14-bit counter that counts the actual number of bits transmitted for each packet. See DLCR7 and DLCR15 description for full details of operation.

If EtherStar detects a collision during transmission ($\overline{XCOL}$ input asserted in Ethernet mode, internal detection in StarLAN mode), it will automatically try to retransmit the packet until sixteen attempts have been made. Status bits in the transmit status register are set in case of a collision and sixteen consecutive collisions.

STARLAN ENCODER/DECODER

This unit is operational when the MB86950 is set for StarLAN mode by tying the ET/$\overline{STAR}$ configuration pin LOW.

When transmitting data, the encoder section converts the 1Mbit/sec serial NRZ stream from the DLC to Manchester code and detects collisions. EtherStar monitors its receive input during transmission and assumes a collision has occurred if the received Manchester encoded data is not valid (i.e., anything but valid Manchester). However, this received data is not transferred to the data buffer unless the loopback mode has been enabled.

When receiving, a digital phase locked loop within the decoder section extracts a synchronized clock from the received data stream, while simultaneously converting the Manchester encoded data to NRZ form. The synchronized clock and data are then passed to the data link controller.

REGISTERS

The operation of the MB86950 is programmed prior to beginning operation by writing control words into appropriate registers within the device. Operational feedback is provided by status registers which can be read by the CPU. Certain bits in the control registers can also be manipulated during operation to change the device's operation, e.g., which status bits are

enabled to cause interrupts. The user accessible registers within EtherStar are divided into two sets: the data link control register set and the buffer memory port register set. Table 1 defines the address decoding for these registers.

The data link control register set, consisting of the 16 registers DLCR0-DLCR15, contains transmit control and status registers, receive control and status registers, transmit and receive interrupt masks, and node ID registers. The registers within this set are byte aligned and byte accessible. The node ID registers (DLCR8-DLCR13) are protected; their contents can only be changed when the data link controller is disabled by setting the enable data link controller bit, DLCR6<7>, to a '1', or immediately after device reset.

The buffer memory port register set provides the host with the mechanism to access the transmit and receive buffers, as well as controlling DMA operation. This set contains the buffer memory port register (BMPR0), transmit packet length registers (BMPR2-BMPR3), and a DMA control register (BMPR4). These registers are word aligned and byte or word accessible. When the host reads from or writes to BMPR0, the $\overline{RDY}$ output synchronizes the data transfer, since there may be higher priority requests for access to the buffer memory pending from the data link controller and/or from the DRAM refresh controller. If the buffer manager cannot respond to the host's access request within 2.4μs, it sets an appropriate status bit (bus read error or bus write error) and then asserts $\overline{RDY}$ while simultaneously asserting the corresponding interrupt line ($\overline{RINT}$ or $\overline{TINT}$). This will not typically occur during normal operation, but only if the host attempts to read from an empty receive buffer or to write to a full transmit buffer.

In byte mode (B/$\overline{W}$ = 1), all registers are accessed as bytes. Note that when accessing the buffer memory in byte mode, successive bytes are read or written from BMPR0. When the interface is configured for word mode (B/$\overline{W}$ = 0), all transactions to the buffer memory port must be word transactions; successive words are read or written from BMPR0. The other registers in the BMPR set can be accessed as bytes or as words, depending on the state of the $\overline{BHE}$ and SA0 inputs, as described in the Pin Descriptions table.

Tables 2 and 3 provide an overview of the contents and functions of each register in the DLCR set and the BMPR set, respectively. Detailed descriptions of the registers are given in tables 4 and 5.

Table 1. Internal Register Address Map

BYTE/ WORD	BACK	DSEL	RSEL	SA3	SA2	SA1	SA0	ADDRESS	DESCRIPTION
BYTE	1	1	0	0	0	0	0	DLCR0	TRANSMIT STATUS
BYTE	1	1	0	0	0	0	1	DLCR1	TRANSMIT MASKS
BYTE	1	1	0	0	0	1	0	DLCR2	RECEIVE STATUS
BYTE	1	1	0	0	0	1	1	DLCR3	RECEIVE MASKS
BYTE	1	1	0	0	1	0	0	DLCR4	TRANSMIT MODE
BYTE	1	1	0	0	1	0	1	DLCR5	RECEIVE MODE
BYTE	1	1	0	0	1	1	0	DLCR6	SOFTWARE RESET
BYTE	1	1	0	0	1	1	1	DLCR7	TDR (LSB)
BYTE	1	1	0	1	0	0	0	DLCR8	NODE ID0
BYTE	1	1	0	1	0	0	1	DLCR9	NODE ID1
BYTE	1	1	0	1	0	1	0	DLCR10	NODE ID2
BYTE	1	1	0	1	0	1	1	DLCR11	NODE ID3
BYTE	1	1	0	1	1	0	0	DLCR12	NODE ID4
BYTE	1	1	0	1	1	0	1	DLCR13	NODE ID5
BYTE	1	1	0	1	1	1	0	DLCR14	RESERVED
BYTE	1	1	0	1	1	1	1	DLCR15	TDR (MSB)
BOTH	1	0	1	0	0	0	0	BMPR0	BUFFER MEMORY PORT
BOTH	1	0	1	0	0	1	0	BMPR2	PACKET LENGTH LSB
BOTH	1	0	1	0	0	1	1	BMPR3	PACKET LENGTH MSB
BOTH	1	0	1	0	1	0	0	BMPR4	DMA ENABLE/CONTROL
BOTH	0	1	1	X	X	X	X	BMPR0	BUFFER MEMORY PORT

Table 2. Data Link Controller Register Set Summary

DLCR	REGISTER	READ/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	TRANSMIT STATUS	READ	TMT OK	NET BSY	TMT REC	SRT PKT	UDR FLO	COL	16 COL	BUS WR ERR
		WRITE	—	—	—	—	CLR	CLR	CLR	CLR
1	TRANSMIT INTERRUPT MASKS	READ	MASK TMT OK	—	MASK TMTREC	—	MASK UDR FLO	MASK COL	MASK 16 COL	—
		WRITE	MASK TMT OK	—	MASK TMTREC	—	MASK UDR FLO	MASK COL	MASK 16 COL	—
2	RECEIVE STATUS	READ	PKT RDY	BUS RD ERR	—	RMT RST	SRT PKT	ALG ERR	CRC ERR	OVR FLO
		WRITE	CLR	CLR	'0'*	—	CLR	CLR	CLR	CLR
3	RECEIVE INTERRUPT MASKS	READ	MASK PKT RDY	—	—	MASK RMTRST	MASK SRT PKT	MASK ALG ERR	MASK CRCERR	MASK OVR FLO
		WRITE	MASK PKT RDY	—	—	MASK RMTRST	MASK SRT PKT	MASK ALG ERR	MASK CRCERR	MASK OVR FLO
4	TRANSMIT MODE	READ	COLCTR 3	COLCTR 2	COLCTR 1	COLCTR 0	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC
		WRITE	—	—	—	—	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC
5	RECEIVE MODE	READ	TST	BUF EMP	BUF FUL	ADD SZE	ENA SRT PKT	ENA REMRST	AM1	AM0
		WRITE	TST	—	—	ADD SZE	ENA SRT PKT	ENA REMRST	AM1	AM0
6	ENABLE DATA LINK CONTROLLER	—	—	—	—	—	—	—	—	—
		WRITE ONLY	$\overline{ENA\ DLC}$	—	—	—	—	—	—	—
7	TDR (LSB)	READ ONLY	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
8	NODE ID	READ WRITE	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0 *
9	NODE ID	READ WRITE	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
10	NODE ID	READ WRITE	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
11	NODE ID	READ WRITE	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
12	NODE ID	READ WRITE	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
13	NODE ID	READ WRITE	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
14	RESERVED	—	—	—	—	—	—	—	—	—
15	TDR (MSB)	READ ONLY	—	—	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

1. * A '1' should never be written into these bits.
2. The shaded bits indicate those that should be closely monitored/controlled by the host. Other status bits in DLCR2 and DLCR4 are automatically handled by EtherStar and are for information only, so thus may normally be masked.

Table 3. Buffer Manager Port Register Set Summary

BMPR	REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	BUFFER MEMORY PORT	READ	IN BYTE MODE, CONSECUTIVE **BYTES** ARE READ FROM OR WRITTEN TO THE BUFFER MEMORY BY READING/WRITING BMPR0. IN WORD MODE, CONSECUTIVE **WORDS** ARE READ FROM OR WRITTEN TO THE BUFFER MEMORY BY READING/WRITING BMPR0.							
		WRITE								
2	PACKET LENGTH LSB	—	—	—	—	—	—	—	—	—
		WRITE ONLY	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
3	PACKET LENGTH MSB	—	—	—	—	—	—	—	—	—
		WRITE ONLY	TMST	—	—	—	—	PL10	PL9	PL8
4	DMA ENABLE/ STATUS	READ	—	—	—	—	EOP INT MASK *	EOP *	—	—
		WRITE	—	—	—	—	EOP INT MASK *	CLR EOP STATUS*	RENA	TENA

1. * These bits are not implemented in the MB86950**A** version of EtherStar.

Table 4. Data Link Controller Register Descriptions

DLCR0 — Transmit Status, Read/Write

This register provides transmit status to the host. The user may program the assertion of bits 7, 5, 3, 2 and 1 of this register to cause the assertion of the Transmit Interrupt output ($\overline{TINT}$ = 0) by setting the corresponding bits in DLCR1. Assertion of bit 0 of this register will cause assertion of $\overline{TINT}$— this bit is not maskable.

Bits <3:0> may be cleared individually or in any combination by writing a '1' to those bits. The state of bits written with a '0' is not affected. Bit <7:4> are cleared automatically as described below.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	TMT OK	NET BSY	TMT REC	SRT PKT	UDR FLO	COL	16 COL	BUS WR ERR
WRITE	—	—	—	—	CLR	CLR	CLR	CLR

BIT	SYMBOL	DESCRIPTION
0	BUS WR ERR	**BUS WRITE ERROR:** This error condition occurs if a $\overline{RDY}$ response cannot be issued within 2.4μs after the $\overline{WR}$ signal is asserted by the host system when writing to the buffer memeory port register, BMPR0. Occurs when the transmit buffer memory is full. This should not happen during normal operation.
1	16COL	**16 COLLISION:** This bit is set after the sixteenth unsuccessful transmission of the same packet.
2	COL	**COLLISION:** This bit is set if a collision occurs during transmission of a data packet. The buffer manager will automatically attempt to transmit the current packet up to 16 times. The user may determine the number of consecutive collisions by reading the collision counter, DCLR4<7:4>.
3	UDR FLO	**UNDERFLOW:** This register is set when data from the transmit section of buffer memory is not available for serial transmission. EtherStar will continue to send out this data frame. This should not occur during normal operation.
4	SRT PKT	**SHORT PACKET:** Set if the Received Carrier Detect input (XCD) is negated during a packet transmission. This can be caused by a collision or a shorted LAN media. Automatically cleared as each transmission begins.
5	TMT REC	**TRANSMIT RECEIVED:** Indicates that a good packet was received by the receiver shortly after transmission was completed. This is used to indicate self-reception of the packet. This allows the software to take advantage of the hardware address matching even in systems which are designed for half duplex operation. This bit is cleared as each transmission begins.
6	NET BSY	**NET BUSY:** This is a copy of XCD, the Receive Carrier Detect pin.
7	TMT OK	**TRANSMIT OKAY:** This bit is set when a data packet is successfully transmitted. EtherStar clears this bit automatically as each transmission begins and sets it automatically at the finish of each data packet transmission.

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR1 — Transmit Interrupt Masks, Read/Write

Bits 7, 5, 3, 2, 1 are the transmit interrupt masks. They can be set individually depending on system requirements. Setting a bit to a '1' causes the assertion of the corresponding bit in DLCR0 to assert $\overline{TINT}$.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ WRITE	MASK TMT OK	—	MASK TMT REC	—	MASK UDR FLO	MASK COL	MASK 16 COL	—

DLCR2 — Receive Status, Read/Write

This register provides receive status to the host. The user may program the assertion of bits 7 and <4:0> of this register to cause the assertion of the Receive Interrupt output ($\overline{RINT}$ = 0) by setting the corresponding bits in DLCR3. Assertion of bit 6 of this register will cause assertion of $\overline{RINT}$— this bit is not maskable.

Bits <7:6> and <3:0> may be cleared individually or in any combination by writing a '1' to those bits. The state of bits written with a '0' is not affected. Bit 4 is cleared automatically as described below.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PKT RDY	BUS RD ERR	—	RMT RST	SRT PKT	ALG ERR	CRC ERR	OVR FLO
WRITE	CLR	CLR	'0'	—	CLR	CLR	CLR	CLR

BIT	SYMBOL	DESCRIPTION
0	OVR FLO	**OVERFLOW.** This bit is asserted if a received packet is discarded because there is insufficient memory space in the receive buffer memory to accommodate the complete data packet. The space remaining is made available for shorter data packets.
1	CRC ERR	**CRC ERROR:** This bit is set when the calculated CRC does not match the CRC at the end of the received packet.
2	ALG ERR	**ALIGNMENT ERROR:** Set if a packet has bad CRC at the last octet boundary and the number of bits are not divisible by eight.
3	SRT PKT	**SHORT PACKET:** Set if a data packet does not meet the minimum length requirements of 60 bytes, or 6 bytes when the enable short packet bit, DLCR5<3>, is on.
4	RMT RST	**REMOTE RESET:** This bit will be set when the ENA RMT RST bit, DLCR5<2>, is on and a receive packet with the special data length 0900H is successfully received. The RMT RST bit, when set, will assert the PRES pin. The bit is cleared at the beginning of the next packet reception. This bit is set only if the node ID matches, not on multicast or broadcast addresses, in any address match mode (see DLCR5<1:0>).
5	—	**RESERVED:** Never write a "1" into this bit.
6	BUS RD ERR	**BUS READ ERROR:** This error condition occurs if a $\overline{RDY}$ response cannot be issued within 2.4μs after the $\overline{RD}$ signal is asserted by the system when reading the buffer memory port register, BMPR0. Occurs when trying to read when the receive buffer memory is empty.
7	PKT RDY	**PACKET READY:** Set after the successful reception of packet data into the receive buffer memory.

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR3 — Receive Masks , Read/Write

Bits 7 and <4:0> are the receive interrupt masks. Setting a bit to a '1' causes the assertion of the corresponding bit in DLCR2 to assert $\overline{RINT}$.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ WRITE	MASK PKT RDY	—	—	MASK RMT RST	MASK SRT PKT	MASK ALG ERR	MASK CRC ERR	MASK OVR FLO

DLCR4 — Transmit Mode, Read/Write

This register controls certain transmit functions and provides the count of successive collisions on transmission attempts.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	COL CTR 3	COL CTR 2	COL CTR 1	COL CTR 0	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC
WRITE	—	—	—	—	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC

BIT	SYMBOL	DESCRIPTION
0	DSC	**DISABLE CARRIER DETECT:** When this bit is set the transmitter disregards XCD, the Carrier Detect signal.
1	$\overline{LBC}$	**LOOPBACK CONTROL:** This bit controls the loopback function of the external encoder/decoder in Ethernet mode, and the internal loopback function in StarLAN mode. The LBC pin signal value is the complement of the value of this bit. '0' = Loopback, '1' = No Loopback.
2	$\overline{TM}$	**TEST MODE:** A bit whose complement is available as signal pin TM. Used for controlling power to the transceiver or any other function external to the chip.
3	CHP TST	**CHIP TEST:** Fujitsu internal use. Always write a '0' to this bit for normal operation.
<7:4>	COL CTR	**COLLISION COUNTER:** Bits <7:4> keep track of the number of consecutive collisions during transmission of a data packet.

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR5 — Receive Mode, Read/Write

This register controls certain receiver functions and provides receive buffer memory status.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	TST	BUF EMP	BUF FUL	ADD SZE	ENA SRT PKT	ENA REM RST	AM1	AM0
WRITE	TST	—	—	ADD SZE	ENA SRT PKT	ENA REM RST	AM1	AM0

BIT	SYMBOL	DESCRIPTION
<1:0>	AM1, AM0	**ADDRESS MATCH MODE:** These two bits control address recognition and matching. Bit 1 / Bit 0 / Function: 0 / 0 / Accept no packets. 0 / 1 / Accept physical address, multicast-group addresses which match the first three bytes, and broadcast address. 1 / 0 / Accept physical address, all multicast addresses, and broadcast address. 1 / 1 / Accept all packets (promiscuous mode).
2	ENA RMT RST	**ENABLE REMOTE RESET:** This bit is used to enable/disable the receipt of packets with the special data length 0900H. See DLCR2<4>.
3	ENA SRT PKT	**ENABLE SHORT PACKET:** When set to "1", the receive section will receive packets as short as six bytes. When reset to "0", the receive section of buffer memory will receive packets between 60 bytes and two Kbytes.
4	ADD SZE	**ADDRESS SIZE:** When set, this bit reduces the node ID address match to five bytes rather than the normal six bytes. This is used where the node is used to perform some multiplex function on the least significant byte of the destination address.
5	BUF FUL	**BUFFER FULL:** This bit provides real-time status of the receive buffer memory. As a packet is being loaded into the buffer memory from the data link controller, this bit will be set if the empty space remaining becomes equal to or less than eight bytes. This bit will automatically clear when the space remaining becomes more than eight bytes due to a) the packet being rejected and sufficient memory freed by the buffer manager or b) the host reading enough data from the buffer.
6	BUF EMP	**BUFFER EMPTY:** Indicates that the buffer memory is empty. A "0" indicates that there is at least one good data packet in the receive section. A "1" indicates that the receive section is empty. This bit gives the host software an indication to continue reading additional data frames from the receive buffer after successful reading of a packet.
7	TST	**TEST:** This bit is used for testing purposes. When EtherStar is in the receive mode, this bit set to "1" fixes four bytes of the CRC to C7, 04, DD, 7B. This value is shifted into the CRC register and checked without being modified. When EtherStar is transmitting, the backoff algorithm is changed to $2e^{(n-1)} + 1$, where n is the number of collisions.

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR6 — Enable Data Link Controller, Write Only

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WRITE ONLY	$\overline{\text{ENA DLC}}$	—	—	—	—	—	—	—

BIT	SYMBOL	DESCRIPTION
<6:0>	—	**Not used.**
7	$\overline{\text{ENA DLC}}$	**ENABLE DATA LINK CONTROLLER:** This bit must be cleared by writing a "0" into the location after the other DLC registers have been programmed. After this bit is cleared, EtherStar is ready to transmit and receive. At least 15 microseconds must elapse between the end of the hardware reset pulse falling edge and the writing of $\overline{\text{ENA DLC}}$. "1" will release EtherStar from any activity on the network. Node ID registers DLCR8-13 read/write only when this bit is "1".

DLCR7 — TDR Register LSBs, Read Only, DLCR15 — TDR Register MSBs, Read Only

A Time Domain Reflectometer (TDR) function is provided by this 14-bit counter that counts the number of bits successfully transmitted for each packet. The purpose of this function is to provide a rough measure of the distance of the unit on the network to some media fault, either a short or an open.

The counter is cleared at the beginning of each transmission and counts bits from that time until the Carrier Detect input (XCD) negates or a collision is detected. The counter is also cleared after each successful data packet transmission. The LSBs are read from DLCR7, the MSBs from DLCR15.

	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DLCR7	READ ONLY	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
DLCR15	READ ONLY	—	—	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR8:DLCR13 — Node ID Registers, Read/Write

The node ID is comprised of the six bytes contained in DLCR8 through DLCR13. EtherStar compares this node ID with the destination field of all packets on the LAN media to determine if there is a match. If the two addresses match, and the address match mode in DLCR5<1:0> allows reception, the packet is received into buffer memory. DLCR8 is the LS byte and DLCR13 is the MS byte of the node ID. The node ID is reduced to the five MS bytes (DLCR9 to DLCR13) if DLCR5<4> is set to a '1'.

These registers are accessible for read/write operations only when the data link controller has been disabled via DLCR6<7> or immediately after reset.

	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DLCR8	READ WRITE	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0*
DLCR9	READ WRITE	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
DLCR10	READ WRITE	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
DLCR11	READ WRITE	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
DLCR12	READ WRITE	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
DLCR13	READ WRITE	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40

*Do not program to '1'.

Table 5. Buffer Manager Port/Register Descriptions

BMPR0 — Buffer Memory Port Register, Read/Write

This register provides the host access to the buffer memory. Writing a byte/word to this port transfers that data to the currently addressed location in the transmit buffer and increments the transmit buffer pointer to point to the next byte/word. Reading a byte/word from this port transfers the contents of the currently addressed location in the receive buffer to the host and increments the receive buffer pointer to point to the next byte/word. See DLCR0<0>, DLCR2<6>, DLCR5<5> and DLCR5<6> for additional information.

This register is byte access only in byte mode and word access only in word mode (the upper and lower bytes cannot be accessed independently in word mode).

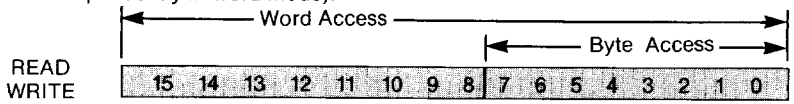


Table 5. Buffer Manager Port/Register Descriptions (Continued)

BMPR3:BMPR2 — Packet Length Registers, Write Only

The host writes to these registers to define the length of the packet which was loaded for transmission into the currently addressed transmit buffer. The LS byte is in the BMPR2, the MS bits are in BMPR3. The transmit start bit, TMST in BMPR3, is set when BMPR3 is written to inform the buffer manager that the data and packet length have been provided and that it should initiate transmission of that packet via the data link controller.

In byte access mode, the LS byte must be written first, followed by the MS bits and TMST in BMPR3.

	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BMPR2	WRITE ONLY	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
BMPR3	WRITE ONLY	TMST	—	—	—	—	PL10	PL9	PL8

BMPR4 — DMA Control and Status Register, Read/Write

This register enables/disables DMA operation for accessing the buffer memory, and provides DMA status.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	—	—	—	—	EOP INT MASK	EOP	—	—
WRITE	—	—	—	—	EOP INT MASK	CLR EOP	RENA	TENA

BIT	SYMBOL	DESCRIPTION
0	TENA	**TRANSMIT DMA ENABLE:** A '1' enables DMA write operation between the host and the buffer memory. A '0' disables DMA write operation between the host and the buffer memory. Write only.
1	RENA	**RECEIVE DMA ENABLE:** A '1' enables DMA read operation between the host and the buffer memory. A '0' disables DMA read operation between the host and the buffer memory. Write only.
2	EOP	**END OF PROCESS:** Indicates that an entire packet has been transferred between the buffer memory and the host. Set to a '1' when the external DMA controller asserts the EOP input. The host should respond by clearing RENA or TENA. When this bit is set, the Receive Interrupt output, $\overline{RINT}$, will be asserted if this action has been enabled by setting bit 3 of this register. Writing a '1' to this bit clears the status bit, writing a '0' has no effect. Read/write. **Note:** This function is not implemented in the MB86950A version of EtherStar.
3	EOP INT MASK	**EOP Interrupt Mask:** Writing a '1' to this bit will cause RINT to be asserted when the EOP status bit, bit 2 of this register, is also set. Writing a '0' to this register masks $\overline{RINT}$ from being asserted by that condition. Read/write. **Note:** This function is not implemented in the MB86950A version of EtherStar.
<7:4>	—	Not used.

OPERATION

The operation of the MB86950 can be considered in four major operational phases: reset, initialization, packet transmission, and packet reception. Although described separately here, packet transmission and reception can be performed concurrently in actual operation. In the sections that follow, interrupt-driven operation is assumed.

RESET

A reset pulse with a minimum duration of 2μsec is applied to the RESET input after power on, or at any other time, to reset the internal pointers and other logic within the MB86950. Reset disables the data link controller (effectively setting DLCR6<7> to a '1'), sets DLCR5<6>, BUF_EMP, to a '1', and clears the following bits:

DLCR0	5, 6, 7
DLCR1	0, 4, 6
DLCR2	4, 7
DLCR3	5, 6
DLCR5	5
BMPR4	0, 1, 2, 3

The state of all other bits within the registers after reset is indeterminate.

INITIALIZATION

Initialization is performed by software to place EtherStar into a known functional state. This includes setting the transmit and receive interrupt conditions, transmission and reception modes, and the node address that EtherStar responds to. A flow chart of the initialization process is shown in figure 4.

Before any initialization begins, EtherStar should be disabled by writing a value of H'80' to DLCR6. This disables the data link controller and enables access to the node ID registers (DLCR8 through DLCR13). The DLCR register set is then initialized, in any order, based on the communication requirements. The basic programming is as follows:

DLCR0 — Transmit Status: A value of H'0F' is written to clear all transmit errors.

DLCR1 — Transmit Interrupt Masks: The transmit interrupts are disabled by writing a value of H'00' at initialization. Desired interrupts should be enabled prior to a packet transmission.

DLCR2 — Receive Status: The value H'CF' is written to clear all receive errors.

DLCR3 — Receive Interrupt Masks: Required receive interrupts are enabled by writing the appropriate value. These may be changed during operation, based on reception criteria.

DLCR4 — Transmit Mode: Normally, a value of H'02' is written to disable chip test, test mode and loopback, and to enable carrier detect.

DLCR5 — Receive Mode: A value is written per system requirements to enable/disable CRC testing, set the address size, enable/disable short packet reception, enable/disable remote reset packet reception, and to set the address recognition mode.

DLCR8 to DLCR13 — Node ID Registers: The six byte address programmed into these registers must be unique. It is used in conjunction with the address match mode bits (DLCR5<1:0>) for packet reception.

If this initialization is part of an error recovery procedure, BMPR0 should be read twice to assure that certain internal pipeline registers are cleared. If a BUS_RD_ERR results from these read operations, it should be ignored.

When this initialization is completed, the data link controller is enabled by writing H'00' to DLCR6. A delay of 15μsec, the time needed by EtherStar to complete internal initialization, must be guaranteed between the trailing edge of reset and clearing of DLCR6. In StarLAN mode only, an additional delay of 120μsec after the DLC is enabled is required before EtherStar is ready to begin transmit or receive operations.

PACKET TRANSMISSION

An outbound packet is transmitted in two phases. In phase one, the packet is transferred from host memory to a transmit buffer in EtherStar and the transmission is initiated. In phase two, a transmit interrupt is used to report successful transmission or a transmit error condition.

Transmit Initiation

The first phase is illustrated in figure 5. To transmit a packet, the host loads the outbound packet into a transmit buffer, initiates transmission, waits for EtherStar to clear the TMT_OK bit, sets a transmit pending flag, and sets the transmit interrupt masks.

A transmit packet, figure 6, contains a six byte Destination Address, a six byte Source Address, a

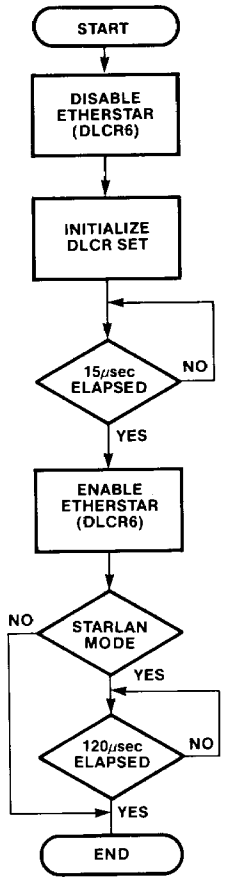


Figure 4. MB86950 Initialization

two byte Data Length, and data. EtherStar is capable of transmitting packets with a total packet length of six to 2,048 bytes, depending on the configuration set at initialization. (Software conforming to the IEEE 802.3 specification must guarantee that the total packet length is in the range of 64 to 1,518 bytes including the four-byte CRC, which is calculated by EtherStar and appended to the packet when it is transmitted.)

The packet is loaded into a transmit buffer using the buffer memory port register (BMPR0). At initialization or the initiation of a transmission, EtherStar's internal pointers are advanced to the beginning of the next available transmit buffer. The packet is transferred from the host to a transmit buffer by successive writes of data, starting at the beginning of the packet, to BMPR0. The internal pointers manage the placement of the data into the current transmit buffer. When the entire packet has been loaded, EtherStar is requested to send the packet by writing the total length of the transmit packet (with the TMST bit set) to the packet length register (BMPR3:BMPR2). Note that the packet length value is in *bytes* regardless of whether the MB86950 is configured in word mode or in byte mode. If operating in word mode, and the packet length is an odd value, the MS byte of the last word sent to the buffer will not be transmitted.

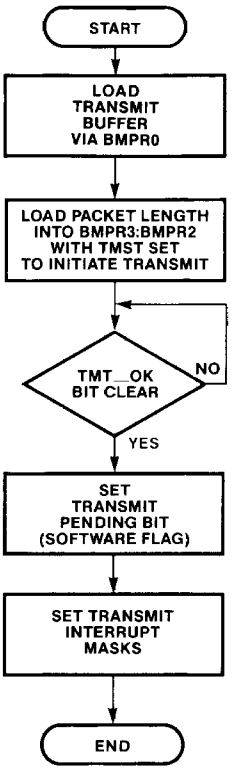


Figure 5. Transmit Initiation

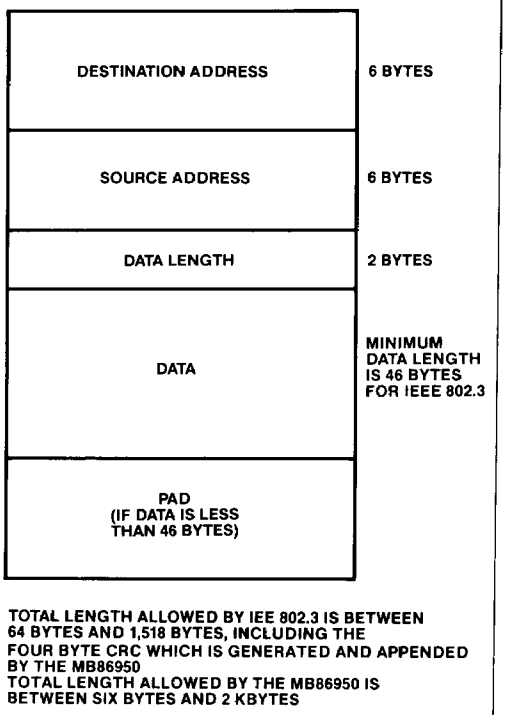


Figure 6. Transmit Packet Format

When the network is free and EtherStar actually begins transmitting the packet to the LAN, it will clear the TMT_OK bit. The TMT_OK_MSK bit must not be set until TMT_OK is cleared to prevent an erroneous transmit interrupt from being generated. The host can load the next packet into the second transmit buffer immediately after it sets TMST for the previous packet, but the TMST bit cannot be set for that second packet until the first packet has been successfully transmitted to the LAN.

When using a common interrupt service routine (ISR) to handle both transmit and receive interrupts, a transmit pending flag is required within the driver to distinguish whether TMT_OK was set to indicate the completion of a pending transmission or is the residue of a previous transmission, since the software does not have the ability to clear TMT_OK after completion of a pending transmission.

Once the transmit has been initiated and the TMT_OK bit is cleared by EtherStar, the transmit interrupt masks are set. Typically, a value of H'82' is written to the transmit masks register (DLCR1) to enable transmission interrupts based on transmit complete, and 16-collision error. The COL and underflow error interrupts may optionally be enabled.

Transmit Interrupt Routine

When a packet is successfully transmitted or a transmit error condition occurs which has its corresponding transmit interrupt mask set in DLCR1, a transmit interrupt ($\overline{TINT}$) is generated. A typical transmit interrupt service routine (ISR) to service this interrupt is shown in figure 7.

On entering the ISR, the transmit interrupt masks are cleared by writing H'00' to DLCR1, to prevent nested interrupts. These masks may need to be saved and rewritten prior to exiting the ISR. If the transmit pending flag is set, the status of TMT_OK is checked. If it is set, the packet has been successfully transmitted; the routine clears the transmit pending flag and takes any other driver specific action. This may include signaling successful transmission to the upper layer network software and/or initiating another transmission.

The major error conditions which must be handled by the ISR are bus write error and 16-collision error. BUS_WRT_ERR is not the result of a transmission by the DLC, but indicates that an attempt was made to transfer data to a transmit buffer and the transmit buffer was full. The ISR clears the bit, increments a bus write error counter in the driver for diagnostic purposes, and performs any other driver specific recovery action. 16_COL indicates that sixteen collisions have occurred in the transmission of a single packet and that EtherStar has aborted attempting to transmit that packet. This error is handled by clearing the error bit, incrementing a 16-collision error counter in the driver for diagnostic purposes, and performing any driver specific recovery algorithms.

Note: If, after 16 collisions have occurred, the host wishes to attempt to transmit the same packet again, it must reload that packet into one of EtherStar's transmit buffers.

UDR_FLO will not occur during normal operation, but may be the result of some other error condition. This error is handled in a manner similar to 16_COL.

Setting of the collision error status bit, COL, indicates that at least one collision occurred in the transmission of a single packet. EtherStar will continue to retransmit the packet up to sixteen times. Each time the

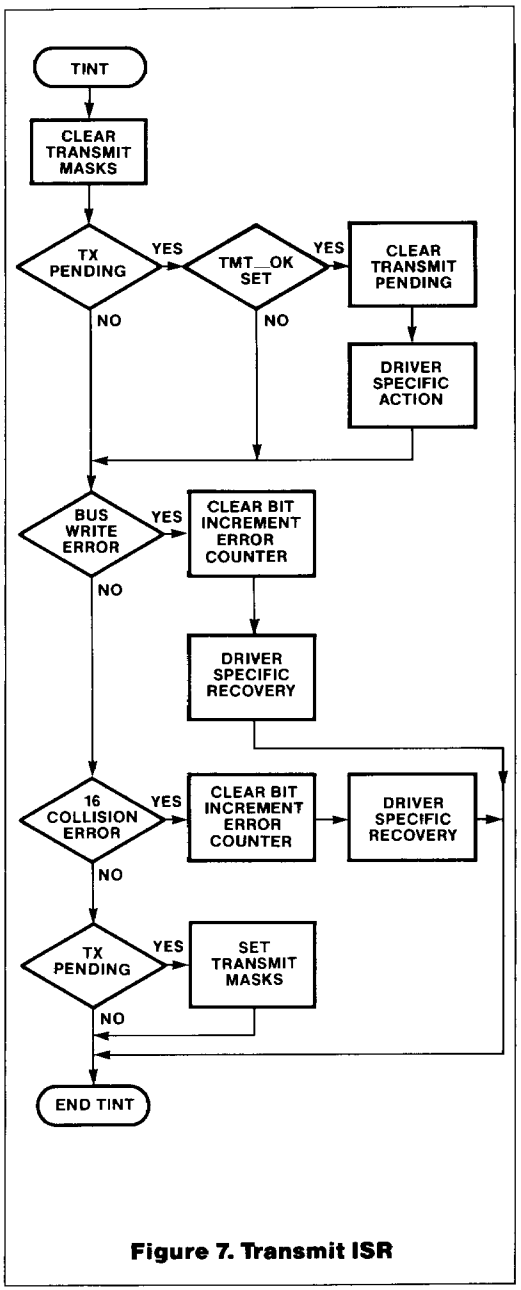


Figure 7. Transmit ISR

packet fails to transmit due to collision, a collision counter in the transmit mode register (DLCR4<7:4>) is incremented. When the collision counter wraps around to 0, 16_COL is set and EtherStar will not retransmit. If COL is set and 16_COL is not set, the collision counter will contain the number of collisions encountered on that transmission. Recovery is accomplished by clearing the COL bit and incrementing a collision error counter if desired.

Prior to exiting the ISR, the transmit pending flag is checked to see if there is an outstanding transmission. If set, then the transmit interrupt masks, which were cleared on entering the ISR, must be written back to DLCR1 to interrupt when the transmission completes.

PACKET RECEPTION

Incoming packets are examined for a match in the destination address field of the Ethernet header. Reception is based on the address match mode bits and the ADD_SZE bit in the receive mode register (DLCR5) and the node ID (DLCR8 through DLCR13). When a packet matches the defined reception criteria, it is copied into a receive buffer and checked for overflow, CRC, alignment or short packet errors. If no errors are detected, PKT_RDY in the receive status register (DLCR2) is set and BUF_EMP in the receive mode register (DLCR5) is cleared if not already cleared. If an error is encountered, the packet is discarded, making the buffer memory occupied by that packet available for reception of another packet, and the appropriate error bits are set in DLCR2.

Addressing Modes

In addition to the normal single address match mode, where the incoming address is compared to the programmed node ID, the MB86950 supports three special receiver address match modes: promiscuous receive, multicast address, and multicast group address. These modes are enabled by setting the address match mode bits in the receive mode register appropriately, and may be changed by the driver at any time. It is also possible to set the transmit mode for loopback, so that transmitted packets are not sent to the network, but are simply fed back into the receiver.

In **promiscuous receive mode**, all good incoming packets on the LAN are received into buffer memory. No matching is done on the destination address field of the packet. This can be useful for network monitoring applications and debugging.

A multicast address is identified by a value of '1' in the

least significant bit of the destination address. Using **multicast address mode** will cause all packets having a multicast address to be received. Note that in this mode EtherStar does not provide any hashing on the multicast address and simply receives all multicast packets.

When **multicast group address mode** is set, packets will be received if the three least significant bytes of the address match the address in the node ID registers and the least significant bit of the destination address is '1'.

Receive Packet Structure

When a packet is successfully stored in the receive buffer memory, EtherStar attaches a four byte header in the front of the packet. The first byte is a copy of the receive status register (DLCR2) in which bit 5 is set and the PKT_RDY bit is invalid. The second byte is reserved. The third and fourth bytes contain the LS and MS bytes of the length of the packet, respectively. Note that the packet length value is in *bytes* regardless of whether EtherStar is configured in word mode or in byte mode.

Receive Interrupt Routine

A receive interrupt ($\overline{\text{RINT}}$) is generated when a packet is successfully stored in the receive buffer memory or a receive error condition occurs which has its corresponding interrupt mask set in DLCR3. A typical receive interrupt service routine (ISR) to service this interrupt is shown in figure 8.

On entering the ISR, the receive interrupt masks are cleared by writing H'00' to DLCR3, to prevent nested interrupts. These masks may need to be saved and rewritten prior to exiting the ISR. If BUF_EMP is cleared, there is at least one valid packet in the receive buffer memory, and the ISR proceeds to transfer that packet to the host. First, PKT_RDY is cleared. Then, the receive status byte and reserved bytes are read from the buffer memory via BMPR0. (In this model, these bytes are unused, but must be read to advance internal pointers used to control the extraction of received packets.) The packet length is then extracted to determine the size of the actual received packet, and that packet is copied to host memory by successive reads of BMPR0. The ISR then checks BUF_EMP again to see if additional packets remain in the receive buffer memory and, if so, the steps described above are repeated until all available packets have been copied to the host.

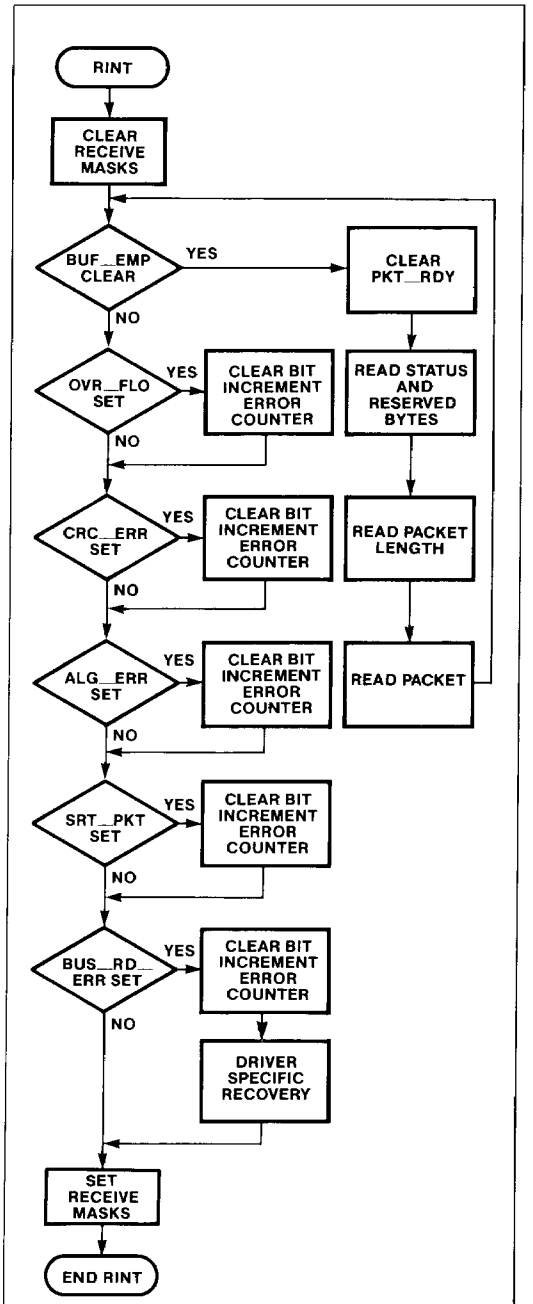


Figure 8. Receive ISR

Note: Reading more than the specified number of bytes extracts a portion of the next receive packet or causes a BUS_RD_ERR. Reading less than the specified number of bytes leaves garbage at the beginning of the next receive packet. These conditions can generate a fatal error condition.

Note: If operating in word mode, and the indicated packet length is an odd value, an extra byte of invalid data will be read out of the buffer on the last word read and should be ignored. There is no danger of reading the first byte of the next packet in this case because the packets in the buffer memory are aligned to start on an eight byte/four word boundary.

Note: When a packet has been completely read out of the buffer, EtherStar will re-assert PKT_RDY if any packets remain in the receive buffer. This feature can be used to cause an interrupt to be generated for each valid packet received and stored in the buffer.

The receive error conditions which can be programmed to cause an interrupt are bus read error, overflow, CRC error, alignment error, and short packet. All except the first do not require host intervention other than tallying the error for diagnostic purposes; EtherStar will automatically reject any packet in which any of these error conditions is detected.

BUS_RD_ERR indicates that an attempt was made to transfer data from a receive buffer to the host when the receive buffers are empty. This should be considered a fatal error, where the hardware or software is faulty. To recover, the ISR clears the BUS_RD_ERR bit, increments a bus read error counter, and performs any other driver specific recovery routine.

OVR_FLO denotes that an incoming packet from the LAN media was rejected because it was longer than the amount of free memory available in the receive buffer area. CRC_ERR indicates that the incoming packet's CRC did not match that calculated by EtherStar. ALG_ERR signifies that the incoming packet has a bad CRC at the last octet boundary and the number of bits were not divisible by eight. SRT_PKT indicates that the incoming packet does not meet the minimum length requirement of 60 bytes, or if the ENA_SRT_PKT bit in DLCR5 is set, six bytes. For these errors, the sample ISR takes no action other than clearing the error condition and incrementing a corresponding error counter.

Prior to exiting the ISR, the receive interrupt masks are restored to enable future receive interrupts.

DMA OPERATION

The MB86950 supports DMA operation for transfers of data between the host system and the dedicated buffer memory. The BREQ and $\overline{\text{BACK}}$ signals are used for handshaking between the external DMA controller and EtherStar.

DMA WRITE (TRANSMIT)

TENA, BMPR4<0>, is set to a '1' to enable DMA write operation for transfers of data packets from the host memory to EtherStar's transmit data buffer. When it is ready to begin to accept data from the host, EtherStar will assert its Bus Request output, BREQ. The host responds by asserting $\overline{\text{BACK}}$ followed by $\overline{\text{WRT}}$ and placing the data on the data bus. EtherStar will negate BREQ and will assert its $\overline{\text{RDY}}$ output when it is ready to complete the current data transfer cycle. When the host negates $\overline{\text{BACK}}$ and $\overline{\text{WRT}}$, EtherStar accepts that data byte/word, moves its internal pointer to point to the next byte/word, and then re-asserts BREQ to repeat the process. The DMA controller must assert the End of Process input, EOP, concurrent with the last byte/word data transfer to indicate that the entire packet has been transferred. EtherStar will then discontinue making further data requests.

To cause the packet to be transmitted, the host must load its packet length into BMPR3:BMPR2, asserting the TMST bit when the MS byte is loaded into BMPR3. TENA must be cleared when the packet transfer is completed, and set again when the host desires to begin loading another packet into the transmit buffer using DMA.

When EOP is asserted by the external DMA controller, the EOP status bit, BMPR4<2>, will be set to a '1' and will cause $\overline{\text{RINT}}$ to be asserted if BMPR4<3>, EOP_INT_MSK, is set. This interrupt can be used by the host to initiate the actions described in the paragraph above. The interrupt is cleared by writing to BMPR4 with bit 2 set, which can be done at the same time as TENA is cleared.

DMA READ (RECEIVE)

Prior to beginning the transfer of a data packet from EtherStar's receive buffer memory to the host memory

via DMA, the host must read the four-byte packet header to determine the number of bytes/words in the packet and should load that number into the counter in the external DMA controller. RENA, BMPR4<1>, is then set to a '1' to enable DMA read operation to transfer the actual packet to the host memory. When it is ready to begin, EtherStar will assert its Bus Request output, BREQ. The host responds by asserting $\overline{BACK}$ followed by $\overline{RD}$. EtherStar will negate BREQ and will assert its $\overline{RDY}$ output when it has placed the byte/word on the data bus and is ready to complete the data transfer cycle. When the host negates $\overline{BACK}$ and $\overline{RD}$, EtherStar moves its internal pointer to point to the next byte/word, and then re-asserts BREQ to repeat the process. The DMA controller must assert the End of Process input, EOP, concurrent with the last byte/word data transfer to indicate that the entire packet has been transferred. EtherStar will then discontinue making further data requests. RENA must be cleared when the packet transfer is completed, and set again when the host desires to begin reading another packet from the receive buffer using DMA.

When EOP is asserted by the external DMA controller, the EOP status bit, BMPR4<2>, will be set to a '1' and will cause $\overline{RINT}$ to be asserted if BMPR4<3>, EOP_INT_MSK, is set. This interrupt can be used by the host to clear RENA. The interrupt is cleared by writing to BMPR4 with bit 2 set, which can be done at the same time as RENA is cleared.

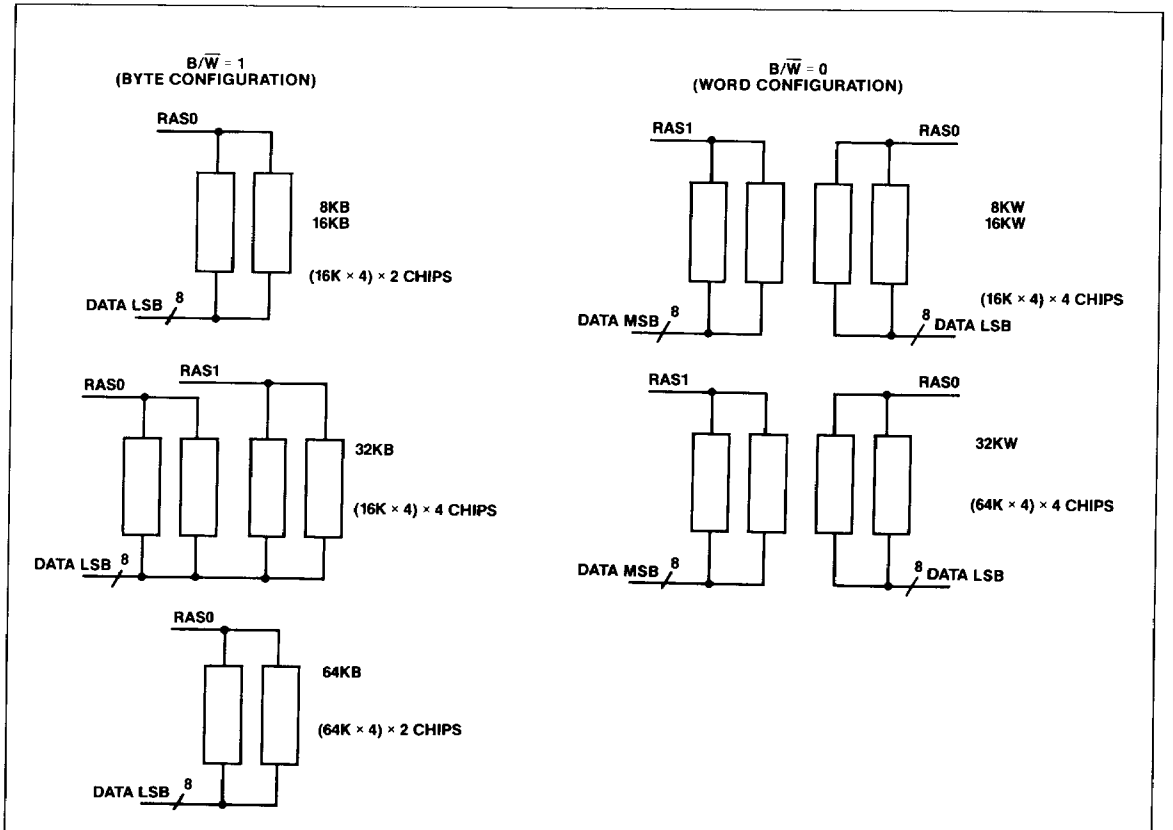


Figure 9. Buffer Memory Implementation with DRAM

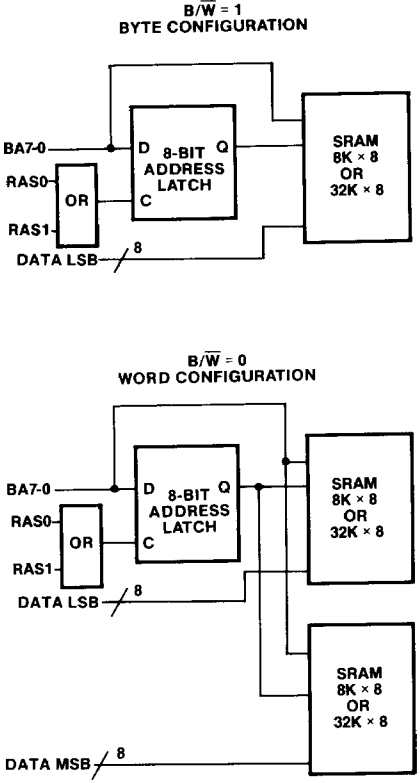


Figure 10. Buffer Memory Implementation with SRAM

BUFFER MEMORY IMPLEMENTATION

EtherStar is configured via the BS0 and BS1 inputs to support buffer memory sizes of 8, 16, 32 or 64 Kbytes. Figures 9 and 10 illustrate the typical implementation of the buffer memory for these options in both byte and word modes using industry standard DRAMs and SRAMs, respectively. Table 6 describes the relationship between the internal address lines A15:A0 and the multiplexed buffer addresses BA7:BA0.

Although not necessary for operational purposes, it is useful for debugging and diagnostic purposes to describe how the network side and the system side access the buffer.

NETWORK ACCESS

The network side always transfers a byte at a time to or from the buffer.

In **word** mode (B/$\overline{W}$ = 0), $\overline{RAS0}$ is asserted for each LS byte transferred to or from the buffer and $\overline{RAS1}$ is asserted for each MS byte transferred to or from the buffer.

In **byte** mode (B/$\overline{W}$ = 1), for 8, 16 or 64 Kbyte configurations, $\overline{RAS0}$ is asserted for every byte transferred to or from the buffer. For 32 Kbyte configuration, $\overline{RAS0}$ is asserted during even byte transfers (A0 = 0), while $\overline{RAS1}$ is asserted during odd byte transfers (A0 = 1).

SYSTEM ACCESS

The system side transfers either a byte at a time or a word at a time to or from the buffer, depending on the mode selected.

In **word** mode (B/$\overline{W}$ = 0), both $\overline{RAS0}$ and $\overline{RAS1}$ are asserted for each word transferred to or from the buffer. It is not possible to address the bytes separately for this mode.

In **byte** mode (B/$\overline{W}$ = 1), for 8, 16 or 64 Kbyte configurations, $\overline{RAS0}$ is asserted for every byte tranferred to or from the buffer. For 32 Kbyte configuration, $\overline{RAS0}$ is asserted during even byte transfers (A0 = 0), while $\overline{RAS1}$ is asserted during odd byte transfers (A0 = 1).

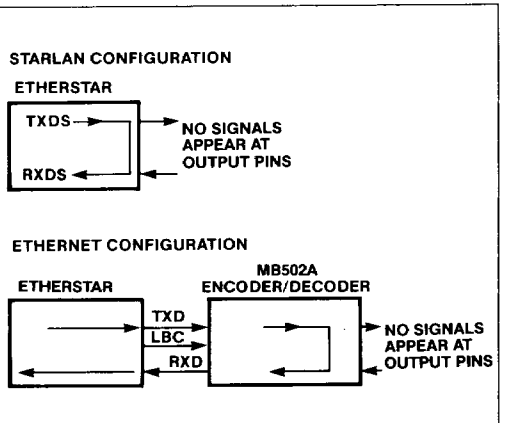


Figure 11. Loopback Operation

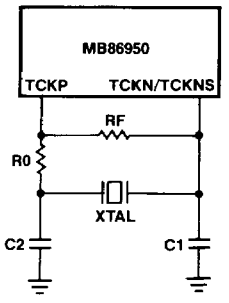


Figure 12. Crystal Connection for StarLAN Mode

LOOPBACK

A loopback capability is provided to allow operation of EtherStar to be exercised without sending signals onto the LAN media. The loopback function is invoked by clearing the $\overline{\text{LBC}}$ bit, DLCR4<1>, to a zero. The complement of this bit appears at the Loopback output, LBC. Operation is illustrated in figure 11.

In StarLAN mode, the TXDS output is internally tied back to the RXDS input. The transmit data is blocked from appearing at the TXDS pin, and the RXDS and $\overline{\text{XCOL}}$ inputs are ignored. Data is routed from the transmit buffer, through the transmit section of the DLC, through the internal Manchester encoder, back to the Manchester decoder, through the receive section of the DLC, and is then stored in a receive buffer.

In Ethernet mode, operation is similar, except that the data is output on TXD and received at RXD. The external Manchester encoder/decoder, such as the Fujitsu MB502A, should respond to assertion of its LBC input by looping its transmitter output to its receiver input internally, and should block the transmit data from appearing at its output pin.

CRYSTAL OSCILLATOR

The MB86950 requires a precise 10MHz clock source for proper operation. In Ethernet mode, this signal is normally supplied from the external encoder/decoder. In StarLAN mode, the signal may be supplied externally, or may be generated from a crystal by connecting the crystal as shown in figure 12.

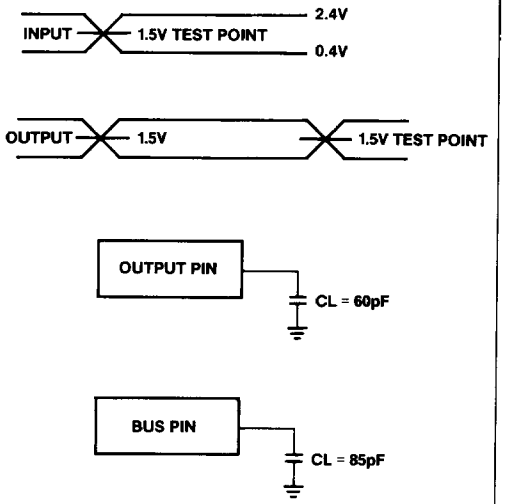


Figure 13. Test Conditions

Table 6. Address Multiplexing on Buffer Address Outputs

External / Internal	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
RAS ADDRESS	A13	A12	A11	A10	A9	A8	A7	A6
CAS ADDRESS	A15	A5	A4	A3	A2	A1	A0	A14

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1,4]

Symbol	Parameter	Min.	Max.	Units
VCC	Supply Voltage	-0.3	6.0	V
VIN[2]	DC Input Voltage	-0.3	VCC + 0.3	V
VOUT	DC Output Voltage	-0.3	VCC + 0.3	V
TSTG	Storage Temperature	-40	150	°C
PWD	Power Dissipation		500	mW

DC SPECIFICATIONS[3,4] T_A = 0°C to 70°C, VCC = 5V ±5%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIL	Low Level Input Voltage		0		0.8	V
VIH	High Level Input Voltage		2.2		VCC	V
VOL	Low Level Output Voltage All Except BREQ BREQ	 IOL = 3.2mA IOL = 12.8mA	 0 0		 0.4 0.4	 V V
VOH	High Level Output Voltage All Except BREQ BREQ	 IOH = -0.4mA IOL = -10.0mA	 4.2 4.2		 VCC VCC	 V V
ILI	Input Leakage Current	VI = 0 or VCC	-10		10	μA
ILZ	Three-State Output Leakage Current	VO = 0 or VCC	-10		10	μA
ICC[6]	Operating VCC Supply Current	No Output Load TCKN = 10MHz RCKN = 10MHz		25	40	mA
ICCS	Static VCC Supply Current	All Inputs Static VI = 0 or VCC			100	μA

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
4. All voltage measurements are referenced to ground (GND). All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V. See figure 13.
6. Limited functional test patterns are performed during device testing for this parameter.

AC CHARACTERISTICS[3, 4, 5] VCC = 5.0V ±5%, TA = 0°C to 70°C

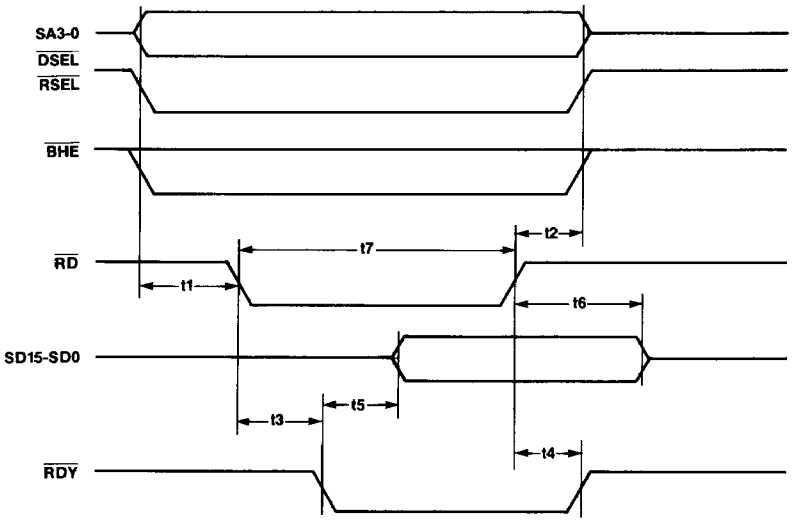


Figure 14. Read Timing

Reference: Figure 14

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	tAVRL	Address, select and control valid to read low	10			ns
t2	tRHAI	Read high to address, select and control invalid	10			ns
t3	tRLRL	Read low to $\overline{RDY}$ low			35[7]	ns
t4	tRHRH	Read high to $\overline{RDY}$ high			35	ns
t5	tRLDV	$\overline{RDY}$ low to data valid			22	ns
t6	tRHDT	Read high to data three state	12		45	ns
t7	tRDW	Read pulse width	35			ns

3. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
4. All voltage measurements are referenced to ground (GND). All time measurments are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V. See figure 13.
5. AC test condition: for bidirectional busses (SD0-SD15, BD0-BD15) CL = 85pF, for all other outputs CL = 60pF. See figure 13.
7. When reading from the buffer memory port, BMPR0, a worst case time of 2.25μsec may occur if the buffer manager is required to service simultaneous access requests from the system, the refresh controller, and the network (operating in loopback mode). The worst case time is 2.4μsec if the system attempts to read an empty receive buffer memory. A BUS_RD_ERR will occur in the latter case.

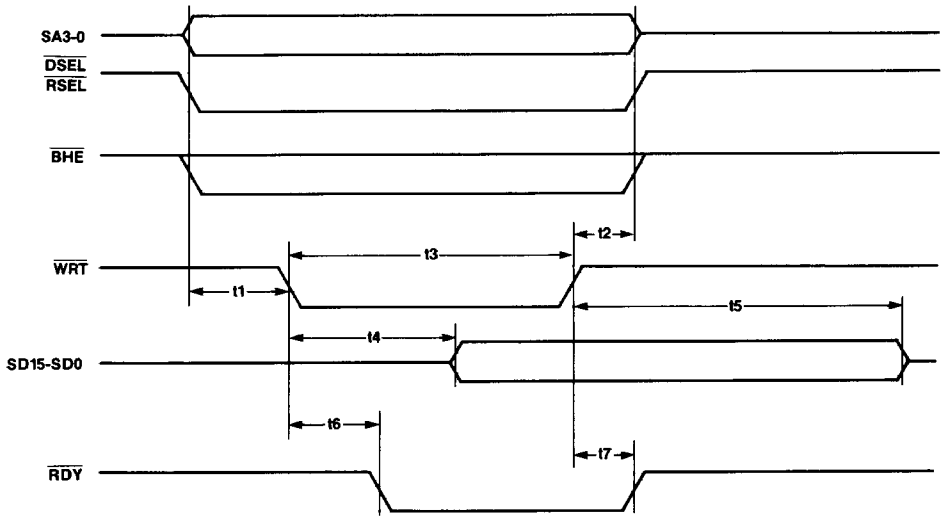


Figure 15. Write Timing

Reference: Figure 15

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	tAVWL	Address, select and control valid to write low	10			ns
t2	tWHAI	Write high to address, select and control invalid	10			ns
t3	tWRW	Write pulse width	35			ns
t4	tDS	Write low to data valid			5	ns
t5	tDH	Write high to data invalid	30			ns
t6	tWLRL	Write low to $\overline{RDY}$ low			35[8]	ns
t7	tWHRH	Write high to $\overline{RDY}$ high			35	ns

8. When writing to the buffer memory port, BMPR0, a worst case time of 2.25μsec may occur if the buffer manager is required to service simultaneous access requests from the system, the refresh controller, and the network (operating in loopback mode). The worst case time is 2.4μsec if the system atempts to write to a full transmit buffer memory. A BUS_WR_ERR will occur in the latter case.

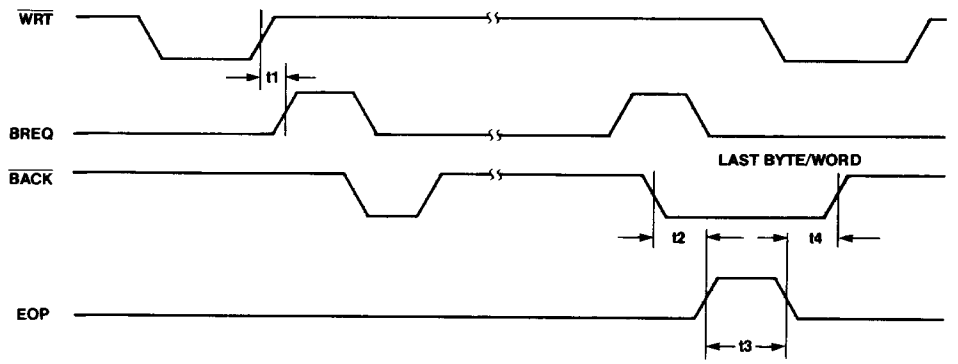


Figure 16. BREQ, $\overline{\text{BACK}}$ and EOP DMA Timing

Reference: Figure 16

Symbol	Parameter	Parameter Description	Min	Typ	Max	Units
t1	tWHBRH	Write high to bus request high	23		62	ns
t2	tBALEH	Bus acknowledge low to end of process high	10			ns
t3	tEPW	End of process pulse width	20			ns
t4	tELBAH	End of process low to bus acknowledge high	10			ns

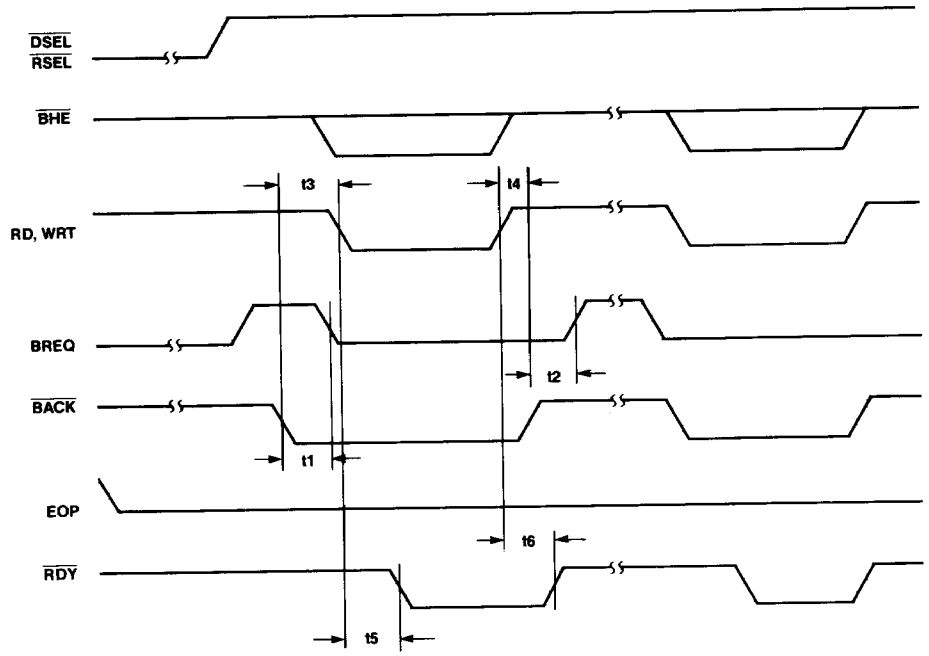


Figure 17. DMA Read and Write Timing

Reference: Figure 17

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	tBALBRL	Bus acknowledge low to bus request low			35	ns
t2	tBAHBRH	Bus acknowledge high to bus request high	8		50[9]	ns
t3	tBAWS	Bus acknowledge low to read/write low	10			ns
t4	tBAWH	Read/write high to bus acknowledge high	10			ns
t5	tRWLRL	Read/write low to $\overline{RDY}$ low			35	ns
t6	tRWLRH	Read/write high to $\overline{RDY}$ high			35	ns

9. A worst case time of 2.25μsec may occur if the buffer manager is required to service simultaneous access requests from the system, the refresh controller, and the network (operating in loopback mode).

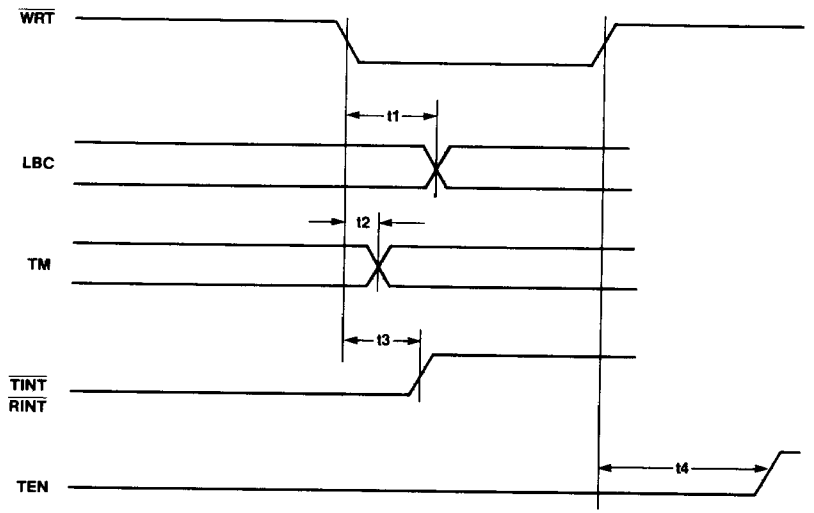


Figure 18. LBC, TM, TINT AND TINT Timing

Reference: Figure 18

Symbol	Parameter	Description	Min.	Typ.	Max.	Units
t1	tLBCD	Loopback control delay	30		90	ns
t2	tTMD	Test mode signal delay	30		80	ns
t3	tINTD	Interrupt signal mask/clear delay	30		80	ns
t4	tTEND	Transmit enable delay		2.3[10]		μs

10.This timing assumes that the network is free.

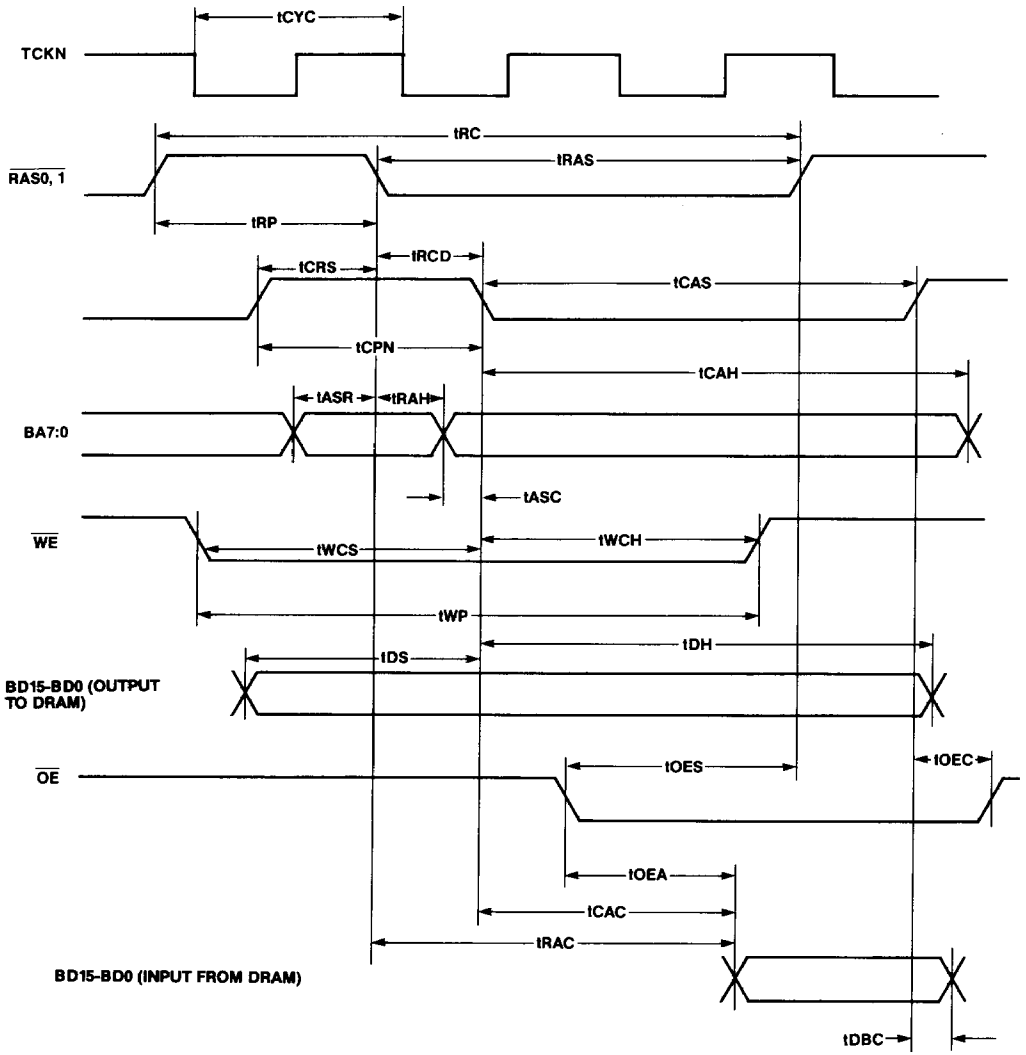


Figure 19. DRAM Interface Timing

Reference: Figure 19

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
tCYC	TCKN cycle		100		ns
tRC	Random read/write cycle		300		ns
tRAC	Access time from $\overline{RAS}$			150	ns
tCAC	Access time from $\overline{CAS}$			100	ns
tOEA	Access time from $\overline{OE}$			90	ns
tDBC	Data hold before $\overline{CAS}$ high	-8			ns
tRP	$\overline{RAS}$ precharge time	100			ns
tRAS	$\overline{RAS}$ pulse width	165			ns
tCPN	$\overline{CAS}$ precharge time	100			ns
tCAS	$\overline{CAS}$ pulse width	160			ns
tASR	Row address setup time	45			ns
tRAH	Row address hold time	23			ns
tASC	Column address setup time	11			ns
tCAH	Column address hold time	166			ns
tWCS	Write command setup time	50			ns
tWCH	Write command hold time	108			ns
tWP	Write command pulse width	185			ns
tDS	Data to $\overline{CAS}$ setup time	55			ns
tDH	Data from $\overline{CAS}$ hold time	120			ns
tOES	$\overline{OE}$ to $\overline{RAS}$ inactive setup time	80			ns
tRCD	$\overline{RAS}$ to $\overline{CAS}$ delay time	50		68	ns
tOEC	$\overline{OE}$ to $\overline{CAS}$ high	6			ns
tCRS	$\overline{CAS}$ to $\overline{RAS}$ setup time	55			ns

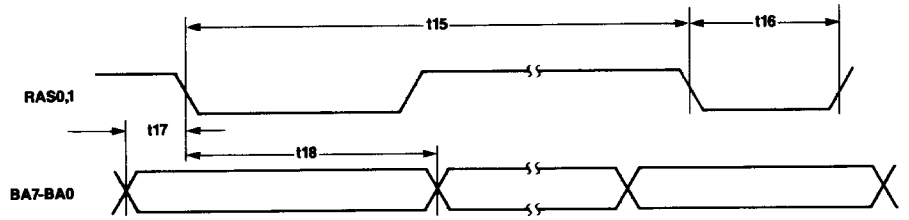


Figure 20. DRAM Refresh Timing

Reference: Figure 20

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t15	tRHC	Refresh cycle		15.5		μs
t16	tRAS	$\overline{RAS}$ pulse width	165			ns
t17	tASR	Row address set up time	45			ns
t18	tRAH	Row address hold time	150			ns

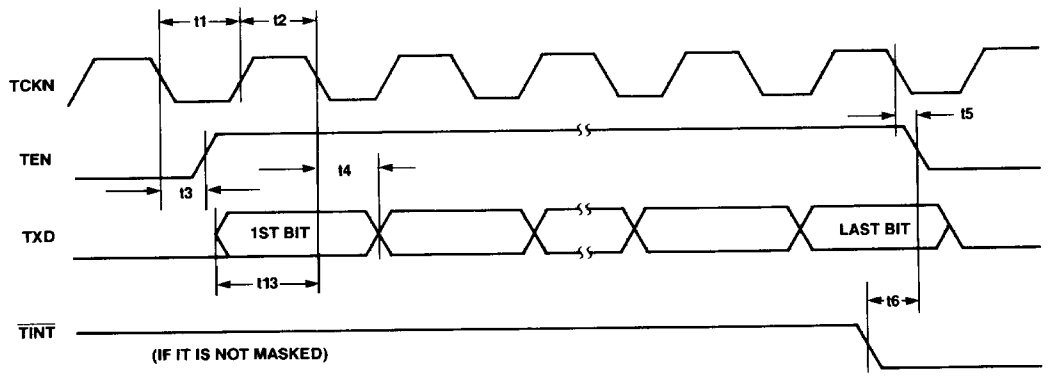


Figure 21. Transmit in Ethernet Configuration

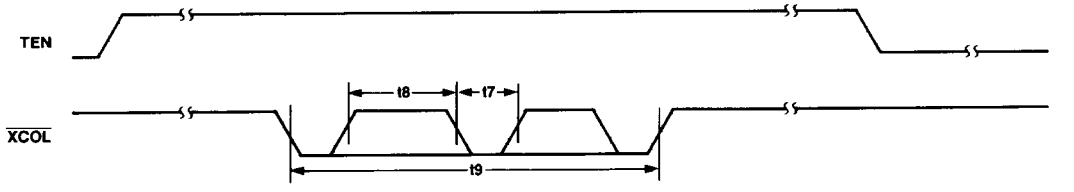


Figure 22. Collision Timing

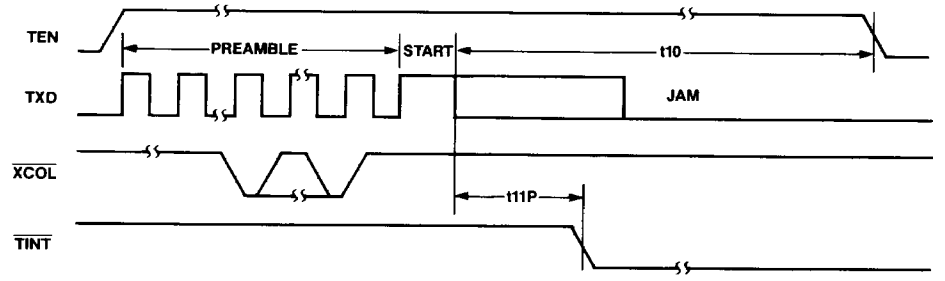


Figure 23. Collision at the Preamble Field

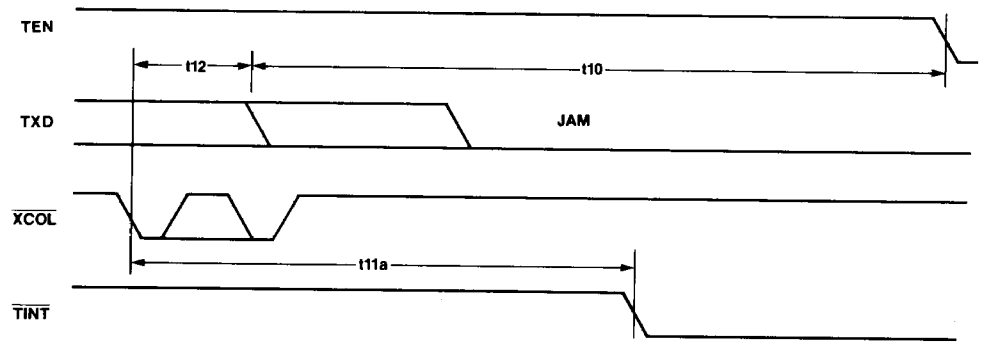


Figure 24. Collision at the Data Field

Reference: Figures 21-24

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	tTCL	Transmit clock low width	35	50		ns
t2	tTCH	Transmit clock high width	35	50		ns
t3	tTED	TCKN low to transmit enable			52	ns
t4	tTDH	Transmit data hold	12			ns
t5	tTEH	Transmit enable hold	13			ns
t6	tTINT	Transmit interrupt to transmit enable low		1		TCKN cycles
t7	tCOLW	Collision detect width	20			ns
t8	tCOLS	Collision inactive spacing			200	ns
t9	tCOLL	Minimum collision length	520			ns
t10	tJAM	Jam period[11]		32		TCKN cycles
t11p	tINTP	Transmit interrupt when collision at preamble		5		TCKN cycles
t11a	tINTA	Transmit interrupt when collision at data field		16		TCKN cycles
t12	tCJ	Collision to first jam bit	4		12	TCKN cycles
t13	tTDS	Transmit data setup	40			ns

11. The 32 jam bits include eight data bits and 24 '0' bits.

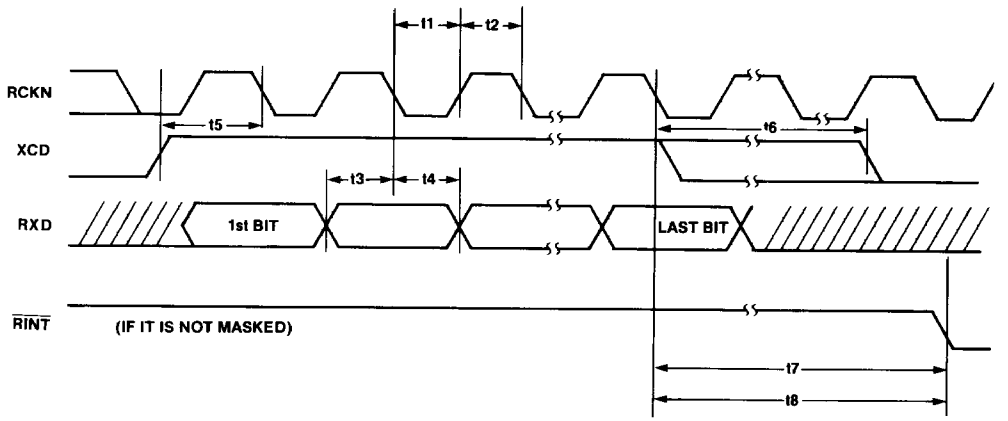


Figure 25. Receive in Ethernet Configuration

Reference: Figure 25

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	tRCL	Receive clock low width	35	50		ns
t2	tRCH	Receive clock high width	35	50		ns
t3	tRDS	Receive data setup	10			ns
t4	tRDH	Receive data hold	10			ns
t5	tRCSS	Receive carrier sense setup	10			ns
t6	tRCSH	Receive carrier sense hold	12		7	ns RCKN cycles
t7	tRINTG	Last bit of good packet received to interrupt		40		RCKN cycles
t8	tRINTE	Receive interrupt after bad packet		15		RCKN cycles

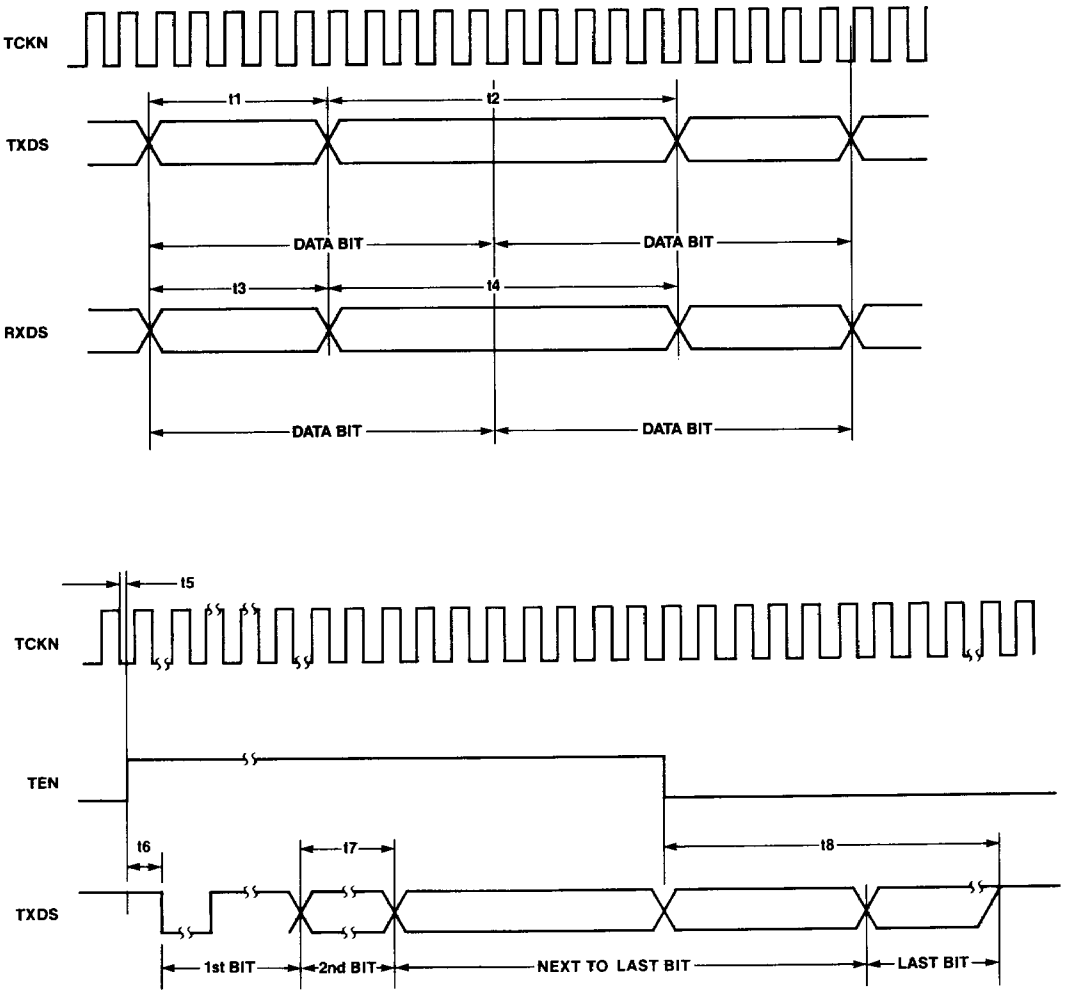


Figure 26. StarLAN Transmit and Receive Timing

Reference: Figure 26

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	tTXS	Transmit width short	4.95		5.05	TCKN cycles
t2	tTXL	Transmit width long	9.95		10.05	TCKN cycles
t3	tRXS	Receive width short	4.1		5.9	TCKN cycles
t4	tRXL	Receive width long	9.1		10.9	TCKN cycles
t5	tCLTE	TCKN low to transmit enable			50	ns
t6	tTAFM	TEN active to first bit Manchester code		10		TCKN cycles
t7	tTWL	Transmit width length		10		TCKN cycles
t8	tTILM	TEN inactive to last bit Manchester code		15		TCKN cycles

EtherStar is a trademark of Fujitsu Microelectronics, Inc.
StarLAN is a trademark of AT&T.

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Consequently, complete information sufficient for design purposes is not necessarily given.

Fujitsu Limited and its subsidiaries reserve the right to change products or specifications without notice. **Fujitsu advises its customers to obtain the latest version of device specifications to verify, before placing orders, that the information being relied upon by the customer is current.**

The information contained in this document does not convey any license under copyrights, patent rights or trademarks claimed and owned by Fujitsu Limited or its subsidiaries. Fujitsu assumes no liability for Fujitsu applications assistance, customer's product design, or infringement of patents arising from use of semiconductor devices in such systems' designs. Nor does Fujitsu warrant or represent that any patent right, copyright, or other intellectual property right of Fujitsu covering or relating to any combination, machine, or process in which such semiconductor devices might be or are used.

Fujitsu Microelectronics, Inc.'s Advanced Products Division's products are not authorized for use in life support devices or systems. Life support devices or systems are devices or systems which are:

1. Intended for surgical implant into the human body.
2. Designed to support or sustain life; and when properly used according to label instructions, can reasonably be expected to cause significant injury to the user in the event of failure.

The information contained in this document has been carefully checked and is believed to be entirely accurate. However, Fujitsu Limited and Fujitsu Microelectronics, Inc. assume no responsibility for inaccuracies.

This document is published by the marketing department of Fujitsu Microelectronics, Inc., Advanced Products Division, 50 Rio Robles, Bldg. 3, San Jose, California, U.S.A. 95134-1806.

Printed in the U.S.A.