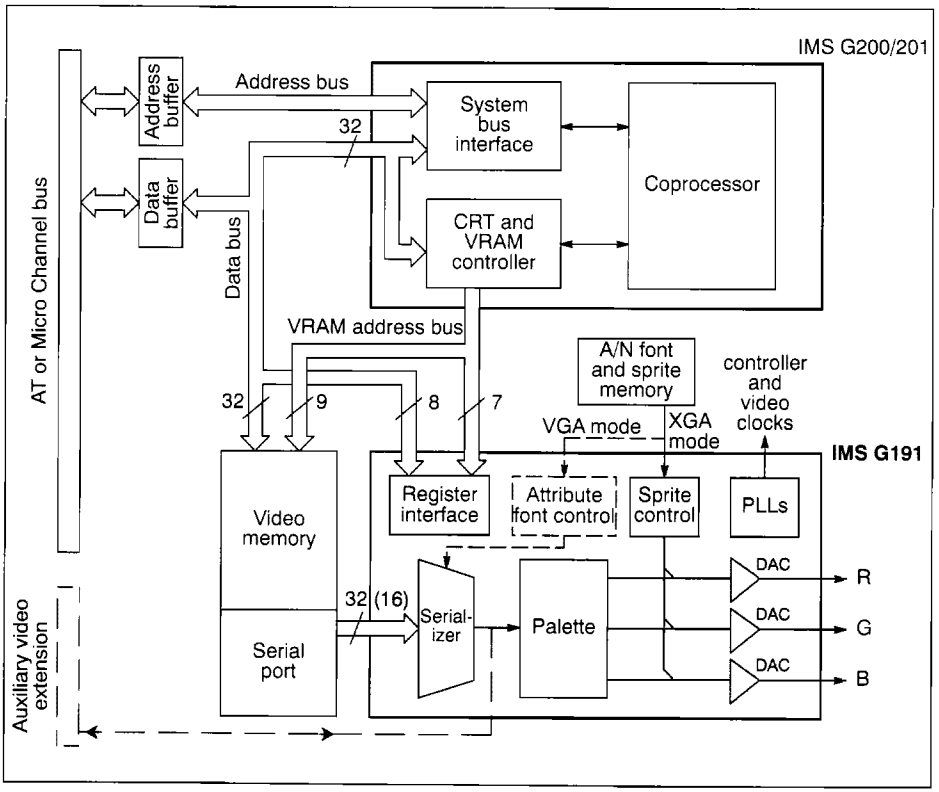
XGA SERIALIZER PALETTE-DAC



FEATURES

- 90 MHz operation
- 8-bit DACs
- 256×24-bit color palette
- 32 or 16-bit serializer input
- 1, 2, 4, 8 and 16 bits per pixel operation
- Post-palette hardware sprite
- Supports higher refresh rates to meet ISO standards
- 1280×1024 with 256 colors (interlaced), 800×600 with 65,536 colors (non-interlaced) and 1024×768 with 256 colors (non-interlaced)
- On-chip PLL clock generators
- On-chip DAC comparators
- 208-pin CQFP package
- Functional superset of IMS G190

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20.1 Detailed IMS G191 block diagram

Figure 20.1 shows the main functional units of the IMS G191 with all pin connections. The following sections of this document include pin details, a description of each of the functional units which make up the IMS G191, and package details.

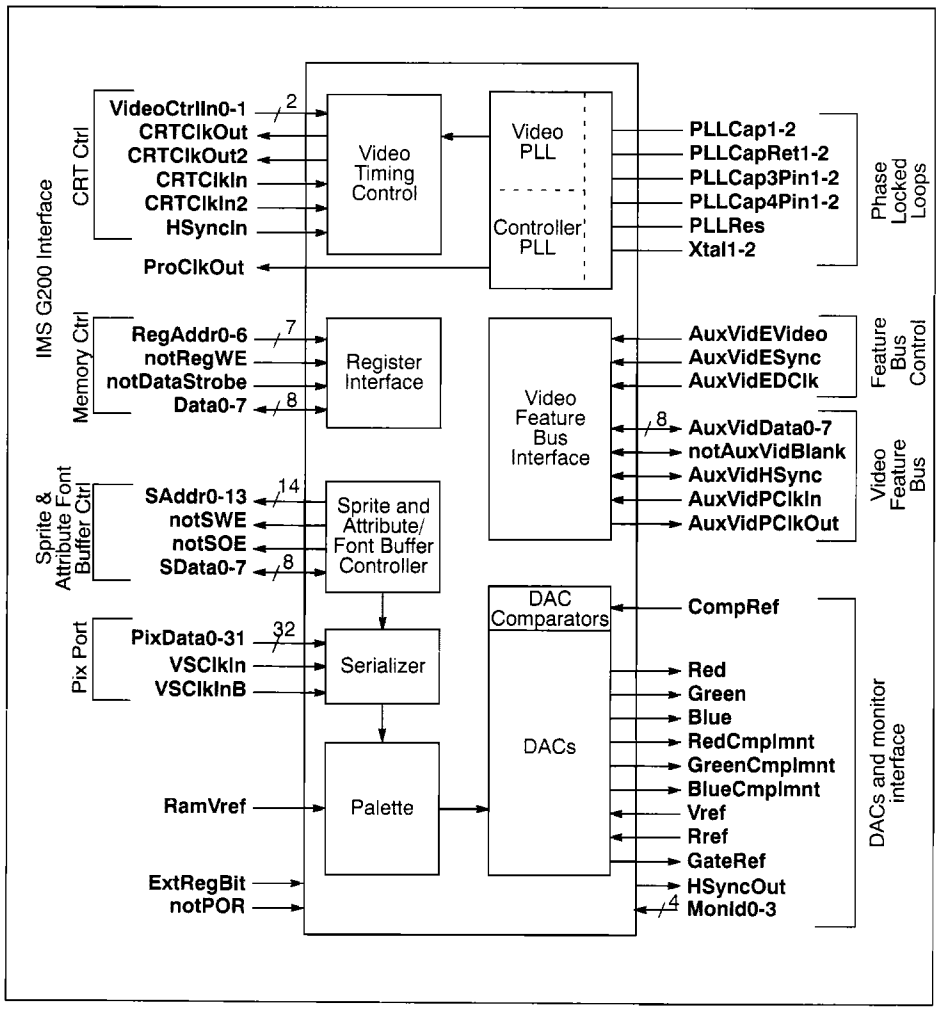


Figure 20.1 IMS G191 block diagram

20.2 Pin function reference guide

Signal names are prefixed by **not** if they are active low, otherwise they are active high.

20.2.1 IMS G200 interface

Signal	I/O	Description
RegAddr0-6	I	These pins provide the address of parameter registers in the IMS G191. They are driven by bits 6:0 of the VRAM address bus generated by the IMS G200. **RegAddr0-6** also carry the control codes, at the start of each line, which indicate the vertical status of the line to be displayed. Together with **VideoCtrlIn0-1,** they allow each line to be displayed correctly.
notRegWE	I	A low level on this pin indicates that the addressed parameter register is being written to, a high level indicates that it is being read. It is driven by bit 8 of the VRAM address bus generated by the IMS G200.
notDataStrobe	I	A low level on this pin indicates that the IMS G191 should perform the action defined by the **RegAddr** and **notRegWE** inputs. This is a signal unique to the IMS G191 generated by the IMS G200.
VideoCtrlIn0-1	I	The levels on these pins, driven by the IMS G200, are encoded to indicate events on a horizontal scan line. **VideoCtrlIn**(1:0)= 00 Blanking 01 Border 10 Picture 11 Picture and start of cursor
Data0-7	I/O	The data from a parameter register being read is put onto these pins by the IMS G191; the data on these pins is used by the IMS G191 when its parameter registers are being written. This data is received/driven by the IMS G200 on the low order eight bits of the data bus which goes to the VRAMs and (via buffers) to the Micro Channel bus.
CRTClkOut **CRTClkIn**	O I	The CRTC clock, driven out from the **CRTClkOut** pin, is generated in the IMS G191 by dividing the pixel clock by the video clock scale factor (see Section 20.3.8). The **CRTClkOut** pin should be connected to **CRTClkIn** in order to drive internal clocks of the IMS G191.
CRTClkOut2 **CRTClkIn2**	O I	**CRTClkOut2** is a divided version of the CRTC clock. It is always half the frequency of **CRTClkOut** in 8bpp modes. In 9bpp modes it continues to be half this frequency but the 'mark' or 'space' is extended by 1 CRTC cycle every 9 CRTC clock cycles. The **CRTClkOut2** pin should be connected to **CRTClkIn2** in order to drive internal clocks of the IMS G191.
ProClkOut	O	This pin is the output of the second phase locked loop oscillator of frequency 40MHz. It should be used as the controller clock for the IMS G200.
HSyncIn	I	This pin is driven by the IMS G200 horizontal sync signal, **MonHSync**.

20.2.2 Auxiliary Video Extension

Signal	I/O	Description
AuxVidEVideo	I	A high level on this pin means that the IMS G191 will drive the **AuxVidData** pins. A low level will make the IMS G191 receive data on the **AuxVidData** pins. **AuxVidEVideo** is pulled to a high level by a 5KΩ 20% resistor external to the IMS G191.
AuxVidESync	I	A high level on this pin means that the IMS G191 will drive the **notAuxVidBlank** and **AuxVidHSync** pins. A low level will make the IMS G191 receive data on these pins. **AuxVidESync** is pulled to a high level by a 5KΩ 20% resistor external to the IMS G191.
AuxVidEDClk	I	A high level on this pin means that the IMS G191 will drive the **AuxVidPClkOut** pin. A low level will make the IMS G191 receive a clock on the **AuxVidPClkIn** pin. **AuxVidEDClk** is pulled to a high level by a 5KΩ 20% resistor external to the IMS G191.
AuxVidData0-7 **notAuxVidBlank** **AuxVidHSync** **AuxVidPClkIn** **AuxVidPClkOut**	I/O	These pins are part of the video feature interface. Their function is as defined by IBM Micro Channel architecture. The **AuxVidPClkIn** and **AuxVidPClkOut** pins should be joined together and connected to the VF DCLK line on the feature bus.

20.2.3 Pixel port

Signal	I/O	Description
PixData0-31	I	The IMS G191 receives video data from the VRAMs on these pins. They are driven by the serial outputs of the VRAMs.
VSClkInB **VSClkIn**	I I	A low level on the buffered VRAM serial clock input pin, **VSClkInB**, strobes the VRAM serial data into the IMS G191. The rising edge of the unbuffered VRAM serial clock input pin, **VSClkIn**, clocks the serial clock counter in the IMS G191. **VSClkIn** is generated by the IMS G200 and is then buffered on the card to drive the serial clock inputs of the VRAMs and the IMS G191 buffered serial clock input (**VSClkInB**).

20.2.4 Sprite and attribute font buffer controller

Signal	I/O	Description
SData0-7	I/O	These pins are used to transfer data to and from the static RAM which holds the character fonts in VGA mode and the sprite definition in extended mode.
SAddr0-13	O	SRAM address bus driven by the IMS G191.
notSOE	O	SRAM output enable
notSWE	O	SRAM write enable

20.2.5 Monitor Interface and DACs

Signal	I/O	Description
Red **Green** **Blue**	O O O	These pins output currents proportional to the intensity value being presented to the 8-bit DACs. Each output is intended to drive a 50Ω load, comprising a 150Ω termination resistor at the IMS G191 in parallel with a 75Ω termination resistor in the monitor.
RedCmpImnt **GreenCmpImnt** **BlueCmpImnt**	O O O	These pins output currents equal to the full scale current less the current being output on the corresponding **Red Green** or **Blue** pin. If complementary video signals are not needed these pins may be connected directly to analog ground.
Vref **Rref**	I I	These pins are used to define the full-scale DAC output current. **Vref** should be connected to a voltage reference device generating 2.5 volts above analog ground. **Rref** should be connected to analog ground via a 1.73KΩ resistor. Both these pins should be decoupled to analog ground via 10nF ceramic capacitors. With these values of **Vref** and **Rref** the full scale output will be 0.7V into 50Ω.
GateRef	O	This pin must be decoupled to **AVDD** by a 10nF ceramic capacitor.
CompRef	I	The voltage on this pin provides the DAC comparator reference voltage. This is normally set to half the full scale video output voltage. Three analog comparators compare the voltage on the three video outputs with the voltage on this pin. The state of these comparators may be read through the Display ID and comparator register (#52). The comparator function is intended for test purposes only.
HSyncOut	O	**HSyncOut** drives the horizontal sync line of the monitor interface. This pin supplies a signal equivalent to that input on **HSyncIn**, but is delayed in some modes by an appropriate amount to match the additional delay on the video data passing through the IMS G191 compared to the IMS G190. If the video feature bus is enabled and is driving the **AuxVidHSync** pin then the signal on **AuxVidHSync** will also appear on **HSyncOut**.
MonId0-3	I	The levels on these pins may be read via one of the parameter registers. These pins are pulled to high levels by 5KΩ 20% resistors external to the IMS G191.

20.2.6 Miscellaneous analogue signals

Signal	Description
RamVref	This pin provides a reference voltage to the palette RAM. It should be connected to a voltage reference device generating 2.5V above ground and decoupled to logic ground by a 10nF ceramic capacitor.

20.2.7 Miscellaneous digital signals

Signal	I/O	Description
ExtRegBit	I	This input provides compatibility between the IMS G191 and IMS G200 processors for clock selection in 132 column mode. It is connected to the bit 7 output of an on-card external register (register address #70). IMS G191 now implements bit 7 of this register internally. This is ORed with the value on the **ExtRegBit** pin to select the appropriate clock frequency for 132 column text mode.
notPOR	I	A low level on this pin initializes the phase locked loop and various latches on the IMS G191. If the IMS G200 is using the **ProClkOut** output of the IMS G191 for its controller clock, the phase locked loop oscillator must be running correctly before channel reset ends. A CMOS level receiver with hysteresis is used for this input so that in many cases it may be driven by a simple RC network between +5V and ground.

20.2.8 Phase locked loop signals

Signal	Description
PLLCap1-2, PLLCapRet1-2 PLLCap3Pin1-2 PLLCap4Pin1-2	These pins should be connected to the phase locked loop filter components. See Section 20.6.5 for details.
PLLRes	This pin should be connected to analog +5V by a 8.7KΩ resistor.
Xtal1-2	These pins should be connected to a 4MHz crystal for use as a reference by the phase locked loop oscillators. See Section 20.6.5 for details of external circuitry relating to the **Xtal1-2** pins. Note that pin 181 (**Xtal1**) should be connected to pin 187 (**Reserved**) to ensure reliable starting of the phase locked loop oscillator.

20.2.9 Supplies

Signal	Description
VDD	Digital VDD
GND	Digital GND
AVDD	A specially decoupled analog +5V supply should be provided. This should be fed from the regular +5V plane via a 1μH choke, and decoupled to the analog ground plane by bulk decoupling and ceramic high-frequency decoupling capacitors.
AGND	A separate analog ground plane should be provided, joined to the regular ground plane at only one point. Only those components associated with the analog circuitry should be placed over and connected to the analog ground plane.
PGND	A separate phase-locked loop (PLL) ground plane should be provided, joined to the regular ground plane at only one point. Only those components associated with the PLL circuitry should be placed over and connected to the PLL ground plane.

20.3 Device description

The IMS G191 Serializer Palette DAC chip, part of the SGS-Thomson XGA chipset family, is designed to operate in an XGA display adapter subsystem in conjunction with an IMS G200 XGA controller chip.

The IMS G191 offers the following enhancements over the IMS G190 whilst maintaining software compatibility:

IMS G191	IMS G190
8-bit DACs	6-bit DACs
90MHz operation	50MHz operation
256×24-bit color palette	256×18-bit color palette
On-chip PLL clock generators (video PLL is programmable)	Multiple external crystal controlled clocks
1024×768 non-interlaced mode at 75Hz	–

The IMS G200 and IMS G191 together support a full XGA and VGA register set. All VGA modes and the 132 column text mode are supported, regardless of the amount of video memory installed. They also support the Extended Graphics Mode (extended mode) at a screen resolution of up to 1024×768 with 256 colors, depending on the amount of video memory.

20.3.1 The serializer, palette and DAC

The serializer takes data from the serial port of video memory in 16 or 32-bit widths (depending on the amount of video memory installed) and converts it to a serial stream of pixel data. In pseudo color modes the pixel data is used to address a palette location containing the color value. The color value is then passed to the DAC, which converts the digital information into analog red, green, and blue signals to the display.

In the 16 bits per pixel direct color mode the pixel data does not address the color palette but is fed directly to the DACs. The pixel data contains three fields in 565 format (5 bits for Red, 6 bits for Green and 5 bits for Blue).

20.3.2 Attribute controller

The attribute controller works together with the font and sprite memory and CRT controller (CRTC) to control the color selection and character generation in the 132-column text mode and VGA text modes.

20.3.3 Palette

The palette is used to translate the pixel value to a displayed color. It has 256 locations, each containing red, green and blue color values in 3 8-bit fields.

Before the pixel value is used to address the palette it is masked by the palette mask register; all bits in the pixel address corresponding to zeros in the palette mask register are forced to zero before reaching the palette.

20.3.4 Sprite controller

This component is used to display and control the position and image of the sprite (or cursor). The sprite is not available in 132-column text mode or VGA modes.

The sprite is a 64×64 pixel image stored in the XGA Sprite buffer. When active, it overlays the picture being displayed. Each 2 bit pixel can take on one of four values, setting the pixel appearance to be one of two preprogrammed colors, transparent or the one's complement of the underlying pixel color. These pixel values can be used to enable the sprite to achieve the effect of a colored marker of arbitrary shape. The sprite is overlaid on the picture, post-palette, and does not appear at the video feature interface.

20.3.5 16 bpp direct color mode

In the 16 bits per pixel direct color mode supported by XGA the pixel data contains three fields in 565 format (5 bits for Red, 6 bits for Green and 5 bits for Blue). This data does not address the color palette but is fed directly to the DACs. The IMS G191 maintains compatibility with the 16 bpp direct color mode implemented in the IMS G190.

20.3.6 Video DACs

The IMS G191 incorporates a triple 8-bit video DAC. The output levels are set by an external voltage reference input in combination with an external resistor.

20.3.7 DAC comparators

The DAC outputs are connected to inputs of three comparators internal to the IMS G191, one for each DAC. The output of the comparators may be read back through the Display ID and comparator register (Index #52). The comparators can be used to detect faults with the IMS G191 circuitry or the off-chip DAC reference. The comparator function is intended for test purposes only.

The reference input of each comparator is connected to the **CompRef** pin. The reference voltage applied is normally 0.35V, which is half way between the DAC high and low levels. The comparator polarity is a high output when the DAC output voltage is less than this reference.

The system is toleranced so that, under the conditions shown in Table 20.1, the comparator outputs are guarenteed to be high for DAC inputs between #0 and #66 and low for inputs between #9A to #FF.

Comparator output	DAC input	DAC output (nominal I)	DAC output (nominal V)
High	0-#66 (steps 0 to 102)	≤5.55mA	≤0.28V
Low	#9A - #FF (steps 154 to 255)	≥8.44mA	≥0.42V
Notes: Nominal DAC full scale output = 14mA, nominal DAC load = 150‖75 ohms (=50 ohms)			

Table 20.1 Conditions for specified comparator outputs

20.3.8 Clock generation and select

Phase locked loop oscillators

The IMS G191 implements two phase locked loop (PLL) oscillators as sources for the following clocks:

- IMS G200 controller clock (40MHz)
- IMS G191 video clock (frequency range 20 - 90MHz)

The use of PLL oscillators removes the need for multiple crystal oscillators external to the device. The controller clock, output from the **ProClkOut** pin of the IMS G191, is automatically set to 40MHz at power-on or reset.

The frequency of the video clock PLL is programmed through the XGA registers. The Fixed clock address and data registers (Indexes #56 and #57) provide access to a number of registers used to set the the controller clock frequency and the video clock frequencies for existing XGA and VGA applications. These registers should **not** be modified, except at power-on or reset. The directly addressed Programmed pixel clock frequency register enables the video clock frequency to be set for other display modes. Further details are given in Section 20.4.2. Note that to avoid interference between the two phase locked loops, the video clock PLL should not be set to the same frequency (i.e. 40MHz) as the controller clock PLL.

The phase locked loops require a number of external components which are detailed in Section 20.6.5. The specification of the PLL oscillators are given in Table 20.21.

Video clock scale factor

The video clock output frequency is divided by the 'video clock scale factor' as selected by the Clock frequency select 1 register (bits 1:0, index #54), according to the mode of operation. This generates the 'CRTC clock', which must be between 20 and 45MHz. This clock is driven out through the **CRTClkOut** pin to drive the CRTC in the XGA display controller (IMS G200). **CRTClkOut** is also fed back into the IMS G191 via the card.

The CRTC clock in IMS G191 is divided by 2 to generate **CRTClkOut2**. The CRTC clocks are used in the display controller to produce the VRAM serial clock. The video clock scale factor therefore affects the serial data bandwidth and hence the color resolution which can be supported at a fixed VRAM width. The maximum resolution for different clock scale factors and VRAM widths are given in Table 20.2 below.

Clock scale factor	VRAM width	Maximum color resolution
1	32	16bpp
1	16	8bpp
2	32	8bpp
2	16	4bpp

Table 20.2 Maximum color resolution for different values of clock scale factor and VRAM width

The upper limit for the CRTC clock has been raised from 40MHz in the IMS G190 to 45MHz in the IMS G191 to increase the maximum color resolutions of some screen modes; e.g. 1024×768 non-interlaced with 85MHz pixel rate at clock scale factor 2 (CRTC clock rate = 42.5MHz) can operate at 8bpp.

Note that increasing the horizontal scale factor also affects the serial data bandwidth; Table 20.2 is valid for a horizontal scale factor of 1. Doubling the horizontal scale factor halves the serial clock rate so that the maximum color resolution increases.

20.4 IMS G191 programming and registers

20.4.1 IMS G200/IMS G191 and Micro Channel interface

This section provides a correlation between the addresses on the IMS G200/IMS G191 interface and the addresses on the Micro Channel interface. All addresses and indexes are in hexadecimal.

All the Micro Channel addresses given are I/O addresses as opposed to memory addresses.

The majority of registers within the IMS G191 and IMS G200 are indexed. All register accesses are decoded by the IMS G200. To access a register in the IMS G191, first write to the index register (I/O address 21xA) followed by a number of writes/reads to the data registers (I/O address 21xB-21xF). The IMS G200 then generates a corresponding IMS G191 address (**RegAddr0-6**) and an address strobe (**notDataStrobe**) to update the IMS G191.

Extended mode addresses

The functions of these registers are described in Section 20.4.2. Note that the IMS G200 indexes are read only.

Micro Channel Address	IMS G200 Index	IMS G191 Address (RegAddr0-6)	Writeable Bits in the IMS G191	Readable Bits in the IMS G191	Register name
N/A	N/A	00	N/A	N/A	Power on reset
21x0	N/A	02	2:1		Operating mode
21xB–F	00	01	1:0	–	Memory configuration
21xB–F	30	03	2:0	2:0	Sprite horizontal start lo
21xB–F	32	04	5:0	5:0	Sprite horizontal preset
21xB–F	36	05	0	0	Sprite control
21xB–F	38	38	7:0	7:0	Sprite color 0 red
21xB–F	39	39	7:0	7:0	Sprite color 0 green
21xB–F	3A	3A	7:0	7:0	Sprite color 0 blue
21xB–F	3B	3B	7:0	7:0	Sprite color 1 red
21xB–F	3C	3C	7:0	7:0	Sprite color 1 green
21xB–F	3D	3D	7:0	7:0	Sprite color 1 blue
21xB–F	50	06	4,1:0	4	Display control 1
21xB–F	51	07	5:4,3,2:0	3	Display control 2
21xB–F	52	08	–	7:5, 3:0	Display ID and comparator
21xB–F	53	09	–	–	RESERVED
21xB–F	54	0A	7,3:0	7,3:0	Clock frequency select 1
21xB–F	55	0B	7:0	7:0	Border color
21xB–F	56	0C	2:0	2:0	Fixed clock frequency address
21xB–F	57	0D	7:0	7:0	Fixed clock frequency data
21xB–F	58	0E	7:0	7:0	Programmed pixel clock frequency
21xB–F	59	0F	–	–	RESERVED
21xB–F	5B	1D	7,5:0	7,5:0	Miscellaneous control 1
21xB–F	60	10	7:0	7:0	Sprite/palette index lo
21xB–F	61	11	5:0	5:0	Sprite index hi
21xB–F	62	12	7:0	7:0	Sprite/palette index lo with prefetch
21xB–F	63	13	5:0	5:0	Sprite index hi with prefetch

Micro Channel Address	IMS G200 Index	IMS G191 Address (RegAddr0-6)	Writeable Bits in the IMS G191	Readable Bits in the IMS G191	Register name
21xB–F	64	14	7:0	7:0	Palette mask
21xB–F	65	15	7:0	7:0	Palette data
21xB–F	66	16	2:0	2:0	Palette sequence
21xB–F	67	17	7:0	7:0	Palette red prefetch
21xB–F	68	18	7:0	7:0	Palette green prefetch
21xB–F	69	19	7:0	7:0	Palette blue prefetch
21xB–F	6A	1A	7:0	7:0	Sprite data
21xB–F	6B	1B	7:0	7:0	Sprite prefetch
21xB–F	6C	1E	0	0	Miscellaneous control 2
21xB–F	6D	1F	–	–	RESERVED
21xB–F	6E	3E	–	–	RESERVED
21xB–F	6F	3F	–	–	RESERVED
21xB–F	70	37	7	7	Clock frequency select 2

VGA mode addresses

In the addresses shown as 3*4 and 3*5, the * has the value B in mono mode and D in color mode.

VGA Address		IMS G200 Index	IMS G191 Address (RegAddr0–6)	Writeable Bits in the IMS G191	Readable Bits in the IMS G191	Register name
Rd @	Wr @					
3C0	3C0	N/A	28	5:0	5 only	Attribute address
3C1	3C0	3C0=0–0F	29	5:0	5:0	Internal palette
3C1	3C0	3C0=10	2A	7:5,3:0	7:5,3:0	Attribute mode control
3C1	3C0	3C0=11	2B	7:0	7:0	Attribute overscan color
3C1	3C0	3C0=12	2C	3:0	3:0	Attribute color plane enable
3C1	3C0	3C0=13	2D	3:0	3:0	Attribute horiz pixel pan
3C1	3C0	3C0=14	2E	7:0	7:0	Attribute color select
3CC	3C2	N/A	20	2,3	2,3	Miscellaneous output
3C2	N/A	N/A	21	–	4	Input status zero
3C5	3C5	3C4=00	22	1:0	None	Sequencer reset
3C5	3C5	3C4=01	23	5:2,0	5:2,0	Sequencer clocking mode
3C5	3C5	3C4=04	24	3	–	Sequencer memory mode
3C6	3C6	N/A	34	7:0	7:0	Palette mask
3C7	3C7	N/A	32	7:0	1:0	Palette pixel address (read)
3C8	3C8	N/A	30	7:0	7:0	Palette pixel address (write)
3C9	3C9	N/A	35	5:0	5:0	Palette data
3CF	3CF	3CE=05	27	6:5	6:5	Graphics mode
3*5	3*5	3*4=14	25	6	–	CRTC underline location
3*5	3*5	3*4=17	26	6	–	CRTC mode control

These registers are fully VGA register compatible and a description of their function can be found in the *Video subsystem* section in the *Video Technical Reference*, IBM document number '42G2193'.

In the attribute section the same address (3C0) is used to write to the index register (called the 'address' register in VGA documentation) and to the register pointed to by this index register. A flip-flop which toggles on each write to 3C0 determines which register is written.

20.4.2 Internal Registers

This section gives brief descriptions of all the extended mode parameter register bits which physically reside in the IMS G191 (Note: some of the registers defined in the XGA architecture are physically split between the IMS G200 and the IMS G191). For a description of the VGA mode register bits refer to VGA documentation.

Memory configuration (Index #00, bits 1:0)

These two bits define the width (16 or 32 bits) of the serial data from the VRAMs.

Operating mode(Address 21x0, bits 2:1)

Bits 2:1 define whether the system is in VGA, 132 column mode or extended (XGA) mode.

In extended mode VGA registers are disabled. Note, however, that some parameter registers are shared between the two modes and may have widely different meanings. For example writing to an extended mode address in VGA mode may change an unexpected VGA parameter. It is recommended that in VGA mode only VGA registers are written to and for extended mode only extended registers are written to.

Sprite horizontal start lo (Index #30, bits 2:0)

These are the low-order 3 bits of the horizontal sprite start position. The IMS G200 uses the higher order bits to control when the video controls go to the cursor state with a granularity of 8 pixels. The IMS G191 uses the 3 low-order bits to position the sprite horizontally to the exact pixel.

Sprite horizontal preset (Index #32, bits 5:0)

These bits define horizontally which is the first sprite pixel to be displayed at the indicated position. A value of 0 means that the whole of the sprite line is displayed. A value of 63 means that only the right-most pixel of the sprite is displayed.

Sprite control (Index #36, bit 0)

This bit controls whether the sprite is displayed. Reading or writing the sprite buffer is not allowed when this bit is in the state which allows the sprite to be displayed. Apart from causing unwanted changes to the appearance of the sprite, attempts to read the sprite buffer while displaying the sprite will return undefined values, and attempts to write the sprite buffer while displaying the sprite may cause the contents of the sprite buffer to be corrupted.

Sprite color 0 red, green, blue (Indexes #38-#3A, bits 7:0)

These three registers define the red, green and blue components of sprite color 0. Color 0 is selected when both of the sprite data bits are 0.

Sprite color 1 red, green, blue (Indexes #3B-#3D, bits 7:0)

These three registers define the red, green and blue components of sprite color 1. Color 1 is selected when bits 0 and 1 of the sprite data are are 1 and 0 respectively.

Display control 1 (Index #50, bits 4, 1:0)

Bit 4 controls the enabling of the video feature interface. When this bit is a 0 the video feature data, blanking and pixel clock output drivers are disabled. The IMS G191 will also ignore the three video feature enable signals so that no data will be received. When this bit is a '1' the video feature signals can be driven or received as normal under the control of the three enable signals.

The video feature interface is not designed to work with a pixel clock frequency higher than 30MHz; bit 4 allows it to be disabled by software whenever clock frequencies higher than this are being used.

Bits 1:0 control display blanking. Bit 1, when 0, forces blanking on. If bit 0 is also 0 a CRTC reset is initiated, initializing various CRTC related functions in the IMS G191.

Display control 2 (Index #51, bits 5:4, 3, 2:0)

Bits 5:4 define the horizontal scale factor (1, 2 or 4). This function is sometimes referred to as horizontal replication, a horizontal scale factor of 2 or 4 causes the same pixel to be replicated and displayed as 2 or 4 consecutive identical pixels. Horizontal scale factor operation is disabled in standard VGA modes. Border pixels and sprite pixels are not replicated.

Bit 3 controls whether the video feature bus output clock is divided or undivided pixel clock.

Bits 2:0 define the number of bits per pixel (1, 2, 4, 8 or 16). For 1, 2, 4 and 8 bits per pixel the palette is used; higher order bits of the palette address are automatically forced to 0. 16 bits per pixel is the direct color mode.

Display ID and comparator (Index #52, bits 7:5, 3:0)

This is a read-only register.

Bits 7:5 indicate the state of the blue, green and red DAC comparators.

Bits 3:0 indicate the state of the four monitor ID inputs to IMS G191.

Clock frequency select 1 (Index #54, bits 7, 3:2, 1:0)

Bit 7 selects the use of the Programmed pixel clock frequency register for the PLL pixel clock value if enabled by Miscellaneous control register bit 1.

Bits 3:2 select which of the Fixed pixel clock registers is used for the PLL pixel clock value. This register must be used in conjunction with the Clock frequency select 2 register (Index #70) which contains an additional clock select bit.

Bits 1:0 selects clock scale factor 1 or 2. The clock scale factor is used to divide the pixel clock down by a value depending on the pixel frequency. This ensures that **CRTClkOut** and **CRTClkOut2** are always within the correct range of frequencies for use by the IMS G200 CRT controller. Further details on the clock scale factor are given in Section 20.3.8.

Border color (Index #55, bits 7:0)

This register is the palette index for the border color which resides in the palette. Bit 7 is also used to force the direct color expansion table to be in the opposite half of the palette to the border.

The border color is output on the video feature interface during blanking (as well as during the borders). This retains compatibility with VGA.

Fixed clock frequency address (Index #56, bits 2:0)

This register is used to address the Fixed pixel clock frequency registers. Bits 2:0 determine which of the fixed registers is accessed through the Fixed clock frequency data register (Index 57). The Fixed pixel clock frequency registers are assigned addresses 001 to 100 (binary); address 000 is reserved (do not write).

Fixed clock frequency data (Index #57, bits 7:0)

This register provides access to the Fixed pixel clock frequency registers addressed by the Fixed clock frequency address register.

Fixed pixel clock frequency registers (Bits 7:6, 5:0)

These four registers are accessed through the Fixed clock frequency address and data registers.They can be programmed to contain frequency values for the internal PLL pixel clock source. Bits 7:6 define the frequency range for the value contained in bits 5:0. These registers are reserved for fixed frequencies relating to existing VGA and XGA applications and should **not** be accessed or updated by applications software after start-up.

Programmed pixel clock frequency (Index #58, bits 7:6, 5:0)

This register can be programmed to contain a frequency value for the internal PLL pixel clock source. This allows additional display modes to be used, beyond those relating to the Fixed pixel clock frequency registers described above. Bits 7:6 define the frequency range for the value contained in bits 5:0.

Miscellaneous control 1 (Index #5B, bits 7,5,4,3,1,0)

This register provides control of the following functions:

Bit	Function	Notes
7	RESERVED	Always write '0'
6	RESERVED	Always write '0'
5	RESERVED	Always write '0'
4	Blanking	Display blanked, DAC outputs to zero
3	6-bit color emulation	Emulation of IMS G190 6-bit DAC resolution
2	RESERVED	Always write '0'
1	Programmed clock enable	Programmed pixel clock frequency register used as pixel clock value for internal pixel clock (see Clock frequency select 1 register, Index #54, bit 7).
0	RESERVED	Always write '0'

Sprite/palette index lo (Index #60, bits 7:0) (used for write & save/restore)

This register specifies the 8-bit palette address or the low-order 8 bits of the sprite buffer address when writing to the sprite buffer or the palette RAM. Accessing this register does not cause any action other than loading or returning the value of the index, unlike the sprite/palette index registers for read (prefetch). This register must be saved and subsequently restored by any interrupting task using the palette or sprite registers.

Writing to this register causes the palette sequence count to be reset to the red state.

Sprite index hi (Index #61, bits 5:0) (used for write & save/restore)

This register specifies the high-order 6 bits of the sprite buffer address used when writing to the sprite buffer. These bits are not used when accessing the palette. Accessing this register does not cause any action other than loading or returning the value of the index, unlike the sprite/palette index registers for read (prefetch). This register must be saved and subsequently restored by any interrupting task using the sprite registers.

Although the sprite only occupies 1 Kbyte of the sprite buffer, access to the entire 16 Kbytes is provided for diagnostic purposes. Reading data back from outside the 1 Kbyte range will return undefined data.

Sprite/palette index lo with prefetch (Index #62, bits 7:0)

This register specifies the 8-bit palette address or the low-order 8 bits of the sprite buffer address when reading the sprite buffer or the palette RAM. Although accessing physically the same register as the 'sprite/

palette index lo' register, writing to it causes both the palette and the sprite buffer to be read and the data saved in their respective data registers. The Sprite/palette index lo register is incremented by one after reading the two RAMs. This incrementing wraps from 255 to 0. Reading this register does not cause any additional activity.

Writing to this register causes the palette sequence count to be reset to the red state.

Sprite index hi with prefetch (Index #63, bits 5:0)

This register specifies the high-order 6 bits of the sprite buffer address used when reading the sprite buffer. Although accessing physically the same register as the 'sprite index hi' register, writing to it causes the sprite buffer to be read and the data saved in the sprite buffer data register. The Sprite index hi register is incremented by one after reading the sprite buffer. Reading this register does not cause any additional activity.

When reading the sprite buffer, either (Index #62) or (Index #63) can be used to cause the prefetch; the other part of the index should be provided using the non-prefetching registers (Index #60) or (Index #61).

Palette mask (Index #64, bits 7:0)

Each display memory pixel value is ANDed with the contents of this register before being used to address the palette. This register must be set to 'FF' hex in direct color mode. The addresses used by software to access the palette through the palette index registers are not ANDed with the palette mask.

Palette data (Index #65, bits 7:0)

This register is used to access the contents of the palette RAM one color value at a time. Because the palette RAM is 24 bits wide, with 8 bits for each color, three writes to the Palette data register are required to write each 24-bit RAM location. The 8-bit color value currently being accessed is controlled by the Palette sequence register. After accessing the Palette data register, the palette sequence count is incremented.

When the palette sequence count changes from blue to red or from green to 'X' (depending on the order selected by palette sequence register bit 2), as a result of *writing* to the Palette data register, the palette is written with the three colors values that have been accumulated in the Palette data register, and the Sprite/palette index lo register is incremented.

When the palette sequence count changes from blue to red or from green to 'X' as a result of *reading* the Palette data register, the Sprite/palette index lo register is incremented and the palette is read into the Palette data register from the new address.

In either case the Sprite/palette index hi is NOT incremented when the Sprite/palette index lo register wraps from 255 to 0 because the palette is being accessed and not the sprite buffer.

The entire palette can be accessed simply by successive reads or writes to the Palette data register.

Palette sequence (Index #66, bits 2, 1:0)

The Palette Sequence Register controls the sequence of read and write accesses to the contents of the palette RAM through the Palette data register. It contains two fields, one defining which RGB element is selected for the next palette data access, the other defining which of the following palette data update sequences will be followed:

1. Red, Green, Blue
2. Red, Blue, Green, X (where X indicates no access, data is ignored)

Bit 2 controls the order in which the palette color values are handled.

Bits 1:0 indicate which color value is currently being handled. For instance, if they indicate 'blue', the next byte written to the palette data register must contain blue data, and the next byte read from the palette data register will be blue data.

Palette red, green, blue prefetch (Indexes #67-#69, bits 7:0)

These registers are not used for any normal function. They are used for save and restore purposes, required during task switches or for interrupts. The contents of these registers must be saved and subsequently restored by any interrupting code that uses the Sprite or Palette RAM registers. Accessing them will not change the Palette sequence register, nor will any palette access occur.

Sprite data (Index #6A, bits 7:0)

This register is used to access the addressed sprite buffer (sprite) location. The 8-bit data represents four 2-bit pixels in the sprite buffer. The pixels are stored in Intel format within the data byte.

After writing this register the sprite buffer is written and the sprite/palette index lo register is incremented.

After reading this register the sprite/palette index lo register is incremented and the sprite buffer is read from the new address and the data put into the sprite data register.

The sprite/palette index hi is also incremented in either case when the sprite/palette index lo register wraps from 255 to 0.

The entire sprite buffer can be written or read simply by successively writing or reading this register.

Sprite prefetch (Index #6B, bits 7:0)

This register is not used for any normal function. It is used for save and restore purposes, required during task switches or for interrupts. The contents of this register must be saved and subsequently restored by any interrupting code that uses the Sprite or Palette RAM registers. Accessing it will not change the palette/sprite index register, nor will any sprite buffer access occur.

Miscellaneous control 2 (Index #6C, bit 0)

Bit 0 when set to '1' blanks the red and blue DACs.

Clock frequency select 2 (Index#70, bit7)

This register is used in conjunction with the Clock frequency select 1 register (Index #54) to provide clock selection in 132 column mode. This register is now integrated into the IMS G191 so that with future controller chips there will be no need to implement this register bit in external logic. To enable the IMS G191 to be used with controller chips which do not map index #70 into the serializer register space, a single input pin, **ExtRegBit**, has been proved to provide compatibility between the IMS G191 and IMS G200. This pin is logically ORed with the internal register bit to provide the select function of the Index #70 register bit.

20.5 IMS G200 / IMS G191 communication

20.5.1 IMS G191 register accesses

The Micro Channel bus interface function is implemented by the IMS G200 display controller. Consequently all updates to registers physically resident in the IMS G191 are decoded by the IMS G200 which then updates the IMS G191.Data for these registers is transferred over the **Data0-7** pins; the address being generated by the IMS G200 **VAddr0-6** pins driving IMS G191 **RegAddr0-6**.

Parameter register accesses are timed by the IMS G200 controller clock (**Clk**), which results in a clock period of 50ns (with the controller operating at 40MHz). A parameter register access occurs whenever **notDataStrobe** is active and address bit 6 is '0'.

There are two basic types of accesses between the IMS G200 and IMS G191, fast accesses and slow accesses. Fast accesses are used for parameter register updates to the IMS G191 and slow accesses are used for sprite/palette accesses since extra time is needed to allow the sprite buffer or the palette RAM to be accessed.

20.5.2 Control codes from the IMS G200 to the IMS G191

The address bits on the IMS G200/IMS G191 interface are used at certain times to carry control data from the IMS G200 to the IMS G191. This data is not transferred as a result of Micro Channel activity, but during each VRAM transfer cycle, in particular during the transfer cycle at the start of each line. This data mainly consists of information about the line that is about to be displayed. The data is not transferred on the data bus, but on the low-order six bits of the address.

These bits are encoded as shown in Table 20.3 with their usage described in Table 20.4.

RegAddr0-6							IMS G191 decoded meaning
6	5	4	3	2	1	0	
0	@	@	@	@	@	@	IMS G191 parameter register address
1	0	N	A	S	U	C	control code
1	1	R	R	R	R	R	control code

Table 20.3 Encoding of register address bits 0-6

Symbol	Register address bit usage
@	Address bits used to address the parameter registers within the IMS G191
N	The 'new font pair' bit. When this bit is '1' it causes a reset of the sprite buffer address register used during alphanumeric font loading.
A	The 'active line' bit. This bit is '1' for picture lines, and '0' for border (overscan) lines and for blank (flyback) lines.
S	The 'scrollable/border line' bit. When it is '1' during an active line it indicates that the line is scrollable. When it is '1' during a non-active line it indicates that the line is a border line.
U	The 'underline/panning sync/sprite line' bit. In an alphanumeric VGA mode it is '1' to indicate that the underline part of a character should be placed on the line. In extended mode it is '1' to indicate that the sprite should be placed on the line. In addition, if this bit is '1' during a non-active line, it causes the horizontal panning sync register to be strobed.
R	In VGA mode these bits are character row bits 4:0. In extended mode these bits hold the sprite prefetch row number, indicating in which row the sprite is to be displayed.
C	C is bit 5 of the sprite row number.

Table 20.4 Register address bit usage

20.5.3 Video control

The video control signals (**VideoCtrlOut0-1**) are generated by the IMS G200 from the IMS G191 CRTC clocks and fed back into the IMS G191 via the **VideoCtrlIn0-1** pins. The video control signals are encoded as shown in Table 20.5 to indicate events on a horizontal scan line.

VideoCtrlOut0-1		Video data function
Bit 1	Bit 0	
0	0	Blanking
0	1	Border
1	0	Picture
1	1	Picture and start of cursor

Table 20.5 **VideoCtrlOut0-1** decoding

20.6 Hardware interfaces

The IMS G191 Serializer Palette DAC interfaces to other XGA subsystem components including the IMS G200 display controller, VRAM, SRAM and video feature bus interface.

20.6.1 IMS G200 display controller interface

Figure 20.2 shows the signals used to connect the IMS G191 to the IMS G200 display controller.

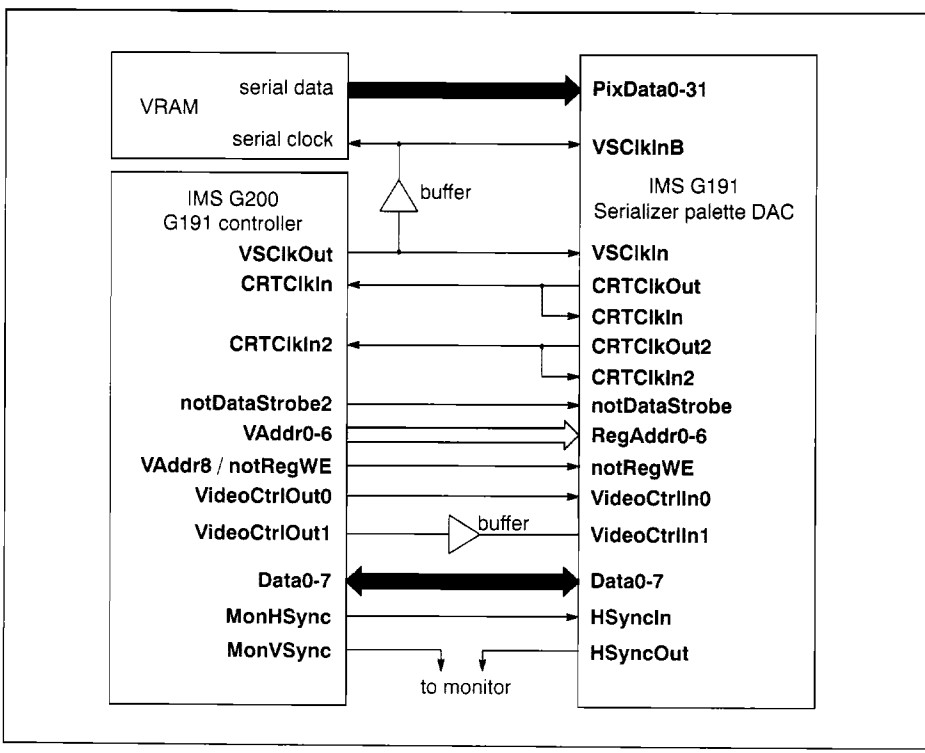


Figure 20.2 IMS G191 interface to the IMS G200

20.6.2 VRAM interface

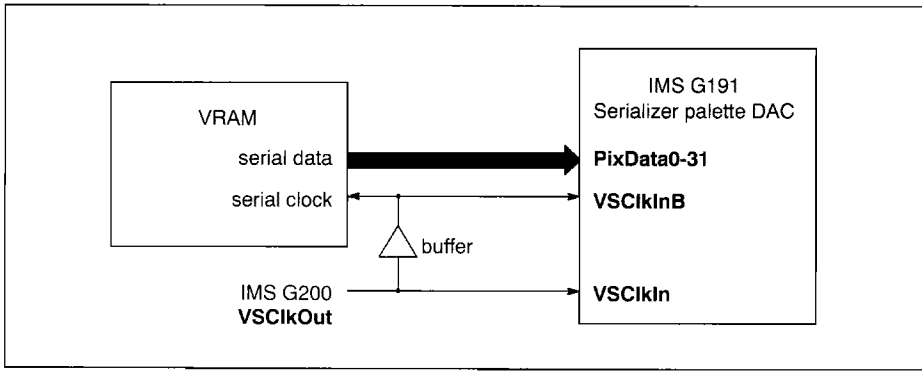


Figure 20.3 IMS G191 VRAM interconnection

The IMS G191 receives video data from the VRAM's on the **PixData0-31** pins. The pins are driven by the serial outputs of the VRAM's.

The **VSClkIn** signal is generated by the IMS G200 from the IMS G191 CRTC clocks, and fed back into the IMS G191. A low level on the buffered VRAM serial clock input pin, **VSClkInB**, strobes the VRAM serial data into the IMS G191. The rising edge of the unbuffered VRAM serial clock input pin, **VSClkIn**, clocks the serial clock counter in the IMS G191.

20.6.3 Video feature bus interface

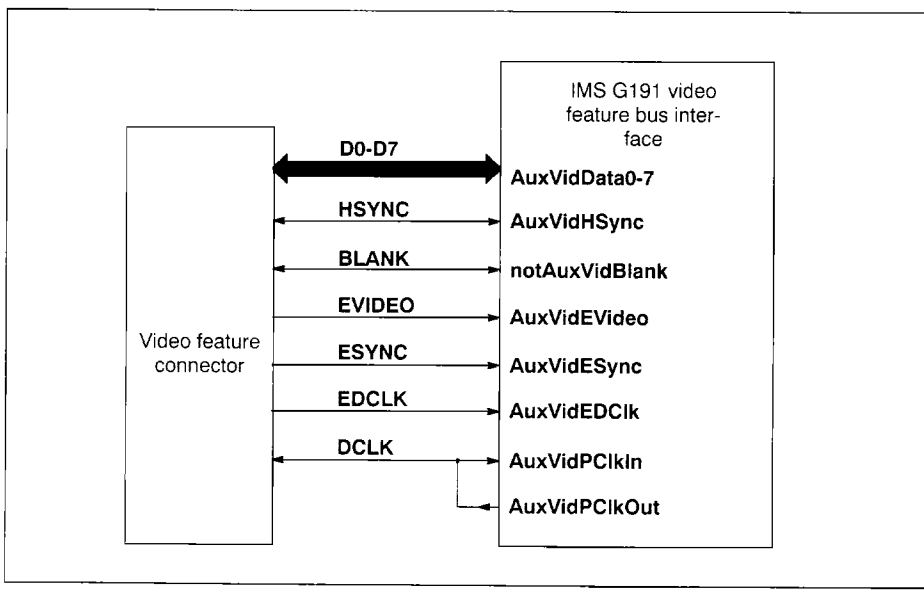


Figure 20.4 IMS G191 interconnection diagram to video feature connector

The **AuxVidData0-7** is the VGA palette address bus. **AuxVidPClkOut** is the pixel clock used by the IMS G191 to latch the digital video signals **AuxVidData0-7**. The signals are latched into the IMS G191 on the rising edge of **AuxVidPClkIn**. When an adapter provides the video information on **AuxVidData0-7**, the adapter must also provide the clock to the IMS G191.

The **notAuxVidBlank** signal connects to the IMS G191 DAC and when active low forces all DAC outputs to zero.

For a full description of these Micro Channel signals refer to the *Video Technical Reference*, IBM document number '42G2193'.

20.6.4 SRAM (sprite and attribute font buffer) interface

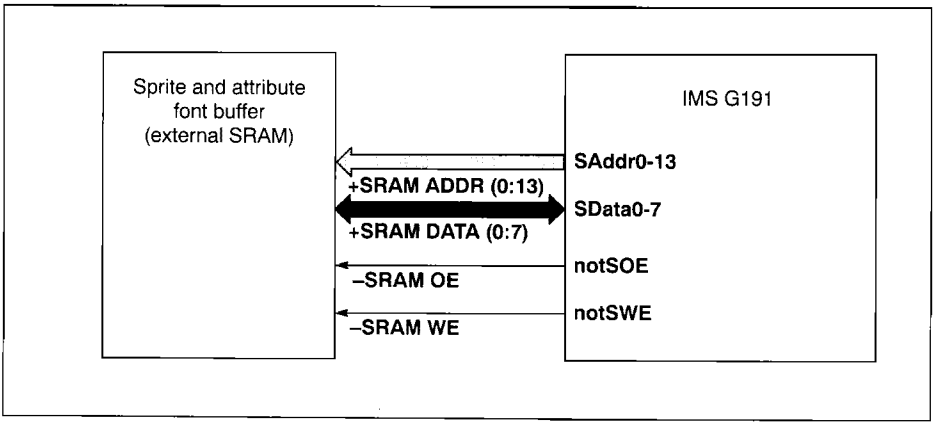


Figure 20.5 IMS G191 SRAM interconnection

This section describes the sprite and attribute font buffer interface. External memory is used as a VGA font buffer in VGA modes and as a hardware sprite buffer in extended mode. The IMS G191 initiates accesses to this external memory when necessary. These accesses are synchronously timed to the CRTC clocks.

In VGA mode two fonts are held in this external memory. These fonts are continuously updated during the active line time of vertical retrace. Each character in the font is 8×32 pixels. Therefore 16 Kbytes are necessary to store the two fonts. In extended mode, the lower 1 Kbyte is used to store the 64×64 sprite.

The **SData0-7** pins transfer data to and from the SRAM. The **SAddr0-13**, **notSWE** and **notSOE** provide the address, write enable and output enable signals required by the SRAM.

20.6.5 Analog interfaces

Phase locked loop

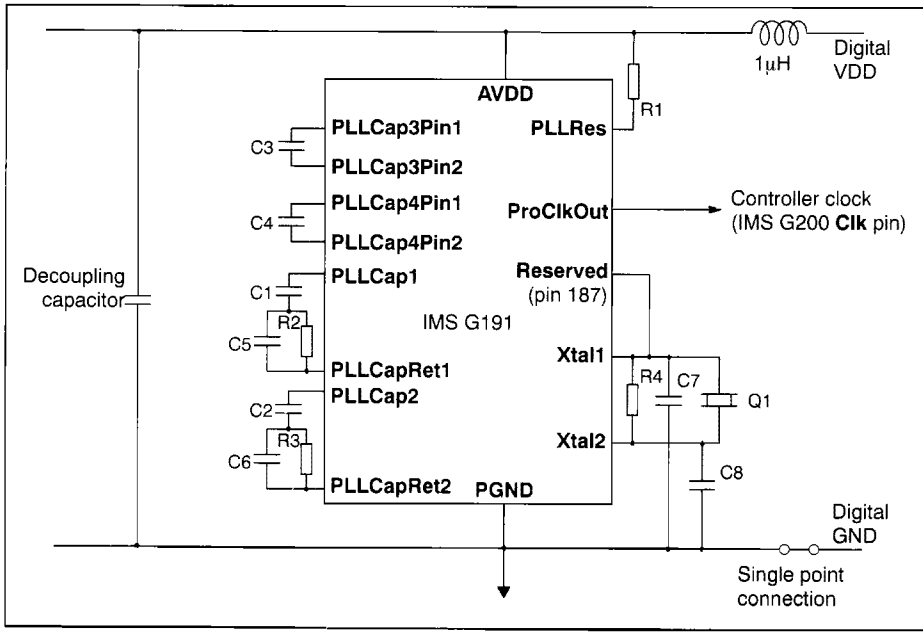


Figure 20.6 IMS G191 phase locked loop connections

Component	Value	Description[1]
Q1	4MHz	crystal, series resonant
C1	8.2nF	10% ceramic capacitor
C2	2.2nF	10% ceramic capacitor
C3	1µF	surface mounted ceramic capacitor[2]
C4	1µF	surface mounted ceramic capacitor[2]
C5	620pF	10% ceramic capacitor
C6	150pF	10% ceramic capacitor
C7,C8	33pF	10% ceramic capacitor
R1	8.66KΩ	1% resistor
R2	1.3KΩ	10% resistor
R3	3.9KΩ	10% resistor
R4	100KΩ	10% resistor

Notes:

1. All the components associated with the phase locked loops should be placed as physically close as possible to the IMS G191.
2. These components should have an effective series resistance ≤1Ω and effective series inductance ≤5nH. Connecting tracks from the IMS G191 should be no longer than 10mm and no narrower than 0.25mm on a 1oz copper PCB. They should be shielded from any noisy signals.

Table 20.6 Phase locked loop external component list

Monitor interface

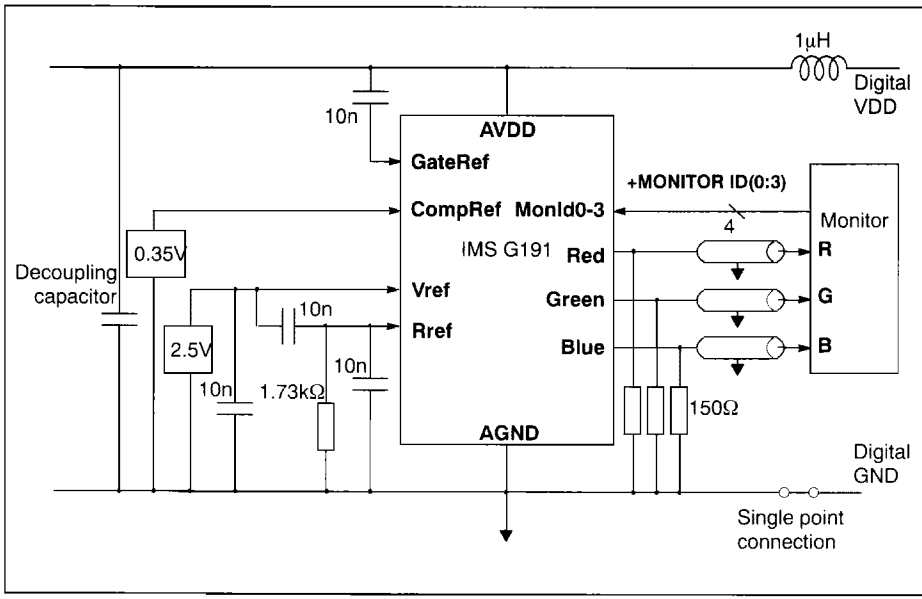


Figure 20.7 IMS G191 monitor connections

The IMS G191 interfaces directly to a color or monochrome monitor. The three video signals **Red**, **Green** and **Blue** are designed to drive a 50 ohm load comprising a 75 ohm monitor load in parallel with a 150 ohm resistor at the IMS G191.

The current out of the DAC's should be set to 14mA, by applying a 2.5V voltage reference to the **Vref** pin and connecting a 1.73kΩ resistor between **Rref** and **GND**. The 14mA full-scale current from the DAC, across a 50 ohm load will then give a 0.7V full scale voltage.

The IMS G191 receives four monitor ID bits (**MonId0-3**) back from the monitor which enable the XGA subsystem to determine the type of monitor which is connected. These monitor ID bits can be read from the Display ID and comparator register.

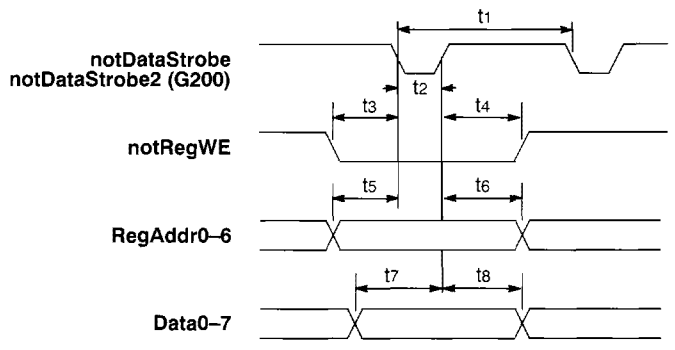
The IMS G191 takes in a further voltage reference (**CompRef**). This should be set to 0.35V. The IMS G191 contains internal comparators which compare this voltage with each of the DAC outputs. The results of these comparisons can be read back from the Display ID and comparator register.

The comparator polarity is a high output when the DAC output voltage is less than the 0.35V reference.

20.7 Timing reference guide

20.7.1 IMS G200 display controller interface timings

Write to IMS G191 register timings



Note: These cycles are synchronous to the IMS G200 processor clock

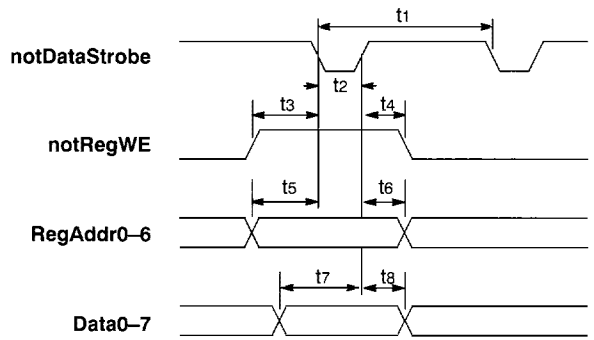
Figure 20.8 Write to IMS G191 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe** period – fast access	60.0		ns	
	notDataStrobe period – slow access	500.0		ns	
	notDataStrobe period – control codes	35.0		ns	
t2	**notDataStrobe** width – fast access	40.0		ns	
	notDataStrobe width – slow access	130.0		ns	
	notDataStrobe width – control codes	15.0		ns	
t3	**notRegWE** set up to **notDataStrobe**	10.0		ns	
t4	**notRegWE** hold after **notDataStrobe**	10.0		ns	
t5	**RegAddr0–6** set up to **notDataStrobe**	10.0		ns	
t6	**RegAddr0–6** hold after **notDataStrobe**	10.0		ns	
t7	**Data0–7** set up to **notDataStrobe**	40.0		ns	
t8	**Data0–7** hold after **notDataStrobe**	10.0		ns	

Note:
Fast accesses are used for all parameter register write accesses. Slow accesses are used for all palette and sprite write accesses. Control code cycles occur only at the start of an active line or during a mid-line reload of the VRAM. Control code cycles do not make use of the PC data bus (**Data0-7**).

Table 20.7 Write to IMS G191 register timings

Read from IMS G191 register timings



Note: These cycles are synchronous to the IMS G200 processor clock

Figure 20.9 Read from IMS G191 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe** period – fast access	150.0		ns	
	notDataStrobe period – slow access	500.0		ns	
t2	**notDataStrobe** width – fast access	100.0		ns	
	notDataStrobe width – slow access	130.0		ns	
t3	**notRegWE** set up to **notDataStrobe**	10.0		ns	
t4	**notRegWE** hold after **notDataStrobe**	10.0		ns	
t5	**RegAddr0–6** set up to **notDataStrobe**	10.0		ns	
t6	**RegAddr0–6** hold after **notDataStrobe**	10.0		ns	
t7	**Data0–7** data set up to **notDataStrobe**	40.0		ns	
t8	**Data0–7** hold after **notDataStrobe**	4.0		ns	

Note:
Fast accesses are used for all parameter register read accesses. Slow accesses are used for all palette and sprite read accesses.

Table 20.8 Read from IMS G191 register timings

20.7.2 CRTC controller timings

CRTC clock timings

The CRTC clocks are generated by the IMS G191. They provide synchronization of signals between the IMS G200, VRAM and the IMS G191. Their frequency is determined by the video clock output frequency divided by the 'video clock scale factor' as selected by the Clock frequency select 1 register (bits 1:0, index #54), see Section 20.3.8.

The interface timing requirements of the clocks are given below. **CRTClkOut2** is always half the frequency of **CRTClkOut**.

Video control timings

The video control signals (**VideoCtrlOut0–1**) are generated by the IMS G200 from the CRTC clocks and are encoded to indicate events on a horizontal scan line.

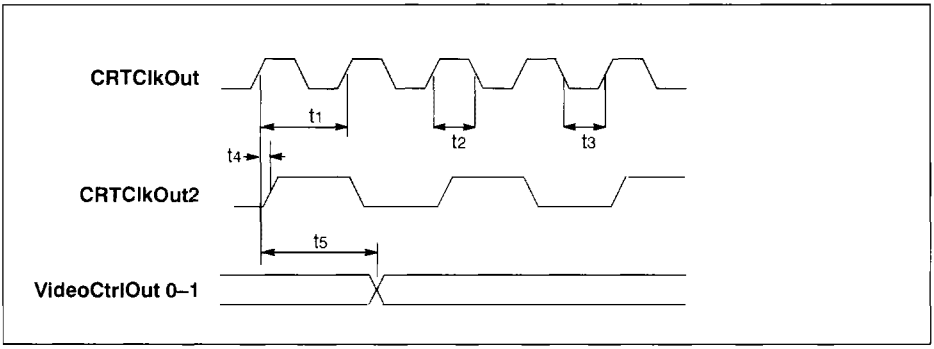


Figure 20.10 CRTC clock and video control timings

Symbol	Parameter	Min	Max	Units
t1	IMS G191 **CRTClkOut** period	22.2	50.0	ns
t2	IMS G191 **CRTClkOut** pulse width high	9.4	30.4	ns
t3	IMS G191 **CRTClkOut** pulse width low	8.4	30.4	ns
t4	IMS G191 **CRTClkOut** to **CRTClkOut2** delay	0.0	3.9	ns
t5	IMS G191 **CRTClkOut** to IMS G200 **VideoCtrlOut0-1**	see note	32.6	ns

Note:
VideoCtrlOut0-1 change on the first **VSClockIn** cycle of a horizontal line. They must change a minimum of 1.1ns after **VSClockIn** rises under worst case conditions.

Table 20.9 CRTC clock and video control timings

20.7.3 HSync interface

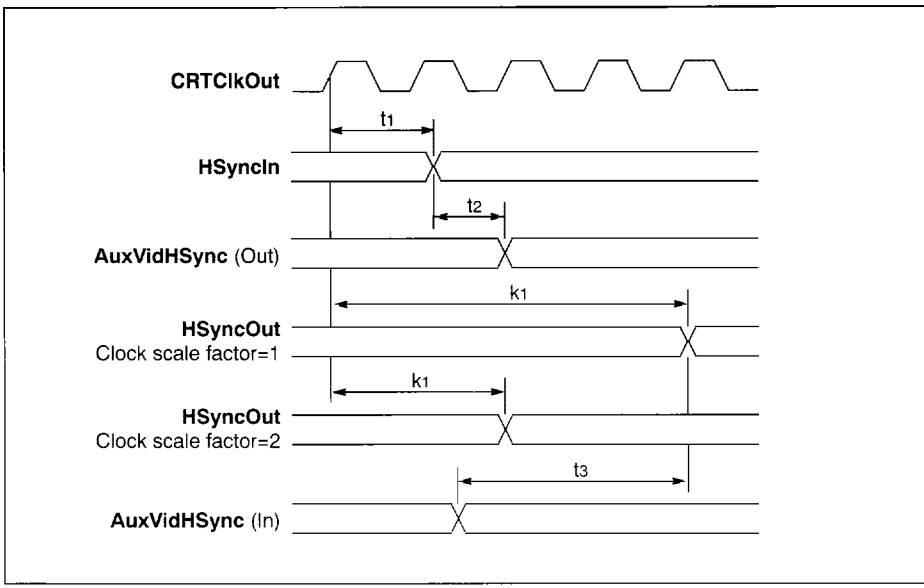


Figure 20.11 HSync timing

Symbol	Description	Value		Units
k1	IMS G191 HSync adjustment (video clock scale factor 1 and 2)	4		pixels
		Min	**Max**	
t1	IMS G191 **CRTClkOut** to IMS G200 **MonHSync**	2.2	43.5	ns
t2	**HSyncIn** to **AuxVidHSync** (out) delay		19.6	ns
t3	**AuxVidHSync** (in) to **HSyncOut** delay		18.8	ns

Table 20.10 HSync timing

20.7.4 Video feature bus timings

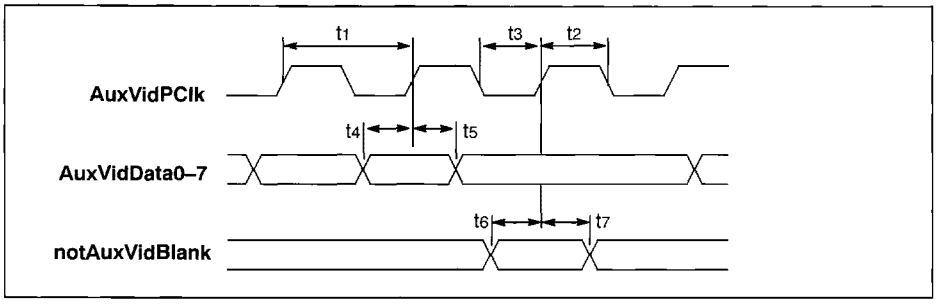


Figure 20.12 Video feature receive timings

Symbol	Parameter	Min	Max	Units	Notes
t1	**AuxVidPClk** period	28.0	72	ns	
t2	**AuxVidPClk** pulse width high	7.0	60	ns	
t3	**AuxVidPClk** pulse width low	9.0	60	ns	
t4	**AuxVidData0–7** set up time	4.0	–	ns	
t5	**AuxVidData0–7** hold time	4.0	–	ns	
t6	**notAuxVidBlank** set up time	4.0	–	ns	
t7	**notAuxVidBlank** hold time	4.0	–	ns	

Note:
AuxVidPClk must be a continuous clock signal

Table 20.11 Video feature receive timings

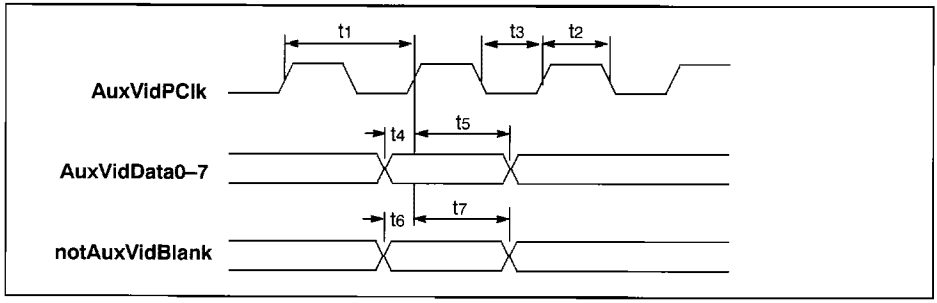


Figure 20.13 Video feature send timings

Symbol	Parameter	Min	Max	Units	Notes
t1	**AuxVidPClk** period	28.0	62.5	ns	
t2	**AuxVidPClk** pulse width high	9.0	53	ns	
t3	**AuxVidPClk** pulse width low	9.0	53	ns	
t4	**AuxVidData0–7** set up time	4.0	–	ns	
t5	**AuxVidData0–7** hold time	10.0	–	ns	
t6	**notAuxVidBlank** set up time	4.0	–	ns	
t7	**notAuxVidBlank** hold time	10.0	–	ns	

Note:
AuxVidPClk must be a continuous clock signal

Table 20.12 Video feature send timings

20.7.5 VRAM interface timings

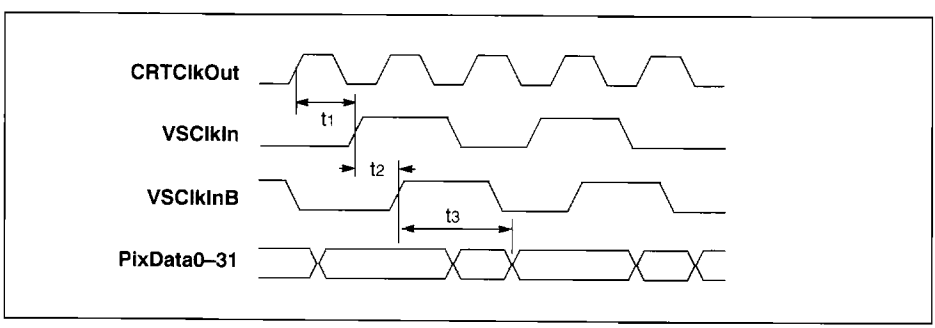
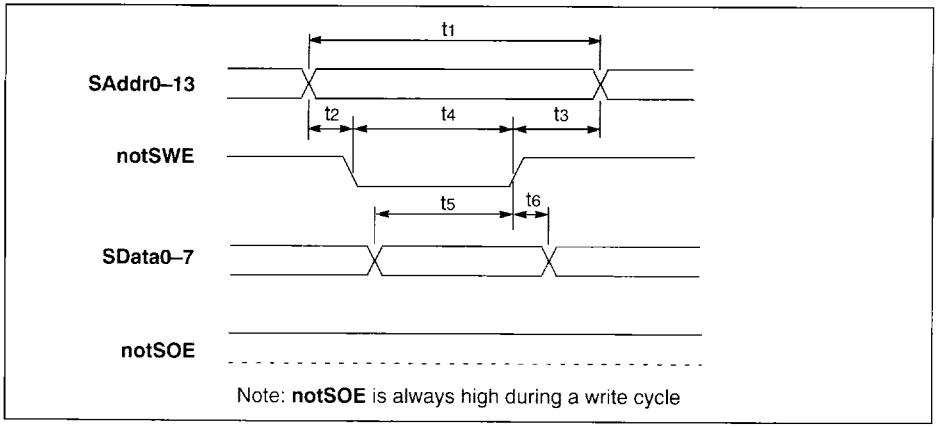


Figure 20.14 VRAM interface timings diagram

Symbol	Parameter	Min	Max	Units	Notes
t1	**CRTClkOut** high to **VSClkIn** high	-	25.6	ns	
t2	On-card buffer delay	-	7.0	ns	
t3	VRAM access time	-	35.0	ns	

Table 20.13 VRAM interface timings

20.7.6 SRAM (sprite buffer) timings



Note: **notSOE** is always high during a write cycle

Figure 20.15 SRAM write cycle timings diagram

Symbol	Parameter	Min	Max	Units	Notes
t1	Write cycle time	155.0		ns	
t2	**SAddr0–13** set up time	5.0		ns	
t3	**SAddr0–13** hold time	40.0		ns	
t4	**notSWE** pulse width low	110.0		ns	
t5	**SData0–7** set up time	75.0		ns	
t6	**SData0–7** hold time	15.0		ns	

Table 20.14 SRAM write cycle timings

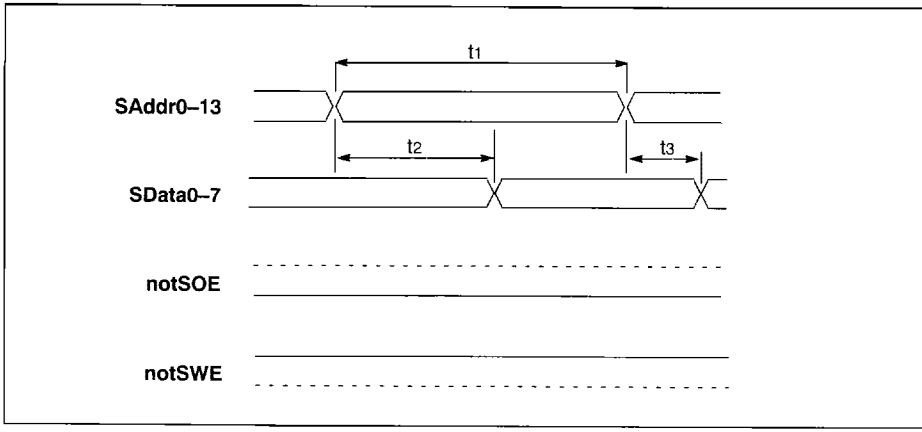


Figure 20.16 SRAM read cycle timing - VGA alphanumeric font reads for 100ns SRAM

Symbol	Parameter	Min	Max	Units	Notes
t1	Read cycle time	125.5		ns	
t2	**SAddr0–13** access time		100.0	ns	
t3	**SData0–7** hold from **SAddr0–13** change	0.0		ns	

Table 20.15 SRAM read cycle timings - VGA alphanumeric font reads for 100ns SRAM

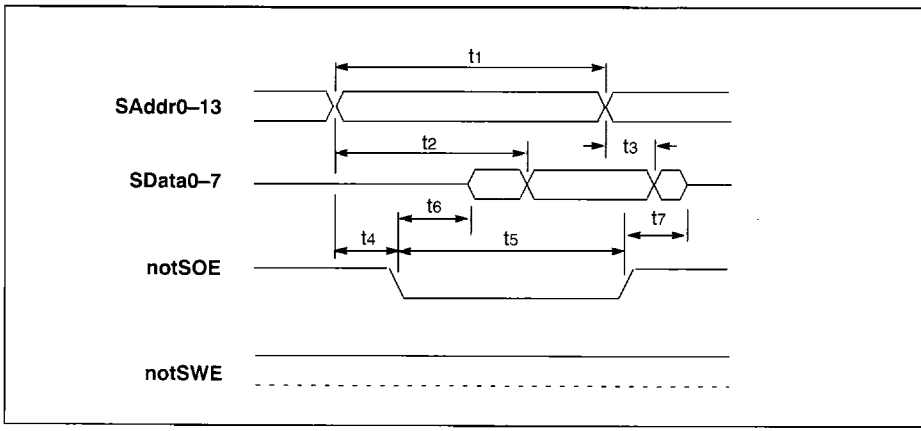


Figure 20.17 SRAM read cycle timing - sprite pre-fetch and reads

Symbol	Parameter	Min	Max	Units	Notes
t1	Read cycle time	177.6		ns	
t2	**SAddr0–13** access time		100.0	ns	
t3	**SData0–7** hold from **SAddr0–13** change	0.0		ns	
t4	**SAddr0–13** to **notSOE** set up time	26.0		ns	
t5	**notSOE** pulse width low	133.5		ns	
t6	**notSOE** to **SData0-7** low Z		19.2	ns	
t7	**notSOE** to **SData0-7** high Z		35.0	ns	

Table 20.16 SRAM read cycle timings - sprite pre-fetch and reads

20.7.7 DAC characteristics

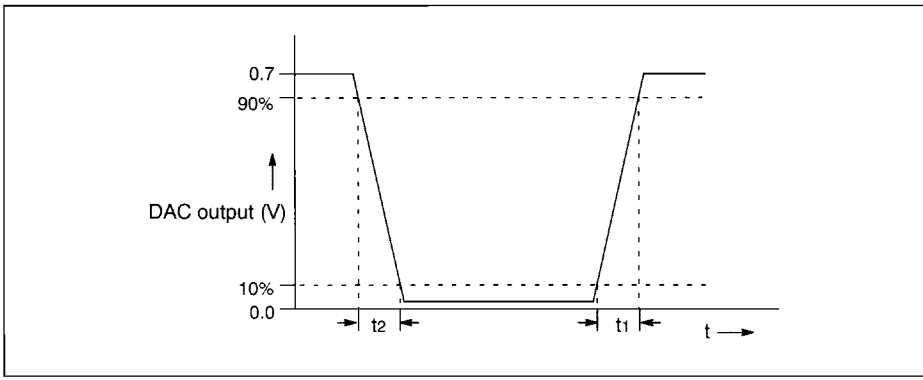


Figure 20.18 DAC output timing

Symbol	Parameter	Max	Units
t1	rise time	8	ns
t2	fall time	8	ns

Table 20.17 DAC output timing

Symbol	Parameter	Value	Units	Notes
	Resolution	8	bits	
IO	Peak output current (absolute)	14	mA	
	Full scale error (absolute)	±5	%	
	DAC to DAC correlation error	±1	%	
	DAC linearity	±1	LSB	1
Vref	Reference voltage (absolute)	2.5	V	
	Max clock frequency	90	MHz	
Note: 1 Monotonicity guaranteed				
These figures are not characterized and are subject to change				

Table 20.18 DAC characteristics

20.8 Electrical specifications

20.8.1 Absolute Maximum Ratings

Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply Voltage	0.0	7.0	Volts
V_I	Voltage on input pin	−0.5	V_{DD}+0.5	Volts
V_O	Voltage on output pin	−0.5	V_{DD}+0.5	Volts
T_S	Storage temperature	−55	125	°C
T_A	Temperature under bias	−40	85	°C

Table 20.19 Absolute maximum ratings

20.8.2 Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	DC supply Voltage	4.75	5.25	Volts	
T_c	Case temperature under bias			°C	1,2
P_D	Power dissipation		2.6	Watts	1,3
I_{IN}	Digital input current	−10	+10	µA	

Note:

1 Information on thermal management of the IMS G191 has been made available in a Technical Note published separately (document number 72 TCH 131 00).

2 T_c refers to temperature measured at the centre of the package lid.

3 At 90MHz operating frequency and V_{DD}=5.25V.

Table 20.20 Operating conditions

Worst case timings are applicable only if the device is within these recommended parameters.

20.8.3 Pin loading characteristics

Signal name	Input capacitance (pF)	Max V_{IL}	Min V_{IH}	Max load (pF)	Max V_{OL}	Min V_{OH}	Level	Driver current (mA)
Digital input signals								
AuxVidEDClk AuxVidESync AuxVidEVideo AuxVidPClkIn CRTClkIn CRTClkIn2 ExtRegBit HSyncIn MonId0-4 notRegWE notDataStrobe PixData0-31 RegAddr0-6 VSClkIn VSClkInB VideoCtrlIn0-1	5.0	0.7	2.2				TTL	
notPOR	5.0	1.6	3.3				CMOS	
Digital bi-directional signals								
AuxVidData0-7 notAuxVid-Blank	6.0	0.6	2.2	55.0	0.6	2.4	TTL	5.0
AuxVidHSync	6.0	0.6	2.2	55.0	0.6	2.4	TTL	5.0
Data0-7	6.0	0.6	2.2	112.0	0.6	2.4	TTL	5.0
SData0-7	6.0	0.6	2.2	25.0	0.6	2.4	TTL	5.0
Digital output signals								
AuxVidPClkOut				59.0	0.4	2.4	TTL	8.0
CRTClkOut CRTClkOut2				30.0	0.4	2.4	TTL	2.5
HSyncOut				144.0	0.4	2.4	TTL	8.0
notSOE notSWE				30.0	0.4	2.4	TTL	5.0
ProClkOut				25.0	0.4	2.4	TTL	5.0
SAddr0-13				20.0	0.4	2.4	TTL	5.0

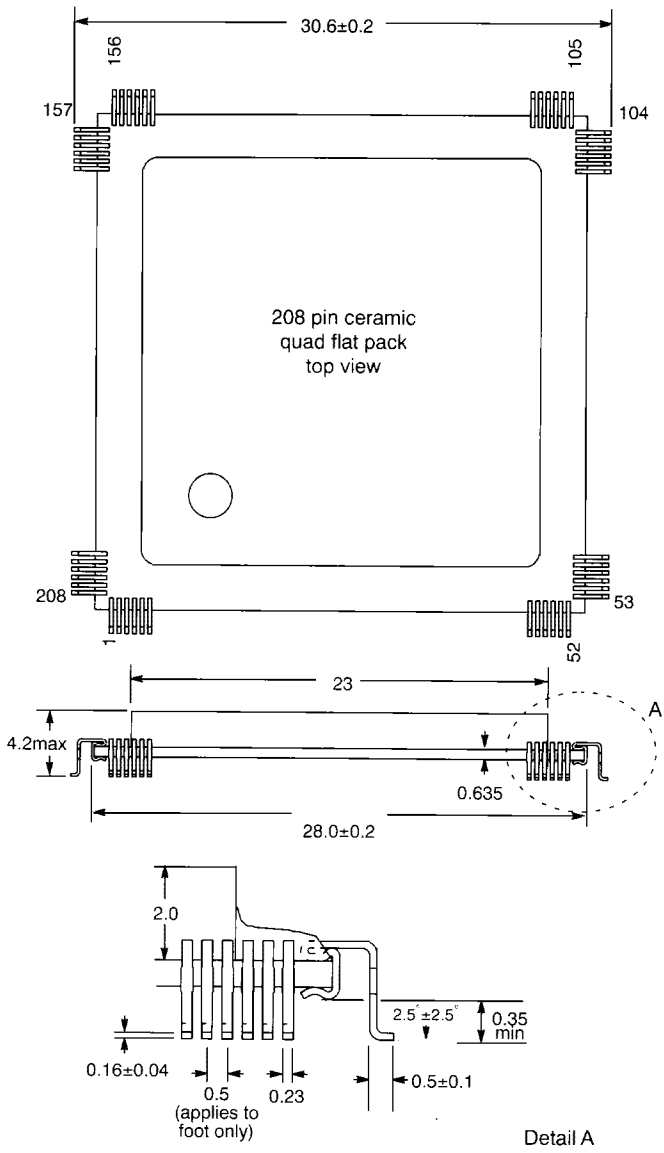
20.8.4 Phase locked loop specifications

Parameter	Value	Units	Notes
Processor clock PLL frequency	40	MHz	
Video clock PLL output range	65 - 90 32.5 - 64 20 - 32	MHz MHz MHz	in 1MHz steps in 0.5MHz steps in 0.25MHz steps

Table 20.21 Phase locked loop specifications

20.9 Package specifications

208-pin ceramic quad flat pack package



Notes: All dimensions in millimeters. All tolerances ±0.05mm unless stated.

Figure 20.19 208-pin ceramic quad flat pack dimensions

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**VDD**	53	**GND**	105	**VDD**	157	**GND**
2	**PixData12**	54	**AuxVidPClkOut**	106	**SData6**	158	**PixData0**
3	**Data7**	55	**RegAddr3**	107	**SAddr6**	159	**PixData1**
4	Reserved	56	**AuxVidPClkIn**	108	**SAddr1**	160	Reserved
5	Reserved	57	Reserved	109	**SAddr10**	161	Reserved
6	Reserved	58	Reserved	110	**SData1**	162	**PixData3**
7	**Data4**	59	Reserved	111	**SData7**	163	Reserved
8	**ProClkOut**	60	Reserved	112	**SAddr11**	164	**PixData2**
9	Reserved	61	Reserved	113	**SData0**	165	Reserved
10	**PixData31**	62	**HoldToGND**	114	**SAddr13**	166	**PixData18**
11	**PixData29**	63	Reserved	115	**SAddr12**	167	Reserved
12	**Data5**	64	**HoldToGND**	116	**SData4**	168	Reserved
13	**CRTClkIn2**	65	**RegAddr4**	117	**SAddr0**	169	Reserved
14	**CRTClkOut2**	66	**HSyncIn**	118	**SData3**	170	**PLLCap3Pin1**
15	Reserved	67	**GND**	119	**AuxVidESync**	171	**PGND**
16	**GND**	68	**AGND**	120	**GND**	172	**PLLCap3Pin2**
17	Reserved	69	**AGND**	121	**HoldToGND**	173	**AGND**
18	**CRTClkOut**	70	**CompRef**	122	**MonId0**	174	**PLLCapRet1**
19	**CRTClkIn**	71	**GateRef**	123	**AuxVidEVideo**	175	**PLLCap1**
20	**RegAddr2**	72	**Rref**	124	**AuxVidEDClk**	176	**PLLRes**
21	**PixData28**	73	**Vref**	125	**PixData27**	177	**PLLCapRet2**
22	**VideoCtrlIn1**	74	**Red**	126	Reserved	178	**PLLCap2**
23	Reserved	75	**RedCmpImnt**	127	**PixData26**	179	**AGND**
24	**RegAddr5**	76	**Green**	128	Reserved	180	**Xtal2**
25	**VSClkIn**	77	**GreenCmpImnt**	129	**PixData9**	181	**Xtal1**
26	**VDD**	78	**AVDD**	130	**AVDD**	182	**AVDD**
27	**VDD**	79	**AVDD**	131	**AVDD**	183	**PLLCap4Pin2**
28	**ExtRegBit**	80	**Blue**	132	**RamVref**	184	**PLLCap4Pin1**
29	**PixData30**	81	Reserved	133	**AGND**	185	**AGND**
30	**RegAddr6**	82	**BlueCmpImnt**	134	**PixData24**	186	**notPOR**
31	**VideoCtrlIn0**	83	**HoldToGND**	135	Reserved	187	Reserved
32	**VSClkInB**	84	Reserved	136	**PixData16**	188	**PixData11**
33	**RegAddr1**	85	**MonId2**	137	**PixData8**	189	**PixData20**
34	**notRegWE**	86	Reserved	138	Reserved	190	Reserved
35	**notDataStrobe**	87	**HoldToGND**	139	**PixData25**	191	Reserved
36	**GND**	88	Reserved	140	**AGND**	192	Reserved
37	**GND**	89	**GND**	141	**AGND**	193	**GND**
38	Reserved	90	**notSOE**	142	**PixData17**	194	**PixData22**
39	**AuxVidData6**	91	**MonId3**	143	Reserved	195	Reserved
40	**notSWE**	92	**SAddr3**	144	**PixData14**	196	**PixData21**
41	**AuxVidData1**	93	**SAddr4**	145	**PixData15**	197	**PixData23**
42	**AuxVidData4**	94	Reserved	146	Reserved	198	Reserved
43	**AuxVidData5**	95	**MonId1**	147	**PixData13**	199	Reserved
44	**AuxVidData0**	96	Reserved	148	**PixData10**	200	**PixData5**
45	**AuxVidData3**	97	**SAddr5**	149	**Data3**	201	**PixData7**
46	**RegAddr0**	98	**SAddr8**	150	**Data2**	202	**Data6**
47	**AuxVidData7**	99	**SAddr9**	151	**Data0**	203	**PixData6**
48	**AuxVidData2**	100	**SAddr7**	152	**Data1**	204	Reserved
49	**AuxVidHSync**	101	**SAddr2**	153	Reserved	205	Reserved
50	**notAuxVidBlank**	102	**SData2**	154	Reserved	206	**PixData4**
51	**HSyncOut**	103	**SData5**	155	**PixData19**	207	Reserved
52	**GND**	104	**VDD**	156	**GND**	208	**VDD**

Table 20.22 208-pin ceramic quad flat pack pinout by pin number

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AGND	68	GND	156	PixData29	11	Reserved	161
AGND	69	GND	157	PixData30	29	Reserved	163
AGND	133	GND	193	PixData31	10	Reserved	165
AGND	140	Green	76	PLLCap1	175	Reserved	167
AGND	141	GreenCmpImnt	77	PLLCap2	178	Reserved	168
AGND	173	HoldToGND	62	PLLCap3Pin1	170	Reserved	169
AGND	179	HoldToGND	64	PLLCap3Pin2	172	Reserved	187
AGND	185	HoldToGND	83	PLLCap4Pin1	184	Reserved	190
AuxVidData0	44	HoldToGND	87	PLLCap4Pin2	183	Reserved	191
AuxVidData1	41	HoldToGND	121	PLLCapRet1	174	Reserved	192
AuxVidData2	48	HSyncIn	66	PLLCapRet2	177	Reserved	195
AuxVidData3	45	HSyncOut	51	PLLRes	176	Reserved	198
AuxVidData4	42	MonId0	122	ProClkOut	8	Reserved	199
AuxVidData5	43	MonId1	95	RamVref	132	Reserved	204
AuxVidData6	39	MonId2	85	Red	74	Reserved	205
AuxVidData7	47	MonId3	91	RedCmpImnt	75	Reserved	207
AuxVidEDClk	124	notAuxVidBlank	50	RegAddr0	46	Rref	72
AuxVidESync	119	notDataStrobe	35	RegAddr1	33	SAddr0	117
AuxVidEVideo	123	notPOR	186	RegAddr2	20	SAddr1	108
AuxVidHSync	49	notRegWE	34	RegAddr3	55	SAddr2	101
AuxVidPClkIn	56	notSOE	90	RegAddr4	65	SAddr3	92
AuxVidPClkOut	54	notSWE	40	RegAddr5	24	SAddr4	93
AVDD	78	PGND	171	RegAddr6	30	SAddr5	97
AVDD	79	PixData0	158	Reserved	4	SAddr6	107
AVDD	130	PixData1	159	Reserved	5	SAddr7	100
AVDD	131	PixData2	164	Reserved	6	SAddr8	98
AVDD	182	PixData3	162	Reserved	9	SAddr9	99
Blue	80	PixData4	206	Reserved	15	SAddr10	109
BlueCmpImnt	82	PixData5	200	Reserved	17	SAddr11	112
CompRef	70	PixData6	203	Reserved	23	SAddr12	115
CRTClkIn	19	PixData7	201	Reserved	38	SAddr13	114
CRTClkIn2	13	PixData8	137	Reserved	57	SData0	113
CRTClkOut	18	PixData9	129	Reserved	58	SData1	110
CRTClkOut2	14	PixData10	148	Reserved	59	SData2	102
Data0	151	PixData11	188	Reserved	60	SData3	118
Data1	152	PixData12	2	Reserved	61	SData4	116
Data2	150	PixData13	147	Reserved	63	SData5	103
Data3	149	PixData14	144	Reserved	81	SData6	106
Data4	7	PixData15	145	Reserved	84	SData7	111
Data5	12	PixData16	136	Reserved	86	VDD	1
Data6	202	PixData17	142	Reserved	88	VDD	26
Data7	3	PixData18	166	Reserved	94	VDD	27
ExtRegBit	28	PixData19	155	Reserved	96	VDD	104
GateRef	71	PixData20	189	Reserved	126	VDD	105
GND	16	PixData21	196	Reserved	128	VDD	208
GND	36	PixData22	194	Reserved	135	VideoCtrlIn0	31
GND	37	PixData23	197	Reserved	138	VideoCtrlIn1	22
GND	52	PixData24	134	Reserved	143	Vref	73
GND	53	PixData25	139	Reserved	146	VSClkIn	25
GND	67	PixData26	127	Reserved	153	VSClkInB	32
GND	89	PixData27	125	Reserved	154	Xtal1	181
GND	120	PixData28	21	Reserved	160	Xtal2	180

Table 20.23 208 pin ceramic quad flat pack pinout designations by signal name

20.10 Ordering information

Device	Clock rate	Package	Part number
IMS G191	88MHz	208-pin ceramic quad flat pack	IMS G191F-88S