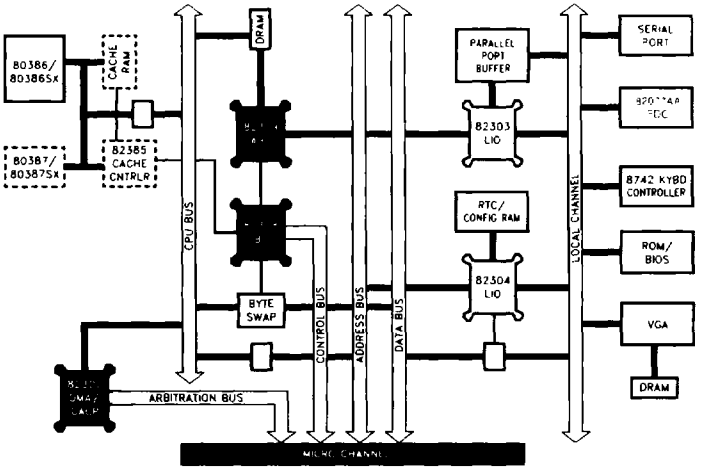
82311
HIGH INTEGRATION Micro Channel COMPATIBLE PERIPHERAL CHIP SET

- **High Integration VLSI Components to Implement Micro Channel Compatible Motherboard**
- **Single Architectural Solution for 386 DX 16 MHz, 20 MHz and 25 MHz Systems and 386 SX 16 MHz Systems**
- **Full Compatibility with IBM Micro Channel Architecture**
- **Zero-Wait State Performance**
- **Cache Interface (82385) for Highest Performance Compatible System Implementation with 386 DX**
- **Supports up to 16 MB of Memory on Motherboard**
  — Extended Memory for OS/2 Support
- **100% IBM Compatible VGA Graphics**
- **Flexible Memory Architecture Support**
  — Up to 4 Banks of Interleaved Page Memory
  — 256K, 1M, 4M DRAM Support
- **Supports the 82077AA Single Chip Floppy Disk Controller, Which Supports 3½" and 5¼" Disk Drives**
- **Keyboard and BIOS Support from 3rd Party**
- **Math Coprocessor(s) Interface (387 DX, 387™ SX)**
- **Surface Mount Packaging for Small Footprint Design (0.025" Pitch)**
- **Low Power CHMOS Technology**
- **Available in 100 & 132-Pin Plastic Quad Flat Pack Packages.**
  (See Packaging Spec. # 231369)

Intel's peripheral chip family is designed to support the new generation of Micro Channel compatible systems. Intel's Micro Channel compatible peripheral solution consists of highly integrated VLSI components designed to support 386 DX systems up to 25 MHz, as well as 16 MHz 386 SX systems.

The Intel solution is based on the high performance IBM* Model 80 register model but it is highly integrated to provide full compatibility across all models. The specifications for 82311 VLSI components conform to architectural specifications defined for the Micro Channel Bus Architecture. The VLSI components are implemented in 1.5 micron CHMOS technology and packaged in space saving surface mount JEDEC flat pack packages.

*IBM is a registered trademark of IBM.



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INTRODUCTION

The new generation of Personal Computer systems from IBM offers significant technological advantages over the PC/AT and XT systems. The most significant advancement is in the *Architectural* definition of the bus—Micro Channel Bus. Unlike the AT bus, the Micro Channel is well defined in terms of bus protocol timings. To create a compatible Micro Channel system requires adherence to the Micro Channel timings and electrical drive characteristics.

All IBM Micro Channel models have increased system functionality included on the motherboard. In the older PC/AT architecture, such functionality required the addition of peripheral cards. Specific features added to the motherboard include the Serial Port, Bi-directional Parallel Port and Video Graphics Control.

Micro Channel ARCHITECTURE

The Micro Channel Bus is defined to support an open architecture providing Multi-Master capability, Multi-Device arbitration with fairness, arbitration capability and easy configurability of the total system (Programmable Option Select-POS). Providing full details about the Micro Channel Bus Architecture is beyond the scope of this document. Please refer to IBM Technical Reference Manuals on Micro Channel systems.

To provide Multi-Master capability as defined in the Micro Channel Architecture, each Master device is responsible for driving the Address, Data, arbitration and control signals. For operation reliability and compatibility there are significant constraints in terms of timing and drive levels. These constraints are well documented in IBM's Technical Reference Manual for Micro Channel systems. Intel's chip set is designed to meet the Micro Channel timings.

The Micro Channel has four modes of Memory and I/O Bus cycles. These are Default cycle, Synchronous Extended cycle, Asynchronous Extended cycle and Matched Memory cycle. Each of these bus cycles is supported by the Intel Peripheral chip set.

COMPATIBILITY METRICS

The Intel chip set provides full compatibility with the IBM Micro Channel solution. All Bus cycles comply with the Micro Channel timings. Selection of buffers for drive level with minimum delays to meet Micro Channel timings are specified in the Intel *82311 Micro Channel Compatible Peripheral Chip Set Designers Guide.*

MEMORY PERFORMANCE

With the Intel chip set, Micro Channel compatible motherboards can be designed to provide zero-wait performance. Performance is predicated on memory design and DRAM speed selection. The Intel chip set offers flexible memory design support to meet various cost/performance goals.

SYSTEM CONSIDERATIONS

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System Components

82303 Local I/O Support Chip
82304 Local I/O Support Chip
82307 DMA/CACP Controller
82308 Micro Channel Bus Controller
82309 Address Bus Controller
82077AA Floppy Disk Controller

Note that the above names/numbers are frequency independent; i.e., they refer to a generic functional VLSI device. To actually implement for example, a 20 MHz system, however, requires an 82311-20 Chip Set as opposed to an 82311-16 Chip Set. The 25 MHz version of the 82308 (dubbed the 82308HS-25) cannot be used at 16 MHz or 20 MHz.

To implement a minimum configuration Micro Channel compatible motherboard, each of the seven system components listed above are required in addition to the following components:

- 386 DX or 386 SX Microprocessor
- TTL Buffers for Various Buses in the System
- 8742 Keyboard Controller with Firmware for 101 and 102 Keyboard Interface
- Battery-Backed Real Time Clock with CMOS RAM
- Serial Port
- *Memory*

— ROM BIOS
— DRAMs for Main Memory
— DRAMs for VGA

- System Clock Sources
- Mechanical Connectors/Components

The Intel solution is supported by a fully compatible BIOS firmware from a third-party vendor.

82311 CHIP SET SYSTEM CLOCK REQUIREMENTS

- **Introduction**
- **Clock Definitions**
- **Clock Requirements**

INTRODUCTION

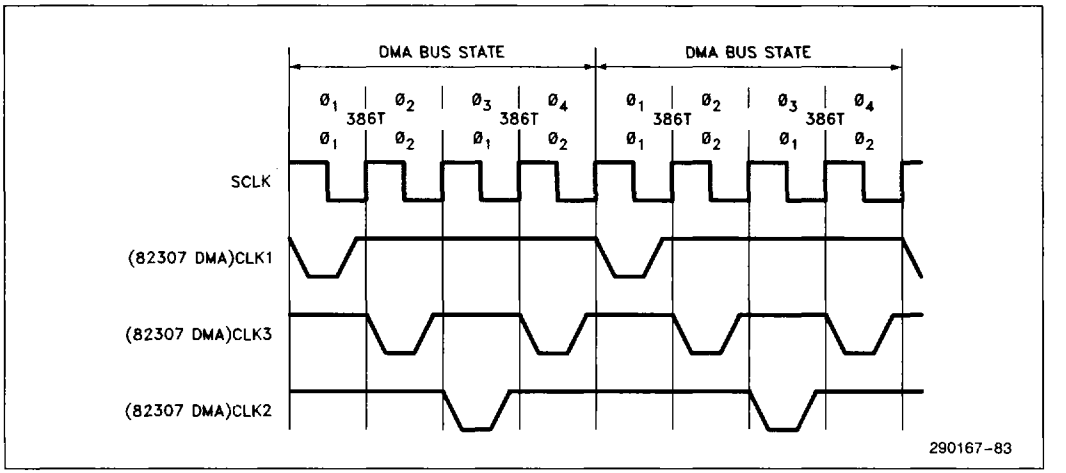
This section describes the basic clocking scheme of the host CPU (386 DX or 386 SX), LIO (82304), DMA (82307), BC (82308) and ABC (82309). Although each component spec individually describes its own clock requirements, this section describes the synchronous relationship that exists between them. (Note that several other clocks exist in a Micro Channel system. However, this section describes only those clocks that are synchronously related to the CPU clock.)

The clocking scheme essentially divides the DMA bus state into four phases as depicted in the figure. Note that there is a direct 2-to-1 mapping of 386 state to DMA state. The DMA (82307) comprehends phases by inputting distinct, active low, non-overlapping clock phases. The Address Bus Controller, Bus Controller and LIO device learn the system phase by synchronously sampling the falling edge of RESET, as described in the component specifications.

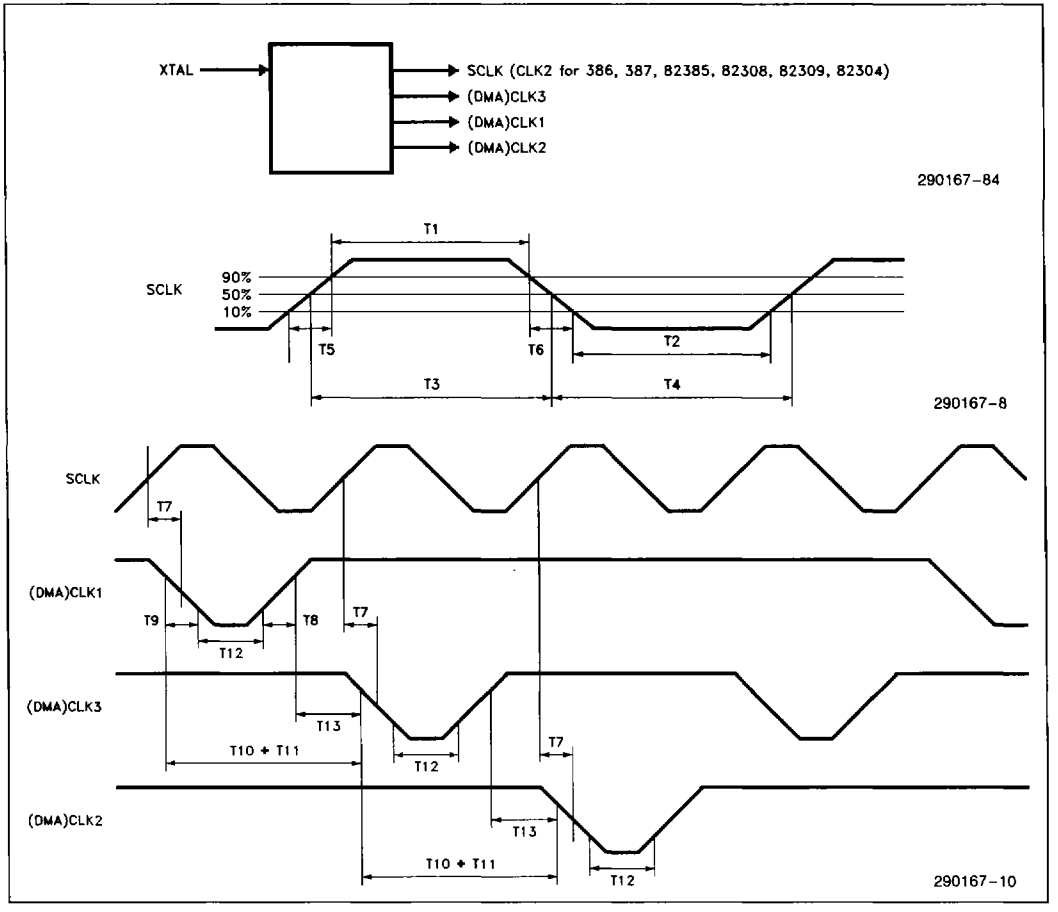
SYSTEM CLOCK CONSIDERATIONS

- SCLK load should be evenly divided between SCLKA, SCLKB, SCLKC, and SCLKD.
- The calculated characteristic impedance of all clock lines should be as near as possible to 100Ω.
- All clock lines should be kept as short as possible with no stubs.
- Clock lines should be driven at one end, with optional parallel termination at the other end. Series termination should be as close as possible to the driver.
- Guidelines in the *386™ Hardware Reference Manual,* Chapter 11, Sections 2 and 3, for clock design should be followed.
- A pull-down 100Ω resistor is needed on signal CLK3 (82309 pin 13) to terminate the signal properly.

BASIC FOUR-PHASE CLOCKING REQUIREMENT



CLOCK CIRCUIT DEFINITION



SYSTEM CLOCK REQUIREMENTS

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		Notes
		Min	Max	Min	Max	Min	Max	
T1	SCLK High Time (90%)	8		6.5		5.5		
T2	SCLK Low Time (10%)	8		6.5		5.5		
T3	SCLK High Time (50%)	12		10		9		1
T4	SCLK Low Time (50%)	12		10		9		1
T5	SCLK Rise Time		3.5		3.5		3.5	
T6	SCLK Fall Time		3.5		3.5		3.5	
T7	SCLK-To-DMACLK(N) Skew	−2	3	−2	3	−2	3	2
T8	DMACLK(N) Rise Time		2		2		2	
T9	DMACLK(N) Fall Time		2		2		2	
T10	SCLK Period							
T11	DMACLK-To-DMACLK Skew	−2	2	−2	2	−2	2	2
T12	DMACLK Low Time	15		15		12		
T13	DMACLK Non-Overlap Time	4		4		2		

NOTES:
1. Needed to enforce a duty cycle between 40% and 60% (45% and 55% at 25 MHz).
2. Limiting skew to this level is recommended.