National Semiconductor

ADVANCE INFORMATION

February 1992

Token-Ring Protocol Interface Controller (TROPIC™)

General Description

The Token-Ring Protocol Interface Controller (TROPIC) is a microCMOS VLSI device designed for easy design and implementation of IEEE 802.5 Token-Ring LAN interface adapters. The TROPIC chip includes integrated Analog and Digital Token-Ring interfaces and bus interface support for ISA, MCA, and 68xxx hosts. Transmit and receive buffers are implemented in shared RAM, with buffer arbitration and control provided by the TROPIC chip.

TROPIC provides full IEEE 802.5 compatibility, including Medium Access Control (MAC) and Logical Link Control (LLC) protocol handling, and is IBM 802.5 certified. Network performance exceeds current 802.5 Jitter Requirements. The TROPIC supports both 16 Mbps and 4 Mbps operation, which are chip-selectable.

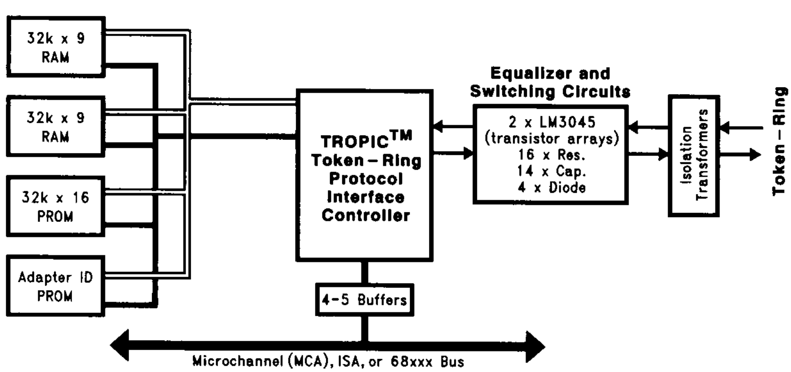
TROPIC integrates both digital and analog CMOS technologies in a single 175-pin, 1.48″ (37.2 mm) module. Operation is driven by an integral Microprocessor Unit (MPU), which is microcoded for flexible functionality. The microcode controlling the MPU (provided with TROPIC) is stored in an external PROM, which allows simple PROM upgrades to remain current with any future changes to the IEEE 802.5 standard. External RAM is used for data, control, and scratch-pad storage. The TROPIC chip provides an interface for directly attaching the required external PROM and RAM devices.

Host Transmit and Receive buffers and control blocks are provided through Shared Host RAM, which is managed by a TROPIC integral controller. The control blocks are used to pass commands and messages between the Host system and TROPIC.

Features

- Complete Token-Ring Adapter solution
- Integrated Bus Interface support for ISA, 68xxx, and MCA, including MCA POS registers
- MCA Layer 802.5 and LLC executed in integral microprocessor unit (MPU), minimizing Host software
- MPU microcode provided
- Chip-selectable 16/4 Mbps operation
- Minimal supporting hardware required
- Single +5V supply required
- CMOS for low power dissipation
- Configurable RAM size and Page size
- Optional Parity on Host interface
- Shared buffer memory using standard 16k by 9 or 32k by 9 RAM
- Support for IBM Source Routing Bridges
- Minimal Host memory space required

1.0 System Diagram



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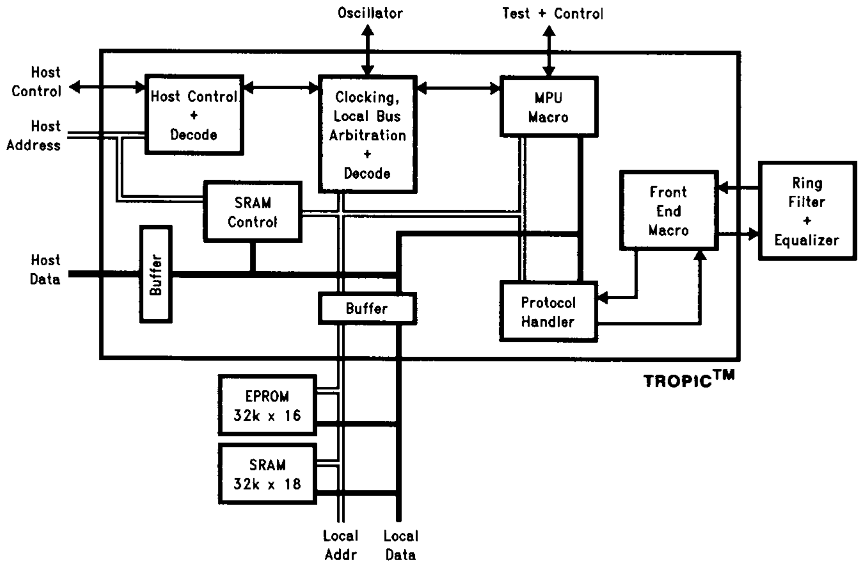

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3.0 Functional Description

TROPIC provides three external interfaces (Token-Ring, Host Bus, and Local Storage). TROPIC also requires certain Host system resources.

TOKEN-RING INTERFACE

The Front End Macro within TROPIC supplies a Ring Interface. This provides signals and inputs for external equalization and transformer circuits that form the actual Token-Ring Serial interface. The external Token-Ring Serial Interface provides physical connection to the Token-Ring LAN Media. It must include appropriate filter circuits (one Transmit filter and two Receive filters, one each for 4 Mbps and 16 Mbps operation), switching circuitry to switch between the 4 Mbps and 16 Mbps Receive filters, and line protection and conditioning components.

HOST BUS INTERFACE

The Host Bus interface allows the Host system to transfer data to and from TROPIC. This interface includes a twenty-four bit address bus, a sixteen bit data bus with optional parity, and control signals to allow the TROPIC Host Bus interface to attach directly, as a bus slave, to any of the three supported busses (ISA, MCA, or 68xxx). This makes TROPIC appear to be a memory device on the Host Bus that can be read or written using MMIO (Memory Mapped I/O) procedures.

LOCAL STORAGE INTERFACE

This interface provides direct attachment to local (to the adapter) PROM and RAM devices, which TROPIC uses exclusively. It includes an eighteen bit data bus and sixteen bit address bus, plus control lines to choose proper memory devices and control read and write operations.

HOST SYSTEM RESOURCE REQUIREMENTS

The TROPIC requires four Host system resources for MCA and ISA bus Hosts and three system resources for 68xxx bus Hosts, as follows:

- One Interrupt
- 16k or 64k of Shared RAM for shared buffers and control blocks (which allow the passing of high-level commands and status codes between TROPIC and the Host software)
- ROM/MMIO space (8k for MCA or ISA, 0.5k for 68xxx)
- For MCA and ISA *only,* 4 bytes of I/O space

Each of these resources is described in more detail later in this document.

TROPIC INTERNAL ELEMENTS

TROPIC can be implemented with an understanding of just its external interfaces and Host requirements. However, some consideration of TROPIC's internal structure and data flow is useful.

TROPIC consists of four main logical blocks:

- Front End Macro (FEM)
- Protocol Handler
- Integral MPU
- Shared Memory Controller

The functions of each of TROPIC's internal logical elements is best understood by considering data flow through the device during reception and transmission of Token-Ring data, as described next (these discussions assume some understanding of Token-Ring message structures).

3.0 Functional Description (Continued)

TROPIC DATA FLOW—RECEPTION

Front End Macro

The Front End Macro (FEM), combined with external equalizer components, provides the interface needed to transmit and receive Manchester coded data over the Token-Ring media at either 4 Mbps or 16 Mbps. The provided functions include:

- Equalization of transmission channel
- Detection of receive signal
- Clock recovery and re-timing of received signal
- Transmission of output data
- Control functions, such as wrap test of interface circuit
- Ring Insertion and Wire Fault detection

The Front End Macro provides D-to-A and A-to-D signal conversion only. The Protocol Handler and MPU perform MAC and LLC processing, encoding, and decoding of data streams.

Received signals that have been demodulated to digital form are sent to the Protocol Handler, along with a derived clock.

Protocol Handler

When data is received from the Front End Macro, the Protocol Handler first converts it into a form usable by the MPU, and generates parity on the received data for subsequent internal validity checks.

At the proper time during the receive sequence, the Protocol Handler begins bit-wise CRC (Cyclic Redundancy Check) accumulation on the received data. At the proper point in the received message, the Protocol Handler extracts the Token-Ring destination address. It then compares it with the values loaded into the Protocol Handler to determine if the message should be copied by this station. If so, the Protocol Handler begins transferring the message to TROPIC's internal RAM for additional MPU operations.

The Protocol Handler transfers, in order, the physical control field, the Token-Ring destination and source addresses, the data fields, and the message's CRC characters. When the CRC-protected portion of the message has been received, the received CRC characters are checked for validity.

If there is a CRC mismatch, the internal RAM area used to store the message is released and the message is not processed. Otherwise, proper changes are made to the frame status byte after the end of frame delimiter. At this point, processing moves from the Protocol Handler to the MPU.

MPU

The MPU assembles the transfers from the Protocol Handler into multi-byte segments. The areas where the message data has been stored are set up as valid for transfers to the Host Bus via the Shared Memory buffers.

The actual mapping and management of data into the buffers is controlled by the MPU microcode, and is also affected by certain host-controlled parameters and status codes from the Protocol Handler.

Shared Memory Controller

The actual transfer of data to the shared memory buffers is performed by the MPU, Protocol Handler, and Shared Memory Controller. When the transfer is complete, a status code is written to the appropriate buffer control block address in Shared RAM and an interrupt is issued to the Host. The Host software can then transfer the received data out of the Shared Memory area.

TROPIC DATA FLOW—TRANSMISSION

Transmissions from the Host are essentially the opposite of receptions. The Host software writes a transmit command code to the correct buffer control block address in Shared RAM, and issues an interrupt to TROPIC. When ready, TROPIC alerts the Host that it can transfer data into the appropriate buffer area in Shared Memory. When this transfer is made, the Shared Memory Controller alerts the MPU that a message is waiting for transmission, and passes the data location and length. The MPU then sets up the Protocol Handler to begin a transfer from Shared Memory to TROPIC's internal RAM.

When the Protocol Handler senses a pending transmission, it begins transferring the data into its buffers. When enough data is buffered to allow continuous transmission through the Front End Macro, the Protocol Handler waits for a token on the LAN. When a token is acquired, it is converted to a frame. Applicable control characters are generated, encoded, and transmitted (via the FEM), and the transmission continues with destination and source addresses, followed by the information field. When the entire information field has been transferred, the Protocol Handler inserts the CRC characters that it has accumulated into the message, followed by the encoded delimiter and frame status byte.

4.0 Initialization

The TROPIC can be configured to work in a number of environments. The Power-On Reset configuration is initialized in three ways:

- By **setting TROPIC input pins** to steady state levels using switches, jumpers, pullup/pulldown resistors, or custom wiring on the adapter
- By **gating Jumper values (or POS values** for MCA bus Hosts) into control registers during Power-On Reset (gating is triggered by the Jumper Select signal)
- By **Microcode** setting of control switches

Initialization can also be invoked by Host software during operation by using the Soft Reset Control Register (as described later).

BY TROPIC INPUT PINS

Host Configuration

The Host Configuration Pins 0, 1, and 2 are used to identify the type of bus used by the Host, i.e. ISA 8-bit, ISA 16-bit, MCA 8-bit, MCA 16-bit, 68xxx 8-bit, or 68xxx 16-bit. The Host Configuration setting affects a number of operating aspects, including memory mapping and register definitions.

BY JUMPERS (OR POS REGISTERS)

The control items described below are gated from Jumpers or MCA POS registers to TROPIC control registers (POS registers are described in more detail later). The status of many of these control registers are available in a Read-only mode during operation through the Jumper Registers (described later in Section 6.0).

4.0 Initialization (Continued)

Host Base Address

Defines the initial Base Address for Shared RAM (which can be relocated during operation).

Host Interrupt Level

For ISA and MCA busses, defines the interrupt level to use.

Ring Speed

Selects 4 Mbps or 16 Mbps Ring Speed operation (which is then reflected by the state of the Ring Speed status pins).

Shared Memory Page Size

Selects either a 16k or 64k Shared RAM size.

Primary/Secondary Adapter Select

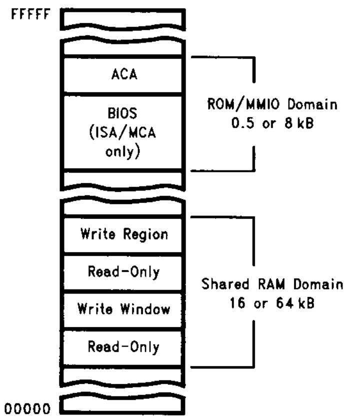
For ISA and MCA busses, sets TROPIC to function as either a primary or secondary adapter.

BY MICROCODE

Several TROPIC control registers are initialized by the microcode in the PROM. These registers control mostly memory mapping and management and internal parity functions, and are generally not available to the Host (even in Read-only mode).

5.0 Shared Memory Structure

TROPIC's Shared Memory is divided into two domains: the Shared RAM domain and the ROM/MMIO domain, as shown below:



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Shared Memory—Host Address Map

SHARED RAM DOMAIN

As discussed in the Functional Description section, transmission and reception data and control blocks are transferred between TROPIC and the Host via the TROPIC Shared RAM area. This area can be either 16 kB or 64 kB, depending on Host buffer size requirements. The Shared RAM domain's size and initial base address are configured during Reset initialization.

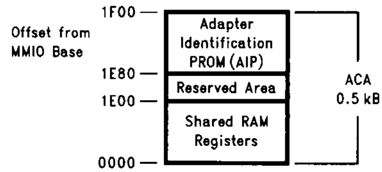
The Shared RAM is relocatable and pageable during operation. Current location and paging status is available through the Shared RAM address translation parameters defined in the RAM Relocation Register (RRR) and Shared RAM Paging Register (SRPR); these are described later in the Registers section.

The actual mapping of the buffers and control blocks in the Shared RAM area is controlled by microcode. Buffer management and handshaking are summarized in Section 7 of this document. More complete details are beyond the scope of this document, and are covered in a separate programming document.

ROM/MMIO DOMAIN

For MCA and ISA Hosts, the ROM/MMIO domain is 8k and includes 7.5k for BIOS and 0.5k for an area called the Attachment Control Area (ACA). For 68xxx hosts, the ROM/MMIO domain is 0.5k and contains only the ACA.

The structure of the ACA is shown below.



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Access Control Area (ACA)—Relative Address Map

The Adapter Identification PROM (AIP) area is a read-only region that contains unique adapter parameters, such as the IEEE node address and serial number.

The area from x1E00 to x1E80 is reserved and *should not* be accessed by the Host.

The Shared RAM Registers provide several important status and control registers that are accessible to the Host during operation. These are discussed in the next section.

6.0 Registers

The Host communicates with and controls TROPIC using three methods: Shared RAM, interrupts, and registers.

TROPIC supports three register areas: Programmed I/O (PIO) Registers, Shared RAM Registers, and MCA Standard POS Registers. Register usage varies according to bus type, as shown in the table below.

Register Usage by Bus Type

Bus Type	Shared RAM Registers	PIO Registers	MCA POS Registers
MCA	Yes	Yes	Yes
ISA	Yes	Yes	No
68xxx	Yes	No	No

The following sections briefly describe the contents of each of these register areas. Details on each register, including byte and bit level definitions, are covered in separate programming and application documents.

SHARED RAM REGISTERS

The Shared RAM Registers are used by all bus types and are located within the ACA Shared Memory area. They include mostly read-only status registers, with a few Read/Write control registers. For ISA and MCA buses, some of these registers are replicated in the PIO Registers; in such cases, one register is usually read-only while the alternative location is read/write. Note that addresses are relative to the ROM/MMIO Base Address.

6.0 Registers (Continued)

x1E00 RAM Relocation Register (RRR)

Used to relocate the Shared RAM region and indicate its page size and location. Also contains bits used to control different TROPIC operating modes.

x1E02 Write Region Base Register (WRBR)
x1E04 Write Region Open Register (WWOR)
x1E06 Write Region Close Register (WWCR)

The WRBR is a read-only register that indicates the base address of the primary Host write region in Shared RAM. The WWOR and WWCR read-only registers together define the starting and ending addresses of a secondary Host-defined write region. All three registers are used to control the read-write access areas of Shared RAM, which are used to pass commands and data to TROPIC.

x1E08 Host Interrupt/Status Register (HISR)

Read-only register contains interrupt and control bits to allow TROPIC to issue interrupts to Host software.

x1E0A TROPIC Interrupt/Status Register (TISR)

Read/write register that provides interrupts (for Shared RAM management, plus errors, timeouts, and other events) and control information that allow Host software to issue interrupts to TROPIC (letting the Host and TROPIC MPU communicate asynchronously). For ISA and MCA Hosts, this register also indicates which PIO addresses (x0A20 to x0A23 or x0A24 to x0A27) select the PIO addressable registers.

x1E0C Timer Control Register (TCR)
x1E0E Timer Value Register (TVR)

This register pair provides a Host-programmable general purpose timer for use by the Host. It is also used for Ring timing.

x1E12 Soft Reset Register
68xxx use only

A one-bit register that, when set to ONE, holds the TROPIC MPU in a reset state. This register is not directly accessible to ISA and MCA busses, but is instead set and reset through the PIO registers.

x1E14 Interrupt Vector Register (IVR)
68xxx use only

Contains an interrupt vector for use in Motorola Vectored Interrupt management.

x1E16 Jumper Register (JR)
68xxx use only

Contains static information required by TROPIC, most of which is loaded from Jumpers at Power-On Reset. Some of these values are duplicated in other registers. For ISA and MCA bus Hosts, the Jumper Register data is available in the PIO register area, as described later.

x1E18 Shared RAM Page Register (SRPR)

Allows the Host system to use memory paging schemes to allocate a smaller Shared RAM size (in the Host memory space) to the TROPIC adapter than actually exists. For example, if the adapter needs 64k of Shared RAM, but the Host system can allocate only 16k, the adapter RAM can be mapped to the 16k Host space as four separate 16k pages, any one of which is "visible" at a given moment. Note that TROPIC always has full access to the entire 64k space even if the Host is using a smaller page size.

PIO REGISTERS (ISA and MCA Only)

The PIO Registers provide access to certain Shared RAM Register data or controls that are unavailable to ISA and MCA Hosts via the Shared RAM Buffers. This includes Jumper Register information, Soft Reset Control (Enable Reset and Release Reset functions), and ROM/MMIO Address information. The PIO registers also provide a Status/Check read-only register for ISA bus Hosts.

If the adapter has been initialized as the Primary adapter (see the Initialization section), the PIO address locations range from x0A20 to x0A23. If the adapter has been initialized as the Secondary adapter, the PIO address locations range from x0A24 to x0A27.

The PIO registers are accessed using IN and/or OUT instructions. The same address can have different definitions based on whether IN or OUT access is used.

MCA POS REGISTERS (MCA Only)

TROPIC also provides POS registers for polling and initializing adapters in MCA Hosts. These registers let configuration information be written correctly from the non-volatile POS memory on the MCA motherboard to the TROPIC Jumper Bits, in keeping with MCA architecture.

7.0 Software Operation of TROPIC

As mentioned earlier, once TROPIC initialization is complete, the Host software communicates with and controls TROPIC through three methods: Shared RAM, interrupts, and registers. This section describes procedures for using those methods to operate TROPIC.

SHARED RAM CONTROL BLOCKS

One use of Shared RAM is to provide buffers for passing Token-Ring data between TROPIC and the Host. A second, equally important use of the Shared RAM is to allow the passing of specialized data between TROPIC and the Host software in *Control Blocks*. Control Blocks are used to pass *Commands* (i.e. requests), and the status of requests between TROPIC and the Host software.

There are four Control Blocks:

- **System Request Block (SRB)**—used to pass a command from the Host software to TROPIC and to pass return codes back to the Host software
- **System Status Block (SSB)**—if an SRB command requires further processing, this block is used to pass the ultimate results of the command from TROPIC to the Host software
- **Adapter Request Block (ARB)**—used to pass a command or information from TROPIC to the Host software and to pass return codes (if required) back to TROPIC
- **Adapter Status Block (ASB)**—used by the Host software to respond to an ARB command received from TROPIC, usually with an indication of successful or unsuccessful completion

These Control Blocks are used in conjunction with interrupts to provide event-driven, asynchronous operation of TROPIC, as described later.

Control Block Commands include high level requests from the Host software to TROPIC for DLC (Data Link Control), MAC (Media Access Control), and LLC (Logical Link Control) services, which are provided within TROPIC by its MPU and Protocol Handler. The Host software is therefore relieved from having to manage DLC, MAC, or LLC services, greatly reducing Host program size and complexity.

SHARED RAM BUFFERS

Shared RAM includes two types of buffers for passing Token-Ring data between TROPIC and the Host:

- Transmit Buffers (also called Data Holding Buffers, or DHBs)
- Receive Buffers

Transmit Buffers (DHBs)

TROPIC assembles and transmits frame data from the Transmit Buffers (based on transmit commands issued through the SRB [System Request Block] by the Host software).

The number and size of the Transmit Buffers is determined when TROPIC is issued an Open Adapter command (as described later).

Receive Buffers

TROPIC takes frame data from the Token-Ring and writes it into Receive Buffers in Shared RAM. It then places a Receive command in the ARB and issues an interrupt to the Host software. Among other things, the Receive command information will include the starting address of the Receive buffer.

The total size of the Receive Buffers is determined indirectly when TROPIC is issued an Open Adapter command (described later): all Shared RAM that is not needed for work areas, control blocks, communication areas, and Transmit Buffers is configured as Receive Buffers. Multiple Receive Buffers may be chained together to hold a complete frame, in which case each buffer will contain a pointer to the next buffer in the chain (and the Receive command will indicate the starting address of the first Receive Buffer).

INITIALIZATION HANDSHAKING

Before beginning an operating session with TROPIC, the Host software must first perform an initialization to ensure a known starting point. The typical method is as follows:

1. Invoke a Reset condition on TROPIC (using an Adapter Reset PIO Register access for MCA and ISA, or using direct Shared RAM Register Access for 68xxx).
2. Delay for at least 50 milliseconds.
3. Invoke a Reset Release (using a Reset Release PIO Register access for MCA and ISA, or using direct Shared RAM Register Access for 68xxx).
4. Set the Enable Interrupt bit of the HISR register (Host Interrupt/Status Register).
5. Wait for 1 to 3 seconds until TROPIC sets the "SRB Response" bit of the HISR register (indicating initialization and TROPIC's Adapter Diagnostics Program are complete).
6. Read the WRBR (Write Region Base Register) and the Shared RAM Segment address (using PIO Register access for MCA and ISA, or using direct Shared RAM Register Access for 68xxx). Use the offset in the WRBR and the Shared RAM Segment Address to calculate the initial location of the SRB where TROPIC has posted the results of the initialization (including any diagnostics failure messages).
7. Read and evaluate the results in the SRB and store important parameters. If diagnostics code indicates successful completion, proceed with operations.

HOST-TO-TROPIC COMMAND HANDSHAKING

The commands which can be issued from Host software to TROPIC using the SRB are summarized in a table later in this section. The general procedure for issuing a command to TROPIC is as follows:

1. Host software writes the appropriate Command code and related parameters into the SRB.
2. Host software sets the TISR register's "Command in SRB" bit to issue an interrupt to TROPIC.
3. TROPIC checks the validity of the SRB contents and either:
   — completely processes the command, sets a return code other than xFF in the SRB, and issues an interrupt to the Host software (by setting the HISR register's "Response in SRB" bit).
   — performs initial processing only, sets the return code to xFF in the SRB, and provides a "command correlator. " TROPIC issues an interrupt to the Host software (by setting the HISR register's "Response in SRB" bit) *only* if an SRB Free Request Interrupt is issued by the Host software (by setting the TISR register's "SRB Free Request" bit).
4. Depending on the command, TROPIC may request more data using the ARB (Adapter Request Block) and DHB (i.e. the Receive Buffer). The Host software uses the ASB (Adapter Status Block) to indicate that the requested data has been moved to the appropriate Shared RAM location.
5. When processing is completed for a command in process (i.e. return code is xFF in Step 3), TROPIC puts the final return code in the SSB (System Status Block) and interrupts the Host software by setting HISR "SSR Response" bit).
6. After the Host software reads the return code from the SSB, it interrupts TROPIC by setting the TISR "SSB Free" bit.

TROPIC-TO-HOST COMMAND HANDSHAKING

The commands which can be issued from TROPIC to the Host software using the ARB are summarized in a table later in this section. The general procedure for issuing a command to the Host software is as follows:

1. TROPIC writes the appropriate Command code and related parameters into the ARB.
2. TROPIC sets the TISR register's "ARB Command" bit to issue an interrupt to the Host software.
3. The Host software reads the ARB contents and issues an interrupt to TROPIC by setting the TISR register's "ARB Free" bit (to acknowledge command receipt and to indicate that TROPIC can re-use the ARB).
4. If a response is required based on the command, the Host software writes the response information into the ASB (Adapter Status Block) and issues an interrupt to TROPIC by setting the TISR register's "Response in ASB" bit.

5. After TROPIC reads the ASB response, it either:
   — sets a return code of xFF in the SRB, and issues an interrupt to the Host software by setting the HISR register's "ASB Free" bit *only* if the "ASB Free Request" interrupt bit is set.
   — sets an error return code indicating that an error has been detected, and issues an interrupt to the Host software by setting the HISR register's "ASB Free" bit, regardless of the status of the "ASB Free Request" interrupt bit.

SRB (Host-to-TROPIC) Command Summary

DIRECT INTERFACE COMMANDS

These commands affect TROPIC as a whole, rather than specific SAPs (Service Access Points) or link stations, and do not involve LLC processing.

Command Name	Code (Hex)	Description
DIR.CLOSE.ADAPTER	04	Closes the adapter, terminating all Ring communications (or Open Wrap test, if in process).
DIR.INTERRUPT	00	Forces a TROPIC interrupt; has no effect on Ring communications.
DIR.MODIFY. OPEN. PARMS	01	Modifies adapter options previously set by DIR.OPEN.ADAPTER.
DIR.OPEN.ADAPTER	03	Opens adapter with specified options, preparing the adapter for either normal ring operations (in automatic receive mode) or adapter wrap test.
DIR.READ.LOG	08	Reads and resets adapter error counters.
DIR.RESTORE.OPEN.PARMS	02	Modifies adapter options set by DIR.OPEN.ADAPTER.
DIR.SET.FUNCT.ADDRESS	07	Sets the functional address for the adapter to receive Ring messages.
DIR.SET.GROUP.ADDRESS	06	Sets the Group address for the adapter to receive Ring messages.

DLC (IEEE 802.2 SAP and Station Interfaces) COMMANDS

These commands affect SAPs (Service Access Points) or link stations, and make use of LLC protocols.

Command Name	Code (Hex)	Description
DLC.CLOSE.SAP	16	Closes (deactivates) an SAP and frees associated control block(s).
DLC.CLOSE.STATION	1A	Closes one link station; will not complete while Ring is "beaconing".
DLC.CONNECT.STATION	1B	Initiates a SABME_UA exchange to place the local and remote link stations in a data transfer state, or completes such an exchange that has been initiated by the remote station.
DLC.FLOW.CONTROL	1D	Controls the flow of data across a specified link station on an SAP, or every link on an SAP.
DLC.MODIFY	1C	Modifies selected working values on an open link station or the default values of an SAP.
DLC.OPEN.SAP	15	Opens (activates) an SAP and allocates an individual SAP control block.
DLC.OPEN.STATION	19	Allocates resources to support a logical link connection.
DLC.REALLOCATE	17	Removes a given number of link station control blocks from an SAP and returns them to the adapter pool, or removes a given number of link station control blocks from the adapter pool and returns them to an SAP.
DLC.RESET	14	Resets one SAP and all associated link stations, or all SAPs and all associated link stations.
DLC.STATISTICS	1E	Reads statistics for a specific link station.

SRB (Host-to-TROPIC) Command Summary (Continued)

TRANSMIT COMMANDS

There is actually only one transmit command with various subcommands to indicate the type of data to be transmitted. All the commands have the same format with the only difference being the actual command code. When a transmit command is issued to TROPIC, it indicates a request to send data. The actual data is not moved to the Transfer Buffer until TROPIC responds with a TRANSMIT.DATA.REQUEST command back to the HOST software.

Command Name	Code (Hex)	Description
TRANSMIT.DIR.frame	0A	Requests transmission of a Direct transmission; the application must assemble the entire message, leaving room for the source address, which TROPIC inserts; no LLC protocol assistance is provided in this mode.
TRANSMIT.I.frame	0B	Requests transmission of I-format (Information transfer format) frame.
TRANSMIT.UI.frame	0D	Requests transmission of UI-format (Unsequenced Information transfer format) frame.
TRANSMIT.XID.CMD	0E	Requests transmission of XID-format (Exchange Identification format) Command frame.
TRANSMIT.XID.RESP.FINAL	0F	Requests transmission of XID-format final Response frame (in response to a XID Command being received).
TRANSMIT.XID.RESP.NOT.FINAL	10	Requests transmission of XID-format non-final Response frame (in response to a XID Command being received).
TRANSMIT.TEST.CMD	11	Requests transmission of TEST-format Command frame.

ARB (TROPIC-to-Host) Command Summary

Command Name	Code (Hex)	Description
DLC.STATUS	83	Indicates a change in DLC status to the Host.
RECEIVED.DATA	81	Informs the Host that data for a particular STATION.ID has been received; the Host must move the data from the Shared RAM Receive buffers to buffers in Host memory.
RING.STATUS.CHANGE	84	Indicates a change in network status to the Host.
TRANSMIT.DATA.REQUEST	82	Informs the Host that TROPIC now needs data for a Transmit command previously issued by the Host.

Other TROPIC Functions

TROPIC supports two expanded functions: Bridge Operation and a Fast Path transmit method.

BRIDGE OPERATION AND COMMANDS

By using two TROPIC-based adapters in the same workstation, each connected to a separate Ring, a bridge application program can forward frames between the two Rings. This capability is supported by some additional resources:

- Two additional SRB commands
- One additional ARB command
- Two additional Shared RAM areas—a Bridge Transmit Control area and a Bridge Transmission buffer
- Two additional interrupt register bits, one in the HISR and one in the TISR

Bridge handshaking and operations are covered in detail in a separate programming document. The commands are summarized below:

Command Name	Code (Hex)	Description
DIR.CONFIG.BRIDGE.RAM	0C	Tells adapter how much shared RAM to allocate for bridge transmit control areas and buffers.
DIR.SET.BRIDGE.PARMS	09	Lets Host set values and conditions for adapter to use when copying frames for forwarding.
RECEIVED.BRIDGE.DATA	85	Informs Host that adapter has received frame that requires forwarding.

FAST PATH TRANSMIT OPERATION AND COMMANDS

Fast Path Transmit is an alternate transmission interface that replaces the standard method of requesting transmissions across the Shared RAM interface. The Fast Path interface provides a pool of transmit buffers that the Host software can fill asynchronously to the TROPIC MPU processing. The Host software moves Transmit commands and related data *together* to these buffers and then signals TROPIC that the pools have been updated. TROPIC then processes these frames according to each data block's associated command.

The Fast Path transmit interface is activated by issuing a "Configure Fast Path RAM" SRB command to TROPIC. TROPIC will subsequently process transmit commands based on the Fast Path interface procedures. Fast Path handshaking and operations are covered in detail in a separate programming document. The commands are summarized below:

Command Name	Code (Hex)	Description
DIR.CONFIG.FAST.PATH.RAM	12	Tells adapter to use Fast Path interface techniques and sets values for the amount of shared RAM to allocate for the transmit interface and the size of the Fast Path buffers to be used; this command can only be issued when the adapter is in a Closed state.
RETRANSMIT.DATA	86	Lets adapter request a retransmission of frames by the Host due to changes in link station status; the Host responds by moving frames to the transmit buffer pool starting at the frame with the correlator in the ARB.

8.0 Pin Definitions

Pin Number	Pin Type	Description
E01	I-PU	N/C (Note 2)
M01	I-PU	N/C (Note 2)
F01	I-PU	N/C (Note 2)
H12	I-PD	N/C (Note 2)
G13	I-PD	N/C (Note 2)
F11	I-PD	N/C (Note 2)
N01	I-PU	N/C (Note 2)
J01	I-PU	N/C (Note 2)
P11	I-PU	− Driver Disable (Host and Local Storage Bus at TRI-STATE®)
N07	A	Ring In A
P08	A	Ring In B
L12	I-PU	N/C (Note 2)
L11	I-PU	N/C (Note 2)
P12	I-PU	− Inhibit Memory
F14	I	32 MHz In
A01	I	± Host Reset
N10	I-PU	− Host Configuration 0
M10	I-PD	− Host Configuration 1
M09	I-PU	− Host Configuration 2
F09	I-PU	N/C (Note 2)

Note 1: Some pins have different definitions depending on the bus type used, as indicated in the table.

Note 2: N/C indicates a pin *should not* be connected for normal operation.

Pin Types

A = Analog

B = Bidirectional digital

B-PU = Bidirectional digital with internal pullup

I = Input-only digital

I-PU = Input-only digital with internal pullup

I-PD = Input-only digital with internal pulldown

O = Output-only digital

8.0 Pin Definitions (Continued)

Pin Number	Pin Type	Description (if bus-specific)	ISA	MCA	68xxx
D05	I		−MEMW	−S0	−LDS
D04	I		−MEMR	−S1	−UDS
E04	I		−IOR	−CMD	−AS
F03	I		−IOW	−ADL	RNW
C04	I		+AEN	−MIO	−CDT
B01	I		BHE	−SBHE	n/a
P04	I		n/a	−SETP	−IACK
F02	I		−DPEN	−DPEI	−DPEN
P02	I		IRQ2I	+A23	n/a
P01	I		IRQ3I	+A22	n/a
N02	I		IRQ6I	+A21	n/a
L04	I		IRQ7I	+A20	n/a
M12	B	N/C (Note 2)			
M11	B	N/C (Note 2)			
P05	A	Ring Out A			
N05	A	Ring Out B			
P07	A	Phantom Drive A			
P06	A	Phantom Drive B			
P09	A	4 Mbps PLL Filter			
P10	A	16 Mbps PLL Filter			
N09	O	−4 Mbps Ring Speed			
N08	O	−16 Mbps Ring Speed			
L10	O	FERCLK Out			
P14	B-PU	N/C (Note 2)			
P13	B-PU	N/C (Note 2)			
N13	O	N/C (Note 2)			
N12	O	N/C (Note 2)			
N11	O	N/C (Note 2)			
M14	B-PU	N/C (Note 2)			
M13	B-PU	N/C (Note 2)			
N14	O	N/C (Note 2)			
E12	O	−RAM/−Code/Data			
D12	O	−CAS HI/−SRAM Select HI			
D11	O	−CAS LO/−SRAM Select LO			

Note 1: Some pins have different definitions depending on the bus type used, as indicated in the table.

Note 2: N/C indicates a pin *should not* be connected for normal operation.

Pin Types

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B-PU = Bidirectional digital with internal pullup
I = Input-only digital
I-PU = Input-only digital with internal pullup
I-PD = Input-only digital with internal pulldown
O = Output-only digital

8.0 Pin Definitions (Continued)

Pin Number	Pin Type	Description (if bus-specific)	ISA	MCA	68xxx
G12	O	−ROM Select			
F13	O	−AIP Select			
E13	O	−DRAM/EEPROM Write Enable			
E11	O	−SRAM Output Enable			
E14	B	−Storage Write			
C03	O		IRQ2O	−IRQ2	n/a
C01	O		n/a	−DS16	n/a
C02	O		+RDY	+RDY	−DTAK
E03	O		−CHCK	−CHCK	−BERR
D01	O		n/a	−SFBK	−IRPT
D03	O		IRQ6O	−IRQ6	n/a
D02	O		IRQ7O	−IRQ7	n/a
E02	O		IRQ3O	−IRQ3	n/a
F10	O		−BIOS	−BIOS	n/a
P03	B		n/a	+MA24	n/a
B02	B		−REF	−REF	+ADRX
A07	O	−EHDH (Enable Host Data High)			
B07	O	−EHDL (Enable Host Data Low)			
C07	O	HDDIR (Host Data Direction; Low = Read, High = Write)			
A02	O	−EHPI (Enable Host Parity In)			
E10	O	−JMPR			
L02	I	± Host Address 19	(MSB)		
L01	I	± Host Address 18			
K03	I	± Host Address 17			
K01	I	± Host Address 16			
J02	I	± Host Address 15			
H01	I	± Host Address 14			
G01	I	± Host Address 13			
F05	I	± Host Address 12			
N04	I	± Host Address 11			
N03	I	± Host Address 10			
M04	I	± Host Address 9			
M03	I	± Host Address 8			
M02	I	± Host Address 7			

Note 1: Some pins have different definitions depending on the bus type used, as indicated in the table.

Note 2: N/C indicates a pin *should not* be connected for normal operation.

Pin Types

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I = Input-only digital

I-PU = Input-only digital with internal pullup

I-PD = Input-only digital with internal pulldown

O = Output-only digital

8.0 Pin Definitions (Continued)

Pin Number	Pin Type	Description (if bus-specific)	ISA	MCA	68xxx
L03	I	± Host Address 6			
K05	I	± Host Address 5			
K04	I	± Host Address 4			
K02	I	± Host Address 3			
H03	I	± Host Address 2			
H02	I	± Host Address 1			
G02	I	± Host Address 0	(LSB)		
E09	B	± Host Data 15	(MSB)		
D09	B	± Host Data 14			
C09	B	± Host Data 13			
B09	B	± Host Data 12			
A09	B	± Host Data 11			
C08	B	± Host Data 10			
B08	B	± Host Data 9			
A08	B	± Host Data 8			
B03	B	± Host Data P1			
C06	B	± Host Data 7			
B06	B	± Host Data 6			
A06	B	± Host Data 5			
C05	B	± Host Data 4			
B05	B	± Host Data 3			
A05	B	± Host Data 2			
B04	B	± Host Data 1			
A04	B	± Host Data 0	(LSB)		
A03	B	± Host Data P0			
F12	B	− Storage Address 0	(LSB)		
H11	B	− Storage Address 1			
G14	B	− Storage Address 2			
H13	B	− Storage Address 3			
H14	B	− Storage Address 4			
J12	B	− Storage Address 5			
J13	B	− Storage Address 6			
J14	B	− Storage Address 7			
K09	B	− Storage Address 8			

Note 1: Some pins have different definitions depending on the bus type used, as indicated in the table.

Note 2: N/C indicates a pin *should not* be connected for normal operation.

Pin Types

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B-PU = Bidirectional digital with internal pullup
I = Input-only digital
I-PU = Input-only digital with internal pullup
I-PD = Input-only digital with internal pulldown
O = Output-only digital

8.0 Pin Definitions (Continued)

Pin Number	Pin Type	Description (if bus-specific)	ISA	MCA	68xxx
K11	B	– Storage Address 9			
K12	B	– Storage Address 10			
K13	B	– Storage Address 11			
K14	B	– Storage Address 12			
L13	B	– Storage Address 13			
L14	B	– Storage Address 14	(MSB—TROPIC Local Storage)		
D14	B-PU	– Storage Data 0	(LSB)		
C14	B-PU	– Storage Data 1			
B14	B-PU	– Storage Data 2			
A14	B-PU	– Storage Data 3			
D13	B-PU	– Storage Data 4			
C13	B-PU	– Storage Data 5			
B13	B-PU	– Storage Data 6			
A13	B-PU	– Storage Data 7			
A12	B-PU	– Storage Data P0			
D10	B-PU	– Storage Data 8			
C10	B-PU	– Storage Data 9			
B10	B-PU	– Storage Data 10			
A10	B-PU	– Storage Data 11			
C11	B-PU	– Storage Data 12			
B11	B-PU	– Storage Data 13			
A11	B-PU	– Storage Data 14			
C12	B-PU	– Storage Data 15	(MSB)		
B12	B-PU	– Storage Data P1			

Note 1: Some pins have different definitions depending on the bus type used, as indicated in the table.

Note 2: N/C indicates a pin *should not* be connected for normal operation.

Pin Types

A = Analog

B = Bidirectional digital

B-PU = Bidirectional digital with internal pullup

I = Input-only digital

I-PU = Input-only digital with internal pullup

I-PD = Input-only digital with internal pulldown

O = Output-only digital

9.0 Host Hardware Interface

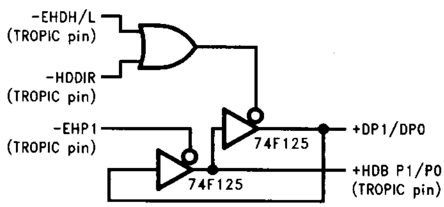
Because TROPIC has a limited number of I/Os and its drivers cannot directly drive the loads encountered on many of the Host interface signals, a certain amount of support components ("glue") must be added to each adapter, as described in this section.

FOR ISA BUS HOSTS

- Bidirectional TRI-STATE buffer module(s), such as a 74ALS245, to buffer data bits. HDB [Host Data Bus] (15–0) is buffered as D15–D0 for a halfword adapter, HDB(7–0) is buffered as D7–D0 for a byte adapter. Its direction pin is attached to the HDDIR signal from TROPIC: its enable pin is attached to the EHDH/L signals from TROPIC.
- Open collector drivers for the CHCK and RDY signals.
- Open collector drivers for the IRQ2/3/6/7O signals. The outputs of the glue from these signals attach directly to the IRQ2/3/6/7I signals.

FOR MCA BUS HOSTS

- Bidirectional TRI-STATE buffer module(s), such as a 74ALS245, to buffer data bits. The direction pins are attached to the HDDIR signal from TROPIC; each enable pin is attached to the EHDH/L signals from TROPIC. Each byte has its own enable pin, as required by MCA architecture.
- TRI-STATE drivers like the 74F125 for the data parity bits and an OR gate like the 74AS32. Each parity bit requires two TRI-STATE gates and an OR gate (as shown below), TROPIC provides the EHPI signal.



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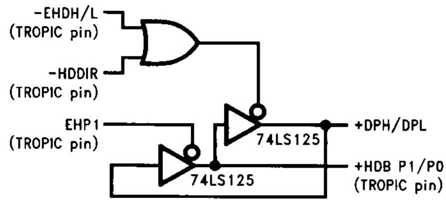
- An open collector driver for the CHCK signal.
- An open collector driver for the DPAREN signal. A 74F125 with both input pins tied to the HDDIR signal should be used, with its DPAREN output tied to the DPENI signal.
- An open collector driver for the IRQn signals.

FOR 68xxx BUS HOSTS

- Bidirectional TRI-STATE buffer module(s), such as a 74ALS245, to buffer data bits. HDB [Host Data Bus] (15–0) is buffered as D15–D0 for a halfword adapter, HDB(7–0) is buffered as D7–D0 for a byte adapter. Direction pins are attached to the HDDIR signal from TROPIC; the enable pin is attached to the EHDH/L signals from TROPIC. If the adapter bus is 8-bit, the buffer module must be tied to the low data byte, i.e. HDB(7–0).
- Open collector drivers for the BERR, IRPT, and DTACK signals.
- TRI-STATE drivers like the 74F125 for the data parity bits and an OR gate like the 74LS32. Each parity bit requires two TRI-STATE gates (as shown below).



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10.0 Specifications

Electrical Characteristics

Absolute Maximum Ratings

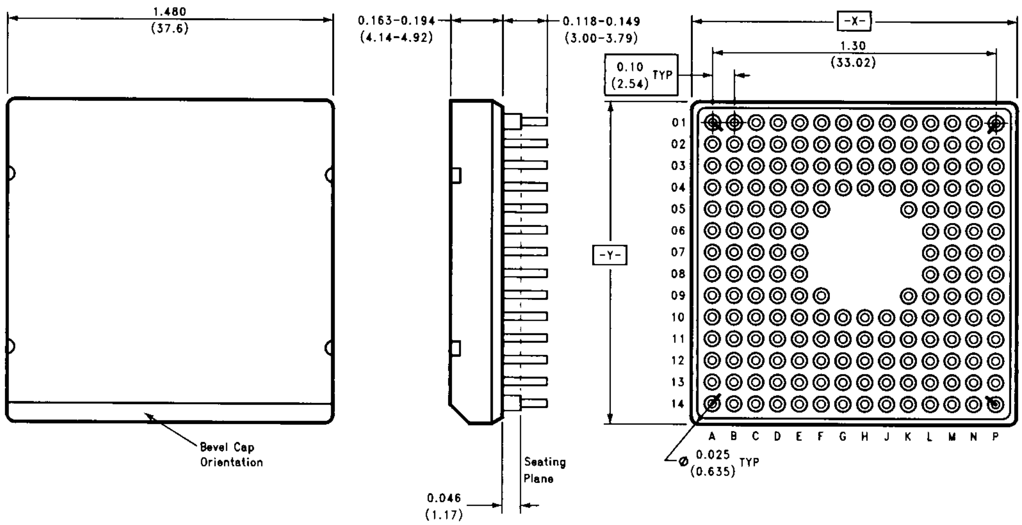
Supply Voltage (V_{CC})	+5.0V ±10%
Power Dissipation (PD)	(@4 Mbps) 800 mW
	(@16 Mbps) 990 mW
Storage Temperature Range (T_{STG})	0.6°C to 60°C

DC Specifications

Symbol	Parameter	Min	Max	Units
V_{OH}	Minimum High Level Output Voltage	3.8		V
V_{OL}	Minimum Low Level Output Voltage		0.5	V
V_{IH}	Minimum High Level Input Voltage	2.0		V
V_{IL}	Minimum Low Level Input Voltage		0.8	V
I_L	Input Leakage Current		10.0	μA
C_{IN}	Input Capacitance		5.0	pF

Physical Package

1.48″ (37.6 mm) metallized-ceramic Molded Pin Grid Array module with 175 module pins set in a 14 x 14 grid array. These include 146 signal pins and 29 power source pins.



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