MC 9010

Micro Channel
Bus Master Interface Chip for
National DP83932 Ethernet Controller

T-52-33-55

April 1992

Features

- Micro Channel Bus Master Interface for National DP83932 Ethernet Controller

- Supports Micro Channel Streaming Data rates to 40 MBytes/sec

- BIOS PROM and Node ID PROM support

- 20 MHz Clock

- Direct connect to System Bus of all Host Interface Control Signals

- Low power CMOS in 128 Pin Plastic QFP Package

General Description

The MC 9010 is designed to provide the most compact, inexpensive and highest performance Micro Channel bus interface for Bus Master adapter boards that use the National Semiconductor 83932 "SONIC" Ethernet Controller Chip.

Use of the 90X0 series minimizes hardware and software development costs and time because similar adapter hardware and driver designs can be used for either AT, Micro Channel or EISA applications.
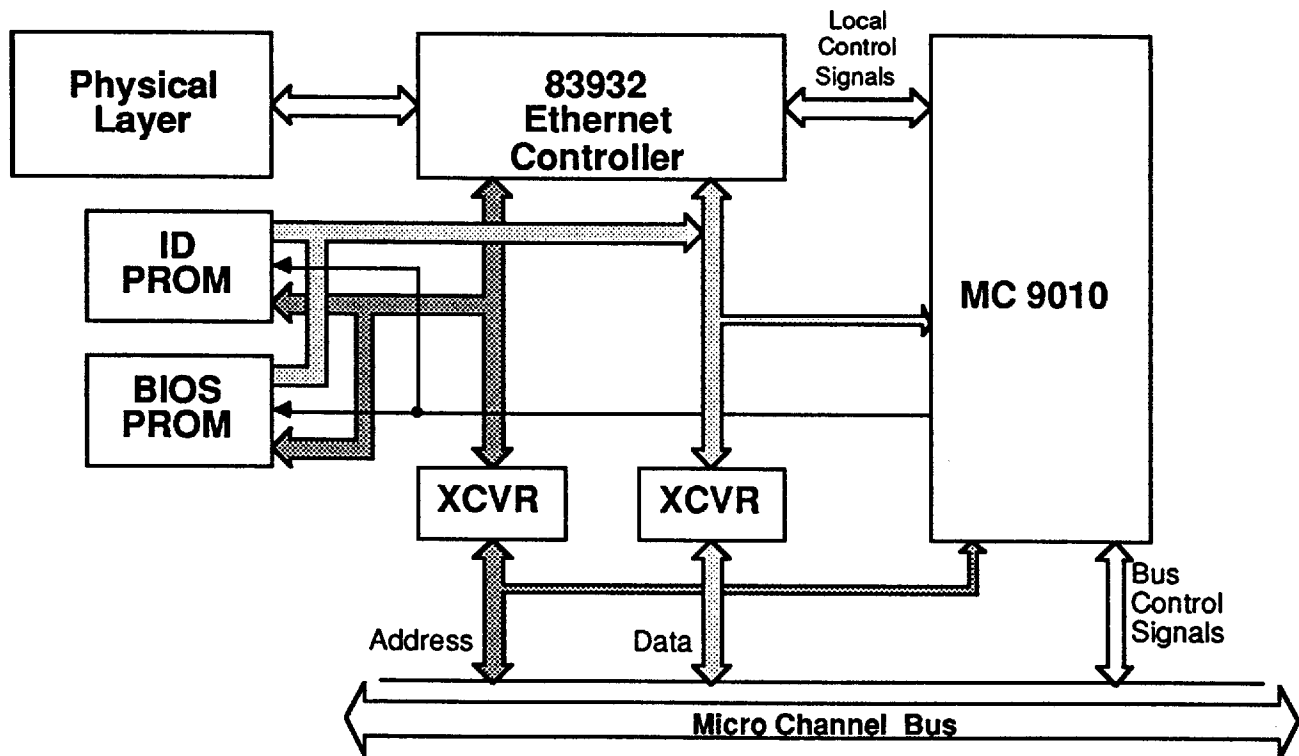

FIGURE 1. MC 9010 Functional Block Diagram

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SECTION 1 - INTRODUCTION

Revision History

Changes to February 1992 data sheet:

1. -HDOE2 (PIN 98) changed from active high to active low.
2. In figure 3, -HDOE2 is connected direct to the buffer input. It is not nanded with HLDA.
3. In Register 2\(POS 102), Bit 6 (Bus Master Data Size) polarity is reversed.

Changes to December 1991 and earlier data sheets:

Refer to February 1992 data sheet. For a complete revision history contact PLX Technology. For designs which were based on December 1991 and earlier data sheets, PLX recommends that designers contact PLX to ensure that all data sheet changes have been incorporated in the design.

MC 9010 GENERAL DESCRIPTION

The MC 9010 is designed to provide the most compact, inexpensive and highest performance Micro Channel bus interface for Bus Master adapters that use the National Semiconductor DP83932 Ethernet Controller Chip. Adapters which use the MC 9010 and the DP83932 can achieve up to eight times the system bus transfer rate of a typical sixteen bit DMA slave LAN board and can be competitive in cost. LAN performance is also enhanced by the more efficient protocol processing capabilities of the SONIC chip. Furthermore, a bus master frees the host processor from managing bus data transfer operations, which improves overall system performance.

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Data Transfer Modes

The MC 9010 supports both 16 and 32 bit Burst and Streaming Data Transfers. In addition, the MC 9010 supports Micro Channel slave mode for initialization of registers and access to other adapter board slave devices such as BIOS PROM and the Node ID PROM functions.

POS Configuration Registers

The MC 9010 supports POS registers 100 through 105 (102 through 105 are internal) which are configured by the host through the Micro Channel card setup routine. Included in these registers are the board ID, interrupt request level, PREEMPT timer configuration, data size, I/O address decode bits, PROM address decode bits, arbitration priority, Channel Check indicator and Data Streaming indicator. The MC 9010 also provides three external user bits for application specific configuration information.

Specific MC 9010 functions

MC 9010 major functions include:

1. **Master Control Signal Protocol Converter.** The chip converts all the handshakes of the DP83932 to Micro Channel bus master handshakes.

2. **Slave controller.** The MC 9010 includes a Micro Channel slave interface for control of adapter board slave functions.

3. **Arbitration.** The MC 9010 contains a 16 level arbiter with programmable PREEMPT timer. The PREEMPT timer can be programmed to release the bus within 4.0 or 6.8 microseconds.

4. **Address decoder.** The MC 9010 decodes host address bits A16-A8, A4-A0 and contains an enable pin for an external A31-A17 or A24-A17 address decoder. The MC 9010 decodes these addresses to generate chip selects and to configure and read POS registers.

5. **Interrupt generator.** The MC 9010 can generate one of four host interrupts from one local interrupt, programmable through POS registers.

6. **External Buffer Controller.** The MC 9010 generates all buffer enable and direction signals for external address and data transceivers.

7. **Clock.** The MC 9010 runs from an inexpensive crystal and can generate a clock up to 40 MHz for external and internal use.

8. **User programmable configuration bits.** The MC 9010 provides up to three external bits which can be configured through the POS registers.

9. **Bus drivers.** All Micro Channel control signals generated by the MC 9010 drive the bus directly, without requiring external drivers. Address and data signals do require buffers or transceivers.

10. **Sonic Port Selector Register.** The MC 9010 contains a transfer status register which latches Local Address 3-5 to provide port select information to the DP83932 chip.

11. **POS Registers.** The MC 9010 supports POS registers 100 through 105 (102 through 105 are internal).

12. **Adapter ID mapping.** The adapter ID number is mapped into I/O address space to allow the option of implementing the ID adapter number in the ID PROM.

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Intel Mode Handshake Signals		Arbitration
POS/Config Logic		Host Bus Control Signals
PROM & Other Chip Selects	Port Selector Register	
Slave & Buffer Control		Address Decode & Interrupt

DP83932 Network Interface Controller

BIOS PROM

ID PROM

Local Control Signals

Local Bus

ADDRESS XCVR

DATA XCVR

Bus Control Signals

Address

Data

Address
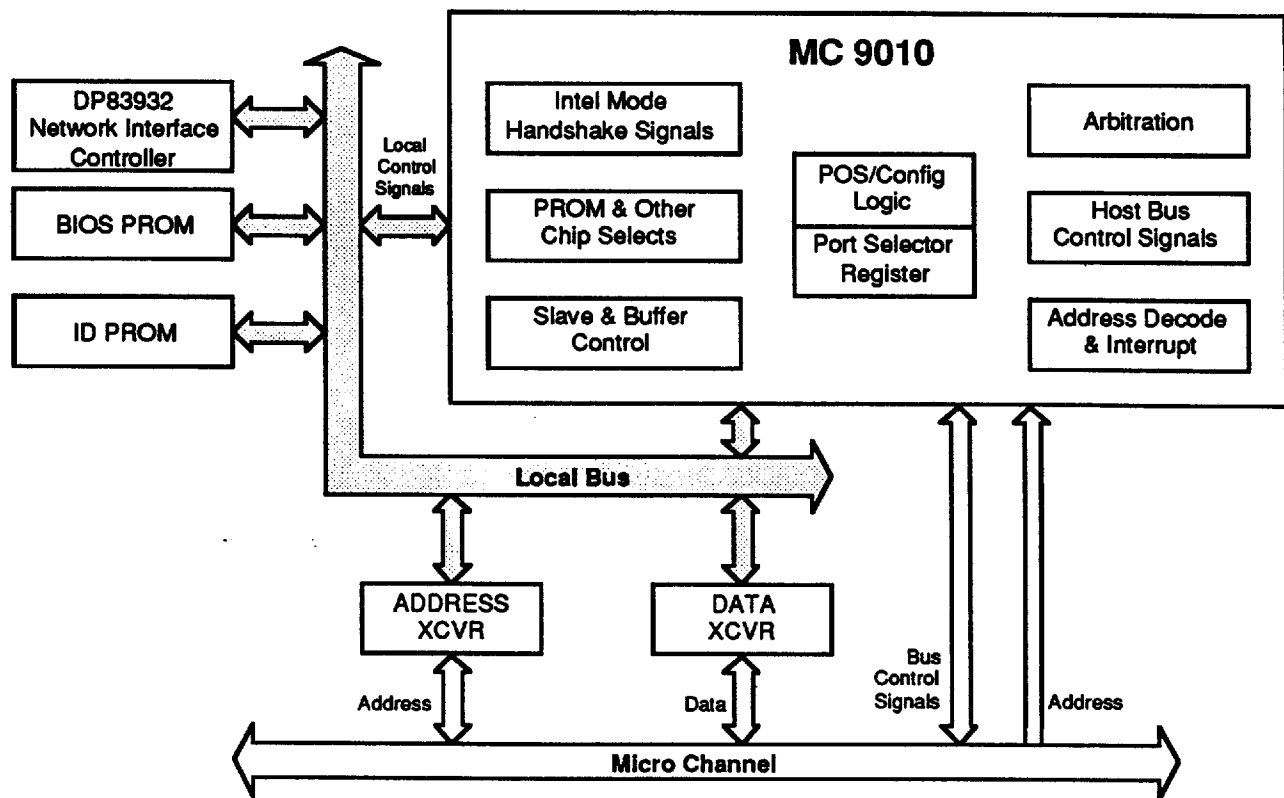
Micro Channel

FIGURE 2. MC 9010 Functional Block Diagram

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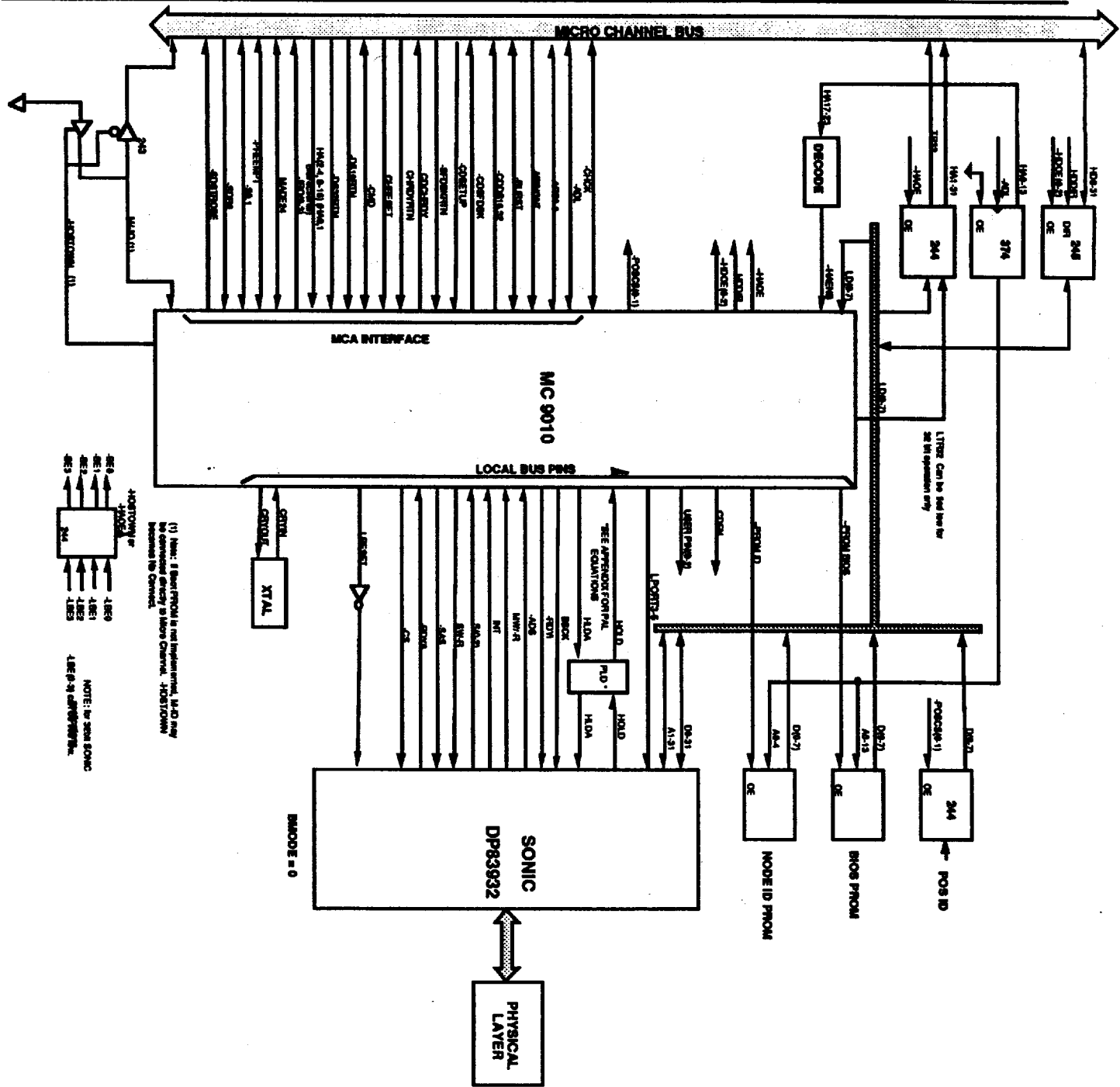
Figure 3
Low cost, Micro Channel
Direct Bus Master Adapter

Top pins (left to right, 128–97):
VSS, -ADL, NC, -SFDBKRTN, NC, CHRDYRTN, MADE24, -CDDS32, -SBHE, -CHCK, USER_PIN0, LD0, LTR32, LD1, LD2, VSS, VDD, VSS, LD3, LD4, LD5, LD6, LD7, -HA0E, NC, NC, HDDIR, NC, -HDOE0, -HDOE1, -HDOE2, VSS

Pin numbers top: 128 127 126 125 124 123 122 121 120 119 118 117 116 115 114 113 112 111 110 109 108 107 106 105 104 103 102 101 100 99 98 97

Left side pins:
VDD	1
ARB0	2
ARB1	3
ARB2	4
NC	5
ARB3	6
ARB/-GNT	7
HA0	8
HA1	9
HA2	10
HA3	11
-BURST	12
-CDDS16	13
-CDSETUP	14
-CDSFDBK	15
VSS	16
VDD	17
CDCHRDYx	18
CHRESET	19
-CMD	20
-DS16RTN	21
-DS32RTN	22
NC	23
NC	24
NC	25
NC	26
HA4	27
NC	28
VDD	29
HA8	30
HA9	31
VSS	32

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Right side pins:
96	VDD
95	-HOST/OWN
94	-SDSTROBE
93	-SDR0
92	NC
91	-S0
90	-S1
89	-PREEMPT
88	-POSCS1
87	-POSCS0
86	M/-IO
85	-IRQ3
84	-IRQ2
83	-IRQ1
82	-IRQ0
81	VSS
80	VDD
79	-HAENB
78	LPORT5
77	LPORT4
76	LPORT3
75	-PROMID
74	-PROMBIOS
73	CRYOUT
72	CRYIN
71	VSS
70	VDD
69	NC
68	CDEN
67	NC
66	NC
65	VSS

Pin numbers bottom: 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64

Bottom pins (left to right, 33–64):
VDD, HA10, HA11, HA12, NC, HA13, HA14, HA15, HA16, -ADS, NC, BSCK, NC, -CS, HOLD, VSS, VDD, HLDA, LINT, MW/-R, USER_PIN2, -RDYi, LRESET, S0, S1, S2, -SAS, NC, SW-R, USER_PIN1, -RDYo, VDD

Figure 4 Pin Out

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SECTION 2 - REGISTER DESCRIPTION

Table 2.1 summarizes the POS register locations of the MC 9010. The "I" registers are internal to the chip. The "E" registers are external components which contain the adapter board ID.

Table 2.1 Register Summary

Register Number	Register Description
0	E - ID Byte 0 (POS 100)
1	E - ID Byte 1 (POS 101)
2	I - Config 0 (POS 102)
3	I - Config 1 (POS 103)
4	I - Config 2 (POS 104)
5	I - Config 3 (POS 105)
15	I - Config 15 (Transfer Status)

The four configuration (POS) registers may be accessed through a normal I/O decode as well as the Micro Channel Card Setup routine. Register 15, the transfer status register, is accessed through an I/O decode only.

The Adapter ID number is mapped into I/O space to allow the option to implement the adapter ID number in the ID PROM.

Address Decode Table

A15-A8	A7-A5	A4	A3-A0	
BASE (See POS 103)	XXX	0	0000-0001	- Adapter ID Number
BASE (See POS 103)	XXX	0	0010	- Config. 0 Register (POS 102)
BASE (See POS 103)	XXX	0	0011	- Config. 1 Register (POS 103)
BASE (See POS 103)	XXX	0	0100	- Config. 2 Register (POS 104)
BASE (See POS 103)	XXX	0	0101	- Config. 3 Register (POS 105)
BASE (See POS 103)	XXX	0	0110-0111	- Reserved
BASE (See POS 103)	XXX	0	1000-1110	- Node ID PROM
BASE (See POS 103)	XXX	0	1111	- Register 15 (Transfer Status)
BASE (See POS 103)	XXX	1	0000-1111	- DP83932 Chip Select

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Register Summary

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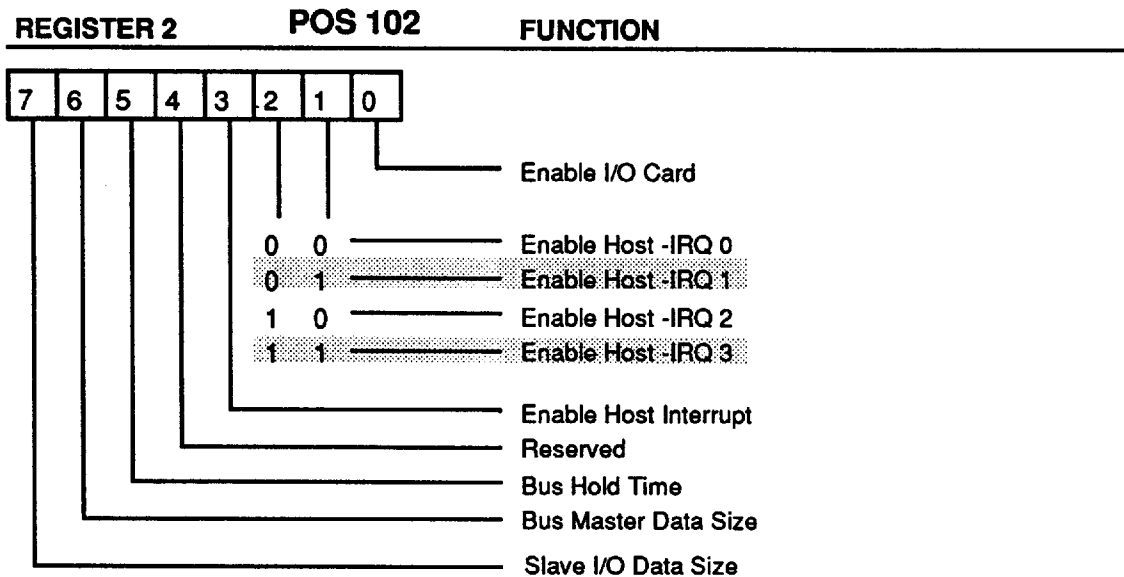### Register 0, 1 - ID Byte 0 and 1 (POS 100, 101)

READ (host)

These external registers contain a unique card slot ID to support automatic I/O board set-up. During set-up the contents of these registers are gated to the host bus by the MC 9010 (enabled through pins -POSCS(0-1)). -POSCS(0-1) can enable the ID from -244s or the Node ID PROM.

Register 2 - Configuration 0   (POS 102)

This POS 102 register contains configuration data that is written by the host during I/O set-up.

WRITE / READ

| REGISTER 2 | POS 102 | FUNCTION |

```
7  6  5  4  3  2  1  0

                         Enable I/O Card

         0  0            Enable Host -IRQ 0
         0  1            Enable Host -IRQ 1
         1  0            Enable Host -IRQ 2
         1  1            Enable Host -IRQ 3

                         Enable Host Interrupt
                         Reserved
                         Bus Hold Time
                         Bus Master Data Size
                         Slave I/O Data Size
```

Bit 0   -   This bit is set to 0 whenever the MC 9010 is hard reset. The host processor writes this bit to a one thus enabling the card (and chip) for normal operation. When this bit is set to 0 the MC 9010 does not respond to any host bus access (except set-up).

Bits 1-2 -   These bits select which Micro Channel interrupt signal to assert when the DP83932 asserts its interrupt request line.

Bit 3   -   When set to 1, this bit enables the -IRQ(0-3) signals. When set to 0 the -IRQ (0-3) outputs will be tristate.

Bit 4   -   Reserved

Bit 5   -   When set to 0, the MC 9010 will hold the bus no longer than 4 microseconds after the MC 9010 detects a -PREEMPT condition. When this bit is set to 1, the MC 9010 holds the bus no longer than 6.8 microseconds after a -PREEMPT condition.

Bit 6   -   This bit specifies the data width for bus master transfers. This bit selects between a 16 bit (when set to 0) or 32 bit (when set to 1) bus master interface. POS 103 bit 3 must also be properly configured.

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Bit 7   -   This bit specifies the data width for slave access to the DP83932. Set to 0 is a 16 bit slave access (-CDDS16). Set to 1 is a 32 bit slave access (-CDDS32).   *T-52-33-55*

Register 3 - Configuration 1 (POS 103)

The Configuration 1 Register (POS 103) contains the I/O address decode range for the MC 9010's chip selects and registers. Bits 4-7 of this register are compared against host address bits A15-A8 to select the I/O address of the board as shown in the "Register 3" description below. This I/O address is a base address which selects a 256 byte I/O address range. The individual chip selects and the POS registers reside in 32 bytes of Micro Channel I/O space as shown at the beginning of this section, decoded from A0-4.

WRITE / READ

REGISTER 3		POS 103		FUNCTION

7	6	5	4	3	2	1	0	
								External USER_PIN0
								External USER_PIN1
								External USER_PIN2
								LTR32

7	6	5	4	FUNCTION
1	1	1	1	Disable I/O Decode
1	1	1	0	Disable I/O Decode
1	1	0	1	I/O Address —> 1e00h - 1effh
1	1	0	0	I/O Address —> 1c00h - 1cffh
1	0	1	1	I/O Address —> 1a00h - 1affh
1	0	1	0	I/O Address —> 1800h - 18ffh
1	0	0	1	I/O Address —> 1600h - 16ffh
1	0	0	0	I/O Address —> 1400h - 14ffh
0	1	1	1	I/O Address —> 1200h - 12ffh
0	1	1	0	I/O Address —> 1000h - 10ffh
0	1	0	1	I/O Address —> 0e00h - 0effh
0	1	0	0	I/O Address —> 0c00h - 0cffh
0	0	1	1	I/O Address —> 0a00h - 0affh
0	0	1	0	I/O Address —> 0800h - 08ffh
0	0	0	1	I/O Address —> 0600h - 06ffh
0	0	0	0	I/O Address —> 0400h - 04ffh

Bits 0-2   -   These bits connect directly to the USER_PINs and allow POS control of external logic.

Bit 3   -   This bit drives the unbuffered TR32 line. Set to 0 for 32 bit mode or set to 1 for 16 bit mode.

Bits 4-7   -   These bits are compared against host address bits A15-A8 to select the I/O address of the board.

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Register 4 - Configuration 2 (POS 104)

This register (POS 104) contains the BIOS PROM address range, I/O board 32 bit bus master address enable, and the card select input enable bit.
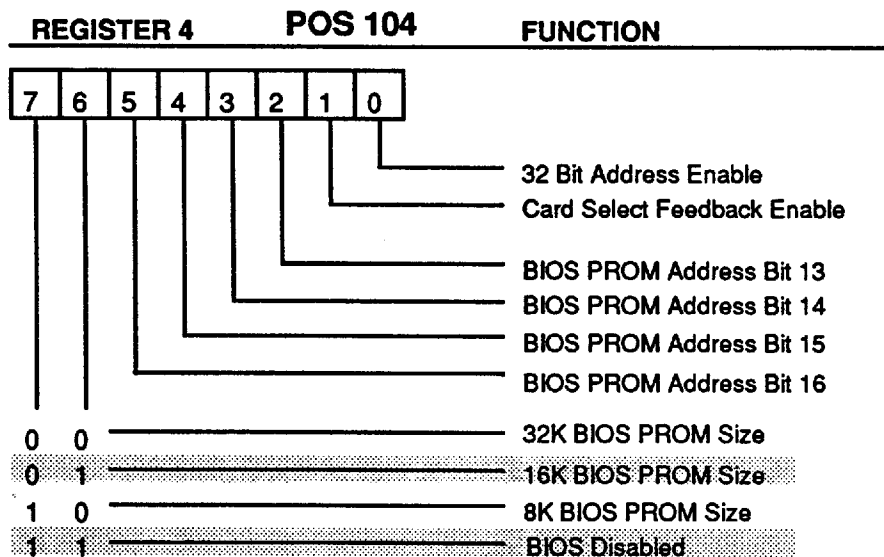
The BIOS PROM starting address and size information is placed in this register. The BIOS PROM normally resides in the 0C0000h to 0DFFFFh address range. The BIOS PROM address and range is written by the host processor during I/O card configuration. For BIOS PROM selection, address bits 23 - 13 are specified below:

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
0	0	0	0	1	1	0	bit5	bit4	bit3	bit2

The adapter board must externally decode address bits A23 - A17 and connect the result of this decode to the -HAENB pin of the MC 9010. For 32 bit addresses the board must, externally decode address bits A31-A17.

The reader should note that the BIOS PROM starting address must be on a memory boundary equal to the size of the BIOS PROM.

WRITE / READ

REGISTER 4   **POS 104**   FUNCTION

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

- 32 Bit Address Enable
- Card Select Feedback Enable
- BIOS PROM Address Bit 13
- BIOS PROM Address Bit 14
- BIOS PROM Address Bit 15
- BIOS PROM Address Bit 16

0	0	32K BIOS PROM Size
0	1	16K BIOS PROM Size
1	0	8K BIOS PROM Size
1	1	BIOS Disabled

Bit 0   -   When this bit is set to 0 the MC 9010 assumes 24 bit addressing when the MC 9010 is the Micro Channel bus master (MADE24 signal is high). When this bit is set to 1 the MC 9010 uses 32 bit addressing when it is the bus master.

Bit 1   -   When this bit is set to 1 the MC 9010 must receive the -SFDBKRTN when it is the bus master on the Micro Channel. If this signal is not received, the current transfer is terminated and -CHCK signal is asserted on the Micro Channel.

Bits 2-5   -   These bits are compared against host address bits 13 - 16 for determining a BIOS PROM access.

Bits 6-7   -   These bits specify the BIOS PROM size and BIOS Disable as indicated above.

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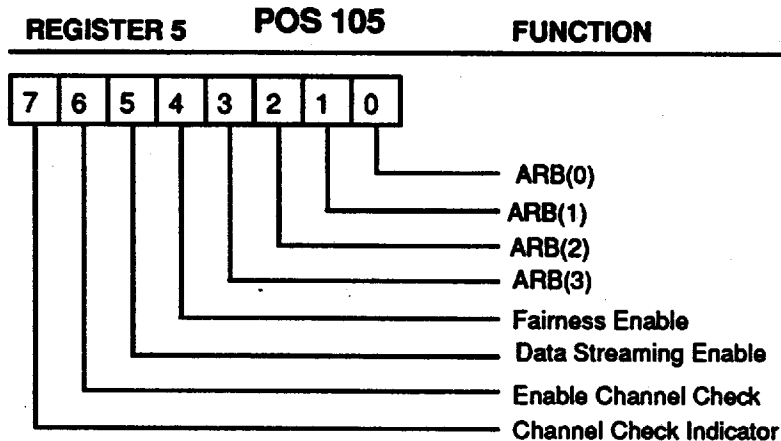
Register 5 - Configuration 3 (POS 105)

This register (POS 105) provides arbitration, data streaming, and channel check configuration information to the MC 9010.

WRITE / READ

REGISTER 5   **POS 105**   FUNCTION

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

- ARB(0)
- ARB(1)
- ARB(2)
- ARB(3)
- Fairness Enable
- Data Streaming Enable
- Enable Channel Check
- Channel Check Indicator

Bits 0-3 -   These bits indicate the arbitration priority for the Micro Channel operation. A hexadecimal value of F (1111) has the lowest priority and a hexadecimal value of 0 (0000) has the highest priority.

Bit 4 -   When this bit is set to 0 the MC 9010 implements the fairness algorithm for host bus arbitration. When this bit is set to 1 the the MC 9010 implements the linear priority arbitration algorithm.

Bit 5 -   When this bit is set to 1 the MC 9010 is enabled for data streaming transfers on the Micro Channel.

Bit 6 -   When this bit is set to 1, the -CHCK signal of the MC 9010 is enabled.

Bit 7 -   This bit is set to 0 by the MC 9010 when the MC 9010 asserts -CHCK. The MC 9010 will assert -CHCK (providing POS 105 bit 6 is asserted) if either a -SFDBK error occurs or when the local adapter is forced off the bus prior to releasing the bus. This second condition may occur if the local adapter incorrectly holds the bus longer than the 7.8 seconds maximum after an external -PREEMPT and the system begins an arbitration cycle before the local adapter releases the bus. In most applications, the potential for this condition will exist only during adapter development and debug. A properly functioning hardware and software design will not allow this condition to occur. This bit is reset by the assertion of RESET. The host could also reset this bit to 1 by writing a 1 to it.
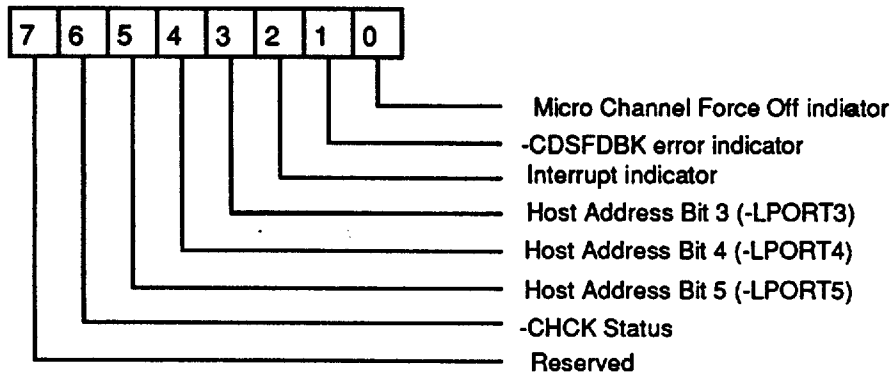
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Register 15 - Configuration 15

This transfer status register (not a POS register) controls and flags interrupt, reset and error conditions.

WRITE / READ

REGISTER 15   **FUNCTION**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Micro Channel Force Off indiator
-CDSFDBK error indicator
Interrupt indicator
Host Address Bit 3 (-LPORT3)
Host Address Bit 4 (-LPORT4)
Host Address Bit 5 (-LPORT5)
-CHCK Status
Reserved

Bit 0   -   If the local adapter was forced off the bus, the MC 9010 sets this bit to a 1. This condition may occur if the local adapter incorrectly holds the bus longer than the maximum 7.8 microseconds after -PREEMPT and the system begins an arbitration cycle before the local adapter releases the bus. In most applications, the potential for this condition will exist only during adapter development and debug. A properly functioning hardware and software design will not allow this condition to occur. **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bit 1   -   If a -CDSFDBK error occurs, the MC 9010 sets this bit to a 1. **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bit 2   -   When the MC 9010 asserts an interrupt, it sets this bit to (1). **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bits 3-5 -   Host Address Bits 3-5 which provide SONIC Port select information

Bit 6   -   If, while it is a bus master, the MC 9010 detects the assertion of -CHCK by another system component it sets this bit to 1. **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bit 7   -   Reserved

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SECTION 3 - PIN DESCRIPTION

Pin Summary

Table 3.1 shows the pin break down for the MC 9010 device.   The following abbreviations are used:

I/O	-	Input and Output Pin
I	-	Input Pin Only
O	-	Output Pin Only
TS	-	Three-State Pin
OC	-	Open Collector Pin
TP	-	Totem Pole Pin

Table 3.1 Micro Channel Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
-ADL	1	I/O	TS	24
ARB(0-3)	4	I/O	OC	24
ARB/-GNT	1	I	-	-
-BURST	1	I/O	OC	24
-CDDS16	1	O	TP	6
-CDDS32	1	O	TP	6
-CDSETUP	1	I	-	-
-SFDBKRTN	1	I	-	-
-CDSFDBK	1	O	TP	6
CDCHRDYx	1	O	TP	6
-CHCK	1	I/O	OC	24
CHRDYRTN	1	I	-	-
CHRESET	1	I	-	-
-CMD	1	I/O	TS	24
-DS16RTN	1	I	-	-
-DS32RTN	1	I	-	-
-IRQ(0-3)	4	O	OC	24
MADE24	1	I/O	TS	24
M/-I0	1	I/O	TS	24
-PREEMPT	1	I/O	OC	24
-S1	1	I/O	TS	24
-S0	1	I/O	TS	24
-SBHE	1	I/O	TS	24
-SDR0	1	I	-	-
-SDSTROBE	1	O	TS	24
LTR32*	1	O	TP	4
TOTAL PINS	**32**			

*Must be buffered if used.

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Table 3.2 Local Bus Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
-ADS	1	I	-	-
BSCK	1	O	TP	4
CDEN	1	O	TP	8
CRYIN	1	I	-	-
CRYOUT	1	O		
-CS	1	O	TP	4
HLDA	1	0	TS	4
HOLD	1	I	-	-
LINT	1	I	-	-
LPORT(3-5)	3	O	TS	4
MW/-R	1	I	-	-
-PROMBIOS	1	O	TP	4
-PROMID	1	O	TP	4
-RDYi	1	O	TP	4
-RDYo	1	I	-	-
LRESET	1	O	TP	4
S(0-2)	3	I	-	-
SW-R	1	O	TP	4
-SAS	1	O	TP	4
USER_PIN(0-2)	3	O	TP	4
TOTAL PINS	**26**			

Table 3.3 Buffer Control, Address and Data Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
HA(0-1)	2	I/O	TS	24
HA(2-4),(8-16)	12	I	-	-
-HAENB	1	I	-	-
-HAOE	1	O	TP	6
HDDIR	1	O	TP	6
-HDOE(0-2)	3	O	TP	4
-HOST/OWN	1	O	TP	4
LD(0-7)	8	I/O	TP	4
-POSCS(0,1)	2	O	TP	8
TOTAL PINS	**31**			

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Table 3.4 Power, Ground and No Connect

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
NC	19			
VDD	10			
VSS	10			
TOTAL PINS	39			

Table 3.5 Micro Channel Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
-ADL	Address Decode Latch	I/O	127	This active low, three-state signal is used to latch the contents of the address bus. The latch is open when this signal is low. Devices on the Micro Channel must latch the address since pipelining is possible. That is, the address may change for the next Micro Channel cycle before the -CMD strobe for the current cycle has been de-asserted.
ARB(3) ARB(2) ARB(1) ARB(0)	Arbitration Bus Priority Out	I/O	6,4,3,2	These active high open collector signals are used to present arbitration bus participant priority levels. The highest value of (hex Fh) has the lowest priority and the lowest value (hex 0h) has the highest priority. The priority level of the MC 9010 is programmed into POS Configuration 3.
ARB/-GNT	Arbitrate/-Grant	I	7	This active high input signal indicates an arbitration cycle is in process. When this signal is low it is the grant to the winner to access the channel.
-BURST	Burst	I/O	12	This active low open collector signal is driven low by arbitrating bus participants to indicate the extended use of the Micro Channel. The MC 9010 asserts this signal for all bus master transfers. It de-asserts -BURST during the last transfer cycle.
-CDDS16	Card Select 16	O	13	This active low totem pole output indicates the MC 9010 is providing 16 bits of I/O information to the system. This pin is programmable in POS Configuration 0, bit 7.
-CDDS32	Card Select 32	O	121	This active low totem pole output indicates the MC 9010 is providing 32 bits of I/O information to the system. This pin is programmable in POS Configuration 0, bit 7.
-CDSETUP	Card Setup	I	14	This active low input signal is used to access POS registers. When it is active the host processor may read or write registers 0 - 7. Register selection is made via the address bits A0, A1, and A2.

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-SFDBKRTN	Select Feedback Return	I	125	This active low input signal is used when the MC 9010 is the bus master to indicate a slave is present at the address requested. This pin can be disabled by POS Configuration 2, bit 1.
-CDSFDBK	Card Select Feedback	O	15	This active low output signal indicates when the MC 9010 is being accessed by the Micro-Channel. It is generated from an address decode of the I/O registers, DP83932 , or PROM chip selects.
CDCHRDYx	Channel Ready Out	O	18	This active high totem pole output indicates that the MC 9010 chip needs additional time to complete the requested read or write operation.
CHRESET	Channel Reset	I	19	This active high input provides a hard reset to the MC 9010 chip. Internal logic is initialized by this signal and any transfer operations are aborted.
-CHCK	Channel Check	I/O	119	This open collector pin indicates an error condition occurred on the host bus. This pin is asserted by the MC 9010 when a bus errors occurs and POS Config 3, bit 6 is asserted.
CHRDYRTN	Channel Ready Return	I	123	This active high input indicates that the slave addressed by the MC 9010 needs additional time to complete the requested read or write operation. When the slave needs more time it pulls this signal low. The MC 9010 inserts wait states until this signal is high.
-CMD	Command	I/O	20	This active low three-state signal is used to define when data is valid on the data bus. During write operations, the data must be valid on the bus throughout the period -CMD is low. For read operations the data must be valid before the trailing edge of -CMD and held on the bus (hold time) until after -CMD is high.
-DS16RTN	Data Size 16 Return	I	21	This active low signal indicates that the slave device is providing(driving or receiving) 16 bits of data.
-DS32RTN	Data Size 32 Return	I	22	This active low input signal indicates that the slave device is providing (driving or receiving) 32 bits of data.
-IRQ(3) -IRQ(2) -IRQ(1) -IRQ(0)	Interrupt Request	O	82,83,84, 85,86,	These active low open collector signals are used to inform the system processor of the completion of a task. The active interrupt line is programmable in POS Configuration 0.
MADE24	Memory Address Enable 24	I/O	122	This active high three-state signal indicates when an extended (address bits 24 -31) address is used on the Micro Channel. When this signal is low a 32 bit memory address is placed on the bus and when high a 24 bit address is on the bus. This signal is programmable in POS Config 2.

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M/-IO	Memory or I/O	I/O	86	This three-state signal distinguishes a memory cycle from an I/O cycle. When this signal is high a memory cycle is in progress. When M/-IO is low an I/O cycle is in progress. If Memory BIOS Boot PROM is to be used, M/-IO needs to be driven low in slave mode.
-PREEMPT	PREEMPT	I/O	89	This active low open collector signal is driven low by arbitrating bus participants to request usage of the channel through arbitration. The requesting arbitration bus participant removes it PREEMPT upon being granted the channel. The MC 9010 asserts this signal when the use of the channel is needed and the fairness algorithm (if enabled through POS Config 3) allows the access.
-S0 -S1	Status Bit 0 and 1	I/O	90,91	These active low three-state signals indicate the start of a Micro Channel cycle and also define the type of cycle when used with the M/-IO signal (see above).When the MC 9010 is a channel slave it latches these bits with the trailing edge of -ADL.
-SBHE	System Byte High Enable	I/O	120	This active low three-state signal enables the transfers of data on the high byte (bits 8-15) of the data bus. It is used with A0 to distinguish between byte 0 (bits 0-7) and byte 1 (bits 8-15) transfers. This signal is actually the -BE(0) pin of MC 9010. The -SBHE function is enabled when POS Configuration 0, bit 6 is de-asserted.
-SDR0	Streaming Data Request	I	93	This active low input signal is driven by a slave device to indicate to the MC 9010 that the slave is capable of streaming data transfers. Data streaming is enabled when POS Configuration 3, bit 5 is asserted.
-SDSTROBE	Streaming Data Strobe	O	94	The MC 9010 asserts this active low output signal to clock data on and off the data bus during streaming transfers.
LTR32	Translate	O	116	This active high totem pole output is driven low when the MC 9010 is performing 32 bit data transfers. When this signal is low the MC 9010 drives Micro Channel signals -BE(0-3) to gate data between 32 bit slaves and the MC 9010. This signal needs to be buffered.

In the -S0/-S1 cell, the following table appears:

M/-IO	-S0	-S1	Function
0	0	0	Reserved
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	Inactive
1	0	0	Reserved
1	0	1	Mem Write
1	1	0	Mem Read
1	1	1	Inactive

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3.6 Local Bus Pins Description

Symbol	Signal Name	I/O	Pin Number	Function
-ADS	Address Strobe	I	42	This active low input signal informs the MC 9010 that the DP83932 has placed a valid address on the bus.
BSCK	Bus Clock	O	44	This active high clock provides the timing for the DP83932 DMA logic. It is asserted synchronous to - RESET to ensure phase lock between the MC 9010 and the DP83932 .
CDEN	Card Enable	O	68	This totem pole output is asserted when the I/O board has been enabled through POS.
CRYIN	Crystal Input	I	72	This input pin provides the timing for all synchronous operations in the MC 9010. It connects to either a TTL clock signal or directly to a crystal.
CRYOUT	Crystal Output	O	73	This output signal connects directly to crystal oscillator.It is a no connect pin when the the CRYIN pin connects to a TTL clock signal.
-CS	Chip Select	O	46	The MC 9010 asserts this active low signal when it has detected an access to the DP83932 's I/O registers. The DP83932 's I/O address is programmable in POS Configuration 1. (BASE + 10h - 1Fh).
HLDA	Bus Hold Acknowledge	O	50	This active high totem pole output signal indicates the MC 9010 has successfully gained access to the host bus. When the DP83932 receives this signal it begins bus master operation.
HOLD	Bus Hold Request	I	47	This active high input indicates the DP83932 needs to gain access to the host bus.
LINT	DP83932 Local Interrupt	I	51	This active high input is active when the DP83932 has an interrupt pending. The MC 9010 asserts one of four host interrupts when this signal is active.The host interrupt line that is asserted is programmable in POS Configuration 0, bits 1 and 2.
LPORT(3-5)	Register Address 3-5	O	76,77,78	These three-state active high pins contain the contents of the DP83932 Port Selector Register. They determine one of the eight ports to be selected on the DP83932 .
LRESET	Reset	O	55	This active high output signal is asserted and de-asserted synchronous to BSCK. It provides a hardware reset to the DP83932. This signal needs to be externally inverted to the DP83932.
MW-R	Memory Write or Read	I	52	This input signal is low when a bus master read operation is requested and high for a bus master write operation.

-PROMBIOS	BIOS PROM Output Enable	O	74	This active low output pin connects to the output enable pin (-OE) of the BIOS Boot PROM. The MC 9010 gates the data from the PROM onto the system data bus. The system memory address of the BIOS PROM is programmable in POS Configuration 2.
-PROMID	ID PROM Output Enable	O	75	This active low output pin connects to the output enable pin (-0E) of the Node ID PROM. The MC 9010 gates the data from the Node ID PROM onto the system data bus. The system I/O address of the ID PROM is programmable in POS Configuration 1.
-RDYi	Ready to DP83932	O	54	This active low output signal informs the DP83932 of the completion of a memory cycle. When it is high, the DP83932 inserts wait states. This signal is sampled by the DP83932 synchronously with BSCK.
-RDYo	Ready from DP83932	I	63	This active low input from the DP83932 is used during system slave accesses to the DP83932 's I/O registers. This signal is asserted when the DP83932 has completed the I/O cycle and is synchronous to BSCK clock.
S(0-2)	Bus Status	I	56,57 58	These status signals from the DP83932 are used by the MC 9010 to enable/disable streaming data transfers. They indicate the current DP83932 bus operation.
-SAS	Slave Address Strobe	O	59	MC 9010 asserts this output signal to indicate to the DP83932 that valid address is on the bus during a register write operation or when the DP83932 can begin sourcing data during a register read operation.
SW-R	Slave Read or Write	O	61	The MC 9010 asserts this output signal to inform the DP83932 whether the current access is a read or write to DP83932 registers.
USER_PIN(2) USER_PIN(1) USER_PIN(0)	User Defined Pin	O	53 , 62, 118	These totem pole output pins are controlled from POS Config 1 for each host interface. They control logic on the I/O board.

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3.7 Buffer Control, Address and Data Pins Description

Symbol	Signal Name	I/O	Pin Number	Function
HA(0-1) HA(2-4) HA(8-16)	Host Address	I I I	8, 9, 10,11, 27, 30, 31 34, 35, 36 38, 39, 40 41	These active high input signals are the host address lines needed for POS, I/O and BIOS PROM space decode. HA(0-2) are used for POS decode and HA(8-15) are used for the BIOS PROM and I/O address space decode. In addition, HA(16) is needed for the BIOS PROM decode. The address ranges are programmed in POS Configuration 1 and 2.
-HAENB	Host Address Enable	I	79	This signal provides for an external decode of Host Address bits (17-23). This pin is used for BIOS PROM decode or memory space decode.
-HAOE	Host Address Output Enable	O	105	This active low totem pole output signal connects to the -OE pin of the LS245s which gate the address bus between the adapter board and the Micro Channel, or AT bus.
HDDIR	Host Data Direction	O	102	This totem pole output signal connects to the -OE pin of the LS245s which gate the data bus between the adapter board and the Micro Channel or AT bus. When this pin is low the host data bus is gated to the adapter board. When this pin is high the data bus from the adapter board is gated to the host data bus.

-HDOE2
-HDOE1
-HDOE0
	Host Data Output	O	98,99,100	These totem pole output signals connect to the -OE pin of the LS245s which gate data between the adapter board and the host bus. These pins are connected as indicated below:
				
				Host byte -HDOE pin
				  0 -HDOE(0)
				  1 -HDOE(1)
				  2 -HDOE(2)
				  3 -HDOE(2)

-HOST/OWN	Host Own	O	95	When this active low totem pole signal is asserted, the MC 9010 is the owner of the host bus.
LD(0-7)	Host Data	I/O	117,115, 114,110, 109,108, 107,106	These three-state data signals program POS Configuration registers in the MC 9010.The host processor may also read back the POS registers thought the 32 byte I/O port (see Configuration 1).
-POSCS(0,1)	POS Chip Select	O	87,88	These active low output pins are asserted when the host system accesses POS registers zero or one. The should be connected to the output enable pin of an LS244 or LS257. The MC 9010 gates the POS data to the host bus.

Table 3.8 Power, Ground and No Connect

Symbol	Signal Name	I/O	Pin Number	Function
NC	No Connect	-	5,23,24, 25,26,28, 37,43,45, 60,66,67, 69,92,101, 103,104, 124,126	
VDD	Power	I	1, 17, 29, 33, 49, 64, 70, 80, 96, 112	5 Volt power supply
VSS	Ground	-	16,32,48, 65,71,81, 97,111, 113,128	Ground

Section 4 - Bus Cycles

This section describes Micro Channel slave and master cycles. Timing relationships are described in more detail in Section 5. For more detailed information on the Micro Channel Bus, see the IBM PS/2 Technical Reference Manual. For detailed information on the DP83932, see the National Semiconductor literature. Contact PLX Technology at 1-800- 759-3753 for assistance or other information.

Slave Cycles

POS Register Access

The MC 9010 responds to a setup routine when it detects the assertion of -CDSETUP by the system controller. When the card is selected, the MC 9010 decodes A0-A2 to determine the POS register to be read from or written to. M/-IO, -S0 and -S1 indicate whether the cycle is a read or write cycle. The MC 9010 has POS 102 through 105 on-chip.

In addition, the MC 9010 will drive the adapter ID number to the data bus (D0-7) when POS 100 or 101 are addressed. When POS 100 or 101 are selected, the MC 9010 will drive -POSCS0 or 1 respectively, which are chip select signals which enable two 244 buffers or the Node ID PROM to the D0-7 data lines.

The POS registers may also be accessed through an I/O read or write operation at the I/O address described at the beginning of Section 2.

DP83932 Register Access

The DP83932 registers are accessed through a Micro Channel slave I/O cycle. The MC 9010 decodes the system address (as determined in POS registers, Section 2) and drives CS to the DP83932. The MC 9010 also includes a register which contains lartched address bits A3-A5 for port select information (pins LPORT3-5). These are active when CS is active. The MC 9010 also drives the data direction signal (HDDIR) to the data buffers to indicate whether the cycle is read or write. If the slave is 32 bit, the MC 9010 drives the data buffer enable signals -HDOE(0,1,2). If the slave is 16 bit, the MC 9010 drives only -HDOE(0,1).

Node ID and BIOS PROM Access

The Ethernet Node ID PROM and BIOS PROM are accessed through a Micro Channel I/O slave cycle and Memory slave cycle respectively. The MC 9010 decodes the system address (as determined by POS 103 and 104, section 2) and drives the -PROMID and -PROMBIOS chip selects. HDDIR and -HDOE(0,1) are enabled for the BIOS PROM access. The MC 9010 automatically inserts a wait state by deasserting -CDCHRDY.

Master Cycles

Bus Request

The DP83932 initiates a Micro Channel Bus Request by asserting HOLD to the MC 9010. When the MC 9010 detects HOLD, it drives -PREEMPT to the Micro Channel. The MC 9010 will assert -PREEMPT only when ARB/-GNT is low (in the grant state). This prevents arbitration errors. During the arbitration state, if -PREEMPT was asserted in the preceding grant state, it will remain asserted. Once -PREEMPT is asserted the local master will participate in the next arbitration cycle.

Arbitration Priority Levels

The MC 9010 can be configured to any of 16 arbitration priority levels through the POS registers (See Section 2). Although it can drive all sixteen levels, note that the IBM PS/2 Technical Reference Manual states that bus masters should have levels 8-15. Levels 0-7 are reserved for DMA slaves.

Arbitration Cycle

When ARB/-GNT enters the ARB state, the MC 9010 will participate in the arbitration cycle provided it has asserted -PREEMPT. The MC 9010 executes the arbitration cycle according to the Micro Channel specification.

When the MC 9010 wins arbitration, it will assert -BURST on the Micro Channel, HLDA to the DP83932, -HAOE and -HOST/OWN. -HAO enables the adapter board's 244 address buffers. -HOST/OWN is always active when the MC 9010 owns the Micro Channel and is a useful signal during the debugging phase of board development.

After asserting HLDA, the MC 9010 releases -PREEMPT. The MC 9010 will continue to drive -BURST throughout the data transfer cycle.

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If the FAIRNESS bit is enabled in POS 105 the MC 9010 will be prohibited from enabling -PREEMPT during subsequent arbitration cycles until all other system adapters have deasserted -PREEMPT, assuming that the local master wins and controls the bus in the current cycle.

BURST and Single Data Transfer Cycle

The data transfer cycle starts when the MC 9010 asserts HLDA, which is an indication to the DP83932 that it may begin transferring data. After detecting HLDA, the DP83932 asserts -ADS to the MC 9010 and LW/-R depending on whether the cycle is Read or Write. In turn, the MC 9010, on the next clock cycle, asserts -ADL and on the following cycle, -CMD. The MC 9010 also enables the address and data buffers in the proper sequence and drives the status lines to the Micro Channel.

When valid data has been transferred to the Micro Channel, the MC 9010 asserts -RDY, which indicates to the DP83932 that it may reassert -ADS and start another cycle.

Data transfers will continue in this way until either the DP83932 deasserts HOLD or the adapter is preempted off the bus by another adapter, or the adapter exceeds the maximum bus hold time limit programmed in POS. If either of the last two conditions occur, the MC 9010 will deassert HLDA.

Provided that the adapter has not exceed the bus hold time limit programmed in POS and no other master has requested the bus, the MC 9010 will actually retain control of the bus for .8 microseconds after the deassertion of HOLD. If the DP83932 does not reassert HOLD within this period, the MC 9010 will release the Micro Channel. This is to allow the DP83932 to retain control of the bus for prefetch operations when the DP83932 will immediately reassert HOLD.

The MC 9010 in conjunction with the DP83932 can sustain typical Read and Write BURST data transfer cycles of 200 ns, provided that the responding slave does not generate CHRDYRTN.

Streaming Data Transfers

To enable streaming, the streaming enable POS 105 bit must be asserted and the slave must be able to support streaming transfers. The MC 9010 combined with the DP83932 will normally stream in 100 ns cycles unless "paced" by the slave to a slower rate via CHRDYRTN.

The streaming data cycle starts the same way as a BURST cycle. After the MC 9010 asserts -ADL it will also assert -SDSTROBE provided the slave has asserted -SDR0 (which indicates it supports streaming) and provided the MC 9010 has received CHRDYRTN. (The MC 9010 will conduct BURST cycles until it detects CHRDYRTN at which time it will transfer in streaming cycles). The MC 9010 cycles the flow of data in or out of the DP83932 during streaming by toggling -RDY.
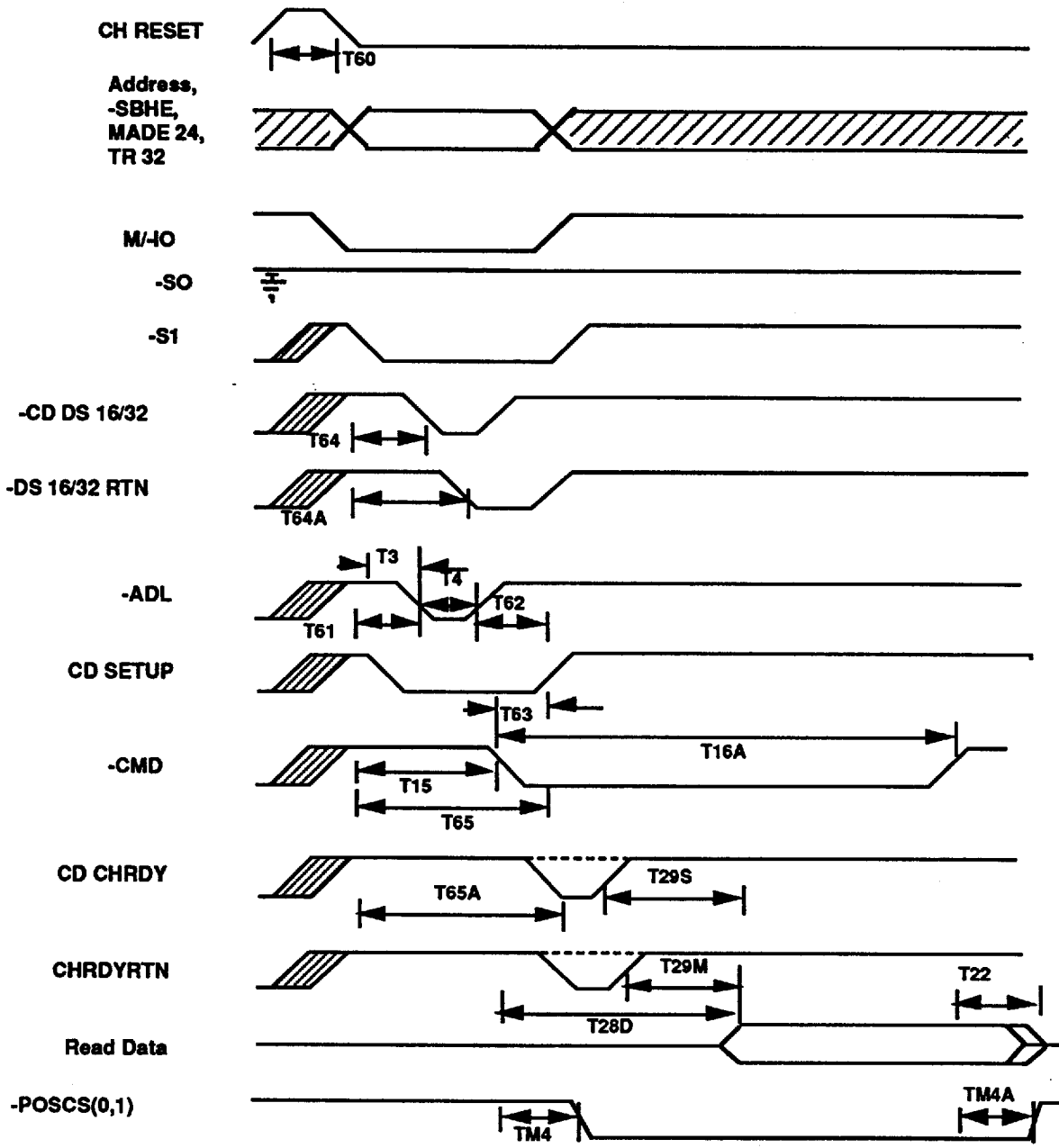
The slave may slow down the streaming cycle by deasserting CHRDYRTN. When the MC 9010 detects this condition it will not issue another -RDY to the DP83932 until CHRDYRTN is reasserted, indicating that the slave is ready for another streaming transfer.

The streaming transfer is terminated by the slave if it deasserts -SDR0. The streaming data transfer is terminated by the DP83932 if it has emptied its FIFO.

The MC 9010 will assert an extra -SDSTROBE cycle at the end of the streaming data transfer. For read cycles, this is of no consequence since the extra read data will not be accepted by the SONIC. For write cycles, the software driver should account for and overwrite at the same address when the DP83932 next acquires the Micro Channel bus.
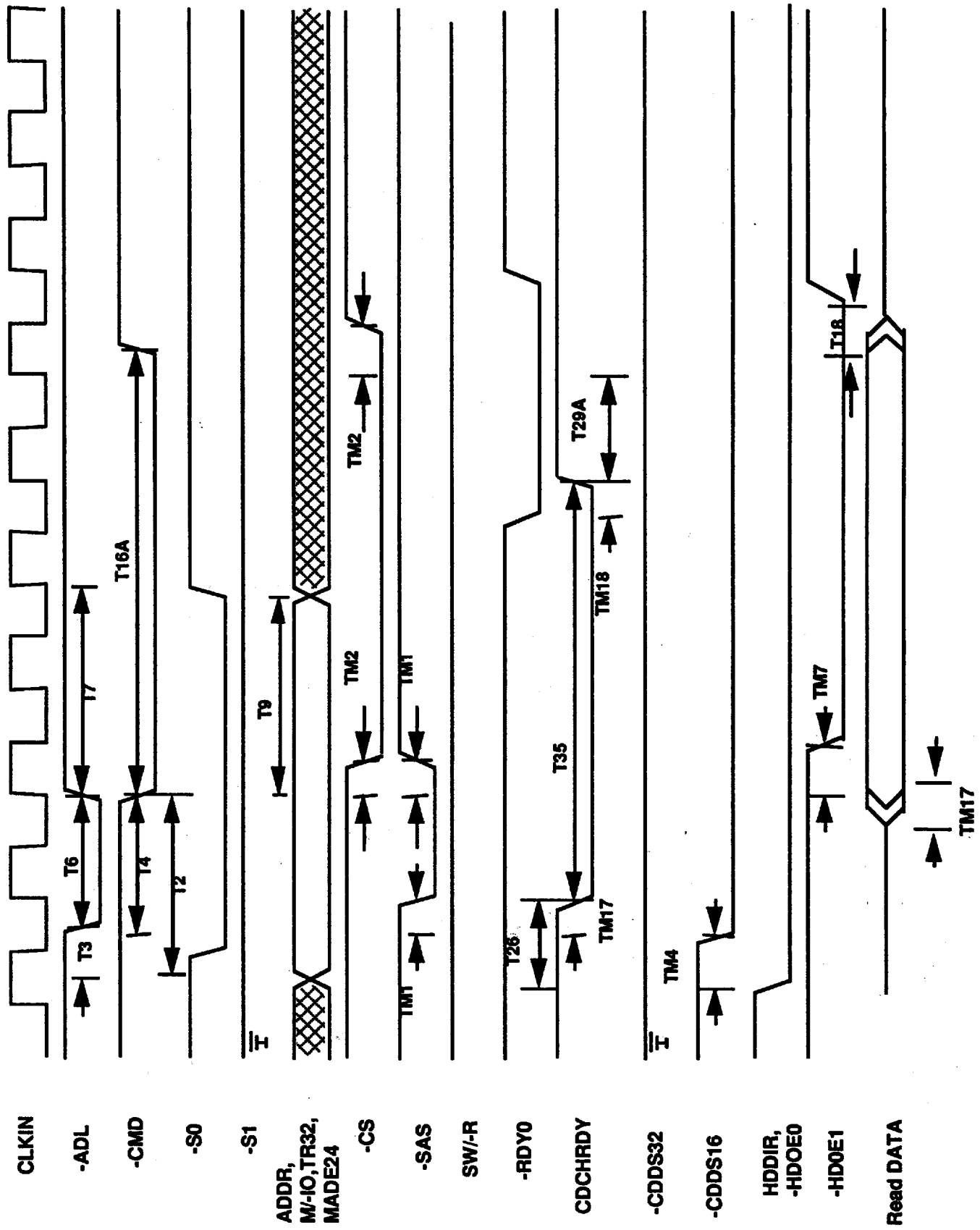
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Section 5 - Timing

CH RESET

Address,
-SBHE,
MADE 24,
TR 32

M/-IO

-SO

-S1

-CD DS 16/32

-DS 16/32 RTN

-ADL

CD SETUP

-CMD

CD CHRDY

CHRDYRTN

Read Data

-POSCS(0,1)

Micro Channel System Configuration Timing

Micro Channel Slave I/O Write (National DP83932)

CLKIN

-ADL

-CMD

-S0

-S1

ADDR,
M/-IO,TR32,
MADE24

-CS

-SAS

SW/-R

-RDY0

CDCHRDY

-CDDS32

-CDDS16

HDDIR,
-HDOE0

-HD0E1

Read DATA

Micro Channel Slave I/O Read (National DP83932)

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P L X TECHNOLOGY CORP   52E D   ■ 6855149 0000479 845 ■PLX
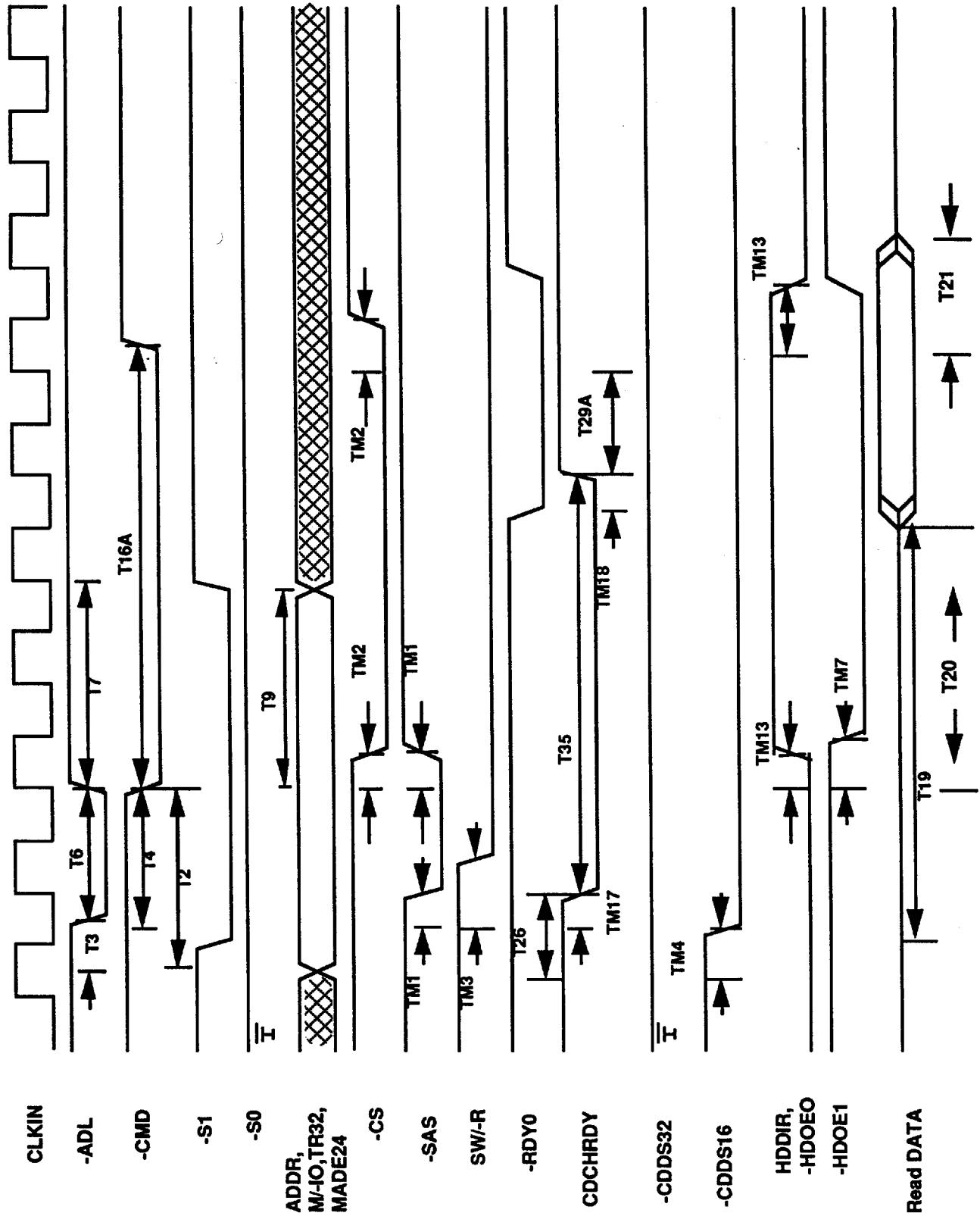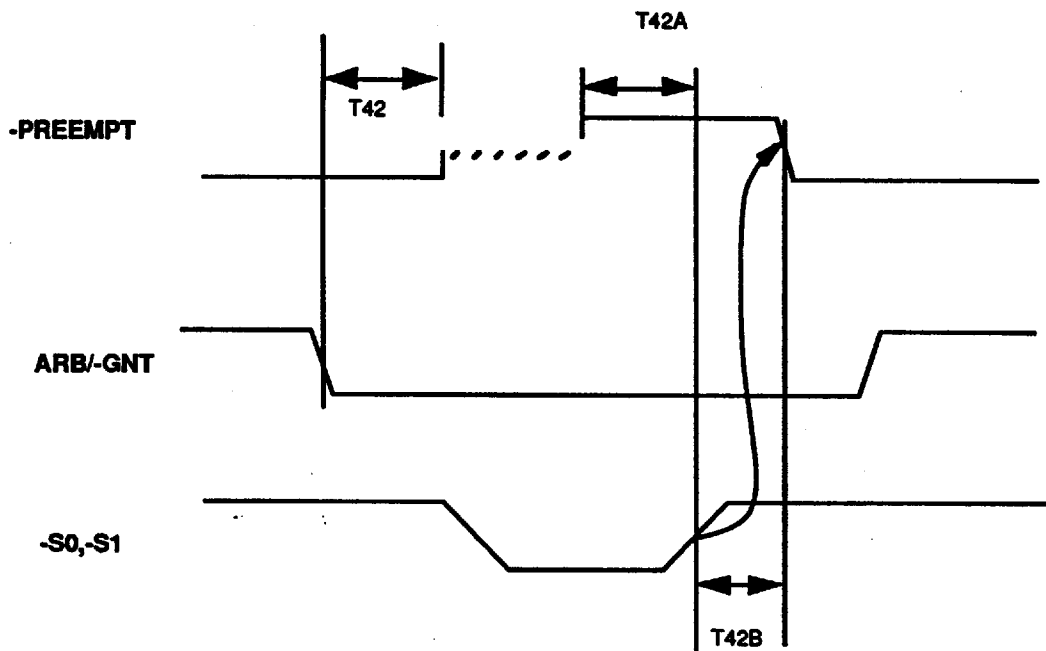
Exiting From the Inactive State
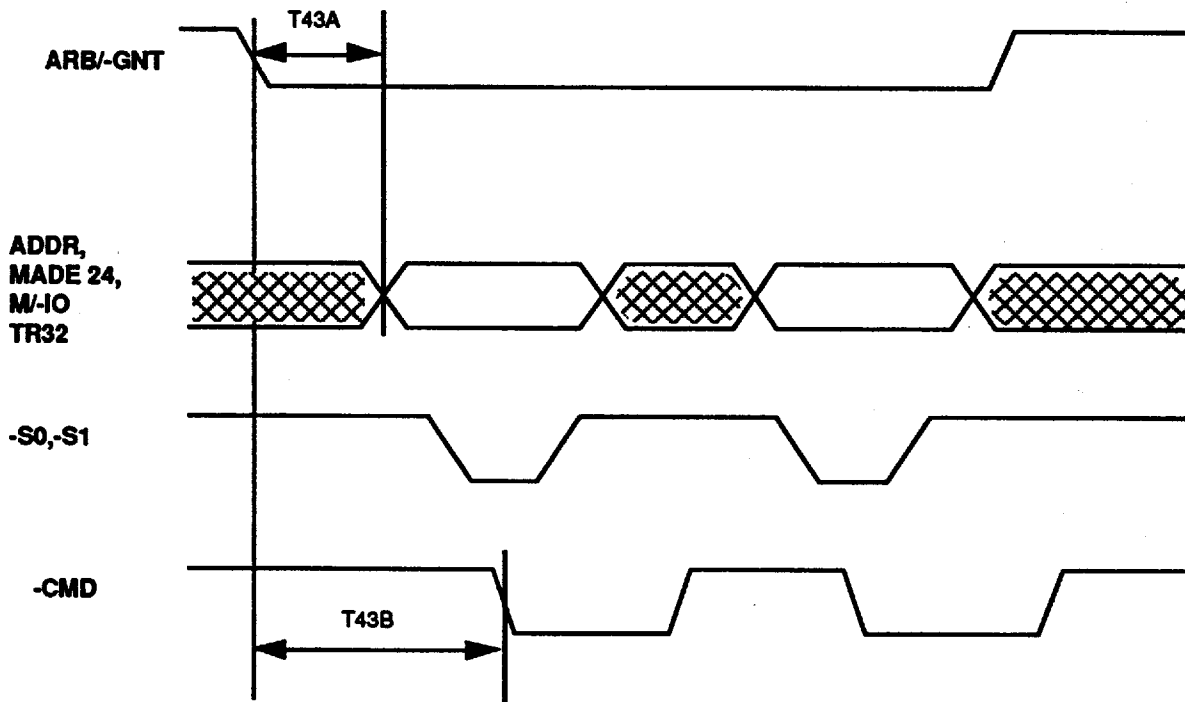
"First" DMA Cycle (after ARB/-GNT low)

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HOLD

HOLDA

TM14

TM15

T40

-PREEMPT

T42

T43

-BURST

T44

T41

ARB/-GNT

T45,45A,46
47,49

ARB(0-3)

T48

-S0
-S1

-CMD
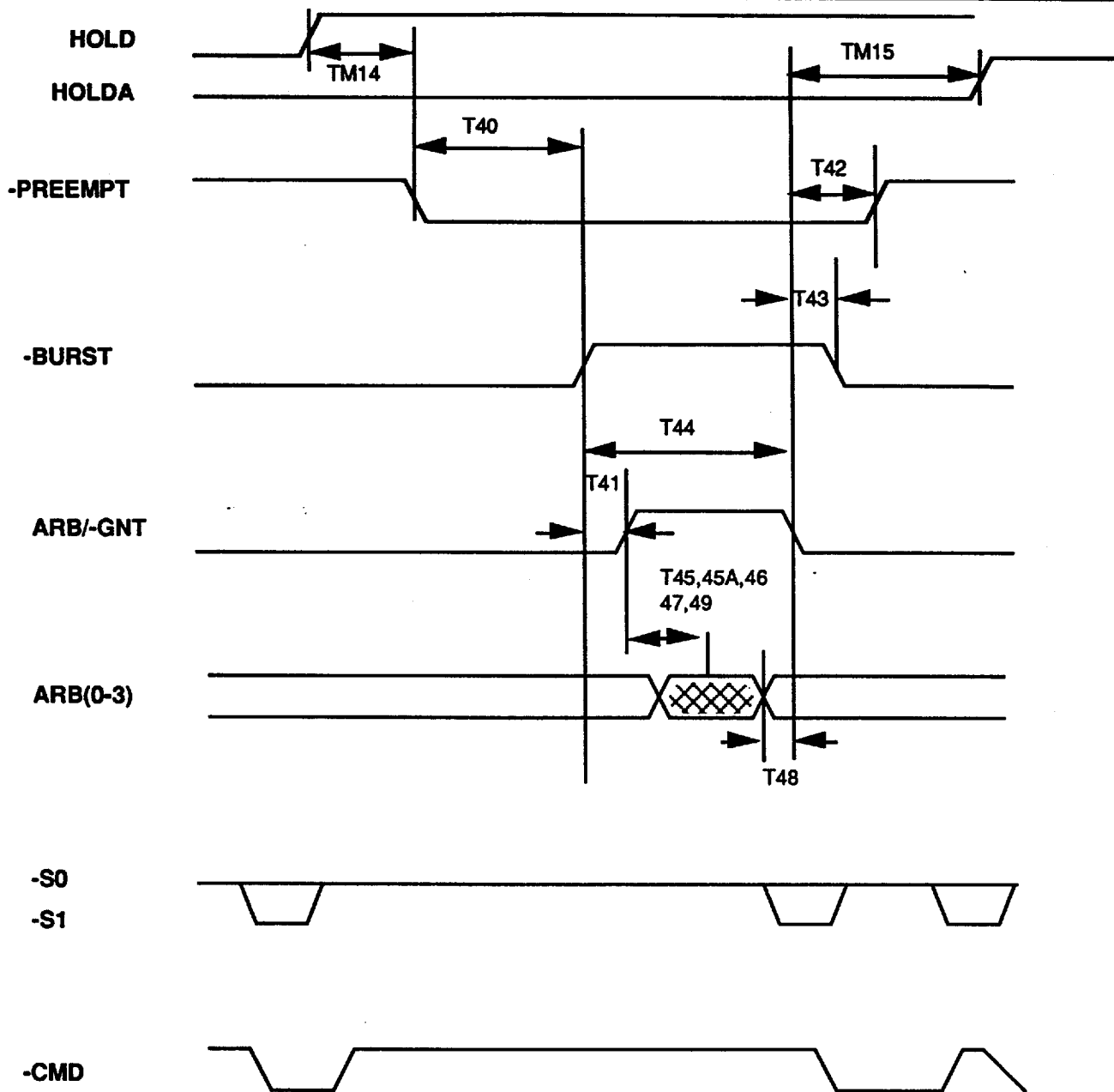
Arbitration Cycle

Micro Channel, Bus Master Default Mode (National DP83932)

| CLKIN |
| HOLDA |
| -ADS |
| -RDYI |
| ADDR, M/-IO, MADE 24, TR 32 |
| -ADL |
| -S0 |
| -S1 |
| CHRDYRTN |
| -CMD |
| MW/-R |
| HDDIR |
| -HOST/OWN, -HAOE |
| READ DATA |

MC 9010 4/15/92
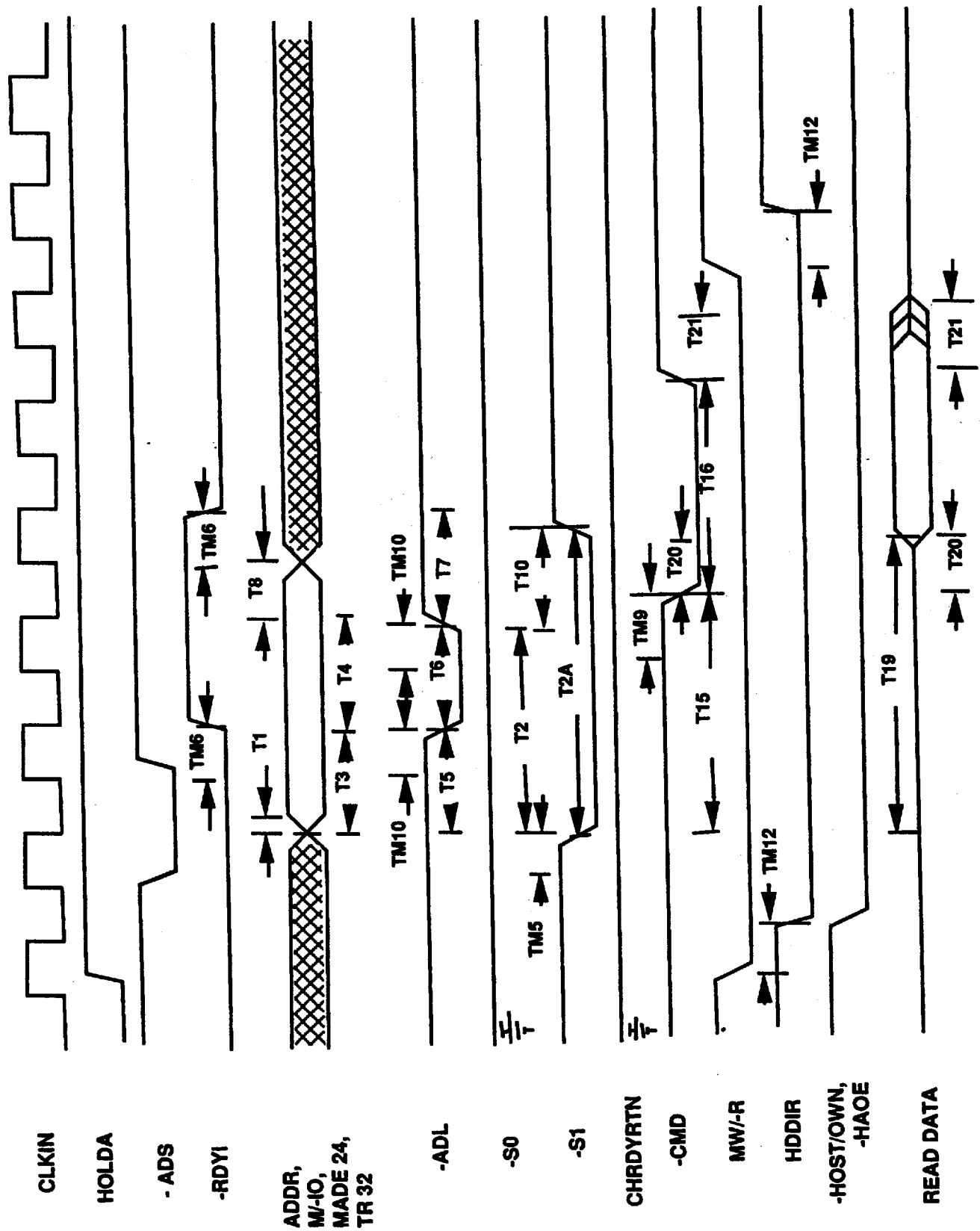
Micro Channel, Bus Master Asynchronous Extended cycles, (National DP83932)

CLKIN
HOLDA
-AS
-RDYI
ADDR,M/-IO, MADE 24,TR32
MW/-R
-ADL
-S1
-S0
CHRDYRTN
-CMD
HDDIR
-HOST/OWN,-H
AOE
READ DATA

TM6, TM6, TM8, TM9, TM11, TM10, T6, TM5, T29M, T16A, T27R, T26R, T1, T20, T19
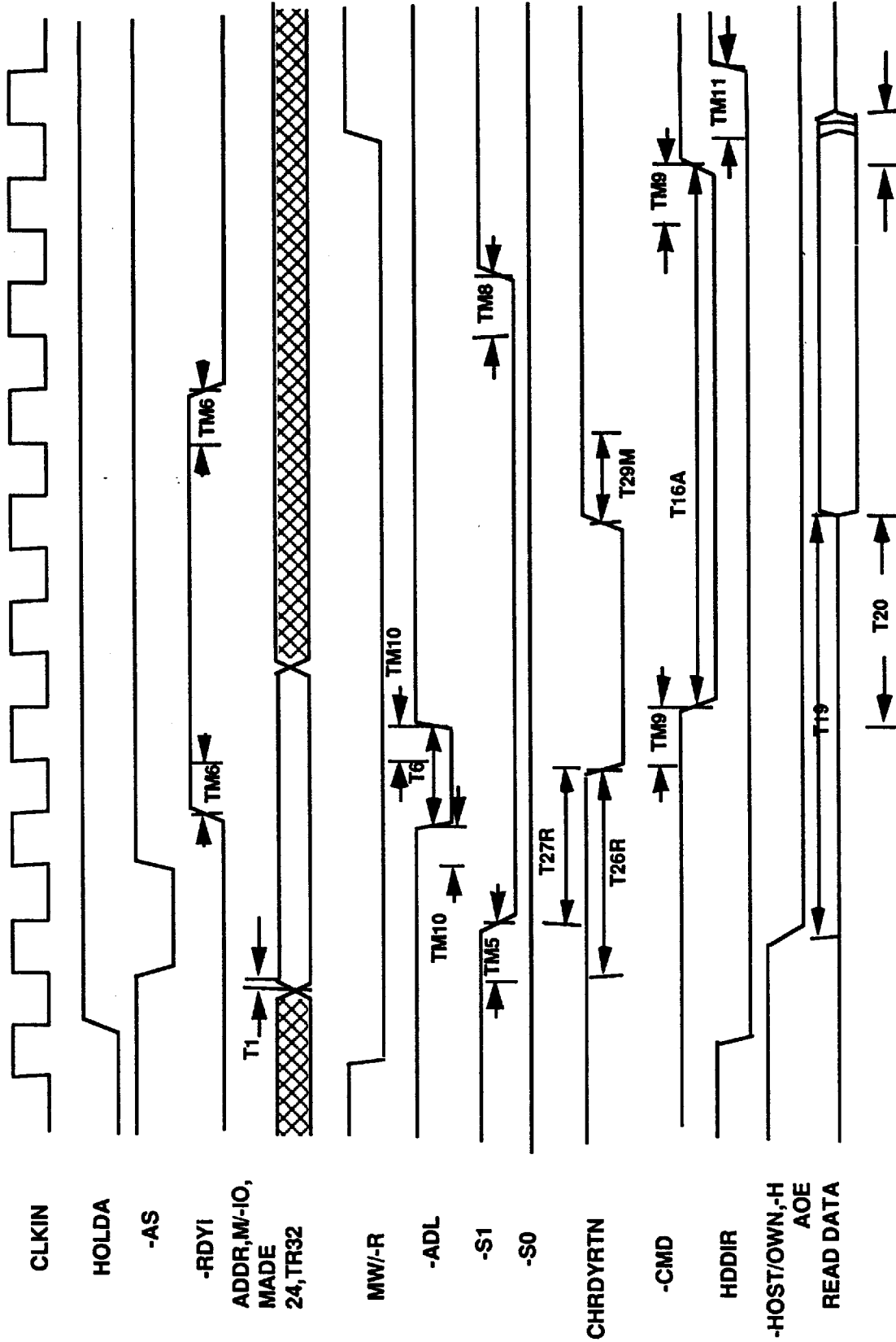
Micro Channel Master Streaming Data Cycle (National DP83932)

CLKIN

HOLDA

-AS

-RDYI

CHRDYRTN

-STROBE

-ADL

-S0

-S1

-CMD

-HOST/OWN, -HAOE

HDDIR

MC 9010 4/15/92
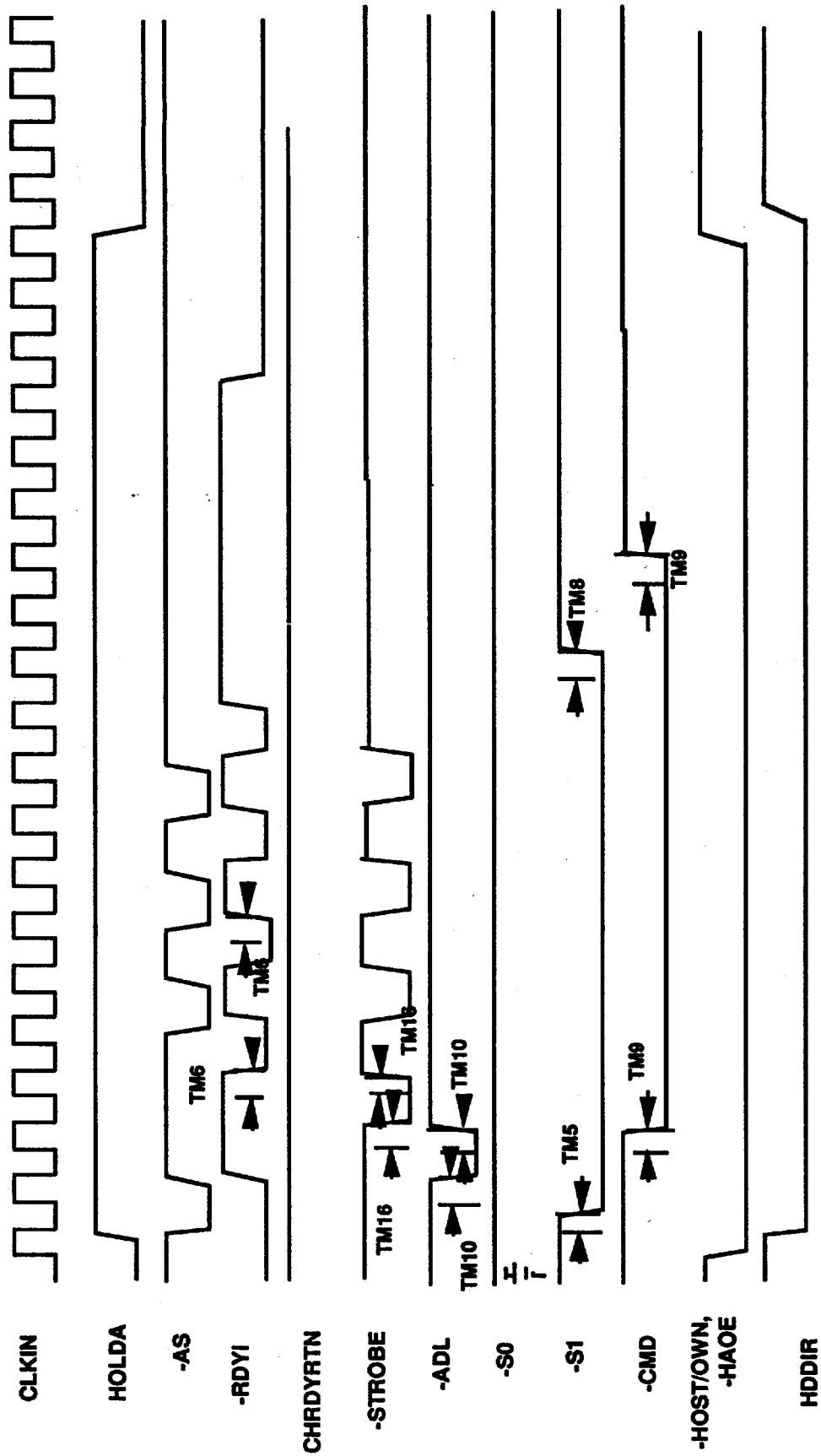
AC Timing Min/Max Specifications

Note: All timing values with a "TMn" label are specific to the MC 9010 device. All other values are from the IBM PS/2 Technical Reference Manual and have the same labels as the Technical Reference Manual.

MC 9010 specific timing

Time	Description	Min	Max	Unit
TM1	-ADL to -SAS valid delay		30	ns
TM2	-CMD low to -CS valid delay		25	ns
TM3	-ADL to SW/-R valid delay		35	ns
TM4	Valid Address to -CDDS 16 valid delay		50	ns
TM5	-AS low to -S(0,1) low delay		35	ns
TM6	Clock high to -RDYi valid delay		35	ns
TM7	-CMD to -HDOE1 valid delay		20	ns
TM8	Clock high to -S(0,1) high delay		35	ns
TM9	Clock high to -CMD valid delay		35	ns
TM10	Clock high to -ADL valid delay		35	ns
TM11	Clock high to HDDIR valid delay		40	ns
TM12	MW/-R to HDDIR valid delay		30	ns
TM13	-CMD to HDDIR valid delay		30	ns
TM14	HOLD high to -PREEMPT low delay		80	
TM15	ARB/-GNT low to HOLDA high delay		120	
TM16	Clock High to -STROBE valid delay		30	
TM17	Valid Status to CDCHRDY low delay		30	
TM18	-RDYo low to CDCHRDY high delay		25	

Micro Channel Timing from IBM PS/2 Technical Reference Manual

Time	Description	Min	Max	Unit
T1	Status active from Address, M/-IO, MADE24, TR32 valid	10		ns
T2	-CMD active from status active	55		ns
T2A				
T3	-ADL active from Address, M/-IO, MADE24, TR32 valid	45		ns
T4	-ADL active to -CMD active	40		ns
T5	-ADL active from status active	12		ns
T6	-ADL pulse width	40		ns
T7	Status hold from -ADL inactive	25		ns
T8	Address, M/-IO, -SBHE, -BE(0-3), MADE24, TR32 from -ADL inactive	25		ns
T9	Address, M/-IO, -SBHE, -BE(0-3), MADE24, TR32 from -CMD active	30		ns
T10	Status hold from -CMD active	30		ns
T15	-CMD active from Address valid	85		ns
T16	-CMD pulse width	90		ns
T16A	-CMD pulse width (Asynchronous extended cycle)	190		ns
T17	Write Data setup to -CMD active	0		ns
T18	Write Data hold from -CMD inactive	30		ns
T19	Status active to Read Data valid (Access Time)		125	ns
T20	Read Data valid from -CMD active		60	ns

Time	Description	Min	Max	Unit
T21	Read Data hold from -CMD inactive	0		ns
T22	Read data bus tri-state from -CMD inactive		40	ns
T26	CD CHRDY inactive from Address Bus valid		60	ns
T26R	CHRDYRTN inactive from Address Bus valid		80	ns
T27R	CHRDYRTN inactive from status valid and previous -CMD inactive		50	ns
T28D	Read valid data from -CMD active		160	ns
T29A	-CMD inactive from CHRDYRTN active	60		ns
T29M	Read Data valid to master from CHRDYRTN active		60	ns
T29S	Read data from salve valid from CD CHRDY active		60	ns
T35	CD CHRDY active from CD CHRDY inactive		3.5	us
T40	-PREEMPT active to EOT (channel release)		7.8	us
T41	ARB/-GNT in the ARB state from EOT (channel release)	30		ns
T42	-PREEMPT inactive from ARB/-GNT in -GNT state		50	ns
T42A	-PREEMPT inactive to status inactive	20		ns
T42B	-PREEMPT inactive from status inactive (Compete for the channel after the inactive state)	0		ns
T43	-BURST active from ARB/-GNT to -GNT state		50	ns
T43A	Address bus valid from ARB/-GNT in the -GNT state	0		ns
T43B	-CMD active from ARB/-GNT in the -GNT state	115		ns
T44	ARB/-GNT in ARB state	100		ns
T45	Driver turn-on delay from ARB/-GNT in ARB state	0	50	ns
T45A	Driver turn-on delay from lower priority line	0	50	ns
T46	Driver turn-off delay from ARB/-GNT in ARB state	0	50	ns
T47	Driver turn-off delay from higher priority line	0	50	ns
T48	Arbitration bus stable before ARB/-GNT in -GNT state	10		ns
T49	Tri-state drivers from ARB/-GNT in ARB state		50	ns
T60	CHRESET active pulse width	100		ms
T61	-CD SETUP active to -ADL active	15		ns
T62	-CD SETUP hold from -ADL active	15		ns
T63	-CD SETUP hold form -ADL inactive	30		ns
T64	-CD DS16/32 active from -CD SETUP active		25	ns
T64A	-DS 16/32 RTN active from -CD SETUP active		45	ns
T65	CD CHRDY inactive from -CD SETUP active and status active		100	ns
T65A	CHRDYRTN inactive from -CD SETUP active and status active		120	ns
T71	-SDR0 inactive from last -SDSTROBE fall (slave terminated cycle)	0	40	ns
T71B	-SDR0 inactive form -S0,-S1 inactive (master terminated, slave ready)	0	40	ns
T76A	CHRDYRTN valid from -SD STROBE fall	3	25	ns
T76B				
T77	Send Data and CD CHRDY hold form -SD STROBE fall	10		ns

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Section 6 - Electrical Specifications & Max Ratings

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS - 0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS - 0.5V VDD + 0.5V

Operating Ranges

T-52-33-55

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0C to +70°C	5V +/- 5%	Min = VSS Max = VDD

Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN =2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min, VIN=VIH or VIL	IOH = -4.0mA	2.4		V
VOL	Output Low Voltage		IOL per Tables 3.1-3.4		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS <= VIN <=VDD VDD = Max		-10	+10	uA
IOZ	Tri-state Output Leakage Current	VDD= Max VSS <= VIN <=VDD		-10	+10	uA
ICC	Power Supply Current	VDD= Max		20	80	mA

Section 7 - Package Mechanical Dimensions

128-pin QFP

UNIT : Inch
(mm)