Chapter 3. Hardware Description

3.1 Segmentation SARA Hardware Description

3.1.1 Segmentation SARA Internal Block Description

Figure 3-1 shows a block diagram of the Segmentation SARA chip.

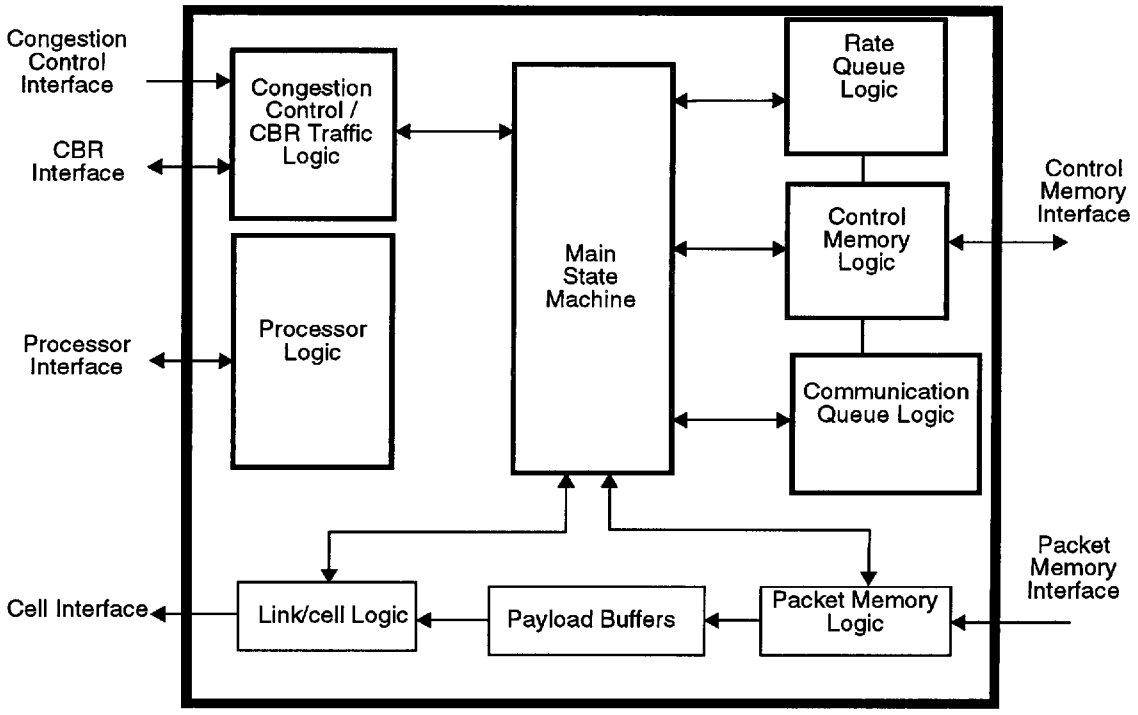


Figure 3-1. Segmentation SARA Block Diagram

The SARA-S internally consists of several functional blocks:

- The *Processor Logic* block interfaces with the processor to access the internal registers of SARA-S and to setup the device. The processor interface is an asynchronous interface.
- The *Control Memory Logic* block generates the bus arbitration signals (to access the control memory) and data transfer signals for the control memory. It can be programmed to generate these signals for both synchronous and asynchronous memory interfaces.
- The *Packet Memory Logic* block generates the bus arbitration signals (to access the packet memory) and data transfer signals for the packet memory. It generates the packet memory address and transfers data from the packet memory to the payload buffer. It can be programmed to generate these signals for both synchronous and asynchronous memory interfaces.
- The *Congestion Control /CBR Traffic Logic* block is used to communicate with the

SARA-R to receive congestion control information and also to communicate with the source generating the constant bit rate traffic.

- The *Cell/Link Logic* is used for transferring ATM cells to the external logic. This block generates the necessary handshake signals needed to interface to a FIFO-like device.
- The *Payload Buffer* is an internal buffer (2 cells deep) that holds the payload ready for transfer to the cell interface.
- The *Rate Queue Logic* contains the rate queue registers and counters. It also contains the priority logic to determine the rate queue to service.
- The *Communications Queue Logic* contains the pointers and queue control logic necessary to pass descriptors between the host and the SARA-S.
- The *Main State Machine* comprises 95 states and controls all internal blocks except the processor interface. It generates all the control signals in proper sequence for correct device operation.

3.1.2 Segmentation SARA Hardware Interfaces

The SARA-S contains the following hardware interfaces:

- Processor Interface
- Cell Interface
- Control Memory Interface
- Packet Memory Interface
- Congestion Control Interface
- Constant Bit Rate Traffic Interface
- Miscellaneous Interface

Notes for Tables:

1. Bit 0 on all busses is the least significant bit.
2. Parity is optional on all data busses that have parity bits.
3. An * at the end of signal name indicates that the signal is an active-low signal.
4. OD indicates an open drain output.
5. POD indicates a programmable open drain output.
6. All input and bi-directional I/O pins have internal pull-ups or pull-downs, which force an inactive state when the pin is left open.
7. All unused input pins must be tied to inactive state.

3.1.2.1 Processor Interface

The processor interface is a slave interface that is used by the local host/processor to read and write the internal registers of the device. These registers are identified in Chapter 4. It is also used to interrupt the processor/host when an unmasked status bit is set. Table 3-1 shows the processor interface pin descriptions.

Symbol	Type	Name and Function
CS*	I	Chip select signal to enable the processor interface for data transfers
DS*	I	Data strobe for enveloping the data transfer
WRT	I	WRITE(1), READ(0) input to indicate the direction of data transfer

Table 3-1. SARA-S Processor Interface Pin Descriptions

Symbol	Type	Name and Function
RDY*	OD	SARA-S signal indicating completion of data transfer
A(7:0)	I	Address bus for internal register selection
D(15:0)	I/O	Processor interface data bus
INTR*	OD	Interrupt signal to the processor

Table 3-1. SARA-S Processor Interface Pin Descriptions

3.1.2.2 Cell Interface

The cell interface is where the transmit ATM cell stream exits the SARA-S. It may be configured to be either eight- or 16-bits wide. Table 3-2 shows the SARA-S cell interface pin descriptions.

Symbol	Type	Name and Function
RDCLK	I	Read clock (free-running) used for operating the cell interface logic.
CELAVL*	O	Cell available signal indicating that an ATM cell is available for transfer (read-out) on the FFD pins.
RDEN	I	Read enable for cell transfer on the FFD bus. The next data word is transferred on to the FFD bus on a low to high transition of RDCLK when CELAVL* and RDEN are active.
FFD(17:0)	O	Cell data output bus. FFD(17) and FFD(16) are the parity bits for FFD(15:8) and FFD(7:0) respectively. Data is driven on FFD(7:0) when this interface is configured in the 8-bit mode and uses FFD(16) as parity.
XON	I	XON input. When low, cell generation on specific rate queues and optionally the CBR traffic is suspended. Cell generation on all queues is enabled when this signal is high.

Table 3-2. SARA-S Cell Interface Pin Descriptions

3.1.2.3 Control Memory Interface

The control memory interface is a bus-master interface to the control memory. It is used to access the communication queues, various data structures, including the buffer descriptors, the prefix and header tables maintained in the control memory. Table 3-3 shows the SARA-S control memory interface pin descriptions.

Symbol	Type	Name and Function
CREQ	O	Control memory bus request.
CGRT	I	Control memory bus grant.

Table 3-3. SARA-S Control Memory Interface Pin Descriptions

Symbol	Type	Name and Function
CMULR	O	Control memory multiple request signal, indicating that more than one data transfer is pending.
CCYCST*	POD	Control memory cycle start signal marking the beginning of data transfer. Programmable as either open drain or as an active output.
CRDY*	I	Control memory ready signal validates each data transfer when CCYCST* is active
CWRT	O	Control memory write signal for direction of transfer. This pin can be programmed as an early write signal to provide additional flexibility in external system design.
CA(23:1)	O	Control memory address bus (16-bit word address).
CD(17:0)	I/O	Control memory data bus. CD(17) & CD(16) are the parity bits for CD(15:8) & CD (7:0) respectively.

Table 3-3. SARA-S Control Memory Interface Pin Descriptions

3.1.2.4 Packet Memory Interface

The packet memory interface is a bus-master interface for reading packet data from packet memory to generate ATM cells. Various bus interfaces are supported.

Table 3-4 shows the SARA-S packet memory interface pin descriptions.

Symbol	Type	Name and Function
PREQ	O	Packet memory bus request
PGRT	I	Packet memory bus grant
PCYCST*	POD	Packet memory cycle start (marks the beginning of data transfers). Programmable as either open drain or as an active output.
PRDY*	I	Packet memory ready, validates each data transfer when PCYCST* is active.
PD(35:32)	I	Input only for packet memory data. PD(35), PD(34), PD(33), PD(32) are the parity bits for PD(31:24), PD(23:16), PD(15:8), PD(7:0) respectively.
PD(31:0)	I/O	Input for data; output for multiplexed address in PM_REQADR mode (Byte address PA(31:0) is presented on these pins during packet memory bus requests).
PA(15:0)	O	Packet memory address bus. This bus is driven with 16-bits of the byte address of the packet memory location being accessed. The selection of the 16-bits is dependent upon the state of the PLWADR pin and the PM_INTRLV mode bit.

Table 3-4. SARA-S Packet Memory Interface Pin Descriptions

Symbol	Type	Name and Function
PLWADR	I	Input signal to multiplex the upper or lower part of the packet memory address on the PA bus.
PAMTCH	O	Indicates that the packet memory address matches with the contents of the address match register. Used to detect the end of the serial address memory (for VRAMs) or page boundaries.

Table 3-4. SARA-S Packet Memory Interface Pin Descriptions

3.1.2.5 Congestion Control Interface

Table 3-5 shows the SARA-S congestion control interface pin descriptions. This interface is used by the SARA-R to transfer congestion information to the SARA-S to throttle the source virtual circuit segmentation rate.

Symbol	Type	Name and Function
CCDATA	I	Serial input stream of congestion control information from SARA-R to SARA-S.
CCXFER	I	Congestion control transfer enable for CCDATA.
CCHLD	O	Hold congestion control transfer.

Table 3-5. SARA-S Congestion Control Interface Pin Descriptions

3.1.2.6 Constant Bit Rate Traffic Interface

This interface is used to communicate with a constant bit rate (CBR) traffic source for transmitting CBR cells.

Table 3-6 shows the SARA-S constant bit rate interface pin descriptions.

Symbol	Type	Name and Function
CBRXMIT	I	CBR cell transmit signal to the SARA-S. This signal may be de-asserted one clock cycle after the CBRDONE signal is driven low.
CBRDONE	O	CBR cell transmit done signal to complete the handshake with CBRXMIT indicating the successful transfer of a CBR cell to the cell interface.

Table 3-6. SARA-S Constant Bit Rate Transfer Interface Pin Description

3.1.2.7 Miscellaneous Signals

Table 3-7 shows the SARA-S pin descriptions for miscellaneous signals. The test pins TE, TEI, and SI are provided for manufacturing test purposes only. They must be tied to "0" (low) in user applications.

Symbol	Type	Name and Function
RST*	I	Hardware reset for SARA-S
CLK	I	Clock input.
TE	I	Scan test enable input.
SI	I	Scan input for SARA-S in scan mode.
SO	O	Scan output for SARA-S in scan mode.
TEI	I	Tri-state all outputs and bidirectional pins

Table 3-7. SARA-S Miscellaneous Signals Pin Description

3.2 Reassembly SARA Hardware Description

3.2.1 Reassembly SARA Internal Block Description

Figure 3-2 shows a block diagram of the Reassembly SARA (SARA-R) chip.

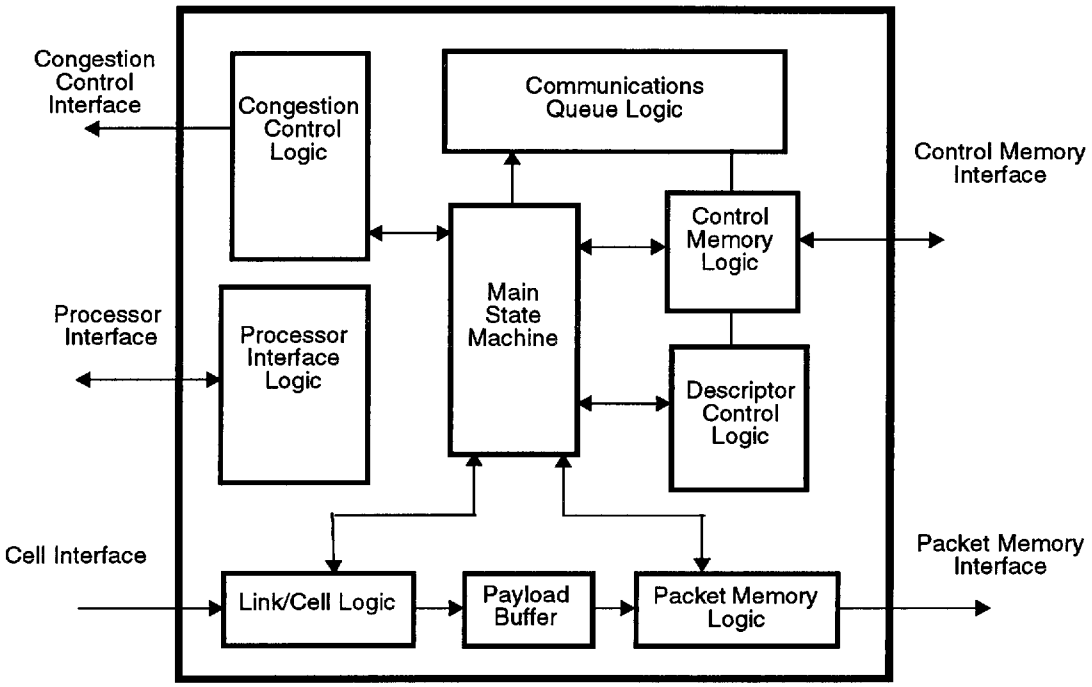


Figure 3-2. Block Diagram of Reassembly SARA

The SARA-R internally consists of several functional blocks:

- The *Processor Interface Logic* block interfaces with the processor to access the internal registers of SARA-R and to issue commands. The processor interface operates asynchronously.
- The *Control Memory Logic* block generates the bus arbitration signals (for access to the packet memory) and data transfer signals to the control memory. It can be programmed to generate these signals for both synchronous and asynchronous memory interfaces.
- The *Packet Memory Logic* block generates the bus arbitration signals (for access to the control memory) and data transfer signals to the packet memory. It also generates the packet memory address and transfers data from the cell buffer to the packet memory. It can be programmed to generate these signals for both synchronous and asynchronous memory interfaces.
- The *Link/Cell Logic* block is used to read the ATM cells from the link. It generates the signals to interface to a FIFO-like device.
- The *Payload Buffer* is an internal buffer (1 cell deep) that holds the payload ready for transfer to the packet memory interface.
- The *Descriptor Control Logic* block maintains working registers and processing logic for the buffer descriptor manipulation. It maintains the various base address registers and generates the control memory address and data bus signals. It also contains a timer for aging packets.

- The *Congestion Control Logic* block is used to communicate with the SARA-S to pass congestion control information.
- The *Communications Queue Logic* block contains all of the pointers and associated pointer logic for the four communication queues in the control memory and the two cell FIFOs in the packet memory. The pointers can be accessed by the host through the processor/host interface.
- The *Main State Machine*, consisting of 64 states, controls the seven blocks described above. It generates all of the control signals and sequences that operate the device.

3.2.2 Reassembly SARA Hardware Interfaces

The SARA-R contains the following types of hardware interfaces

- Processor Interface
- Cell Interface
- Control Memory Interface
- Packet Memory Interface
- Congestion Control Interface
- Miscellaneous Interface

Notes for tables:

1. Bit 0 on all busses is the least significant bit.
2. Parity is optional on all data busses that have parity bits.
3. An * at the end of signal name indicates that the signal is an active-low signal.
4. OD indicates an open drain output.
5. POD indicates a programmable open drain output.
6. All input and bi-directional I/O pins have internal pull-ups or pull-downs, which force an inactive state when the pin is left open.
7. All unused input pins must be tied to inactive state.

3.2.2.1 Processor Interface

The Processor interface is a slave interface that is used by the local host/processor to read and write the internal registers of the device. These registers are identified in Chapter 5. It is also used to interrupt the processor/host when an unmasked status bit is set. Table 3-8 shows the SARA-R processor interface pin descriptions.

Symbol	Type	Name and Function
CS*	I	Chip select signal to enable the processor interface for data transfers
DS*	I	Data strobe for enveloping the data transfer
WRT	I	WRITE(1), READ(0) input to indicate the direction of data transfer
RDY*	OD	SARA-R signal indicating completion of data transfer
A(7:0)	I	Address bus for internal register selection
D(15:0)	I/O	Processor interface data bus
INTR*	OD	Interrupt signal to the processor

Table 3-8. SARA-R Processor Interface Pin Descriptions

3.2.2.2 Cell Interface

The ATM cells are read by the SARA-R through the cell interface. The interface may be configured as either byte or word width and parity is selected by a mode bit. Cells may be received and read-in without boundaries or may be demarcated by either a tag bit or a parity inversion. Table 3-9 shows the SARA-R cell interface pin descriptions.

Symbol	Type	Name and Function
CLAV	I	Cell available in the FIFO(s).
FFMT	I	FIFO empty input that is used to detect data-insufficiency in a FIFO. Active when one or more FIFO(s) are empty.
FFRD(3:0)	O	FIFO Read enable. FFRD(0) is used as read signal, and FFRD(3:1) are used for testing.
FFSL(1:0)	O	These pins are used for testing and should be left open
FFD(17:0)	I	FIFO data-bus. FFD(17) & FFD(16) are the parity bits for FFD(15:8) & FFD(7:0) respectively. Either the full 16-bits or 8-bits of the data bus can be selected to transfer the data. In the 8-bit mode, the data is transferred on FFD(7:0) and uses FFD(16) as parity.
FFLUSH	O	FIFO flush signal is used to request the appropriate FIFO controller to flush the FIFO(s) when data misalignment is detected.
FLSHDONE	I	Asserted when all FIFO(s) are empty acknowledging FFLUSH.

Table 3-9. SARA-R Cell Interface Pin Description

3.2.2.3 Control Memory Interface

The control memory interface is a bus-master interface to the control memory. It is used to access the communication queues, virtual circuit/virtual path lookup tables, the reassembly table and the buffer descriptors maintained in the control memory. This interface supports both synchronous and asynchronous bus interfaces of various speeds. Table 3-10 shows the SARA-R control memory interface pin descriptions.

Symbol	Type	Name and Function
CREQ	O	Control memory bus request.
CGRT	I	Control memory bus grant.
CMULR	O	Control memory multiple request signal, indicating that more than one data transfer is pending.
CCYCST*	POD	Control memory cycle start signal marking the beginning of data transfer. Programmable as either open drain or as an active output.
CRDY*	I	Control memory ready signal indicates the end of each transfer.
CWRT	O	Control memory write signal for direction of transfer. This pin can be programmed as an early write signal to provide additional flexibility in external system design.
CA(23:1)	O	Control memory address bus (16-bit word address).
CD(17:0)	I/O	Control memory data bus. CD(17) & CD(16) are the parity bits for CD(15:8) & CD (7:0) respectively.

Table 3-10. SARA-R Control Memory Interface Pin Descriptions

3.2.2.4 Packet Memory Interface

The packet memory interface is a bus-master interface for writing cells to the packet memory where these cells are reassembled into packets. Various bus interfaces are supported. SARA-R packet memory interface pin descriptions are shown in Table 3-11.

Symbol	Type	Name and Function
PREQ	O	Packet memory bus request
PGRT	I	Packet memory bus grant
PCYCST*	POD	Packet memory cycle start (marks the beginning of data transfers). Programmable as either open drain or as an active output.
PRDY*	I	Packet memory ready, validates each data transfer.
PD(35:32)	O	PD(35), PD(34), PD(33), PD(32) are the parity bits for PD(31:24), PD(23:16), PD(15:8), PD(7:0) respectively.
PD(31:0)	O	Data path to the packet memory. Output for multiplexed address in PM_REQADR mode (Byte address PA(31:0) is presented on these pins during packet memory bus requests).

Table 3-11. SARA-R Packet Memory Interface Pin Descriptions

Symbol	Type	Name and Function
PA(15:0)	O	Packet memory address bus. This bus is driven with 16-bits of the byte address of the Packet memory location being accessed. The selection of the 16-bits is dependent upon the state of the PLWADR pin and the PM_INTRLV mode bit.
PLWADR	I	Input signal to multiplex the upper or lower part of the packet memory address on the PA bus.
PAMTCH	O	Indicates that the packet memory address matches with the contents of the address match register. Used to detect the end of the serial address memory (for VRAMs) or page boundaries.

Table 3-11. SARA-R Packet Memory Interface Pin Descriptions

3.2.2.5 Congestion Control Interface

This interface is used to transfer the VCI and congestion code of the congestion notification cell to the SARA-S. The SARA-S can use this index and the congestion notification code to modify the rate of cell generation of the particular VC source. The SARA-R congestion control interface pin descriptions are shown in Table 3-12.

Symbol	Type	Name and Function
CCDATA	O	Serial input stream of congestion control information from SARA-R to SARA-S.
CCXFER	O	Congestion control transfer enable for CCDATA.
CCHLD	I	Hold congestion control transfer.

Table 3-12. SARA-R Congestion Control Interface Pin Descriptions

3.2.2.6 Miscellaneous Signals

Miscellaneous signal pin descriptions for SARA-R are shown in Table 3-13. The test pins TE, TEI, and SI are provided for manufacturing test purposes only. They must be tied to "0" (low) in user applications.

Symbol	Type	Name and Function
CBRMT*	O	CBR FIFO empty
RST*	I	Hardware reset
CLK	I	Clock
TE	I	Scan test enable input.
SI	I	Scan input for SARA-R in scan mode.
SO	O	Scan output for SARA-R in scan mode.
TEI	I	Tri-state all outputs and bidirectional pins

Table 3-13. SARA-R Miscellaneous Signals Pin Descriptions

3.3 Hardware Interface Operation

3.3.1 Processor Interface

The processor/host interface is used by the external controller to access the internal registers of the SARA chips and to issue commands and instructions to the devices. It is comprised of a chip-select signal (CS*), data-strobe signal (DS*), write/read signal (WRT), ready signal (RDY*), an 8-bit address bus (A[7:0]) and a 16-bit data bus (D[15:0]). It also includes an interrupt signal (INTR*) to the interrupt handler.

It operates as an asynchronous slave interface. An access is triggered when both the CS* and DS* become active. The type of access (write or read) is determined by the state of the WRT signal. For the processor to write to the SARA chips, the WRT signal must be "1"; WRT must be "0" when the processor is to read from the SARA chips. The contents of the address-bus (A[7:0]) selects the register of interest or the command to be issued. Figure 3-3 shows the processor interface functional timing.

If the access is a read, the SARA chip will latch the data of the appropriate register, and then assert the RDY* signal. Upon the assertion of the RDY* signal, the processor/host can read the data on the data-bus and then terminate the access by de-asserting CS* and/or DS*.

If the access is a write, the SARA chip will load the contents of the data-bus into the appropriate register, and then assert the RDY* signal. At this time the processor can terminate the access by de-asserting the CS* and/or DS* signals.

This interface allows only a single data transfer per access. Back-to-back accesses require that either CS* or DS* be de-asserted for a duration of at least one-and-one- half CLK periods.

The INTR* signal is driven active whenever an unmasked bit is set in the status register of the device. The status register of the SARA will be automatically cleared after it is read by the processor through the processor interface. This in turn, will force the INTR* signal inactive. INTR* will not go active until an unmasked bit is set in the status register. Internal circuitry in the devices force the INTR* signal to be inactive for at least four CLK cycles even though an unmasked bit gets set in the status register.

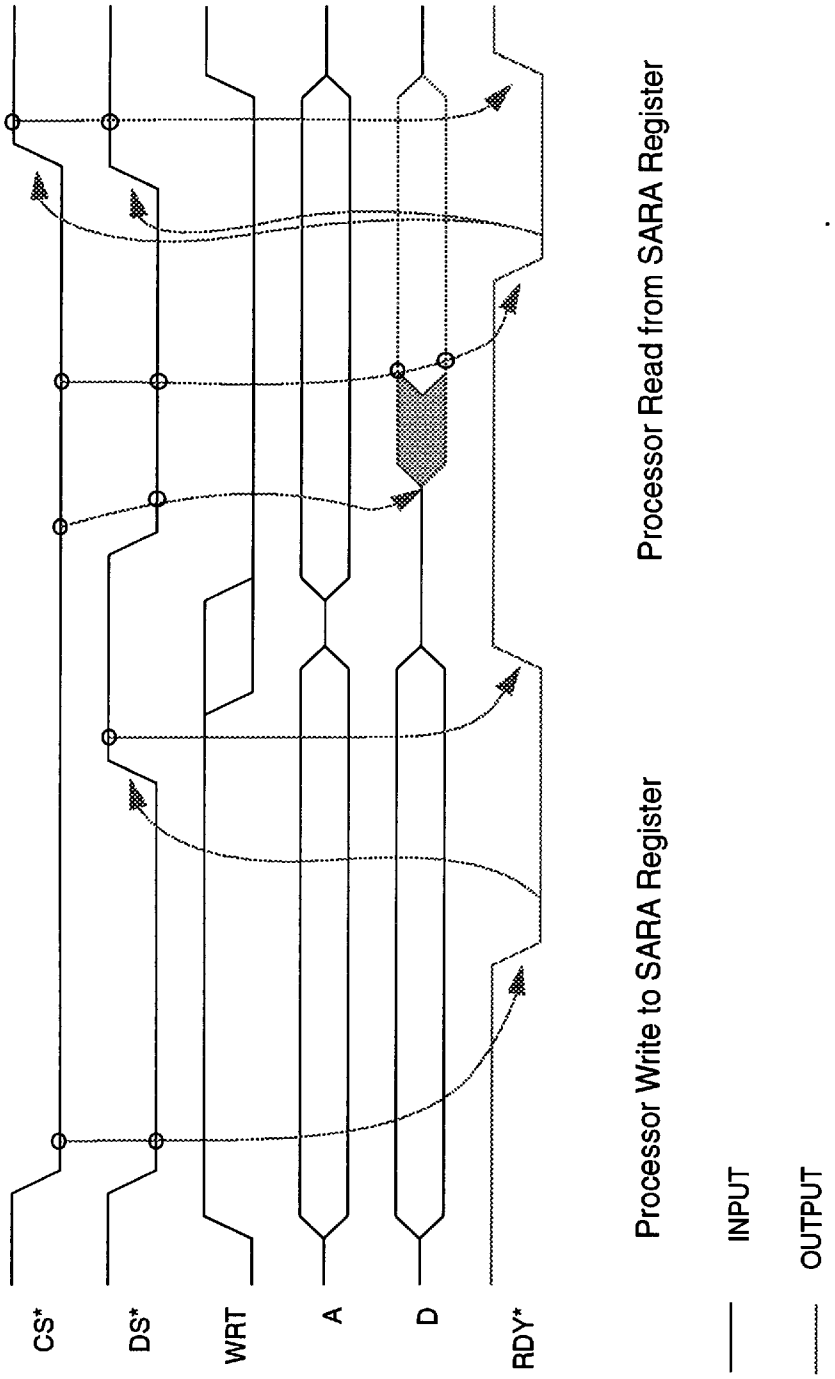


Figure 3-3. Processor Interface Functional Timing

3.3.2 Control Memory Interface

The Control memory interface is used by the SARA chips to access the control data structures and communication queues that are maintained in the control memory. This is a bus-master interface and can be programmed in a synchronous mode of operation, whereby all signals are synchronous to CLK and multiple data transfers are allowed per access, or in an asynchronous mode of operation where the input signals are synchronized inside the device and only single data transfers are allowed per access. This mode is controlled by the mode bit CM_IF_ASYNC in the mode register(s) of the appropriate device.

3.3.2.1 Address Bus CA(23:1)

The address bus is 23-bits wide (16-bit word addresses) and is driven active during the entire duration of the control memory data transfers, i.e. when CCYCST* is active.

3.3.2.2 Data Bus CD(17:0)

The upper 2-bits (17:16) of the data bus are the parity bits of the corresponding bytes. The PARITY bit in the mode register selects the type of parity: 0 - Odd parity, 1 - Even parity. The SARA chips always generate the parity bits during a write operation, but will only check the parity bits if the mode bit CM_PAR_EN bit is set high ("1").

3.3.2.3 Control Interface

The control memory control is composed of two sets of signals. The signals CREQ, and CGRT are used to arbitrate for access to the bus. The signals CMULR, CWRT, CCYCST* and CRDY* are used for data transfer. These signals are further described in detail for both the synchronous and the asynchronous modes of operation.

3.3.2.4 Synchronous Mode

Bus Access

CREQ is driven active when SARA-R or SARA-S needs access to the control memory bus for data transfers to or from the control memory. CREQ remains active until the CGRT input signal becomes active; CREQ is driven inactive on the next clock cycle after CGRT becomes active. CGRT must remain active for the duration of the entire memory access and must be forced inactive after memory access to complete the bus handshake. The SARA will not make a new request until CGRT becomes inactive. Figure 3-4 through Figure 3-8 show the various timings of the control memory interface. Figure 3-5 and Figure 3-8 show examples of an early write cycle, where CWRT terminates one clock cycle before the end of the last write.

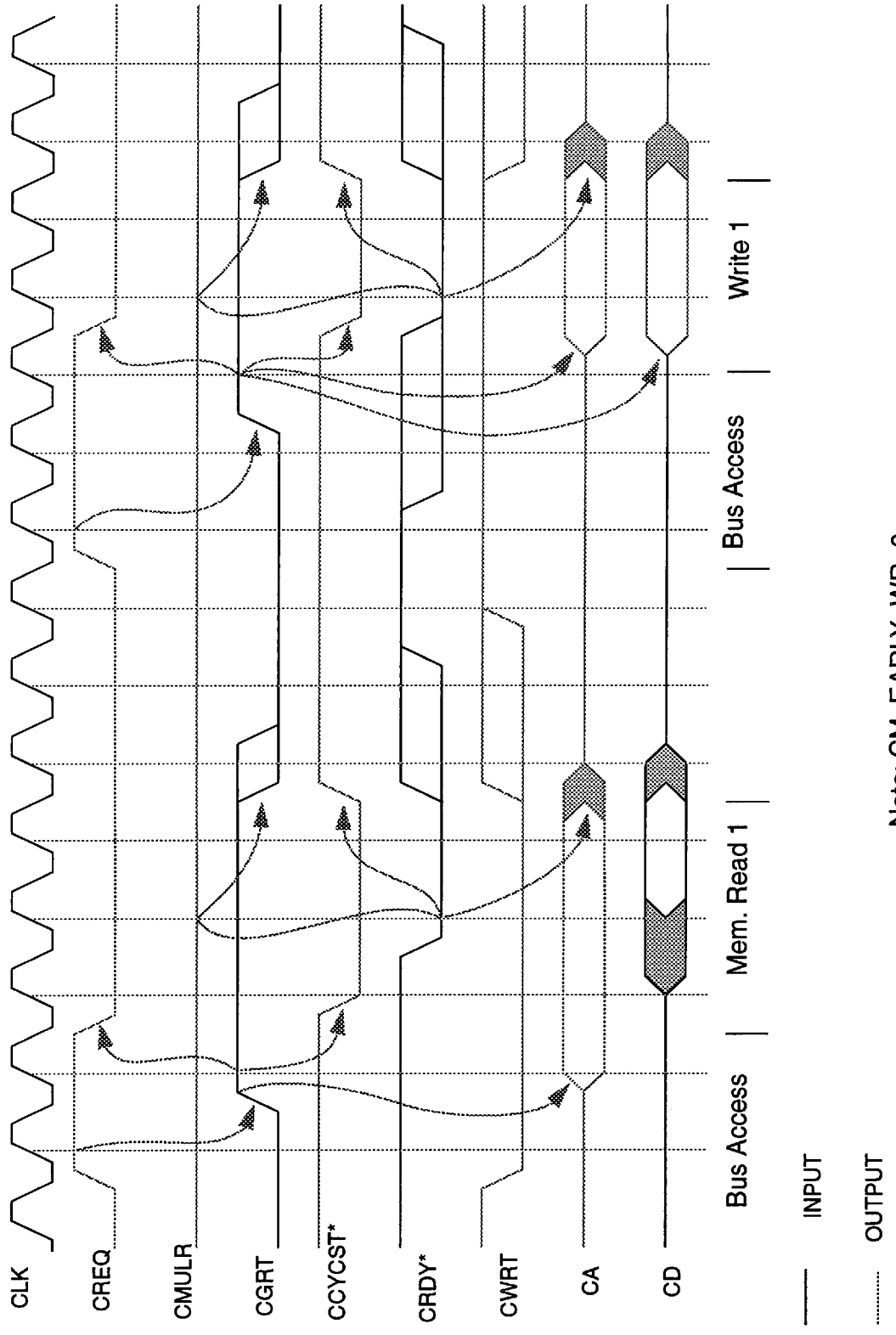


Figure 3-4 Control Memory Interface—Single Access Read and Write—Normal Write Mode

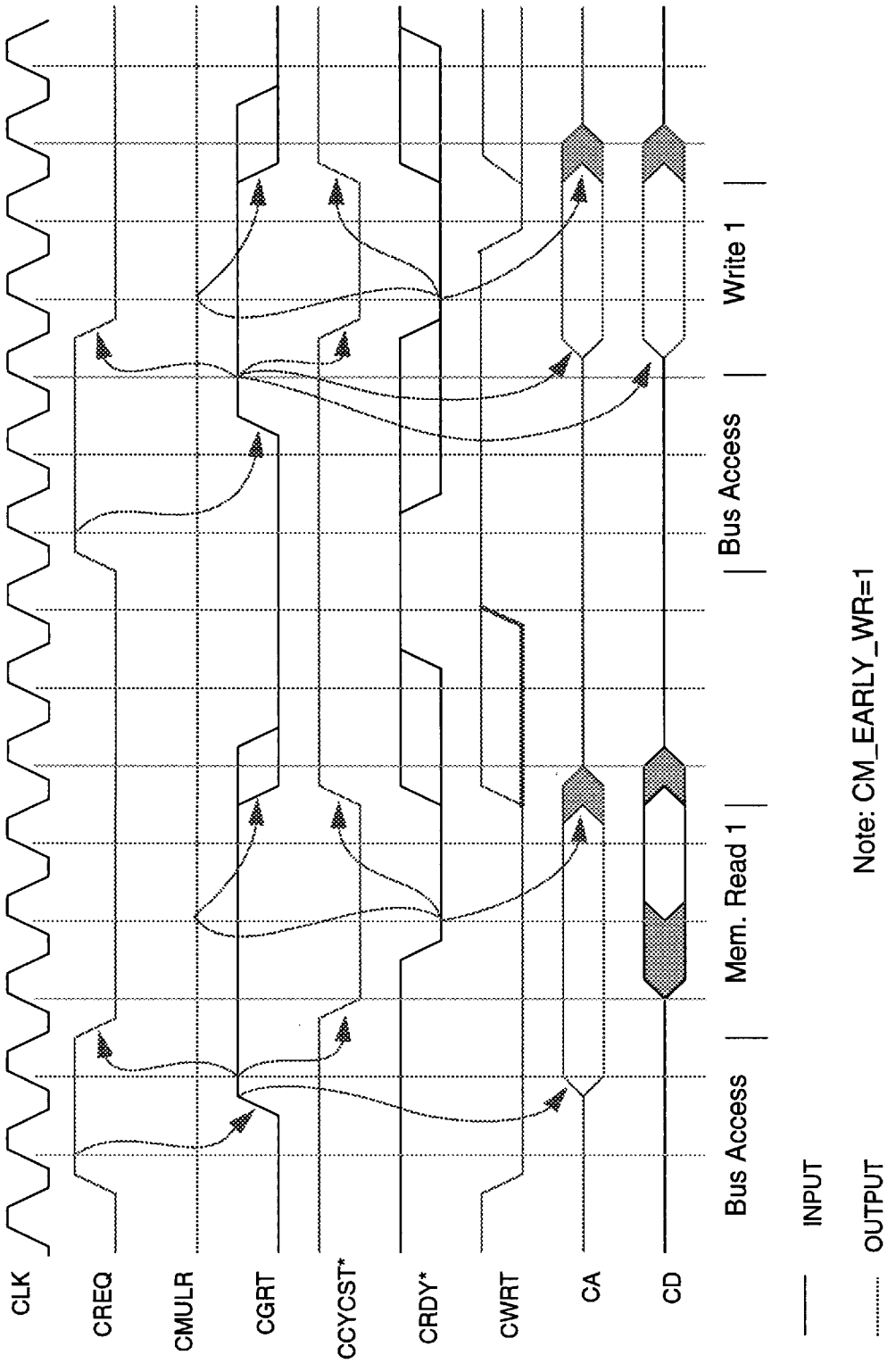


Figure 3-5. Control Memory Interface—Single Access Read and Write—Early Write Mode

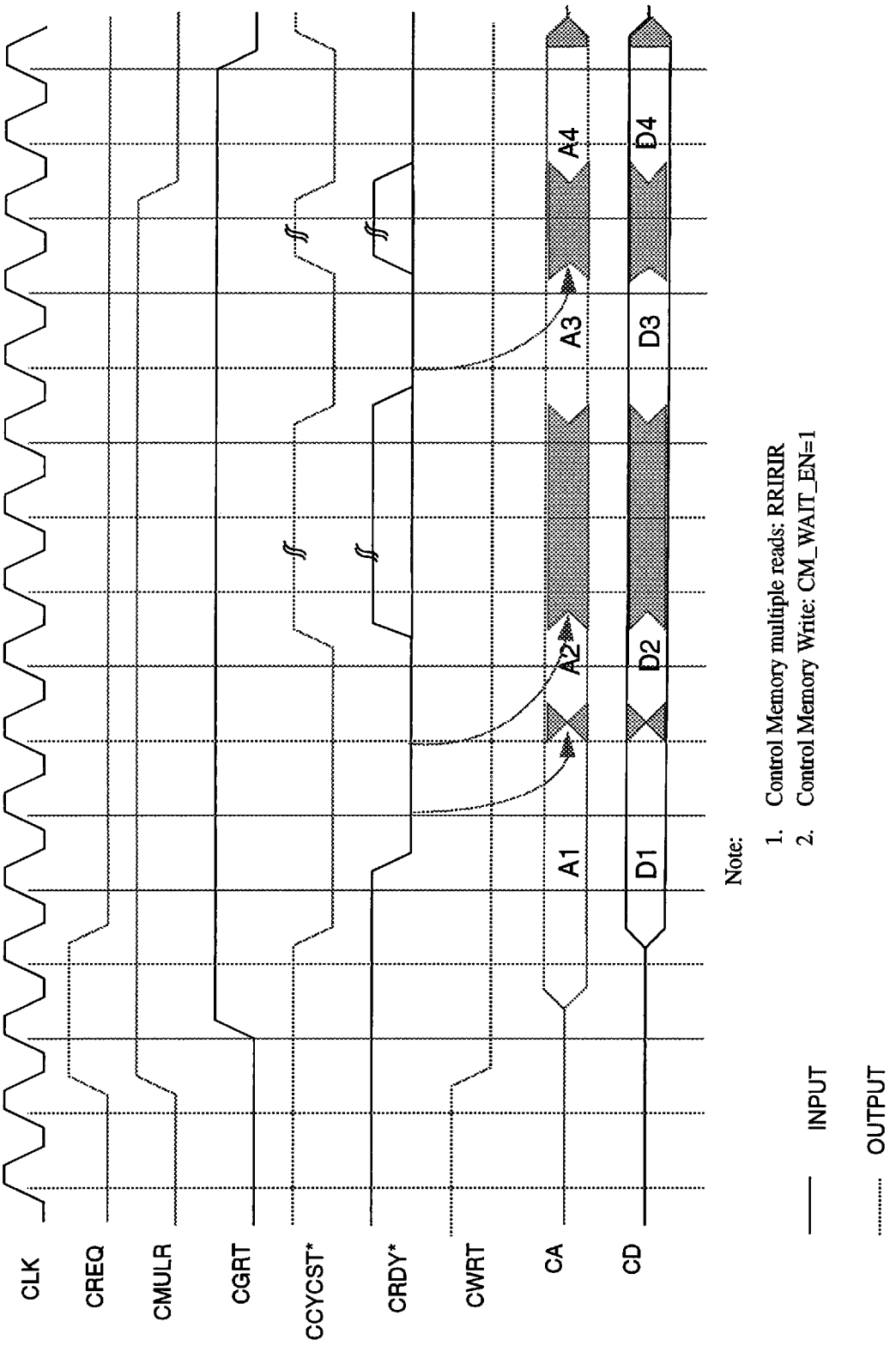
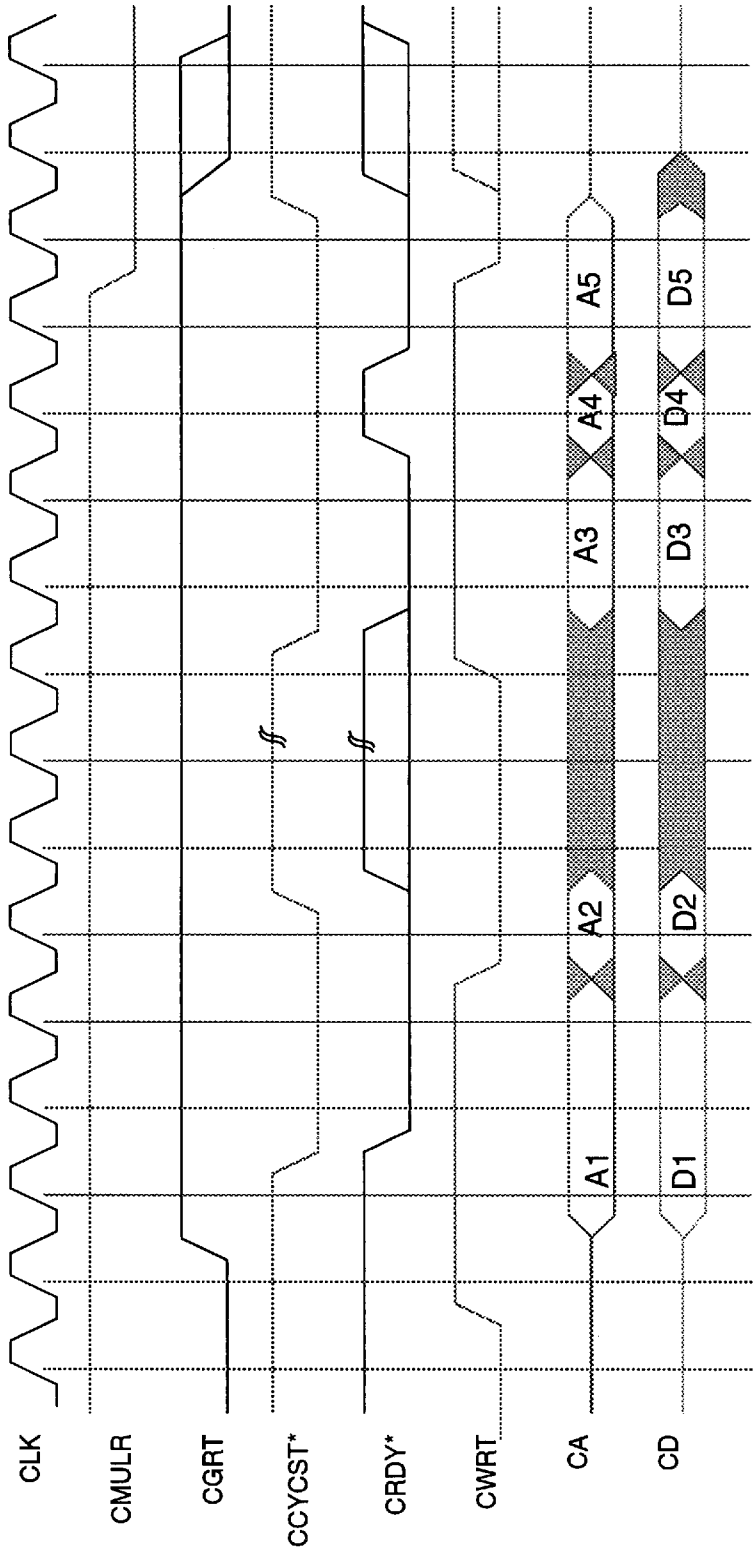


Figure 3-6. Control Memory Interface—Multiple Reads



Note:

1. Control Memory write: WWIWWW
2. Control Memory Write: CM_EARLY_WR=1; CM_WAIT_EN=1
3. CM_EARLY_WR=1 and CM_WAIT_EN=0 is an illegal condition and is not supported.

INPUT

OUTPUT

Figure 3-7. Control Memory Interface—Multiple Writes

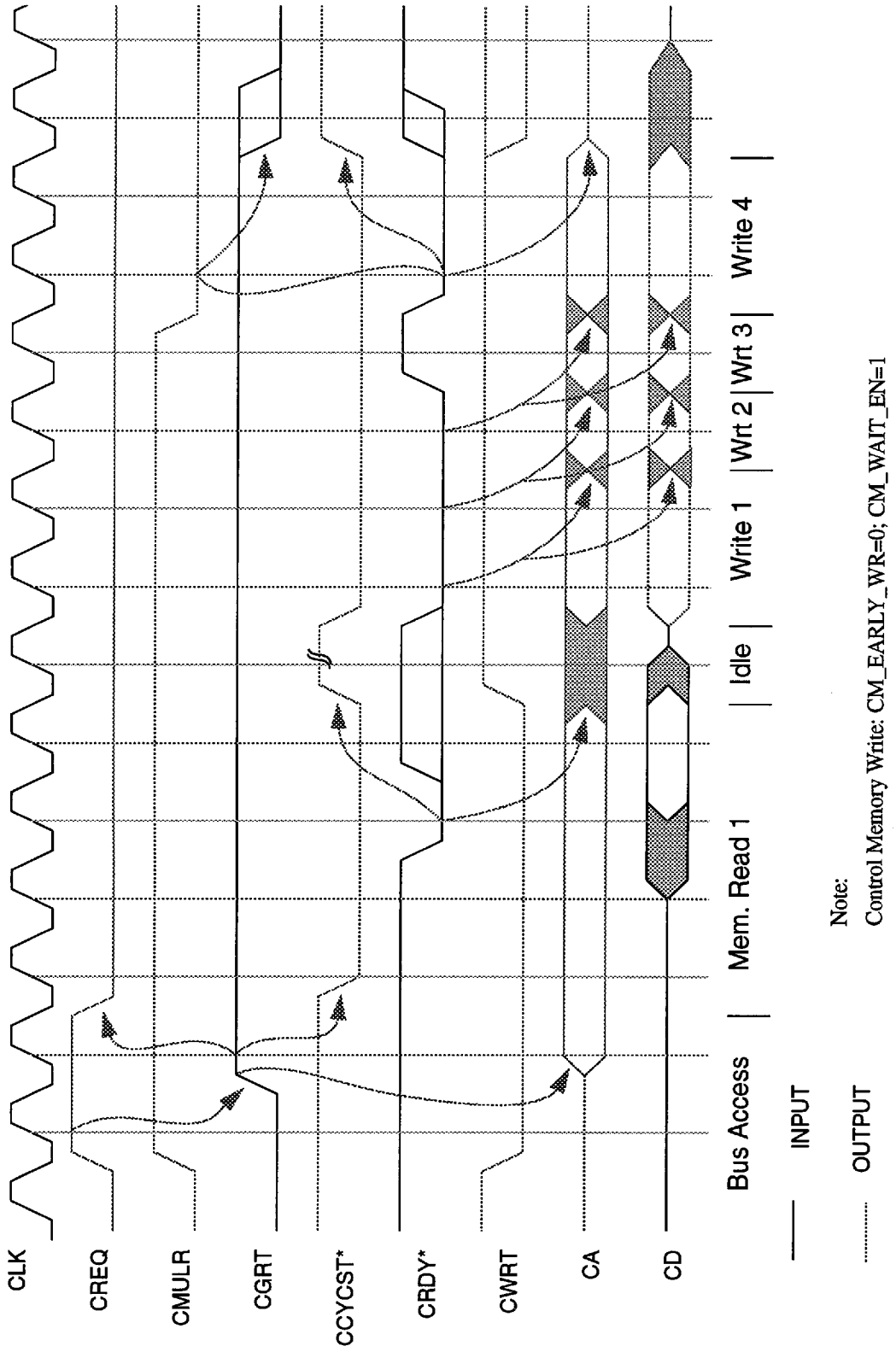


Figure 3-8. Control Memory Interface—Single Read/ Multiple Writes—Normal Write Signal

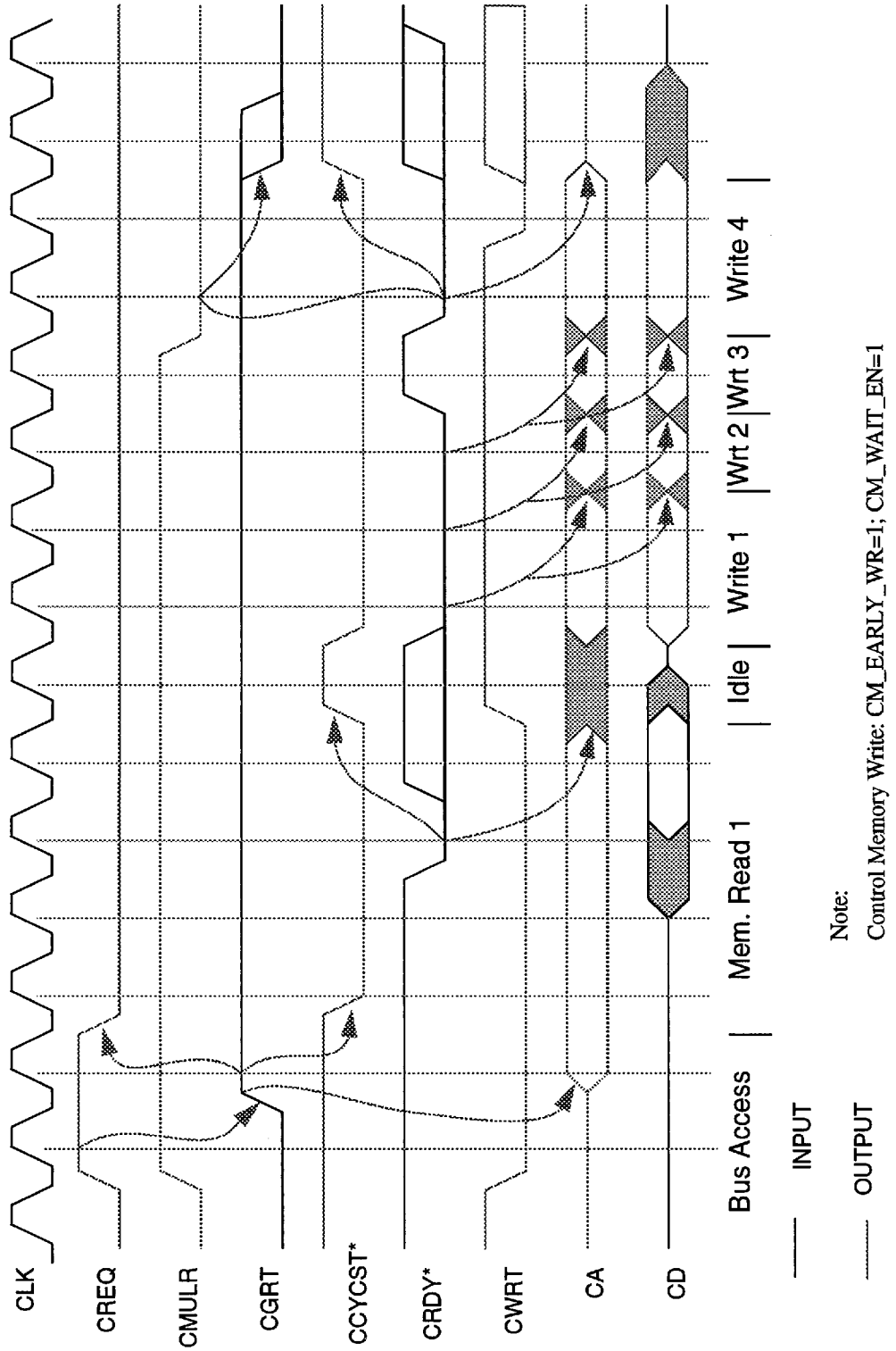


Figure 3-9. Control Memory Interface—Single Read/ Multiple Writes—Early Write Signal

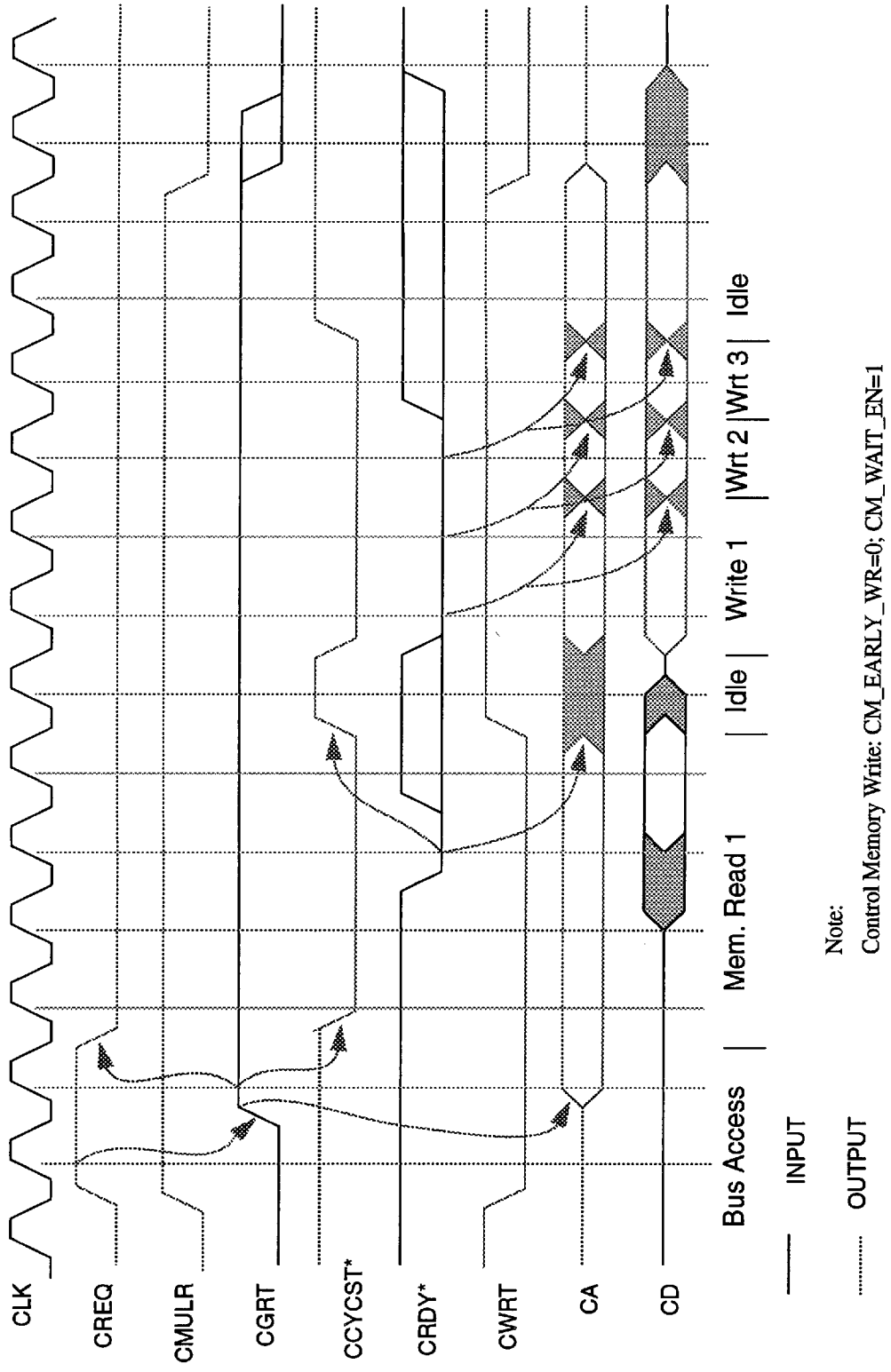


Figure 3-10. Control Memory Interface—Without Last Access

Data Transfer

The CGRT signal going active marks the beginning of the data transfer(s). The signal CCYCST* is driven active in the same cycle when CREQ becomes inactive. If the number of data transfers is expected to be greater than one, the CMULR signal is also driven active. This signal remains active until the end of the penultimate data transfer. The address bus CA(23:1) is driven active (it is 3-stated when CCYCST* is inactive). While CCYCST* is active, the device reads from the data-bus when CWRT is "0" (read data transfer) or drives the data onto the data bus when the CWRT signal is "1" (write data transfer). During a burst of data transfers, if the access changes from a read to a write transfer or from a write to a read transfer or if there are no transfers but the SARA wants to hold the bus, the CCYCST* signal will be driven inactive for at least one cycle, and the CMULR signal will remain active indicating that the SARA is still active on this interface.

Note that if the SARA is holding the control memory interface but not performing any data transfers, it will hold the CMULR signal active and the CCYCST* signal inactive. On the last access the SARA will force the CMULR signal inactive. If the SARA does not need to access control memory after the idle cycle, then it will release the interface by deasserting the CMULR signal, as shown in Figure 3-10.

The duration of each data transfer is controlled by the CRDY* input signal. The CRDY* signal (when CCYCST* is active) is delayed internally by one CLK cycle, then used to latch the data and generate the next address. By holding the CRDY* input signal inactive the duration of the transfer can be extended, since each transfer is completed only when CRDY* is active. On the completion of the last word transfer, the signal CCYCST* is driven inactive and the address and data busses are 3-stated. The CRDY* signal must be forced inactive after the completion of the access.

When the CM_WAIT_EN bit is set to 1, connecting CRDY* to CCYCST* will result in a two cycles for the first data transfer and single clock cycle for the remaining data transfers.

The SARA chips can be preempted on this interface by deactivating the CGRT signal. The data transfers will be terminated in the cycle following the cycle when the CGRT signal becomes inactive. If CM_WAIT_EN = 1, the CRDY* signal must also be forced inactive when CCYCST* is driven inactive. The SARA chips will re-request for the bus and continue from the last valid data transfer.

If the mode bit CM_EARLY_WR is set to a "1" (Figure 3-5, Figure 3-7, and Figure 3-8), then the CWRT pin will be forced to a '0'in the clock cycle before CCYCST* becomes inactive. This allows for external hardware to generate synchronous write signals to the control memory.

3.3.2.5 Asynchronous Mode

Bus Access

CREQ is driven active when the SARA-R or SARA-S needs access to the control memory bus for data transfer to/from the control memory. CREQ is driven inactive after CGRT becomes active. CGRT must remain active for the duration of the entire memory access and must be forced inactive after memory access to complete the bus handshake.

Data Transfer

The CGRT signal going active marks the beginning of data transfer. The signal CCYCST* is driven active in the same cycle when CREQ becomes inactive. (The CMULR and CM_EARLY_WR signals have no meaning in the asynchronous mode of operation.) The address bus CA(23:1) is driven active (it is 3-stated when CCYCST* is inactive). When the CCYCST* is active, the device reads from the data-bus when CWRT is "0" or drives the data onto the data bus when the CWRT signal is "1".

The CRDY* signal (when CCYCST* is active) should be driven active after the data has been written to the memory (write transfer) or when the data is available on the data bus (read transfer). CRDY* is synchronized internally, then used to latch the data. By holding the CRDY* input signal inactive, the duration of the transfer can be extended, since the transfer is completed only when CRDY* becomes active. Once CRDY* is sensed active by the SARA chips, the signal CCYCST* is driven inactive, and the address and data busses are 3-stated. The CRDY* signal must be forced inactive for the completion of the access.

Forcing CGRT inactive before the completion of the access will invalidate the data transfer. The SARA chips will re-request for the bus and continue from the last valid data transfer.

3.3.3 Packet Memory Interface

The packet memory interface is used by the SARA chips to transfer packet data to and from the packet memory. This is a bus-master interface that can be used with a wide variety of memories. It can be programmed in a synchronous mode of operation where all signals are synchronous to CLK and multiple data transfers are allowed per access, or in an asynchronous mode of operation where the input signals are synchronized inside the device and only single data transfers are allowed per access. This mode is controlled by the bit PM_IF_ASYNC in the mode register(s) of the appropriate device.

The interactions of the packet memory interface are also controlled by the contents of the mode registers and the address match register. The effect of the mode bits is described in relation to the appropriate interface signals in the following paragraphs.

3.3.3.1 Data Bus PD(35:0)

The upper 4-bits PD(35:32) of the data bus are the parity bits of the corresponding bytes. The PARITY bit in the mode register of the appropriate SARA selects the type of parity: 0 - odd parity, 1 - even parity. The SARA-R always generates the parity bits, and the SARA-S will only check the parity bits if the mode bit PM_PAR_EN is set to a "1". When the mode bit PM_IF_WORD is set to "1", indicating a 16-bit data-interface, then only the data-bits {PD(33:32), PD(15:0)} of the data bus are used.

If the mode bit PM_REQADR is set to "1" in the mode register of the appropriate SARA, the 32-bit packet memory address is multiplexed onto the data-bus bits PD(31:0) when the SARA is requesting access to the bus (PREQ is active and PGRT is inactive), and when PLWADR signal input is a "1." Table 3-14 shows the state of the 32 bits of the data bus as a function of PREQ, PGRT, and PLWADR.

PREQ	PGRT	PLWADR	PD(31:0)
1	0	0	3-state
1	0	1	Address
1	1	X	Data

Table 3-14. Interactions of PREQ, PGRT, and PLWADR with the Packet Data Bus PD(31:0)

3.3.3.2 Address Bus PA(15:0)

While the PA address bus is 16-bits wide, the packet memory internal to the SARA devices can have 24 bits of address, allowing 16 MBytes of packet data. When the PLWADR signal is "0", the SARA-R and SARA-S multiplexes the upper bits of the packet address onto the address bus PA(15:0). The lower bits of the address (byte address) are correspondingly multiplexed

when the PLWADR signal is a "1". Note that this does not depend on the CLK signal. The upper and lower part of the address overlap on 8-bits (PA(15:8)). This allows a range of DRAMs with different RAS and CAS address-widths.

The actual bits on the address bus also depend upon the state of the bits PM_INTRLV and PM_IF_WORD in the mode registers. When the PM_INTRLV mode bit is set and when the upper address bits are selected, the second or first address bit (rather than the eighth address bit) is driven on PA(0). This is particularly useful if the packet memory is organized as a 2-way interleaved memory, since this allows the selection of the appropriate memory bank when the upper address bits are selected (e.g. RAS address).

Table 3-15 lists the interactions of the mode bits and the state of the PLWADR pin.

PLWADR	PM_INTRLV	PM_IF_WORD	PA(15:0)
(Input pin)	(Mode bit)	(Mode bit)	(Output pins)
0	0	X	Address bits 23 through 8.
0	1	0	Address bits 23 through 9 and address bit 2.
0	1	1	Address bits 23 through 9 and address bit 1.
1	X	X	Address bits 15 through 0

Table 3-15. Mode Bit/PLWADR Interactions

The SARA chips also contain circuitry to support detection of packet memory address boundaries. The packet memory address, PA(13:2) bits are constantly compared with the contents (11:0) programmed in the address match register. The upper four bits are only compared when the corresponding bits (15:12) in the address match register are set to "0". When the packet memory address matches the contents of the address match register, the PAMTCH signal becomes active. This feature can be used by external circuitry to detect page-boundaries, end of SAM (serial address memory) in a VRAM (Video DRAM), etc., and stop the SARA data-transfer to change the page or SAM.

The SARA chips always interrupt the data transfers when the packet address rolls over the 16-bit boundary, by releasing the bus. The SARA chips will re-request the bus and then restart from the next address. This is useful if the upper bits of the address are latched and are used to drive the address lines of memory.

3.3.3.3 Control Signals

The packet memory control is comprised of two sets of signals. PREQ and PGRT are used for the packet memory bus handshake. PCYCST*, PRDY*, PLWADR are used for data transfers. These signals are further described in detail for both modes.

3.3.3.4 Synchronous Mode

Bus Access

The PREQ signal is driven active when the SARA-R or SARA-S needs access to the bus for data transfers to or from the packet memory. The PREQ signal remains active until the PGRT input signal becomes active. The PREQ signal is driven inactive on the next clock cycle after PGRT becomes active. PGRT must remain active for the duration of the entire data transfer, and must be driven inactive after the access to complete the handshake.

Data Transfer

The PGRT signal becoming active marks the beginning of data transfer. The signal PCYCST* becomes active in the same cycle when PREQ becomes inactive. The address bus PA(15:0) is driven active (it is 3-stated when PCYCST* is inactive). There are no packet memory read or write signals on the SARA chips since the SARA-S only reads from and the SARA-R only writes to the packet memory. When the PCYCST* becomes active, the SARA-R drives the data onto the data bus PD(35:0). The signal PCYCST* will remain active through the entire data transfer.

The duration of each data transfer is controlled by the PRDY* signal. The PRDY* signal (when PCYCST* is active) is synchronized internally and is used to generate the next address and latch the input data (SARA-S) or the output data (SARA-R). By driving the PRDY* signal inactive, the access time of the transfer can be extended. On the completion of the last word transfer, the signal PCYCST* is forced inactive and the address and data bus are 3-stated.The PRDY* and PGRT signals must also be driven inactive at the completion of the access. Figure 3-11 and Figure 3-12 show the packet memory interface timings.

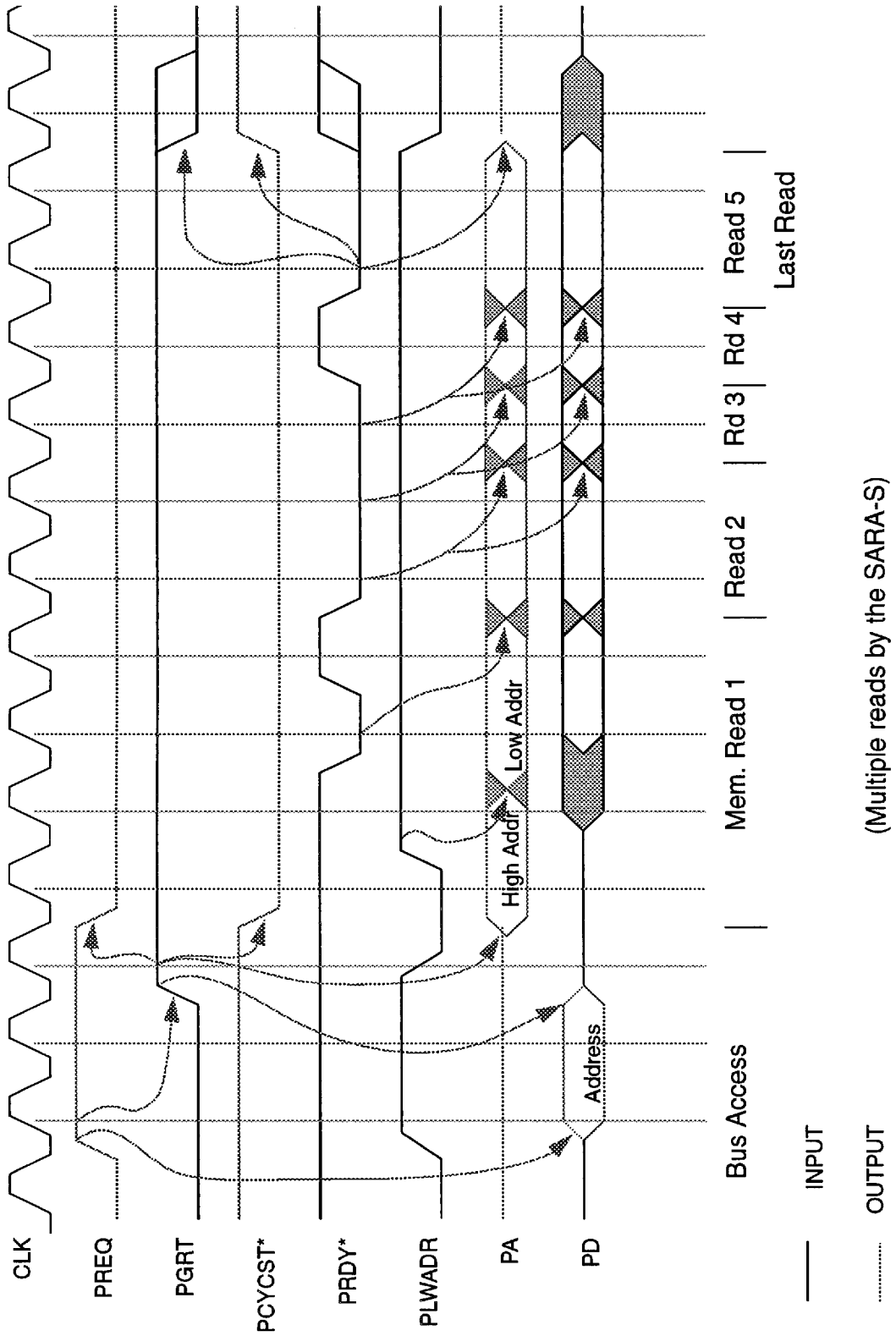


Figure 3-11. Packet Memory Interface—Address Driven on Data Bus During Bus Access

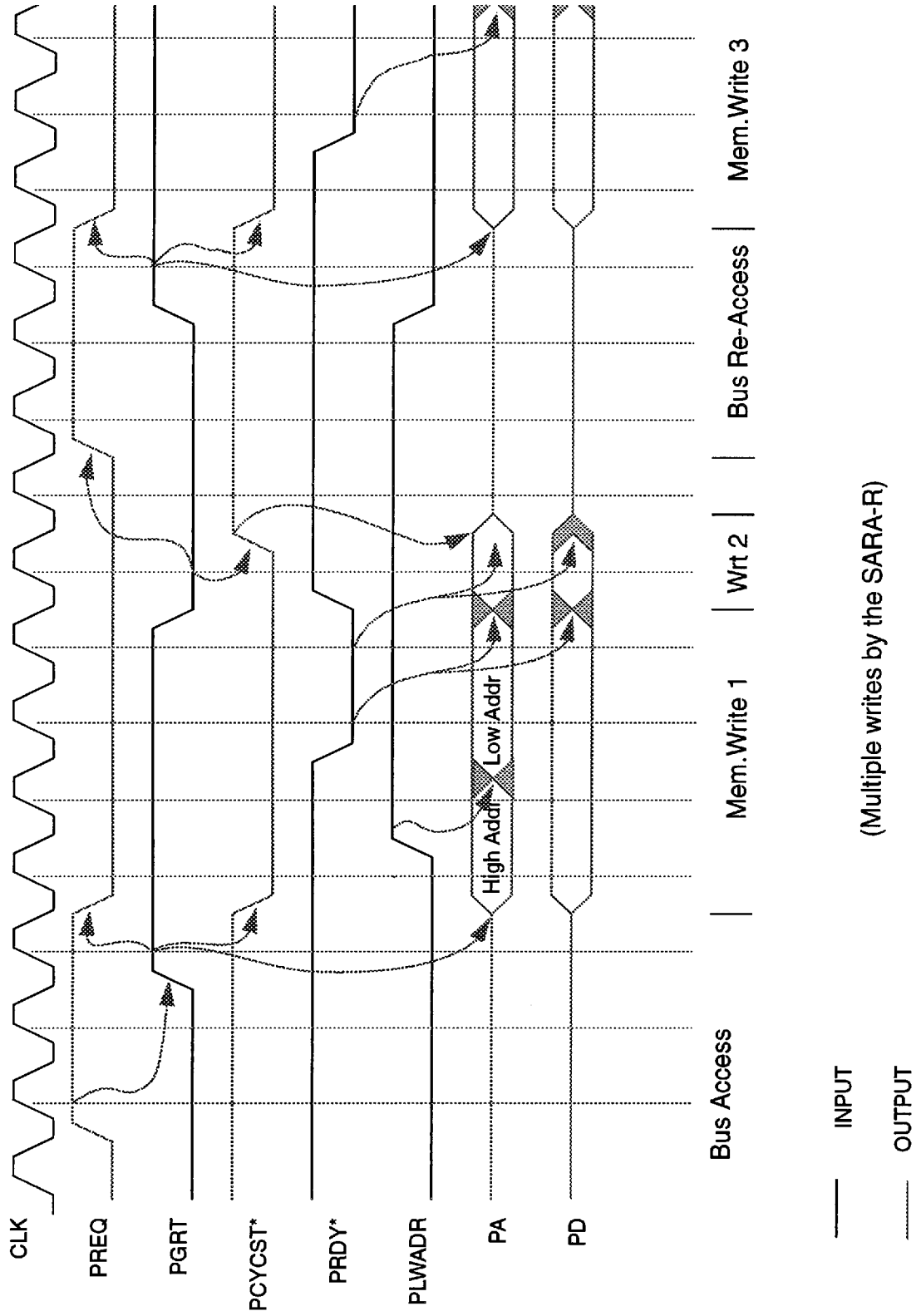


Figure 3-12. Packet Memory Interface—Bus Preempted by De-assertion of PGRT

The SARA chips can be preempted on this interface by de-asserting the PGRT signal. The data transfer will be terminated in the following cycle after the PGRT signal becomes inactive. The SARA chips will re-request for the bus and continue from the last data transfer.

3.3.3.5 Asynchronous Mode

Bus Access

PREQ is driven active when either SARA chip needs access to the bus for data transfer to or from the packet memory. PREQ is driven inactive after PGRT becomes active. PGRT must remain active for the duration of the entire memory access and must be forced inactive after to access to complete the bus handshake.

Data Transfer

The PGRT signal going active marks the beginning of data transfer. The signal PCYCST* is driven active in the same cycle when PREQ becomes inactive. The address bus PA(15:0) is driven active (it is 3-stated when PCYCST* is inactive). When the PCYCST* becomes active, the SARA-R drives the data onto the data bus.

The PRDY* signal (when PCYCST* is active) should be driven active either after the data has been written to the memory (SARA-R), or when the data is available on the data bus (SARA-S). PRDY* is synchronized internally, then is used to latch the data. By holding the PRDY* input signal inactive, the duration of the transfer can be extended, since the transfer is completed only when PRDY* becomes active. Once PRDY* is sensed active by the SARA chips, the signal PCYCST* is driven inactive and the address and data bus are 3-stated. The PRDY* and PGRT signals must be forced inactive for the completion of the access.

Forcing PGRT inactive before the completion of the access will invalidate the data transfer. The SARA chips will re-request for the bus and continue from the last valid data transfer.

3.3.4 Link/Cell Interface

The SARA devices connect to the transmission logic through the link/cell interface. This interface is designed to work synchronously and can be configured to have either an 8- or a 16-bit data path. This interface can optionally be protected by parity. On the receive path, the SARA-R supports demarcation of cells. The beginning of a cell can be indicated by inverting the parity on the first word of the cell. The cell boundary can also be indicated by setting the parity bits to "1" if parity is not used on this interface. The byte ordering of the data on this interface is shown in Table 3-16.

8-bit mode	
FFD16	FFD7-FFD0
t	hdr0
p	hdr1
p	hdr2
p	hdr3
p	hec
p	pyld0
p	pyld1
p	pyld2
p	.
p	.
p	.
p	pyld46
p	pyld47

16-bit mode			
FFD17	FFD16	FFD15 - FFD8	FFD7 - FFD0
t	t	hdr0	hdr1
p	p	hdr2	hdr3
p	p	hec	pyld0
p	p	pyld1	pyld2
p	p	pyld3	pyld4
p	p	pyld5	pyld6
p	p	pyld7	pyld8
p	p	.	.
p	p	.	.
p	p	.	.
p	p	pyld43	pyld44
p	p	pyld45	pyld46
p	p	pyld47	--

Table 3-16. Byte Ordering of Data for Link/Cell Interface

For SARA-S, 't' & 'p', are parity bits of the corresponding bytes; for SARA-R, these bits depend on whether boundary check (mode bit CI_BNDRY_CHK) is enabled or disabled and whether parity check (mode register bit CI_PAR_EN) is enabled or disabled on this interface.

CI_BNDRY_CHK = 1, CI_PAR_EN = 1: p => parity, t => inverted parity

CI_BNDRY_CHK = 1, CI_PAR_EN = 0: p => 0, t => 1

CI_BNDRY_CHK = 0, CI_PAR_EN = 1: p => parity, t => parity

CI_BNDRY_CHK = 0, CI_PAR_EN = 0: p => 0, t => 0

3.3.4.1 SARA-S

For SARA-S, the link/cell interface is designed to emulate a clocked FIFO interface. The interface works on the clock signal RDCLK, which is independent of the SARA-S CLK signal and is typically based on the link clock. When a cell is available for transmission in the payload buffer, the SARA-S sets the signal CELAVL* active and drives the first word (8-bit or 16-bit depending upon the CI_WIDTH16 mode bit) on the FFD(17:0) bus. The external logic asserts the RDEN signal when it is ready to transmit the data. The SARA-S drives the next data word on the FFD(17:0) bus on the rising transition of the RDCLK when RDEN and CELAVL* are both active. CELAVL* will be active for the entire cell transfer duration. When the last word is read out, the SARA-S de-asserts the CELAVL* signal. There is a minimum of four clock cycles before CELAVL* goes active again.

SARA-S responds to the XON input by transferring cells to the cell interface as long as the XON input is always true. If the XON input is false (low), then cell transfers of selected rate queues (and optionally the CBR traffic) are temporarily suspended while the XON signal is false. The suspension occurs gracefully on cell boundaries if the XON signal goes false during rate queue processing.

3.3.4.2 SARA-R

The SARA-R link/cell interface is designed to communicate with the read port of a clocked FIFO. This interface works on the SARA-R clock signal CLK. The CLAV input signal is driven active when a cell is available in the external FIFO (all 53-bytes of the cell must be available). The SARA-R reads either eight- or 16-bit data as determined by the CI_WIDTH16 on the FFD(17:0) bus by asserting the FFRD(0) signal. If the boundary check is enabled, the SARA-R reads the data until it finds the start of cell and then reads the complete cell. The CLAV needs to be valid until the first byte/word is read in. The CLAV may be deasserted any time after that. The SARA-R reads the complete cell before it senses the CLAV signal for the next cell. The SARA-R de-asserts the FFRD(0) signal after reading the first seven bytes (four words) of a cell. The SARA-R then re-asserts the FFRD(0) to continue reading the rest of the cell.

If the external FIFO becomes empty (FFMT goes active) before the entire cell is read in, the SARA-R will terminate the processing on that cell and assert the FFLUSH signal. The FFLUSH signal is also asserted when boundary check is disabled and the SARA-R sees two cells back-to-back with HEC errors. This signal remains active until the external logic asserts FLSHDONE. The external logic must hold-off further writes to the FIFO until a new start of cell is detected. This will prevent the generation of a runt cell in the FIFO after the FLUSH signal is asserted. Figure 3-13 and Figure 3-14 show the cell interface timings.

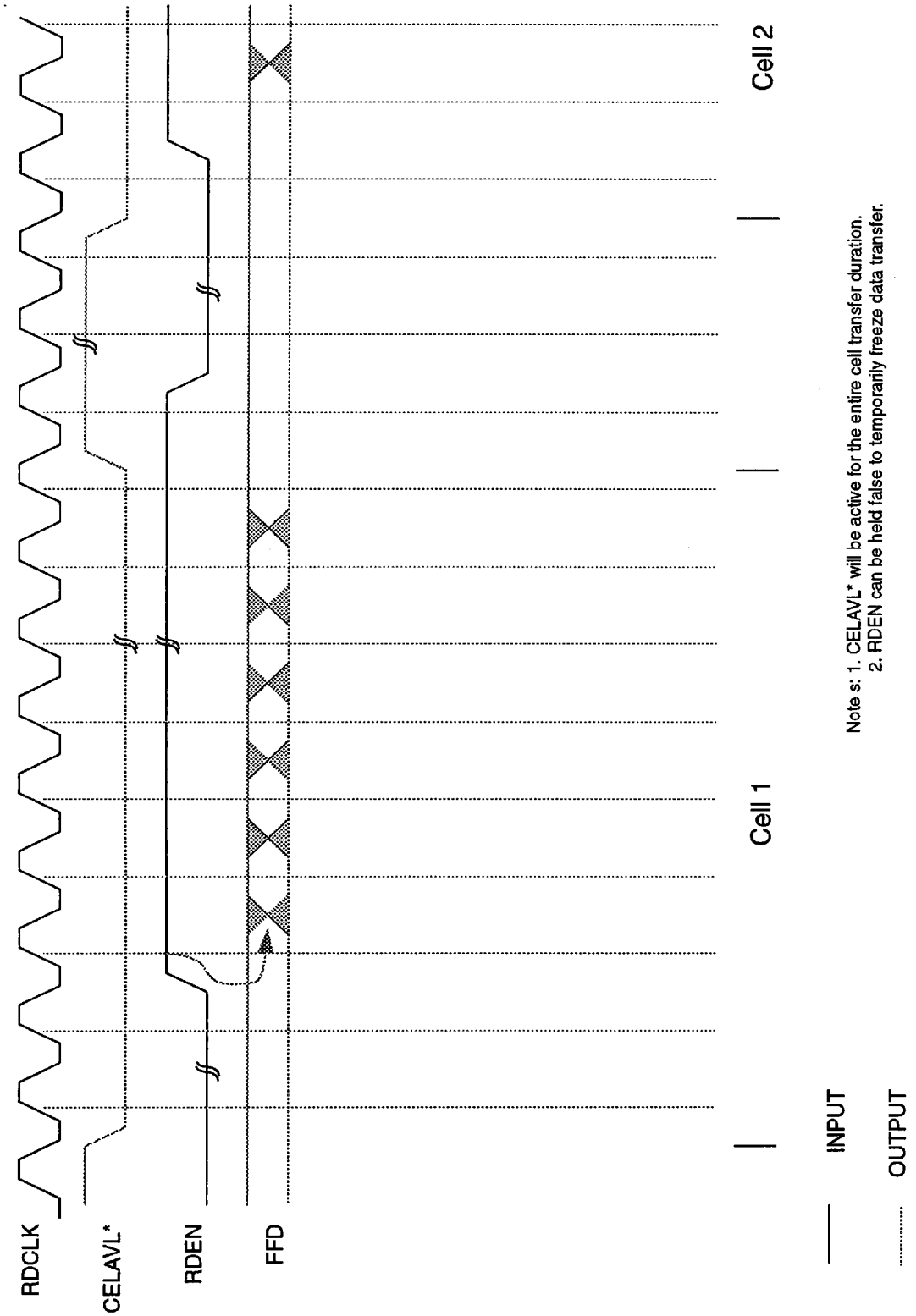


Figure 3-13. Cell Interface—SARA-S

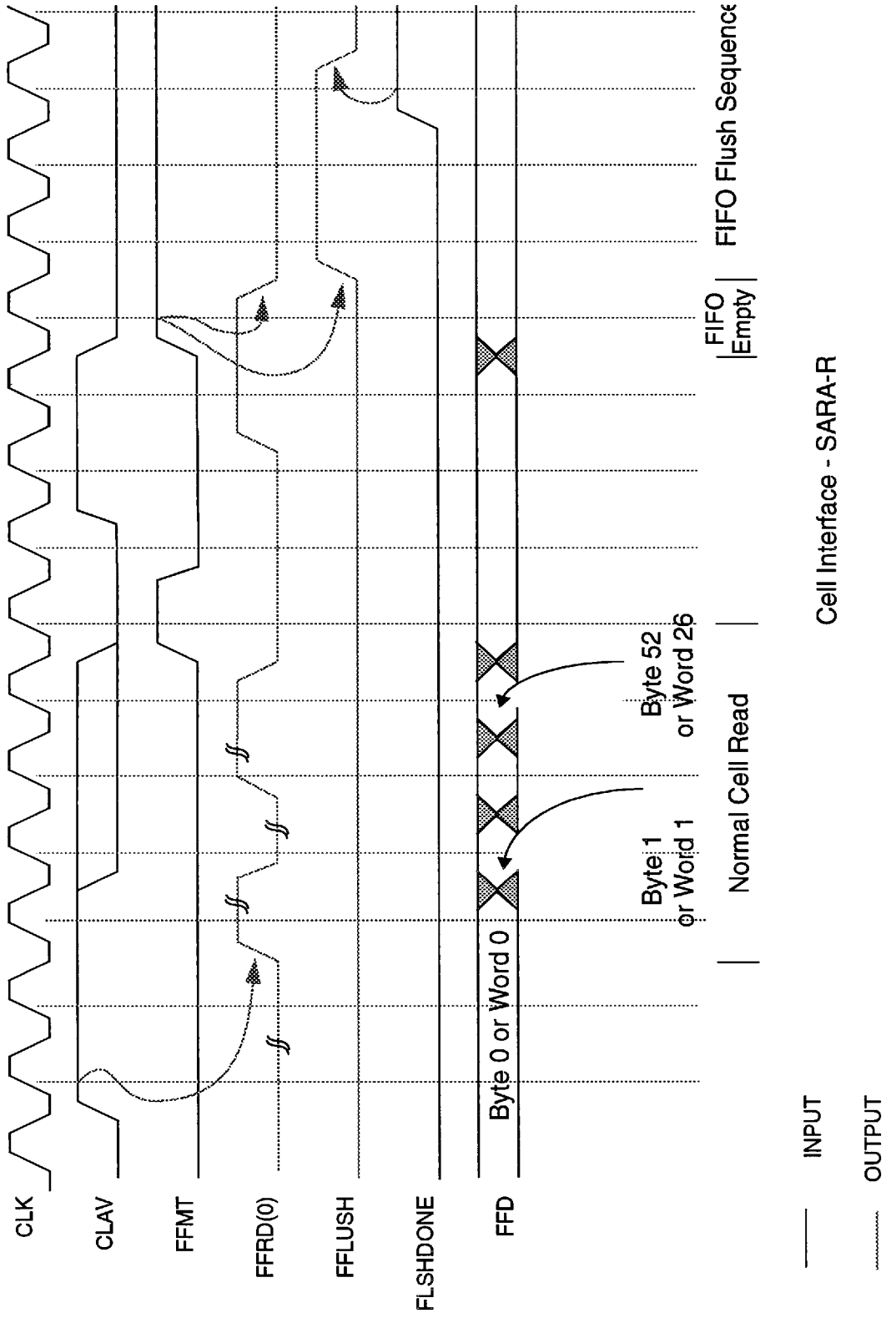


Figure 3-14. Cell Interface—SARA-R

3.3.5 Congestion Control Interface

The congestion control interface is used to transfer the congestion control information from the SARA-R to the SARA-S upon the receipt of a congestion notification cell by the SARA-R. The format of congestion notification cells is defined in Chapter 5.

This interface is comprised of two control signals, CCXFER and CCHLD, and a serial data signal, CCDATA. When a congestion notification cell is received, if CCHLD is inactive, the SARA-R drives CCXFER active and shifts out the 26 bits of serial data on the CCDATA pin. Once the SARA-S receives the congestion control information, it forces CCHLD active until it has processed the information and is ready to receive new congestion control information.

The bits that are transferred from the SARA-R to the SARA-S are shown in Figure 3-15. The most significant bit is shifted out first.

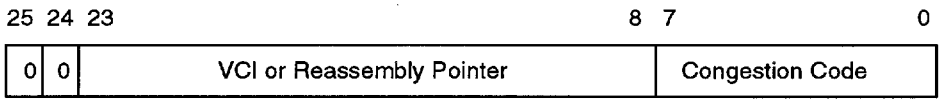


Figure 3-15. CCDATA Format

If the cell is received on a circuit that is setup to reassemble packets using the VCI and MID, then the lower 16 bits of the VCI are shifted out, otherwise if the circuit is setup to reassemble packets using the VPI and VCI fields, then the 16-bit reassembly pointer from the VP table is shifted out.

The congestion code is that which is carried in the payload of the congestion control cell, i.e. the second byte of the 48-byte payload. If the congestion code is 01H, the congestion is considered moderate and the segmentation peak rate on that virtual circuit is throttled by one notch. If the congestion code is 02H, the congestion is considered extreme and the segmentation of packets on that particular virtual circuit is immediately stopped (drops down to fifth notch).

3.3.6 Constant Bit Rate Interface

3.3.6.1 SARA-S

The SARA-S has a pair of signals CBRXMIT and CBRDONE for controlling the transmission of constant bit rate (CBR) traffic. These signals cycle through a complete handshake for every CBR cell transmission. When the external CBR source has loaded the CBR data into a predefined cell buffer in the packet memory, (the location of which is programmed in the SARA-S registers CBR_ADDR_HI and CBR_ADDR_LO), it drives the signal CBRXMIT active. The SARA-S senses this signal and at the next opportunity drives the CBRDONE signal low. The external logic may de-assert the CBRXMIT signal after the CBRDONE signal is driven high by SARA-S. After the cell has been loaded into the payload buffer, the SARA-S asserts the CBRDONE signal. The interface is then ready for the next CBR transmission. Figure 3-16 shows the constant bit rate interface timings.

CBR traffic can also be initiated using a software accessible mode bit (SEND_CBR) in the SARA-S. When the SEND_CBR bit is set, a CBR cell is transferred. The SEND_CBR bit gets automatically cleared after a successful CBR cell transfer (the software may poll if required). In addition, a maskable interrupt bit will be set.

The CBR buffer location in the packet memory could be mapped onto a real FIFO. The CBR data is stored in the buffer as a VC table entry pointer followed by the 48-bytes of payload. The VC pointer is used to fetch the four-byte cell header information from the VC table in the control memory. The 4-byte header, the header checksum, and the 48-byte payload are used to compose the 53-byte cell, which is then transferred to the cell interface

3.3.6.2 SARA-R

Any virtual circuit can be set up for CBR traffic. Cells received on these VCs are treated as CBR cells. The VC setup is described in section 7.3. When the SARA-R receives a cell on a CBR VC, the cell is loaded (header and payload) into a programmable circular chain of buffers in the packet memory. The circular chain of buffers is constructed by programming the SARA-R registers CBR_FIF_ST_ADR, CBR_FIF_ED_ADR, CBR_FIF_RD_PTR and CBR_FIF_-WR_PTR. While this circular queue is not empty, the SARA-R has an output signal CBRMT*, which is driven high. This signal could be used to trigger the CBR receive logic to read the data from the circular buffers.

The destination of the CBR data could also be a real FIFO. To accomplish this, all the above defined CBR registers could be loaded with the location FIFO in the packet memory address space. This will result in the full and empty conditions to be active at same time. To prevent the SARA-R from responding to the full condition and dropping CBR cells, the IGNCBRFL bit in the mode register of the SARA-R could be set to a "1", thus ignoring the full condition of the circular buffer.

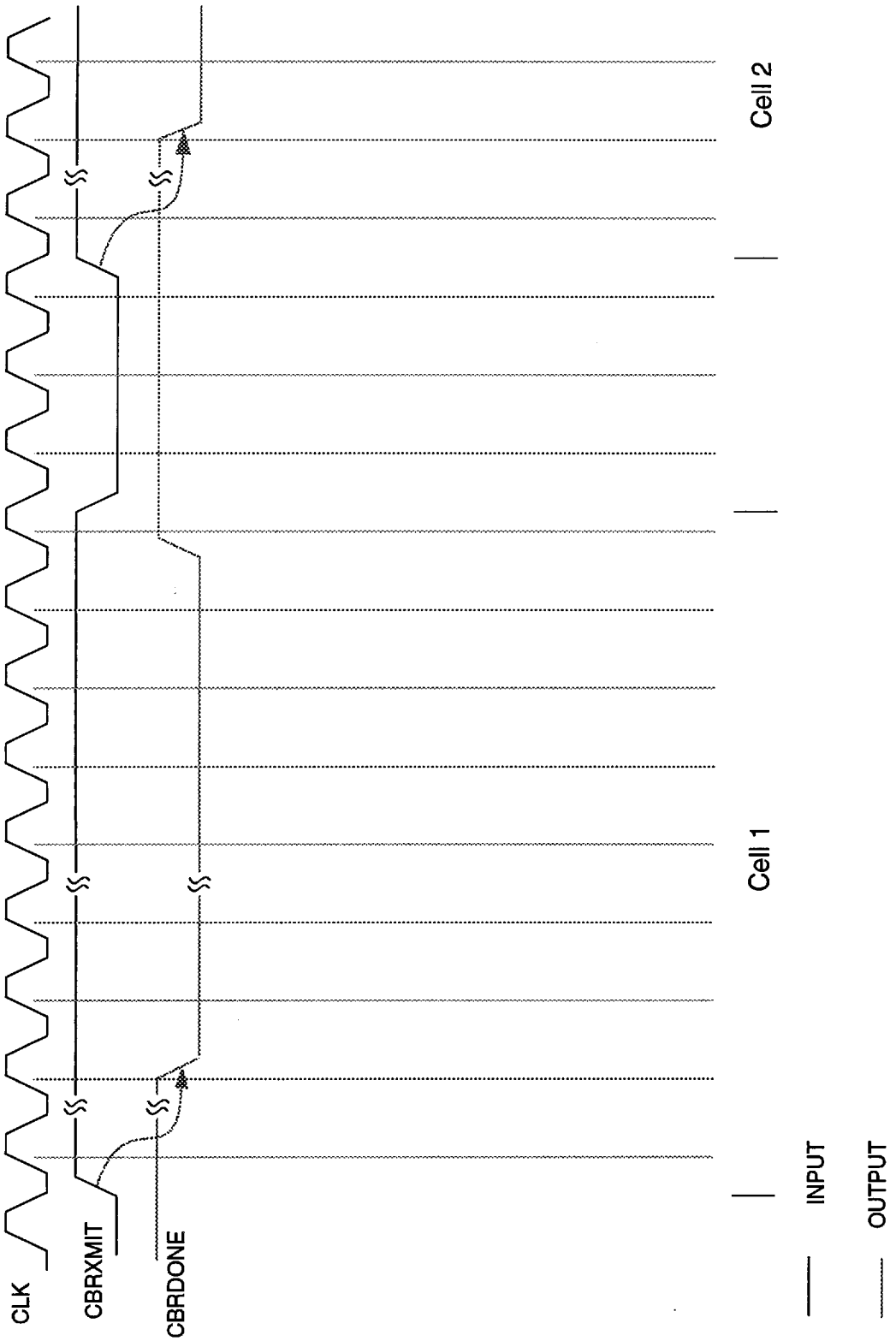


Figure 3-16. Constant Bit Rate Interface—SARA-S

3.3.7 Cross Reference by Pin Name (SARA-S)

Processor Interface		Control Memory Interface		Control Memory Interface (cont'd)		Packet Memory Interface (cont'd)		Cell Interface	
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
D15	130	CD17	32	CA5	75	PD9	198	FFD17	95
D14	131	CD16	33	CA4	76	PD8	199	FFD16	96
D13	132	CD15	34	CA3	77	PD7	200	FFD15	97
D12	133	CD14	36	CA2	78	PD6	201	FFD14	98
D11	134	CD13	37	CA1	79	PD5	202	FFD13	99
D10	135	CD12	38	CMULR	29	PD4	203	FFD12	100
D9	136	CD11	39	CREQ	31	PD3	205	FFD11	101
D8	139	CD10	40	CGRT	23	PD2	206	FFD10	102
D7	140	CD9	41	CWRT	28	PD1	207	FFD9	103
D6	141	CD8	42	CCYCST*	30	PD0	208	FFD8	105
D5	142	CD7	43	CRDY*	24	PA15	1	FFD7	106
D4	143	CD6	46			PA14	2	FFD6	107
D3	144	CD5	47	**Packet Memory Interface**		PA13	3	FFD5	108
D2	145	CD4	48			PA12	4	FFD4	109
D1	146	CD3	49	PD35	166	PA11	5	FFD3	110
D0	147	CD2	50	PD34	167	PA10	6	FFD2	111
A7	149	CD1	51	PD33	168	PA9	8	FFD1	112
A6	150	CD0	52	PD32	169	PA8	9	FFD0	113
A5	151	CA23	54	PD31	170	PA7	10	CELAVL*	94
A4	152	CA22	55	PD30	171	PA6	11	RDCLK	91
A3	153	CA21	56	PD29	173	PA5	12	RDEN	89
A2	154	CA20	57	PD28	174	PA4	13	XON	80
A1	155	CA19	58	PD27	175	PA3	14	**CBR Interface**	
A0	156	CA18	59	PD26	176	PA2	15		
WRT	119	CA17	60	PD25	177	PA1	16	CBRXMIT	117
DS*	120	CA16	61	PD24	178	PA0	17	CBRDONE	114
CS*	121	CA15	64	PD23	179	PREQ	162		
INTR*	129	CA14	65	PD22	180	PGRT	158	**Congestion Control Interface**	
RDY*	128	CA13	66	PD21	181	PCYCST*	163		
		CA12	67	PD20	182	PRDY*	159	CCDATA	87
		CA11	68	PD19	186	PLWADR	160	CCXFER	86
		CA10	69	PD18	187	PAMTCH	164	CCHLD	88
		CA9	70	PD17	188				
		CA8	71	PD16	189			**Miscellaneous Signals**	
		CA7	73	PD15	190				
		CA6	74	PD14	191			RST*	118
				PD13	192			CLK	124
				PD12	193			TE	21
				PD11	196			SI	20
				PD10	197			SO	157
								TEI	22

Table 3-17. Cross Reference by Pin Name for SARA-S

Table 3-17 gives a cross reference by pin name for SARA-S. The signals have been classified by the nature of the hardware interface with which they are associated, following the organization of the previous sections.

3.3.8 SARA-S Pin Configuration

Figure 3-17 shows a diagram of the 208-pin PQFP configuration for SARA-S

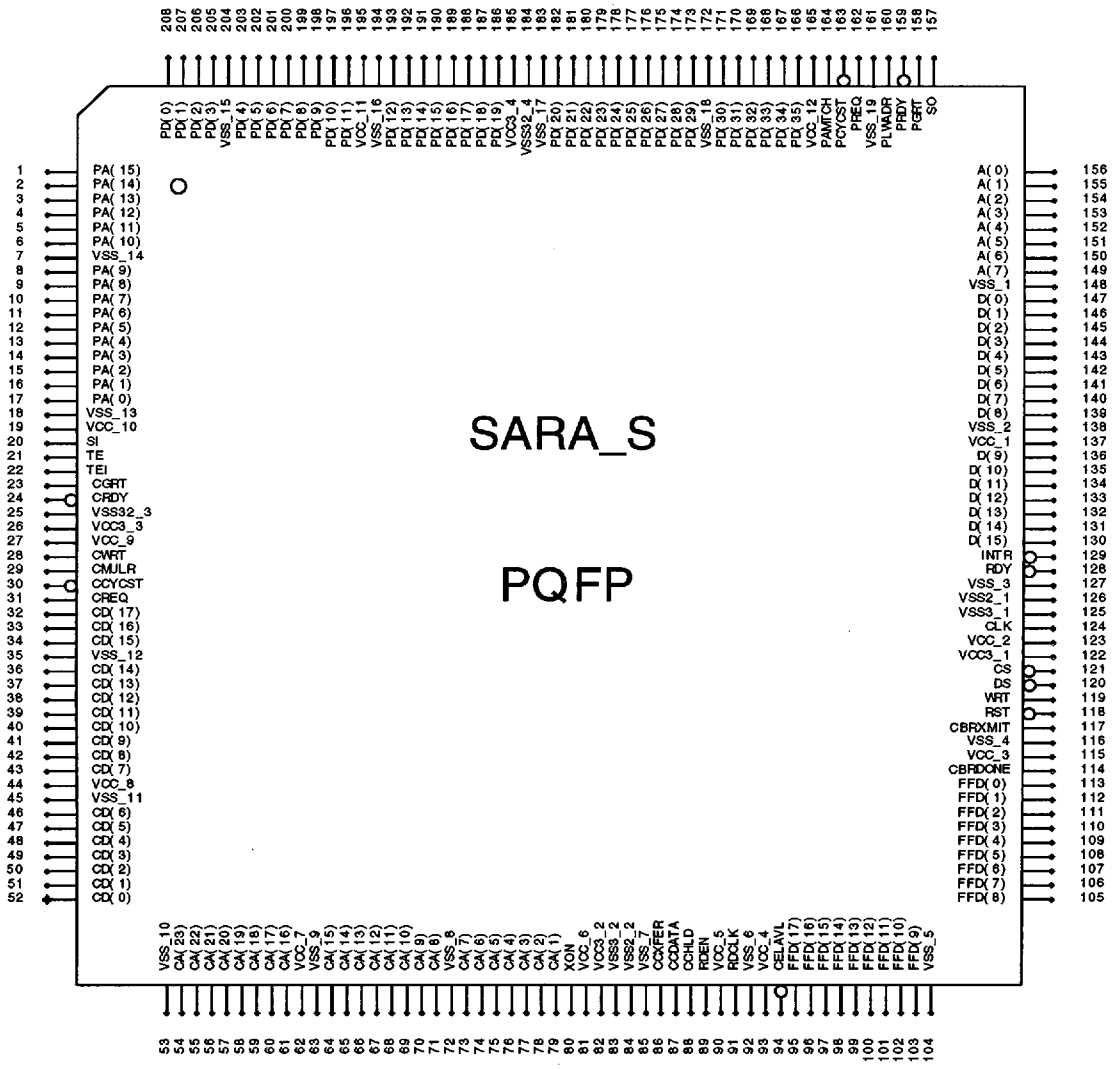


Figure 3-17. 208-pin PQFP Pin Configuration—SARA-S

Processor Interface		Control Memory Interface		Control Memory Interface (cont'd)		Packet Memory Interface (cont'd)		Cell Interface	
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
CS*	36	CREQ	95	CD12	89	PD35	200	FFRD3	110
DS*	37	CMULR	96	CD11	87	PD34	199	FFRD2	109
WRT	38	CGRT	101	CD10	86	PD33	198	FFRD1	108
RDY*	29	CCYCST*	97	CD9	85	PD32	197	FFRD0	107
A7	8	CRDY*	102	CD8	84	PD31	196	FFSL1	112
A6	7	CWRT	98	CD7	83	PD30	195	FFSL0	111
A5	6	CA23	71	CD6	82	PD29	192	FFD17	131
A4	5	CA22	70	CD5	81	PD28	191	FFD16	130
A3	4	CA21	69	CD4	80	PD27	190	FFD15	129
A2	3	CA20	68	CD3	79	PD26	189	FFD14	128
A1	2	CA19	67	CD2	78	PD25	188	FFD13	127
A0	1	CA18	66	CD1	73	PD24	187	FFD12	126
D15	27	CA17	65	CD0	72	PD23	186	FFD11	125
D14	26	CA16	64	**Packet Memory Interface**		PD22	185	FFD10	124
D13	25	CA15	62			PD21	184	FFD9	123
D12	24	CA14	61	PREQ	203	PD20	180	FFD8	122
D11	23	CA13	60	PGRT	207	PD19	179	FFD7	121
D10	22	CA12	59	PCYCST*	202	PD18	178	FFD6	120
D9	21	CA11	58	PRDY*	206	PD17	177	FFD5	119
D8	18	CA10	57	PLWADR	205	PD16	176	FFD4	118
D7	17	CA9	56	PAMTCH	201	PD15	175	FFD3	117
D6	16	CA8	55	PA15	156	PD14	174	FFD2	116
D5	15	CA7	54	PA14	155	PD13	173	FFD1	115
D4	14	CA6	53	PA13	154	PD12	172	FFD0	114
D3	13	CA5	50	PA12	153	PD11	169	CLAV	103
D2	12	CA4	49	PA11	152	PD10	168	FFMT	104
D1	11	CA3	48	PA10	151	PD9	167	FFLUSH	106
D0	10	CA2	47	PA9	149	PD8	166	FLSHDONE	105
INTR*	28	CA1	46	PA8	148	PD7	165	**Congestion Control Interface**	
Miscellaneous Signals		NC	45	PA7	147	PD6	164		
		CD17	94	PA6	146	PD5	163	CCHLD	40
CBRMT*	42	CD16	93	PA5	145	PD4	162	CCXFER	44
RST*	39	CD15	92	PA4	144	PD3	160	CCDATA	43
CLK	33	CD14	91	PA3	143	PD2	159		
TE	136	CD13	90	PA2	142	PD1	158		
SI	137			PA1	141	PD0	157		
SO	208			PA0	140				
TEI	135								

Table 3-18. Cross Reference by Pin Name for SARA-R

3.3.9 Cross Reference by Pin Name (SARA-R)

Table 3-18 gives a cross reference by pin name for SARA-R. The signals have been classified by the nature of the hardware interface with which they are associated, following the organization of the previous sections

3.3.10 SARA-R Pin Configuration

Figure 3-18 shows a diagram of the 208-pin PQFP configuration for SARA-R

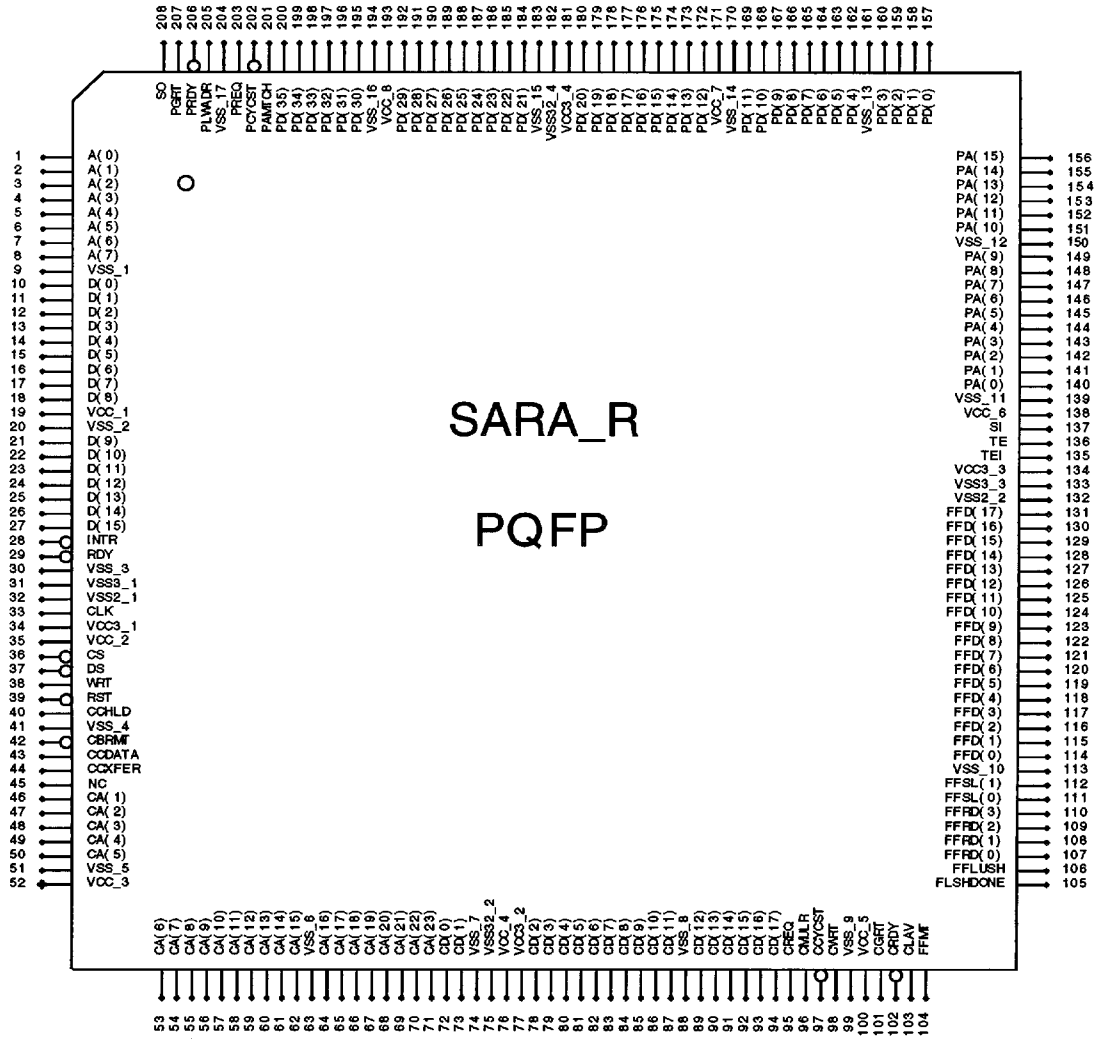
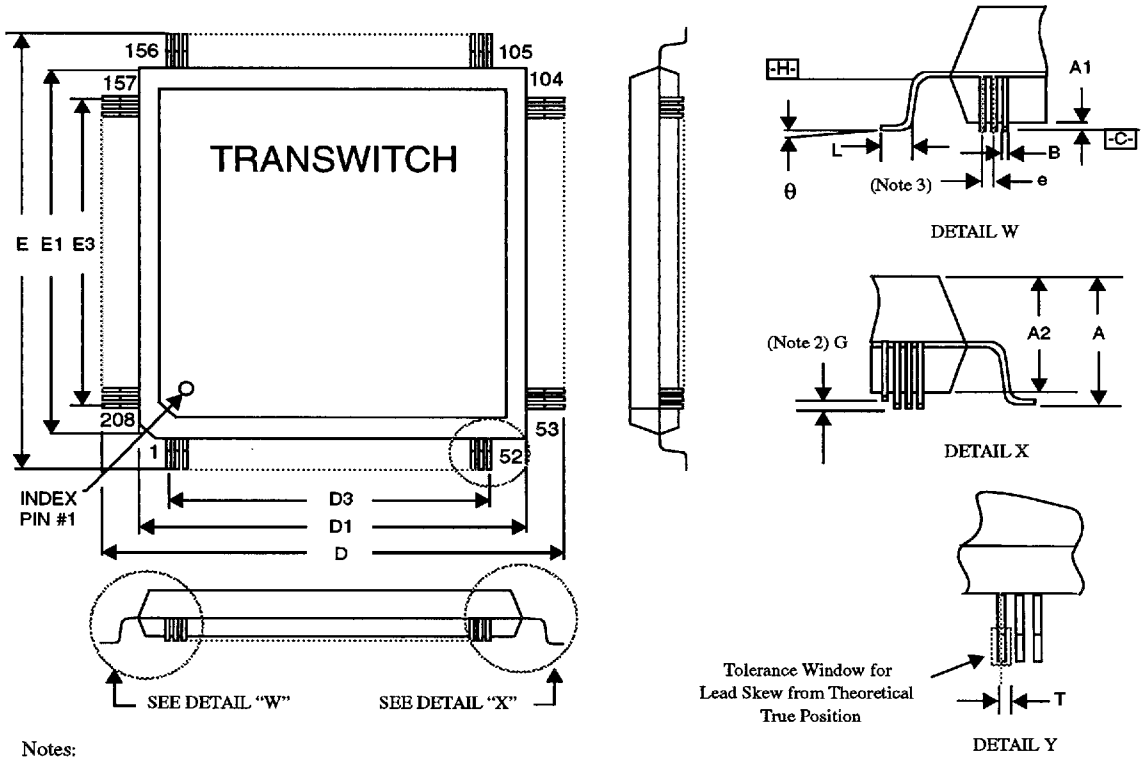


Figure 3-18. 208-pin PQFP Pin Configuration—SARA-R

3.3.11 SARA Packaging Dimensions

Figure 3-19 shows the dimensions of the SARA packaging.



Notes:

1. Controlling dimension - millimeter.
2. Coplanarity of all leads shall be within 0.1 mm (difference between the highest and lowest lead with seating plane -C- as reference).
3. Lead pitch determined at datum -H-.

Figure 3-19. SARA Packaging

A	Max	3.86	D1	Min	27.90	θ	Min	0°
A1	Min	0.25		Max	28.10		Max	5°
	Max	0.36	D3	Ref	25.50	L	Min	0.40
A2	Min	3.30	E	Min	30.40		Max	0.60
	Max	3.50		Max	30.80	G	Max	0.076
B	Min	0.18	E1	Min	27.90	T	Max	0.10
	Max	0.28		Max	28.10			
D	Min	30.40	E3	Ref	25.50			
	Max	30.80	e	BSC	0.50			

Table 3-19. SARA Packaging Dimensions

3.4 DC Characteristics

Based on the temperature and supply voltage given below, Table 3-20 shows the DC Characteristics. Table 3-21 shows the capacitance characteristics.

Temperature, T_A 0 C to 70 C

Supply Voltage V_{CC} 4.75 V to 5.25

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=Max		0.4	V
V_{OH}	Output High Voltage	$I_{OH}=I_{OL}$	2.4		V
I_{OL}(open drain outputs)	Output Low Current			8.0	mA
I_{OL}(all other outputs)	Output Low Current			4.0	mA
I_{OH}	Output High Current			I_{OL}	mA
I_{OZ1}	Output Leakage Current	0.4V <V_{OUT} <V_{CC}	-10	10	µA
I_{OZ2}	Bi-Directional Tri-State I/O Output Leakage Current	V_{OH} =V_{SS} or V_{CC}	-350	10	µA
I_{IX}	Input Leakage Current	0V <V_{IN} <V_{CC}	35	350	µA
I_{CC}	Power Supply Current	V_{CC}=Max. f(CLK)=20 MHz		400	mA

Table 3-20. SARA DC Characteristics Over Commercial Operating Ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Pins[1]			10	pF
$C_{I/O}$	Bidirectional pins			10	pF
Output Drive Capability	Microprocessor Outputs			100	pF
	All Other Outputs			50	pF

Table 3-21. SARA Capacitance Characteristics

1. Unused input pins must be tied to inactive state.

3.5 AC Characteristics

3.5.1 Switching Characteristics

Table 3-5 shows the switching characteristics of both the SARA-R and SARA-S timings over commercial operating conditions.

Symbol	Parameter	Mln.	Max	Units
T1	Clock Period	50		ns
T2	Clock High	20		ns
T3	Clock Low	20		ns
T4	CCHLD to CLK Setup (SARA-R)	9		ns
T5	CLK to CCHLD Hold (SARA-R)	2		ns
T6	CLK to CCHLD Valid (SARA-S)		24	ns
T7	CCXFER to CLK Setup (SARA-S)	0		ns
T8	CLK to CCXFER Hold (SARA-S)	4		ns
T9	CLK to CCXFER Valid (SARA-R)		22	ns
T10	CCDATA to CLK Setup (SARA-S)	0		ns
T11	CLK to CCDATA Hold (SARA-S)	5		ns
T12	CLK to CCDATA Valid (SARA-R)		22	ns
T13	CBRXMIT to CLK Setup (SARA-S)	Async.		ns
T14	CLK to CBRXMIT Hold (SARA-S)	Async.		ns
T15	CLK to CBRDONE Valid (SARA-S)		19	ns
T16	CLK to CBRMT* Valid (SARA-R)		19	ns
T21	WRT, A(7:0), D(15:0) to CS*, DS* Setup	0		ns
T22	CS*, DS* to WRT, A(7:0), D(15:0) Hold	0		ns
T23	CS*, DS* to RDY* Low		(3*T1 + 21)	ns
T24	CS*, DS* to RDY* Deasserted		14	ns
T25	CS*, DS* to D(15:0) Enabled (Read)	0		ns
T26	D(15:0) to RDY* Setup		(T1 - 32)	ns
T27	CS*, DS* to D(15:0) Deasserted (Read)		20	ns

Table 3-22. Switching Characteristics over Commercial Operating Conditions

Symbol	Parameter	Mln.	Max	Units
T28	CS*, DS* High	(1.5 * T1)		ns
T29	INTR* High	(4 *T1 - 24)		ns
T30	RST* Low	(3*T1 + 5)		ns
T31	CLAV to CLK Setup (SARA-R)	0		ns
T32	CLK to CLAV Hold (SARA-R)	5		ns
T33	CLK to FFRD(0) Valid (SARA-R)		20	ns
T34	FFMT to CLK Setup (SARA-R)	8		ns
T35	CLK to FFMT Hold (SARA-R)	4		ns
T36	FFD(17:0) to CLK Setup (SARA-R)	0		ns
T37	CLK to FFD(17:0) Hold (SARA-R)	3		ns
T38	CLK to FFLUSH Valid (SARA-R)		25	ns
T39	FLSHDONE to CLK Setup (SARA-R)	4		ns
T40	CLK to FLSHDONE Hold (SARA-R)	5		ns
T41	RDCLK to CELAVL* Valid (SARA-S)		17	ns
T42	RDEN to RDCLK Setup (SARA-S)	13		ns
T43	RDCLK to RDEN Hold (SARA-S)	2		ns
T44	RDCLK to FFD(17:0) Valid (SARA-S)		25	ns
T45	RDCLK Period	T1		ns
T46	RDCLK Low	T3		ns
T47	RDCLK High	T2		ns
T51	CLK to CREQ Valid		24	ns
T52	CLK to CMULR Valid		24	ns
T53	CGRT to CLK Setup	1		ns
T54	CLK to CGRT Hold	4		ns
T55	CLK to CCYCST* Valid		20	ns
T56	CRDY* to CLK Setup	0		ns
T57	CLK to CRDY* Hold	4		ns
T58	CLK to CWRT Valid		24	ns
T59	CLK to CA(23:0) Asserted	0		ns

Table 3-22. Switching Characteristics over Commercial Operating Conditions

Symbol	Parameter	Min.	Max	Units
T60	CLK to CA(23:0) Valid		19	ns
T61	CLK to CA(23:0) Deasserted		26	ns
T62	CD(17:0) to CLK Setup (Read)	0		ns
T63	CLK to CD(17:0) Hold (Read)	3		ns
T64	CLK to CD(17:0) Asserted (Write)	0		ns
T65	CLK to CD(17:0) Valid (Write)		22	ns
T66	CLK to CD(17:0) Deasserted (Write)		22	ns
T71	CLK to PREQ Valid		22	ns
T72	PGRT to CLK Setup	8		ns
T73	CLK to PGRT Hold	3		ns
T74	CLK to PCYCST* Valid		20	ns
T75	PRDY* to CLK Setup	1		ns
T76	CLK to PRDY* Hold	4		ns
T77	CLK to PA(15:0) Asserted	0		ns
T78	CLK to PA(15:0) Valid		24	ns
T79	CLK to PA(15:0) Deasserted		24	ns
T80	CLK to PD(31:0) Asserted (PM Address)		27	ns
T81	CLK to PD(31:0) Deasserted		27	ns
T82	PD(35:0) to CLK Setup (SARA-S Read)	3		ns
T83	CLK to PD(35:0) HOld (SARA-S Read)	4		ns
T84	PLWADR to PA(15:0) Valid		18	ns
T85	CLK to PAMTCH Valid		27	ns
T86	CLK to PD(35:0) Valid (SARA-R Write)		27	ns
T87	CLK to PD(35:0) Deasserted (SARA-R Write)		27	ns

Table 3-22. Switching Characteristics over Commercial Operating Conditions

3.5.2 Interface Signal Timings

Figure 3-20 through Figure 3-28 show the timings for the congestion control interface, processor, cell interface, control memory interface, and packet memory interface for both the SARA-R and SARA-S.

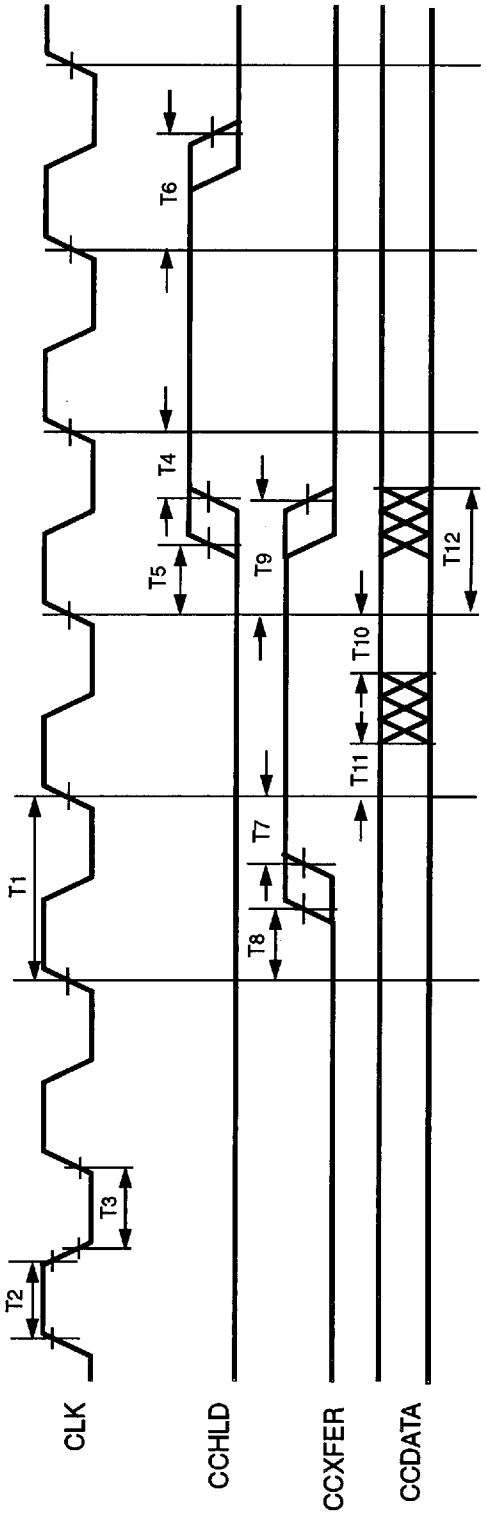


Figure 3-20. Congestion-Control Interface Signals Between the SARA-S and SARA-R

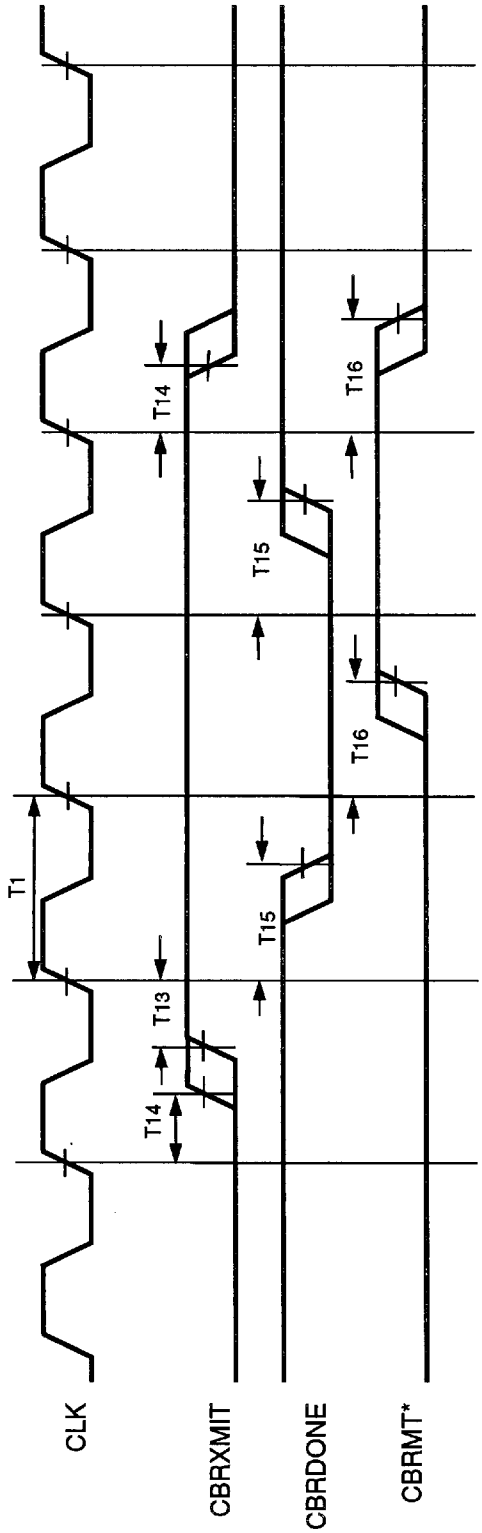


Figure 3-21. Constant Bit Rate Interface Signals of SARA-S & SARA-R

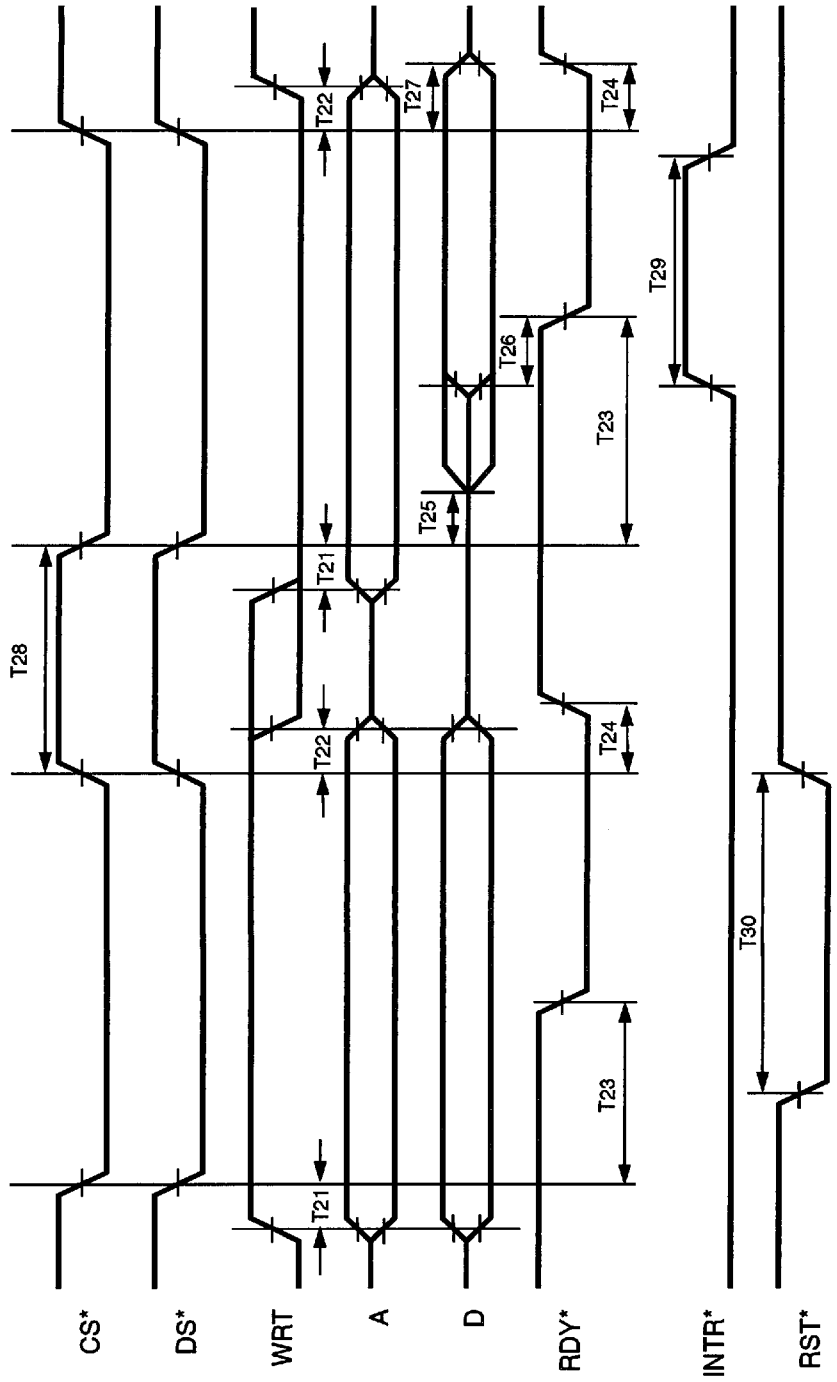


Figure 3-22. Processor-Interface Signal Timing

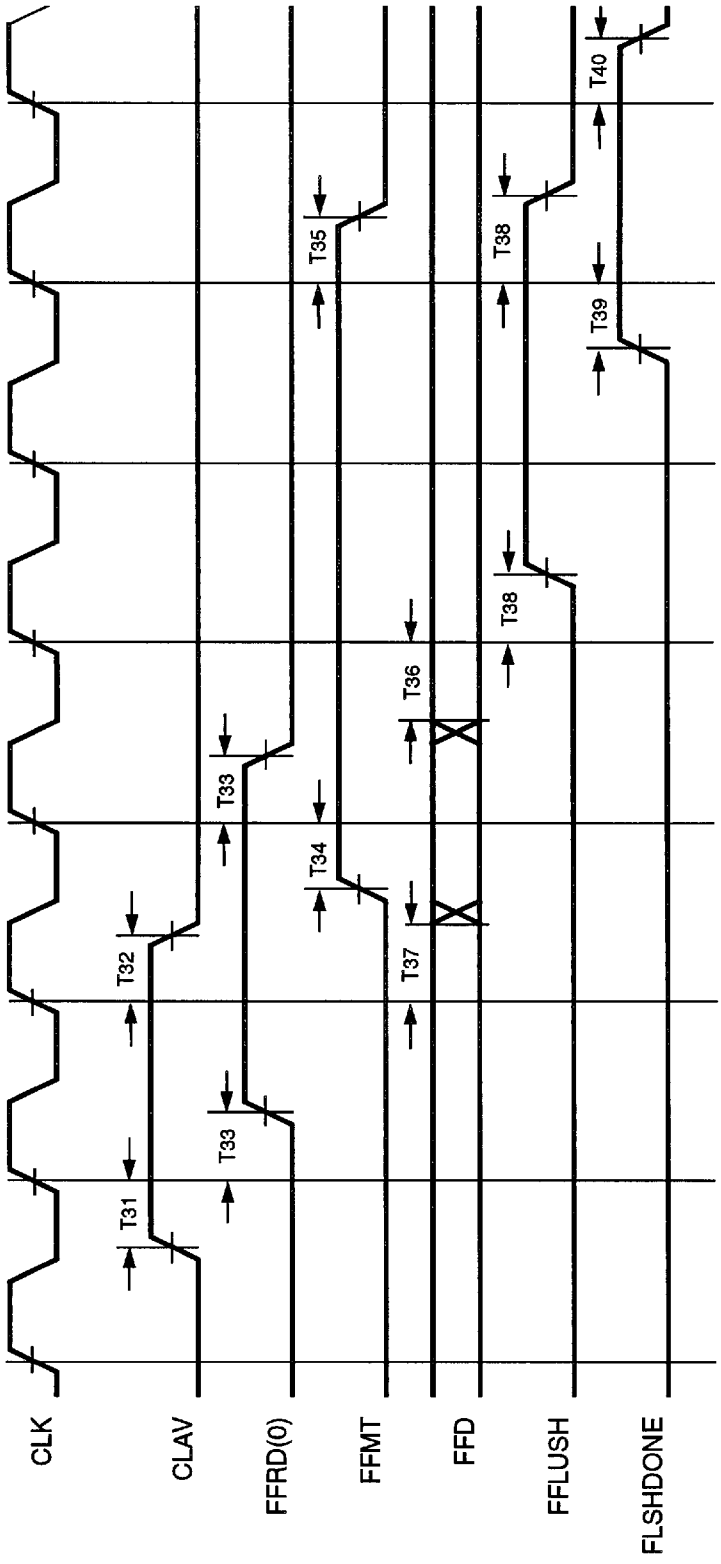
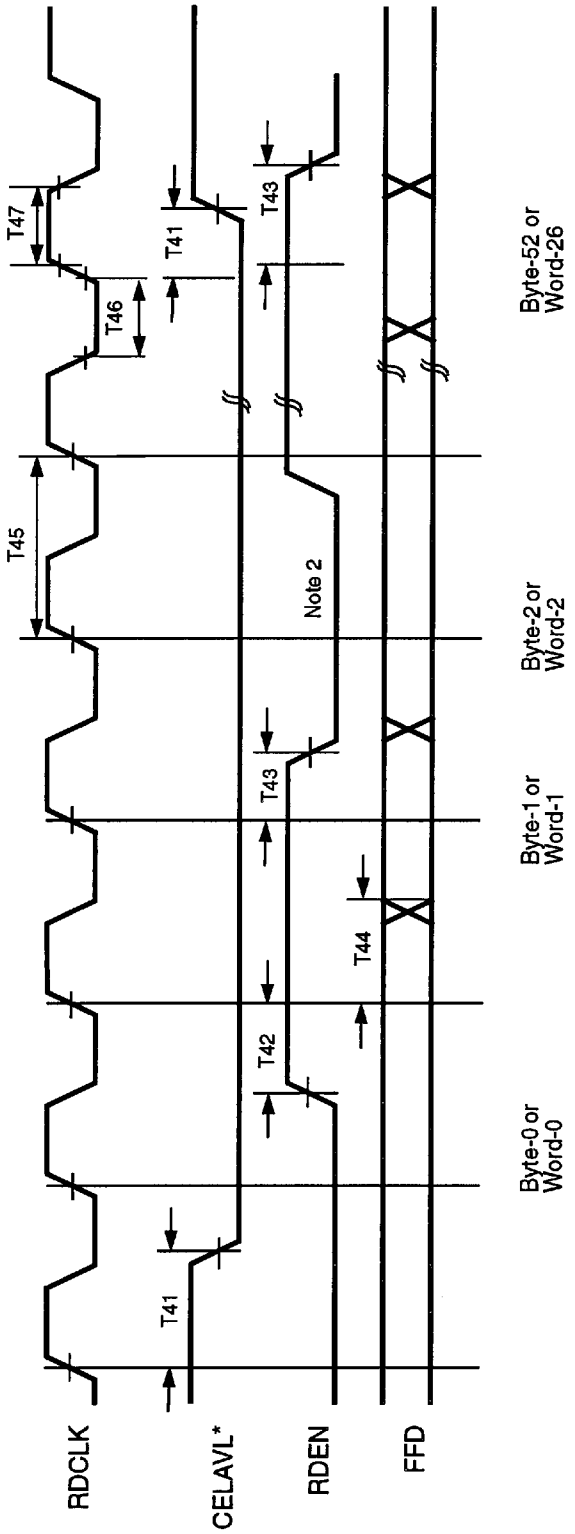
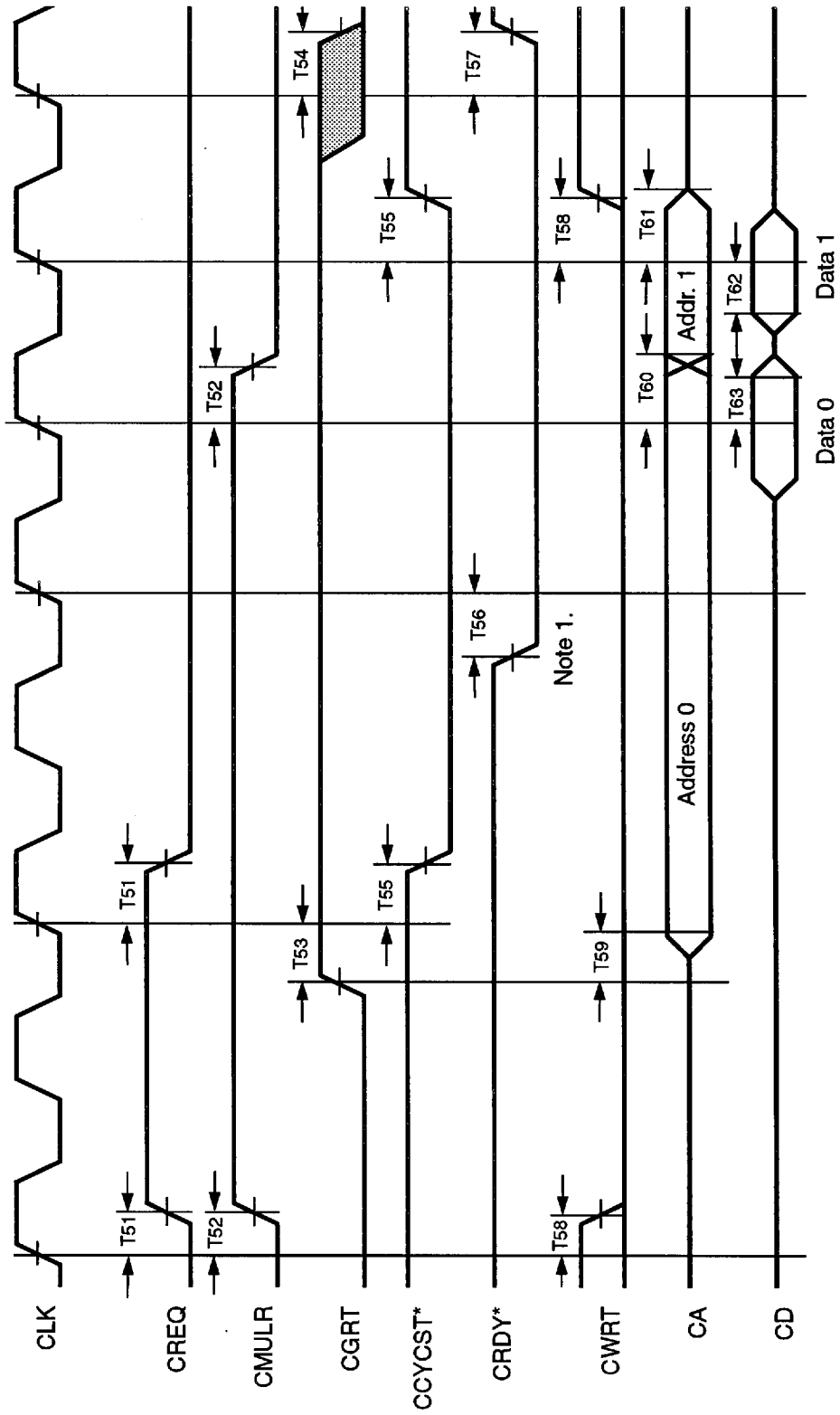


Figure 3-23. Cell-Interface Signals for the SARA-R



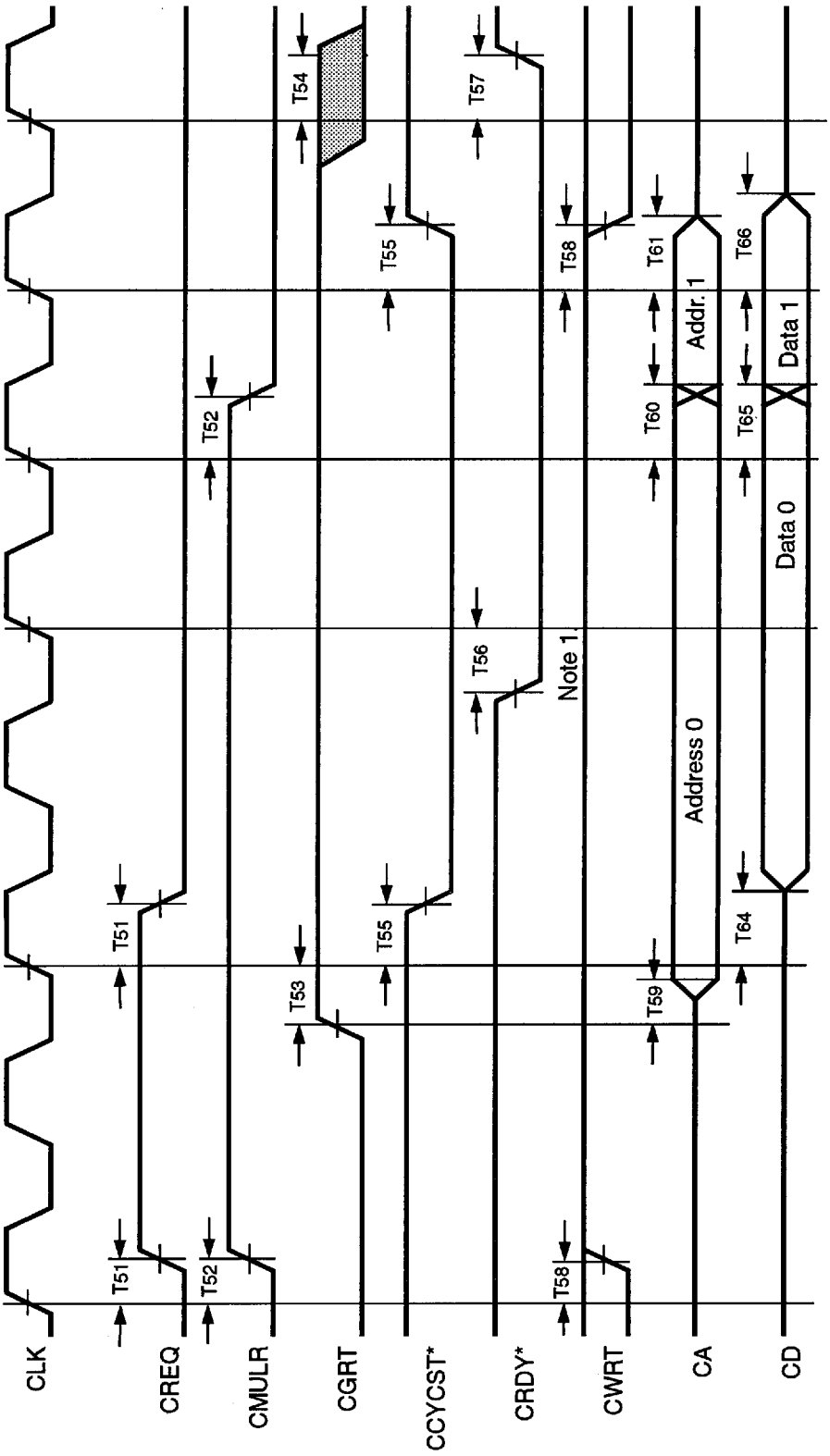
Note:
1. CELAVL* will be active for the entire cell transfer duration.
2. RDEN can be held false to temporarily freeze data transfer.

Figure 3-24. Cell-Interface Signals for the SARA-S



Note:
1. Data transfer does not occur on the very first clock cycle when CRDY becomes active.
2. Mode settings are:CM_WAIT_EN=1 and CM_EARLY_WR=0.

Figure 3-25. Control Memory Interface Signal Timing-Read Operation



Note:
1. Data transfer does not occur on the very first clock cycle when CRDY becomes active.
2. Mode settings are:CM_WAIT_EN=1 and CM_EARLY_WR=0.

Figure 3-26. Control Memory Interface Signal Timings-Write Operation

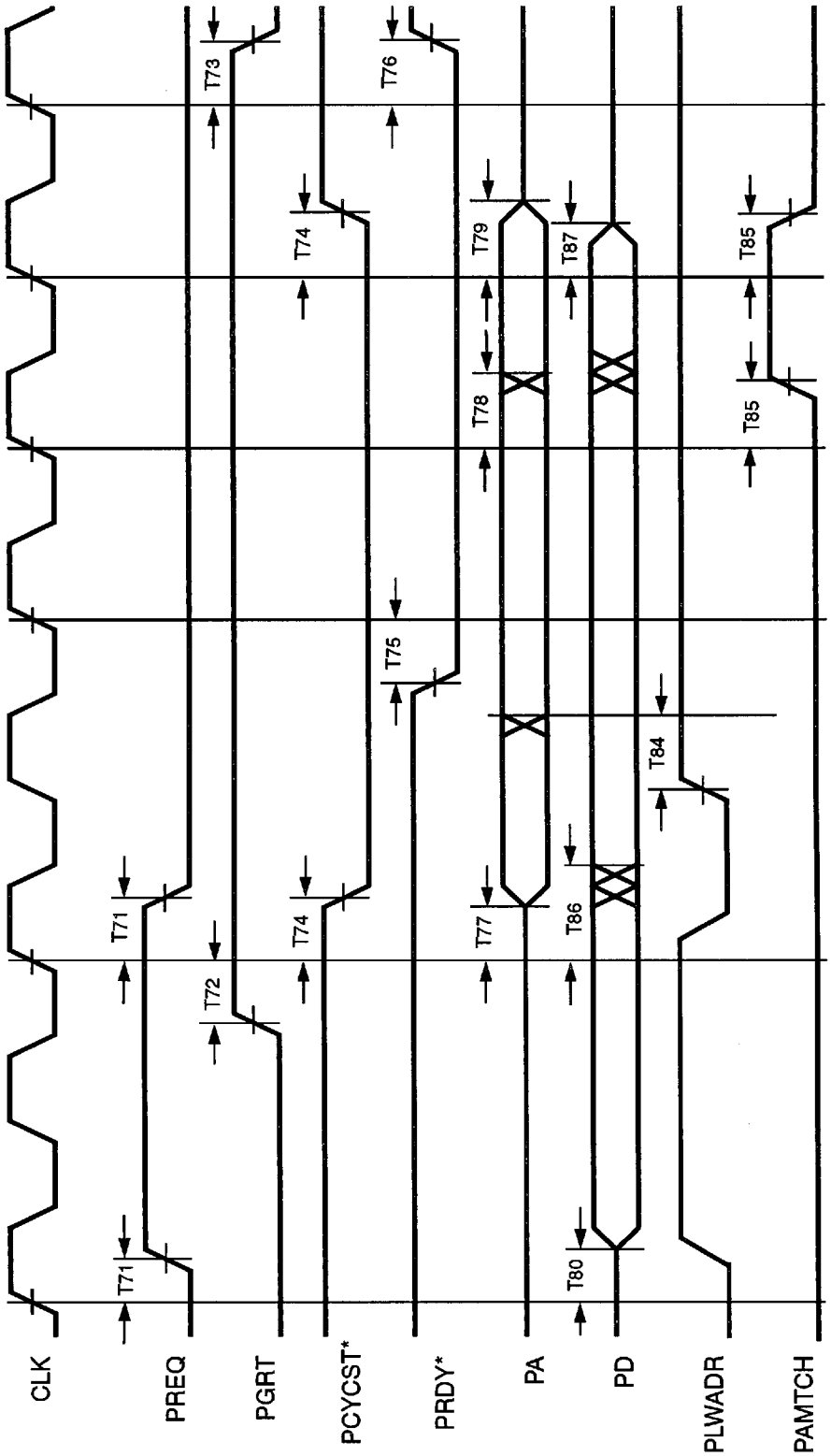


Figure 3-27. Packet Memory Interface Signal Timings-Write Operation for the SARA-R

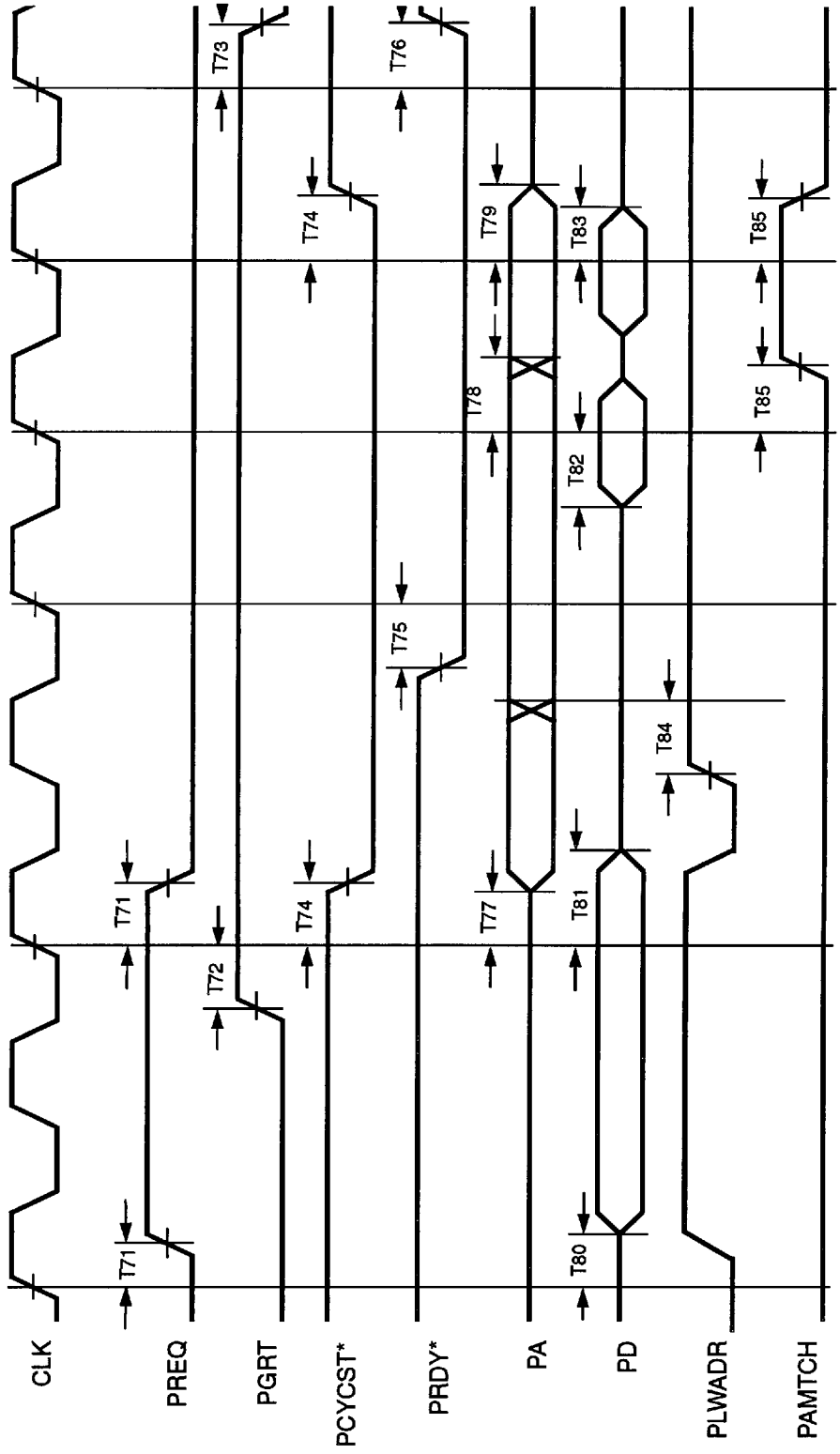


Figure 3-28. Packet Memory Interface Signal Timings-Read Operation for the SARA-S