PM5346

S/UNI™ 155-LITE

S/UNI-155-LITE

SATURN USER NETWORK INTERFACE 155.52 & 51.84 Mbit/s

Issue 6: March, 1996

CONTENTS

FEATURES

- Single chip ATM User-Network Interface operating at 155.52 and 51.84 Mbit/s. Also capable of operating at ATM Forum mid-range PHY subrates of 25.92 and 12.96 Mbit/s.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Processes duplex 155.52 Mbit/s STS-3c/STM-1 or 51.84 Mbit/s STS-1 data streams with on-chip clock and data recovery and clock synthesis.
- Provides Saturn Compliant Interface - PHYsical layer (SCI-PHY™) FIFO buffers in both transmit and receive paths with parity support.
- Inserts and extracts the generic flow control (GFC) bits via a simple serial interface and provides a transmit XOFF function to allow for local flow control.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power, +5 Volt, CMOS technology.
- 128 pin high performance plastic quad flat pack (PQFP) 14 mm x 20 mm package.

The receiver section:

- Provides a serial interface at 155.52 or 51.84 Mbit/s
- Recovers the clock and data; frames to the recovered data stream; descrambles the received data; interprets the received payload pointer (H1, H2); and extracts the STS-3c or STS-1 synchronous payload envelope (VC4) and path overhead.
- Extracts ATM cells from the synchronous payload envelope using ATM cell delineation and provides optional ATM cell payload descrambling, header check sequence (HCS) error detection and error correction, and idle/unassigned cell filtering.
- Provides a synchronous 8-bit wide, four cell FIFO buffer.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (AIS), line remote defect indication (RDI), loss of pointer (LOP), path alarm indication signal (AIS), loss of cell delineation and path RDI.

- Counts received section BIP-8 (B1) errors, received line BIP-8/24 (B2) errors, line far end block errors (FEBE), received path BIP-8 (B3) errors and path far end block errors (FEBE).

- Counts received HCS errored cells that are discarded, received HCS errored cells that are corrected and passed on, and the total received cells passed on.

The transmitter section:

- Provides a synchronous 8-bit wide, four cell FIFO buffer.

- Provides idle/unassigned cell insertion, HCS generation/insertion, and ATM cell payload scrambling; Inserts ATM cells into the transmitted STS-3c (STM-1) or STS-1 synchronous payload envelope using H4 framing

- Generates the transmit payload pointer (H1, H2) and inserts the path overhead; scrambles the transmitted STS-3c (STM-1) or STS-1 stream and inserts framing bytes (A1, A2) and the identity byte (C1).

- Synthesizes the 155.52 MHz, 51.84 MHz transmit clock from a one-eighth frequency reference.

- Provides a serial interface at 155.52 or 51.84 Mbit/s

- Inserts path alarm indication signal (AIS), path remote defect indication (RDI), line alarm indication signal (AIS) and line RDI.

- Inserts path BIP-8 codes (B3), path far end block error (FEBE) indications, line BIP-8/24 codes (B2), line far end block error (FEBE) indications, section BIP-8 codes (B1) to allow performance monitoring at the far end.

- Allows forced insertion of all zeros data (after scrambling) or corruption of framing byte or section, line, or path BIP-8 codes for diagnostic purposes.

APPLICATIONS

- Workstations and Personal Computers
- Switches and Hubs
- Routers
- SONET or SDH ATM Interfaces
- 155 and 51 Mbit/s UTP-5 ATM LANs
- 51, 25 and 13 Mbit/s UTP-3 ATM LANs

REFERENCES

- CCITT Recommendation G.709 - "Synchronous Multiplexing Structure", 1990.
- CCITT Recommendation I.432 - "B-ISDN User-Network Interface - Physical Interface Specification", June 1990.
- Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 1, December 1994.
- ATM Forum - ATM User-Network Interface Specification,V3.0, September 10, 1993
- T1.105, American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specifications (SONET), 1991
- ATM Forum 155 Mbit/s Physical Medium Dependent (PMD) Twisted Pair Copper Specification DRAFT (155-C5-UTP-PMD, Rev 0.2)

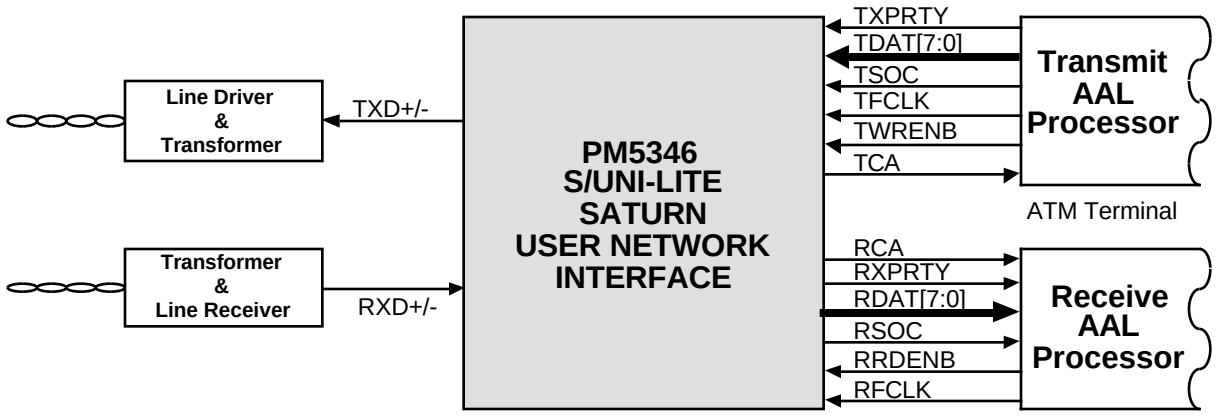
APPLICATION EXAMPLES

The PM5346 S/UNI-LITE is typically used to implement the core of an ATM User Network Interface by which an ATM terminal is linked to an ATM switching system using SONET/SDH compatible transport.

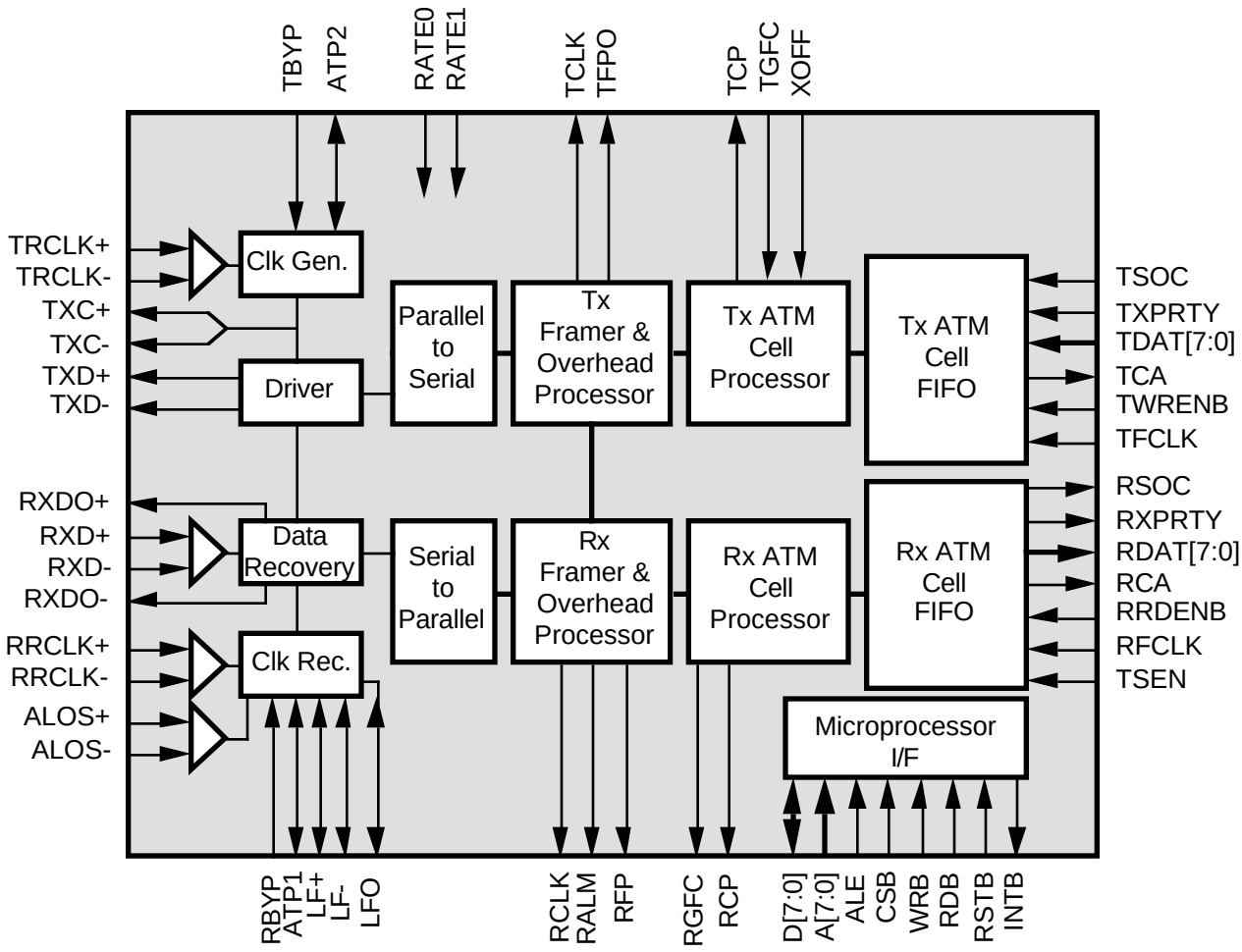
The S/UNI-LITE finds application at either end of terminal to switch links or switch to switch links, both in private network (LAN) and public network (WAN) situations. In this application, the S/UNI-LITE typically interfaces on its line side with a line receiver/equalizer and a line driver.

The S/UNI-LITE may be loop timed internally (the recovered clock is used in the transmit direction) or source timed (separate transmit and receive clocks). The drop side interfaces directly with ATM adaptation layer or ATM layer processors. The initial configuration and ongoing control and monitoring of the S/UNI-LITE is provided via a generic microprocessor interface. The S/UNI-LITE also supports a "hardware-only" operating mode where an external microprocessor is not required. This application is shown in Figure 1.

Fig. 1 Typical ATM Adapter Interface



BLOCK DIAGRAM



DESCRIPTION

The PM5346 S/UNI-LITE Saturn User Network Interface is a monolithic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of a 155 Mbit/s or 51Mbit/s ATM User Network Interface. It is fully compliant with both SONET and SDH requirements and ATM Forum UNI specifications.

The S/UNI-LITE receives SONET/SDH frames via a bit serial interface, recovers clock and data, and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (Z2, G1) are also accumulated. The S/UNI-LITE interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

The S/UNI-LITE frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. Generic flow control (GFC) bits from error free cells are extracted and presented on a serial link for external processing.

Legitimate ATM cells are written to a four cell FIFO buffer. These cells are read from the FIFO using a synchronous 8 bit wide datapath interface with cell-based handshake. Counts of received ATM cell headers that are errored and uncorrectable, those that are errored and correctable and all passed cells are accumulated independently for performance monitoring purposes.

The S/UNI-LITE transmits SONET/SDH frames via a bit serial interface and formats section, line, and path overhead appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (Z2, G1) are also inserted.

The S/UNI-LITE generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. It supports the insertion of a variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics.

ATM cells are written to an internal programmable-length 4-cell FIFO using a synchronous 8 bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell or the XOFF input is asserted. Generic flow control (GFC) bits may be inserted downstream of the FIFO

via a serial link so that all FIFO latency may be bypassed. A Transmission Off (XOFF) input is provided to allow the suspension of active ATM cell transmission independent of the FIFO fill state.

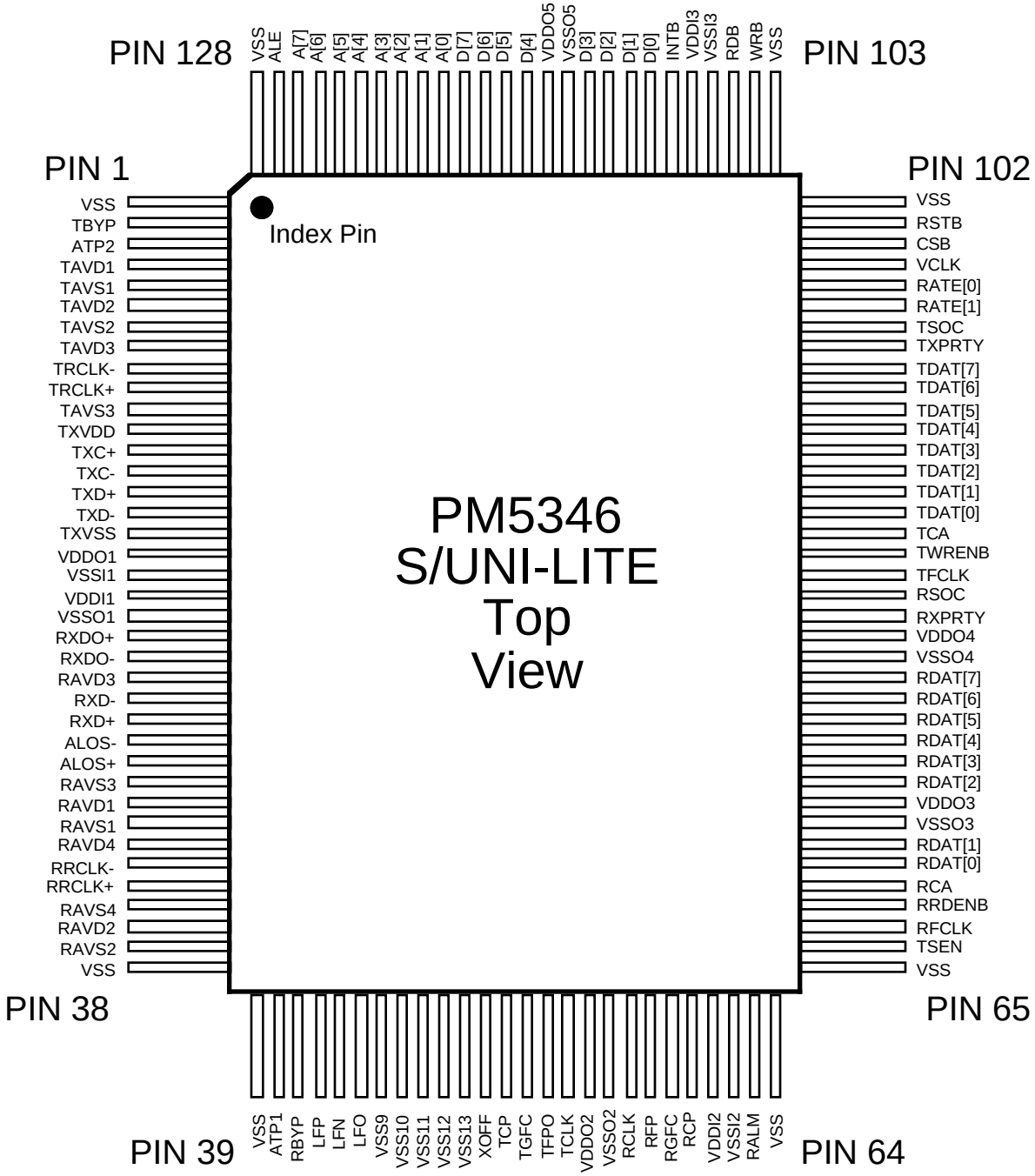
The S/UNI-LITE generates of the header check sequence and scrambles the payload of the ATM cells. Payload scrambling can be disabled.

No line rate clocks are required directly by the S/UNI-LITE as it synthesizes the transmit clock and recovers the receive clock using a 19.44 MHz or 6.48 MHz reference clock.

The S/UNI-LITE is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. It is implemented in low power, +5 Volt CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and TTL compatible outputs and is packaged in a 128 pin PQFP package.

PIN DIAGRAM

The S/UNI-LITE is packaged in an 128 pin PQFP package having a body size of 14mm by 20 mm and a pin pitch of 0.50 mm.



PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
RATE1 RATE0	Input	97 98	The RATE1 and RATE0 inputs select the frame format and line rate for both transmit and receive: RATE[1:0] 11 155.52 Mbit/s, STS-3c/STM-1 transmission convergence (TC) 10 51.84 Mbit/s, STS-1 TC 01 25.92 Mbit/s, STS-1 TC 00 12.96 Mbit/s, STS-1 TC The RATE1 and RATE0 inputs have integral pull up resistors so the default is STS-3c/STM-1.
RBYP	Input	41	The receive bypass (RBYP) input must be tied low for proper operation. RBYP has an integral pull down resistor.
RXD+ RXD-	PECL Input	26 25	The receive differential data inputs (RXD+, RXD-) contain the NRZ bit serial receive stream. The receive clock is recovered from the RXD+/- bit stream. RXD+/- must be connected to a differential data source, single-ended operation is not supported for these inputs.
RXDO+ RXDO-	Output	22 23	The receive differential data outputs (RXDO+, RXDO-) are provided to allow decision feedback equalization (DFE) to correct baseline wander. It is intended that these outputs be low pass filtered and attenuated to create an appropriate correction signal that is summed with incoming data to recover the D.C. component. RXDO+/- are retimed (sampled by the recovered clock) versions of the RXD+ and RXD- inputs. RXDO+/- are squelched (RXDO+ is forced low and RXDO- is forced high) when loss of signal (ALOS+/-) is asserted.
RRCLK+ RRCLK-	PECL Input	34 33	The receive differential reference clock inputs (RRCLK+, RRCLK-) contain a jitter-free 19.44 MHz or 6.48 MHz reference clock.

ALOS+ ALOS-	PECL Input	28 27	The analog loss of signal (ALOS+/-) differential inputs are used to indicate a loss of receive signal power. When ALOS+/- is asserted, the data on the receive data (RXD+/-) pins will be squelched and the phase locked loop shall switch to the reference clock (RRCLK+/-) to keep the recovered clock in range. These inputs must be DC coupled.
RCLK	Output	57	The receive clock (RCLK) output provides a timing reference for S/UNI-LITE receive outputs. RCLK is a divide by eight of the recovered clock. RGFC, RCP, RFP and RALM are updated on the rising edge of RCLK.
RALM	Output	63	The receive alarm (RALM) output indicates the state of the receive framing. RALM is low if no receive alarms are active. RALM is high if line AIS, path AIS, loss of signal (LOS), loss of frame (LOF), loss of pointer (LOP) or loss of cell delineation (LCD) is detected. RALM is updated on the rising edge of RCLK.
RFP	Output	58	The receive frame pulse (RFP) output is an 8 kHz signal derived from the receive line clock. RFP pulses high for one RCLK cycle every 2430 RCLK cycles for STS-3c (STM-1) TC mode or every 810 RCLK cycles for STS-1 TC mode. RFP is updated on the rising edge of RCLK.
TBYP	Input	2	The transmit bypass (TBYP) input must be tied low for proper operation. TBYP has an integral pull down resistor.
TRCLK+ TRCLK-	PECL Input	10 9	The transmit differential reference clock inputs (TRCLK+, TRCLK-) are a jitter-free 19.44 MHz or 6.48 MHz reference clock. This clock provides timing for the S/UNI-LITE transmit functions. TRCLK+/- may be left unconnected when S/UNI-LITE loop timing is enabled (using the S/UNI-LITE Master Control Register).
TXD+ TXD-	Output	15 16	The transmit differential data/positive pulse outputs (TXD+, TXD-) contain NRZ encoded data. TXD+/- is updated on the falling edge of TXC+/-

TXC+ TXC-	Output	13 14	The transmit clock (TXC+, TXC-) outputs are available when the transmit data rate is 51.84 Mbit/s or less. TXD+/- is updated on the falling edge of TXC+ and on the rising edge of TXC-. When STS-3c TC mode is selected, TXC+ is held low and TXC- is held high.
TFPO	Output	53	The active high framing position output (TFPO) signal is an 8 kHz timing marker for the transmitter. TFPO pulses high for one TCLK cycle every 2430 TCLK cycles for STS-3c (STM-1) TC mode or every 810 RCLK cycles for STS-1 TC mode. TFPO is updated on the rising edge of TCLK.
TSEN	Input	66	The tristate enable (TSEN) input selects the configuration of the receive datapath (RDAT[7:0], RSOC). When TSEN is tied high, RDAT[7:0] operates as a tristate bus controlled by RRDENB. When RRDENB is high upon RFCLK rising, RDAT[7:0], RXPRTY and RSOC are tristated. When RRDENB is low upon RFCLK rising, RDAT[7:0], RXPRTY and RSOC are enabled. When TSEN is tied low, RDAT[7:0], RXPRTY and RSOC are always enabled, regardless of the state of RRDENB. TSEN has an integral pull down resistor.
RFCLK	Input	67	The receive read clock (RFCLK) is used to read ATM cells from the receive FIFO. RFCLK must cycle at a 33 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow. RRDENB is sampled using the rising edge of RFCLK. RSOC, RDAT[7:0], RXPRTY and RCA are updated on the rising edge of RFCLK

RRDENB	Input	68	The active low receive read enable input (RRDENB) is used to initiate reads from the receive FIFO. When sampled low using the rising edge of RFCLK, a byte is read from the internal synchronous FIFO and output on bus RDAT[7:0] if one is available. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[7:0] and RSOC is tristated if the TSEN input is high. RRDENB must operate in conjunction with RFCLK to access the FIFO at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDENB at anytime it is unable to accept another byte. When the RCA signal is configured to be deasserted with zero octets (as opposed to four) in the FIFO, it is not an error condition to hold the read enable (RRDENB) active. In this situation, the RCA signal identifies the valid octets.
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7]	Tristate Output	70 71 74 75 76 77 78 79	The receive cell data (RDAT[7:0]) bus carries the ATM cell octets that are read from the receive FIFO. RDAT[7:0] is updated on the rising edge of RFCLK and is tristated when not valid if the TSEN input is high. The RDAT[7:0] bus is always driven when TSEN is low, regardless of the level of RRDENB.
RXPRTY	Tristate Output	82	The receive parity (RXPRTY) signal indicates the parity of the RDAT[7:0] bus. Odd or even parity selection can be made using a register. RXPRTY is updated on the rising edge of RFCLK and is tristated when not valid if the TSEN input is high. RXPRTY is always driven when TSEN is low, regardless of the level of RRDENB.
RSOC	Tristate Output	83	The receive start of cell (RSOC) signal marks the start of cell on the RDAT[7:0] bus. When RSOC is high, the first octet of the cell is present on the RDAT[7:0] stream. RSOC is updated on the rising edge of RFCLK and is tristated when not valid if the TSEN input is high. RSOC is always driven when TSEN is low, regardless of the level of RRDENB.

RCA	Output	69	The receive cell available (RCA) signal indicates when a cell is available in the receive FIFO. RCA can be configured to be deasserted when either zero or four bytes remain in the FIFO. RCA is updated on the rising edge of RFCLK. The active polarity of this signal is programmable and defaults to active high.
RGFC	Output	59	The receive generic flow control (RGFC) output presents the extracted GFC bits in a serial stream. The four GFC bits are presented for each received cell, with the RCP output indicating the position of the most significant bit. The serial link is forced low if cell delineation is lost. RGFC is updated on the rising edge of RCLK.
RCP	Output	60	The receive GFC cell pulse (RCP) indicates the location of the four GFC bits in the RGFC serial stream. RCP is coincident with the most significant GFC bit and is asserted 6 payload octets after the first octet of the cell is written into receive FIFO. RCP is updated on the rising edge of RCLK.
TCLK	Output	54	The transmit byte clock (TCLK) is either a 19.44 MHz or a 6.48 MHz clock derived by dividing the transmit line rate by eight.
TFCLK	Input	84	The transmit write clock (TFCLK) is used to write ATM cells to the four cell transmit FIFO. TFCLK cycles at a 33 MHz or lower instantaneous rate. A complete 53 octet cell must be written to the FIFO before being inserted in the synchronous payload envelope (SPE). Idle/unassigned cells are inserted when a complete cell is not available. TDAT[7:0], TXPRTY, TWRENB and TSOC are sampled on the rising edge of TFCLK. TCA is updated on the rising edge of TFCLK.
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7]	Input	87 88 89 90 91 92 93 94	The transmit cell data (TDAT[7:0]) bus carries the ATM cell octets. Then the transmit cell data (TDAT[7:0]) bus carries the ATM cell octets that are written to the transmit FIFO. TDAT[7:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted.

TXPRTY	Input	95	The transmit parity (TXPRTY) signal indicates the parity of the TDAT[7:0] bus. Odd or even parity selection can be made using a register. TXPRTY is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted. TXPRTY has an integral pull down resistor. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are not filtered, so the TXPRTY input may be unused.
TWRENB	Input	85	The active low transmit write enable input (TWRENB) is used to initiate writes to the transmit FIFO. When sampled low using the rising edge of TFCLK, the byte on TDAT[7:0] is written into the transmit FIFO. When sampled high using the rising edge of TFCLK, no write is performed. A complete 53 octet cell must be written to the transmit FIFO before it is inserted into the SPE. Idle/unassigned cells are inserted when a complete cell is not available.
TSOC	Input	96	The transmit start of cell (TSOC) signal marks the start of cell on the TDAT[7:0] bus. When TSOC is high, the first octet of the cell is present on the TDAT[7:0] stream. It is not necessary for TSOC to be present at each cell. An interrupt may be generated if TSOC is high during any byte other than the first byte. TSOC is sampled on the rising edge of TFCLK
TCA	Output	86	The transmit cell available (TCA) signal indicates when a cell is available in the transmit FIFO. When high, TCA indicates that the transmit FIFO is not full and a complete cell may be written in. When TCA goes low, it indicates either that the transmit FIFO is near full and can accept no more than four writes or that the transmit FIFO is full. Selection is made using a register bit in the TACP FIFO Control register. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the TACP FIFO Control register. If the programmed depth is less than four, additional cells may be written after TCA is asserted. TCA is updated on the rising edge of TFCLK. The active polarity of this signal is programmable and defaults to active high.

XOFF	Input	50	The transmit off (XOFF) input prevents the insertion of cells from the transmit FIFO. If XOFF is asserted high, the next cell transmitted is an idle/unassigned cell regardless of the number of cells in the FIFO. Idle/unassigned cells are transmitted until XOFF is deasserted. XOFF may be treated as an asynchronous signal. XOFF has an integral pull down resistor.
TGFC	Input	52	The transmit generic flow control (TGFC) input provides the ability to insert the GFC value downstream of the FIFO. The four TCLK periods following the TCP output pulse contain the GFC value to be inserted into the current cell. The GFC enable bits of the TACP Configuration register enable the insertion of each serial bit. By default, the GFC values are the contents of the TACP Idle/Unassigned Cell Header Control register for idle/unassigned cells and the value received from TDAT[7:0] for assigned cells. TGFC is sampled on the rising edge of TCLK.
TCP	Output	51	The transmit GFC cell pulse (TCP) indicates where the valid TGFC serial bits are expected. If TCP is asserted high, the most significant GFC bit is expected in the subsequent TCLK period. TCP pulses high for one TCLK for every transmitted cell six payload octets before the first octet of the cell read from the transmit FIFO. TCP is updated on the rising edge of TCLK.
ATP1 ATP2	Analog	40 3	Two analog test points (ATP1, ATP2) are provided for production test purposes. Connect these pins to ground.
LF+, LF-, LFO	Analog	42 43 44	Passive components connected to the recovery loop filter (LF+, LF- and LFO) pins determine the dynamics of the clock recovery unit. Refer to the Operation section for details.
CSB	Input	100	The active low chip select (CSB) signal is low during S/UNI-LITE register accesses. If CSB is not required (i.e. register accesses are controlled using the RDB abd WRB signals only), CSB must be connected to an inverted version of the RSTB input.

RDB	Input	105	The active low read enable (RDB) signal is low during S/UNI-LITE register read accesses. The S/UNI-LITE drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	104	The active low write strobe (WRB) signal is low during a S/UNI-LITE register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	109 110 111 112 115 116 117 118	The bidirectional data bus D[7:0] is used during S/UNI-LITE register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]/TRS	Input	119 120 121 122 123 124 125 126	The address bus A[7:0] selects specific registers during S/UNI-LITE register accesses. The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS has an integral pull down resistor.
RSTB	Input	101	The active low reset (RSTB) signal provides an asynchronous S/UNI-LITE reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	127	The address latch enable (ALE) is active high and latches the address bus A[7:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-LITE to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.

INTB	Open-Drain Output	108	The active low interrupt (INTB) signal goes low when a S/UNI-LITE interrupt source is active, and that source is unmasked. The S/UNI-LITE may be enabled to report many alarms or events via interrupts. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
VCLK	Input	99	The test vector clock (VCLK) signal is used during S/UNI-LITE production testing to verify internal functionality. VCLK has an integral pull down resistor.
VDDI1 VDDI2 VDDI3	Power	20 61 107	The core power (VDDI1 - VDDI3) pins should be connected to a well decoupled +5 V DC in common with VDDO.
VSSI1 VSSI2 VSSI3	Ground	19 62 106	The core ground (VSSI1 - VSSI3) pins should be connected to GND in common with VSSO.
TXVDD	Power	12	The transmit pad power (TXVDD) supplies the TXC+/- and TXD+/- outputs. TXVDD is physically isolated from the other device power pins and should be well regulated +5 V DC and noise free for good performance when driving category 5 unshielded twisted pair cabling.
TXVSS	Ground	17	The transmit pad ground (TXVSS) is the return path for the TXC+/- and TXD+/- outputs. TXVSS is physically isolated from the other device ground pins and should be noise free for good performance when driving category 5 unshielded twisted pair cabling.
VDDO1 VDDO2 VDDO3 VDDO4 VDDO5	Power	18 55 73 81 114	The pad ring power (VDDO1 - VDDO5) pins should be connected to a well decoupled +5 V DC in common with VDDI.
VSSO1 VSSO2 VSSO3 VSSO4 VSSO5	Ground	21 56 72 80 113	The pad ring ground (VSSO1 - VSSO5) pins should be connected to GND in common with VSSI.

VSS1, VSS2, VSS3, VSS4, VSS5, VSS6, VSS7, VSS8 VSS9 VSS10 VSS11 VSS12 VSS13	Thermal Ground	1 38 39 64 65 102 103 128 45 46 47 48 49	The thermal grounds (VSS1 - VSS13) provide a low thermal resistance for the dissipated heat. These pins must be connected to GND for correct operation.
TAVD1	Power	4	The power (TAVD1) pin for the transmit clock synthesizer reference circuitry. TAVD1 should be connected to analog +5V.
TAVD2	Power	6	The power (TAVD2) pin for the transmit clock synthesizer oscillator. TAVD2 should be connected to analog +5V.
TAVS1	Ground	5	The ground (TAVS1) pin for the transmit clock synthesizer reference circuitry. TAVS1 should be connected to analog GND.
TAVS2	Ground	7	The ground (TAVS2) pin for the transmit clock synthesizer oscillator. TAVS2 should be connected to analog GND.
TAVD3	Power	8	The power (TAVD3) pin for the transmit PECL inputs. TAVD3 should be connected to analog +5V.
TAVS3	Ground	11	The ground (TAVS3) pin for the transmit PECL inputs. TAVS3 should be connected to analog GND.
RAVD1	Power	30	The power (RAVD1) pin for receive clock and data recovery block reference circuitry. RAVD1 should be connected to analog +5V.
RAVD2	Power	36	The power (RAVD2) pin for receive clock and data recovery block active loop filter and oscillator. RAVD2 should be connected to analog +5V.
RAVS1	Ground	31	The ground (RAVS1) pin for receive clock and data recovery block reference circuitry. RAVS1 should be connected to analog GND.

RAVS2	Ground	37	The ground (RAVS2) pin for receive clock and data recovery block active loop filter and oscillator. RAVS2 should be connected to analog GND.
RAVD3	Power	24	The power (RAVD3) pin for the RXD+/- and ALOS+/- PECL inputs. RAVD3 should be connected to analog +5V.
RAVD4	Power	32	The power (RAVD4) pin for the RRCLK+/- PECL inputs. RAVD4 should be connected to analog +5V.
RAVS3	Ground	29	The ground (RAVS3) pin for the RXD+/- and ALOS+/- PECL inputs. RAVS3 should be connected to analog GND.
RAVS4	Ground	35	The ground (RAVS4) pin for the RRCLK+/- PECL inputs. RAVS4 should be connected to analog GND.

Notes on Pin Description:

1. All S/UNI-LITE inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except for the TRCLK+, TRCLK-, RRCLK+, RRCLK-, RXD+, RXD-, ALOS+ and ALOS- differential inputs which operate at pseudo ECL (PECL) logic levels.

2. The RDAT[7:0], RXPRTY, RCP, RGFC, RSOC, RCA, TCA, TCP, TCLK, RCLK, TXD+, TXD-, TXC+ and TXC- outputs have a 8 mA drive capability. All other S/UNI-LITE digital outputs and bidirectionals have 4 mA drive capability. All 4 mA and 8 mA outputs are slew rate limited except for the TXD+, TXD-, TXC+, and TXC- outputs.

3. The VSSO and VSSI ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-LITE.

4. The VDDO and VDDI power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-LITE.

5. All analog power and ground pins are sensitive to noise. They must be isolated from the digital power and ground. The TAVD2 and RAVD2 pins power oscillators; therefore, they generate significant switching noise. Care must be taken to decouple these pins from each other and all other analog power and ground pins.

FUNCTIONAL DESCRIPTION

Clock Recovery

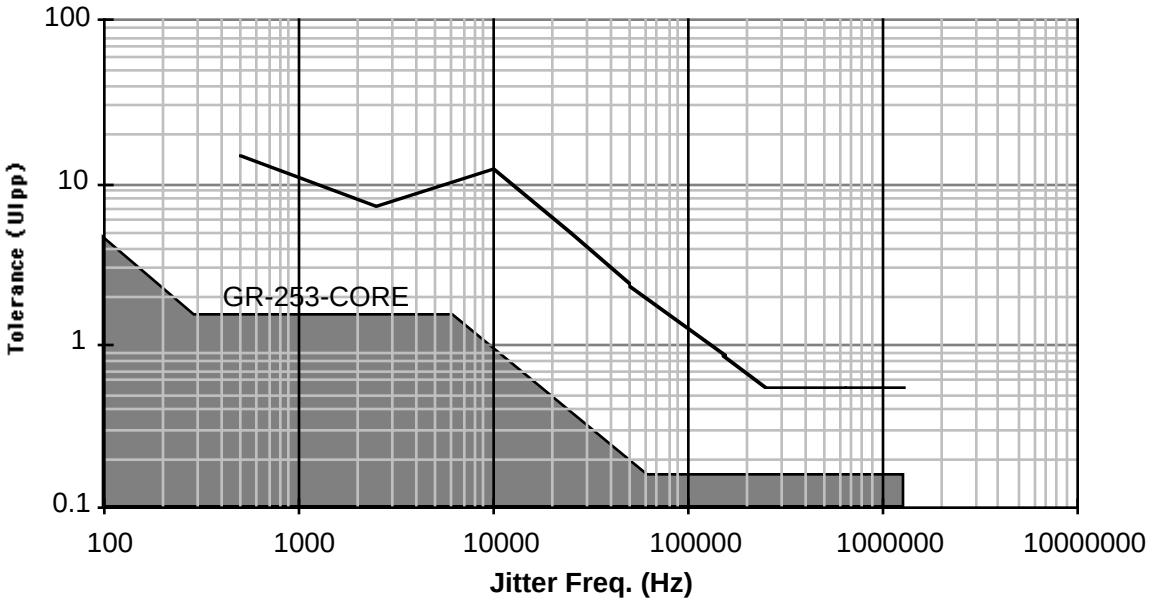
The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit will continue to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit can be configured to utilize reference clocks at 6.48 or 19.44 MHz. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference. The clock recovery unit also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially, the PLL locks to the reference clock, RRCLK+/-. When the frequency of the recovered clock is within 244 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond 244 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the RRCLK+/- reference accuracy in the case of a loss of signal condition. To meet the GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20ppm. When not loop timed, the RRCLK+/- accuracy may be relaxed to +/-50ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance required for SONET equipment by GR-253-CORE (Figure 2).

Fig. 2 STS-3c/STM-1Jitter Tolerance



Note that for frequencies below 300 Hz the jitter tolerance is greater than 15 UIpp; 15 UIpp is the maximum jitter tolerance of the test equipment. Also note that the dip in the tolerance curve between 300 Hz and 10 kHz is due to the S/UNI-LITE's internal clock difference detector: if the recovered clock drifts beyond 244 ppm of the reference, the PLL locks to the reference clock.

The typical jitter tolerance illustrated in Figure 2 is associated with the external loop filter components illustrated in Figure 14a.

Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial SONET stream to a byte serial stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the incoming stream, and performs serial to parallel conversion on octet boundaries.

Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring.

Framer

The Framer Block determines the in-frame/out-of-frame status of the STS-3c or STS-1 data stream. Output RALM reflects this status, and is updated with timing aligned to RCLK.

While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out-of-frame, the SIPO block monitors the bit serial data stream for an occurrence of the framing pattern. When a framing pattern has been recognized, the Framer Block verifies that an error free framing pattern is present in the next frame before declaring in-frame.

Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the received byte serial stream. The generating polynomial is $1 + x^6 + x^7$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the identity bytes (C1) are not descrambled. A register bit is provided to disable the descrambling operation.

Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-3c or STS-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16 bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

Loss of Signal

The Loss of Signal Block monitors the scrambled data of the complete STS-3c or STS-1 stream for the absence of 1's. When 20 ± 3 µs of all zeros patterns is detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. The loss of signal condition asserts the RALM output with timing aligned to RCLK.

Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. To provide for intermittent out-of-frame conditions, the 3 ms timer

is not reset to zero until an in-frame condition persists for 3 ms. The loss of frame is cleared when an in frame condition persists for a period of 3 ms. The loss of frame condition asserts the RALM output with timing aligned to RCLK.

Receive Line Overhead Processor

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring.

Line Remote Defect Indication Detect

The Line RDI Detect Block detects the presence of Line remote defect indication (RDI) in the data stream. Line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. The line RDI status is available through a maskable interrupt and register bits.

Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (AIS) in the data stream. Line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte, for five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. Line AIS detection asserts the RALM output with timing aligned to RCLK.

Error Monitor

The Error Monitor Block calculates the received line BIP-8/24 error detection code (B2) based on the line overhead and synchronous payload envelope of the data stream. The line BIP-8/24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP-8/24 code extracted from the B3 byte(s) of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (24 x 8000) bit errors can be detected per second.

The Error Monitor Block accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, this counter should be polled at least once per second to avoid saturation which in turn may result in missed bit error events.

The Error Monitor Block also accumulates line far end block error indications (contained in the Z2 byte) in a similar manner.

Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm and performance monitoring.

Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-3c (AU4) or STS-1 (AU3) stream.

The Pointer Interpreter Block detects loss of pointer (LOP) in the incoming STS-1 or STS-3c. LOP is declared as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. LOP is removed when the same valid pointer with normal NDF is detected for three consecutive frames.

The Pointer Interpreter Block detects path AIS in the incoming STS-1 or STS-3c stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. PAIS is removed when the same valid pointer with normal NDF is detected for three consecutive frames or when a valid with NDF enabled is detected.

The pointer value is used to extract the path overhead from the incoming stream.

Note that due to anomalies in the standard pointer interpretation rules, certain illegal pointers may not cause the device to declare a loss of pointer (LOP) state. In this situation, however, the device will declare a loss of cell delineation state and return to normal operation when presented with legal pointer values. Such illegal pointers typically can only be generated continuously by test equipment and will not normally occur during live-traffic operation.

Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBE). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path remote defect indication (RDI) is detected by extracting bit 5 of the path status byte. Path RDI is declared when bit 5 is set high for five consecutive frames and is cleared when bit 5 is low for five consecutive frames.

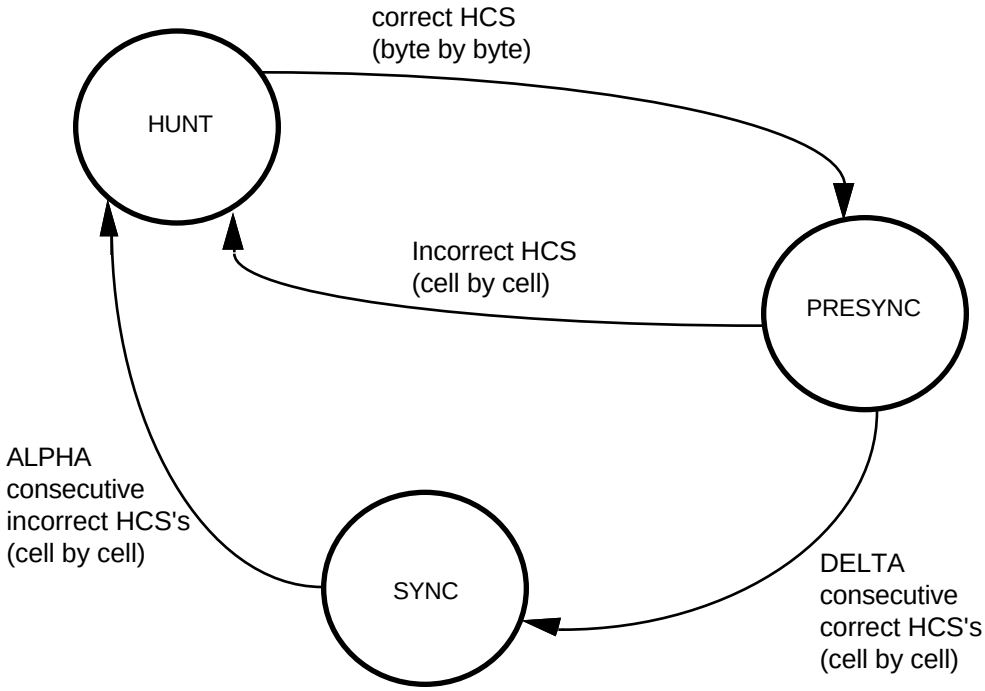
Receive ATM Cell Processor

The Receive ATM Cell Processor (RACP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. The RACP also provides a four cell deep receive FIFO. This FIFO passes a 53 byte data structure and is used to separate the line timing from the higher layer ATM system timing.

Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells must be byte aligned before insertion in the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates one at a time to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary and enters the PRESYNC state. This state validates the cell boundary location. If the cell boundary is invalid then an incorrect HCS will be received within the next DELTA cells, at which point a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period then the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in figure 3.

Fig. 3 Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in a maximum average time to delineate of 31 µs for STS-3c and 93 µs for STS-1.

Descrambler

The self synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the '$x^{43} + 1$' polynomial. The descrambler is disabled for the duration of the header and HCS fields, and may optionally be disabled.

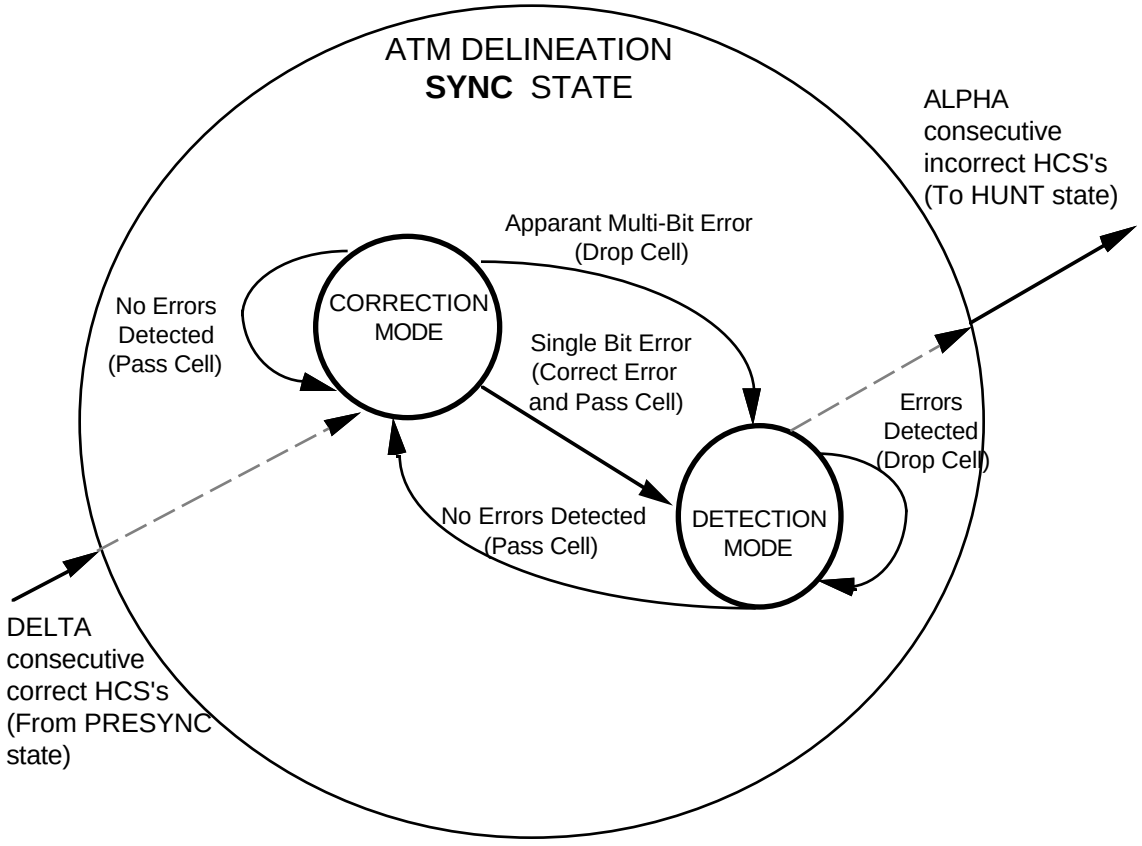
Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RACP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the corrected header contents match the pattern contained in the 'Match Header Pattern' and 'Match Header Mask' registers. Idle or unassigned cell filtering is accomplished by writing

the appropriate cell header pattern into the 'Match Header Pattern' and 'Match Header Mask' registers. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The 'Match Header Pattern' and 'Match Header Mask' registers allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RACP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result. While the cell delineation state machine (described above) is in the SYNC state, the HCS verification circuit implements the state machine shown in figure 4:

Fig. 4 HCS Verification State Diagram



In normal operation, the HCS verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single bit error or a multi bit error, the state machine transitions to the 'Detection Mode' state. In this state, the detection of any HCS error

causes the corresponding cell to be dropped. Cells containing an error-free HCS are passed, and the state machine transitions back to the 'Correction Mode' state.

Performance Monitor

The Performance Monitor consists of two 8-bit saturating HCS error event counters and a 19-bit cell counter. One of the counters accumulates correctable HCS errors (i.e. single HCS bit errors detected while the HCS Verification state machine is in the 'Correction Mode' state described above). The second counter accumulates uncorrectable HCS errors (i.e. HCS bit errors detected while the HCS Verification state machine is in the 'Detection Mode' state or multiple HCS bit errors detected while the state machine is in the 'Correction Mode' state as described above). The cell counter accumulates the number of received assigned cells. All counters are enabled only when the RACP is in the SYNC state.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counters be polled at least once per second so HCS error events or cell counts will not be missed.

GFC Extraction Port

The GFC Extraction Port outputs the received GFC bits in a serial stream. The four GFC bits are presented for each received cell, with the RCP output indicating the position of the most significant bit. The updating of RGFC by particular GFC bits may be disabled through an internal register. The serial link is forced low if cell delineation is lost.

Receive FIFO

The Receive FIFO provides FIFO management and the asynchronous interface between the RACP block and chip pads to the external environment. The receive FIFO can accommodate four cells. The receive FIFO provides for the separation of the STS-1 or STS-3c line or physical layer timing from the ATM layer timing.

Management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun condition, the FIFO is automatically reset. Up to four cells may be lost during the FIFO reset operation. Upon detection of an underrun, the offending read is ignored. FIFO overruns are indicated through a maskable interrupt and register bit. The interface provided indicates the start of a cell (RSOC) when data is read from the receive FIFO (using RFCLK) and indicates the cell available status (RCA).

The cell available status may be configured to change from available to unavailable on read cell boundaries or four reads before the cell boundary.

When the RCA signal is configured to be deasserted with zero octets (as opposed to four) in the FIFO, it is not an error condition to hold the read enable (RRDENB) active. In this situation, the RCA signal identifies the valid octets.

Clock Synthesis

The transmit clock is synthesized from a 19.44 MHz or 6.48 MHz reference. The transfer function yields a typical low pass corner of 500 kHz with a 19.44 MHz reference and 170 kHz with a 6.48 MHz reference, above which reference jitter is attenuated at 12dB per octave. The intrinsic jitter is minimised when the reference frequency is 19.44 MHz. With a jitter free 19.44 MHz differential reference input and a low noise board layout, the intrinsic jitter is typically less than 0.01 UI RMS when measured using a high pass filter with a 12 kHz cutoff frequency.

The TRCLK+/- reference frequency must be within +/-20 ppm of 155.52 MHz to meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification.

Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the internal byte serial stream to a bit serial stream.

Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion.

Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled through an internal register accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the unscrambled data stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3c or STS-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) and identity bytes (C1) into the STS-3c or STS-1 frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit serial stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $1 + x^6 + x^7$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

Transmit Line Overhead Processor

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, and line BIP-8/24 insertion (B2).

BIP Calculate

The BIP Calculate Block calculates the line BIP error detection code (B2) based on the line overhead and synchronous payload envelope of the STS-3c or STS-1 stream. The line BIP code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is inserted into the B2 byte positions of the following frame. BIP errors may be continuously inserted under register control for diagnostic purposes.

Line Remote Defect Indication Insert

The Line RDI Insert Block multiplexes the line overhead bytes into the output stream and optionally inserts line RDI. Line RDI is inserted by this block when enabled via register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the STS-3c or STS-1 stream.

Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP errors (Z2) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit Z2 byte.

Fig. 5 STS-3c/STM-1 Default Transport Overhead Values

A1 (0xF6)	A1 (0xF6)	A1 (0xF6)	A2 (0x28)	A2 (0x28)	A2 (0x28)	C1 (0x01)	C1 (0x02)	C1 (0x03)
B1 (*)	(0x00)	(0x00)	E1 (0x00)	(0x00)	(0x00)	F1 (0x00)	(0x00)	(0x00)
D1 (0x00)	(0x00)	(0x00)	D2 (0x00)	(0x00)	(0x00)	D3 (0x00)	(0x00)	(0x00)
H1 (0x62)	H1 (0x93)	H1 (0x93)	H2 (0x0A)	H2 (0xFF)	H2 (0xFF)	H3 (0x00)	H3 (0x00)	H3 (0x00)
B2 (*)	B2 (*)	B2 (*)	K1 (0x00)	(0x00)	(0x00)	K2 (0x00)	(0x00)	(0x00)
D4 (0x00)	(0x00)	(0x00)	D5 (0x00)	(0x00)	(0x00)	D6 (0x00)	(0x00)	(0x00)
D7 (0x00)	(0x00)	(0x00)	D8 (0x00)	(0x00)	(0x00)	D9 (0x00)	(0x00)	(0x00)
D10 (0x00)	(0x00)	(0x00)	D11 (0x00)	(0x00)	(0x00)	D12 (0x00)	(0x00)	(0x00)
Z1 (0x00)	Z1 (0x00)	Z1 (0x00)	Z2 (0x00)	Z2 (0x00)	Z2 (*)	E2 (0x00)	(0x00)	(0x00)

*** : B1, B2 values depend on payload contents**
Z2 value depends on incoming line bit errors

Fig. 6 STS-1 Default Transport Overhead Values

A1 (0xF6)	A2 (0x28)	C1 (0x01)
B1 (*)	E1 (0x00)	F1 (0x00)
D1 (0x00)	D2 (0x00)	D3 (0x00)
H1 (0x62)	H2 (0x0A)	H3 (0x00)
B2 (*)	K1 (0x00)	K2 (0x00)
D4 (0x00)	D5 (0x00)	D6 (0x00)
D7 (0x00)	D8 (0x00)	D9 (0x00)
D10 (0x00)	D11 (0x00)	D12 (0x00)
Z1 (0x00)	Z2 (*)	E2 (0x00)

*** : B1, B2 values depend on payload contents**
Z2 value depends on incoming line bit errors

Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion, insertion of the synchronous payload envelope, insertion of path level alarm signals and path BIP-8 (B3) insertion.

Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2). The block contains a free running timeslot counter that locates the start of the synchronous payload envelope based on the generated pointer value and the SONET/SDH frame alignment.

The Pointer Generator Block generates the outgoing pointer as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer bytes.

BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the outgoing stream. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. The asynchronous nature of these signals implies that more than eight FEBE events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining FEBEs are transmitted at the next opportunity. Far end block errors may be inserted under register control for diagnostic purposes.

SPE Multiplexer

The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the STS-3c or STS-1 stream.

Fig. 7 Default Path Overhead Values

J1 (0x00)
B3 (*)
C2 (0x13)
G1 (*)
F2 (0x00)
H4 (*)
Z3 (0x00)
Z4 (0x00)
Z5 (0x00)

*** : B3 value depend on payload contents**
G1 value depends on incoming path bit errors
H4 value depends on cell boundary offset

Transmit ATM Cell Processor

The Transmit ATM Cell Processor (TACP) inserts H4 framing, provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. The TACP contains a four cell transmit FIFO. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the FIFO.

Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. An all zeros pattern is

inserted into the VCI/VPI bit locations. The idle cell HCS is automatically calculated and inserted.

Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self synchronous scrambler described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be completely disabled.

HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1 is used. The coset polynomial, $x^6+x^4+x^2+1$ is added (modulo 2) to the residue. The HCS Generator inserts the result into the fifth octet of the header.

GFC Insertion Port

The GFC Insertion Port provides the ability to insert the GFC value downstream of the FIFO. The four GFC bits are received on a serial stream the is synchronized to the transmit cell by a framing pulse. The GFC enable register bits control the insertion of each serial bit. If the enable is cleared, the default GFC value is inserted. For idle/unassigned cells, the default is the contents of the TACP Idle/Unassigned Cell Header Control register. For assigned cells, the default is the value received from TDAT[7:0].

Transmit FIFO

The Transmit FIFO provides FIFO management and a synchronous interface between the S/UNI-LITE device and the external environment. The transmit FIFO can accommodate four cells. It provides for the separation of the physical layer timing from the ATM layer timing.

Management functions include filling the transmit FIFO, indicating when cells are available to be written to the transmit FIFO, maintaining the transmit FIFO read and write pointers, and detecting a FIFO overrun condition. The synchronous interface provided to an external device expects the start of a cell (TSOC) when the first byte of the cell is written to the FIFO (using TFCLK in conjunction with TWRENB) and indicates the cell available status (TCA). The FIFO status changes from cell unavailable to cell available on read cell boundaries. The FIFO status can be configured to change from cell available to cell unavailable on write cell boundaries or four octets before the end of the cell.

The latency through the transmit FIFO can be controlled by setting the fill level at which the cell available (TCA) signal is deasserted. Although all four cell buffers are

always accessible, TCA may be programmed to indicate when the FIFO contains one, two, three or four cells. (The current cell being read out of the FIFO is included in the count. Be aware that setting a depth of one may limit throughput.) If a cell write is started immediately after TCA is asserted, the latency through the device for STS-3c/STM-1 is

latency = depth*(53 line byte periods) + 16 line byte periods (min.)
= depth*(53 line byte periods) + 26 line byte periods (max.).

The latency for STS-1 is

latency = depth*(53 line byte periods) + 10 line byte periods (min.)
= depth*(53 line byte periods) + 14 line byte periods (max.).

The presence of the SONET/SDH overhead accounts for the difference between the minimum and maximum latencies.

When the FIFO contains four cells and the upstream device writes into the FIFO, the TACP indicates a FIFO overrun condition using a maskable interrupt and register bits. The offending write and all subsequent writes are ignored until there is room in the FIFO.

Drop Side Interface

Receive Interface

The drop side receive interface can be accessed through a generic 8-bit wide interface.

External circuitry is notified, using the RCA signal, when a cell is available in the receive FIFO. External circuitry may then read the cell from the buffer as a byte wide stream (along with a bit marking the first byte of the cell) at instantaneous rates of up to 33 MHz.

Transmit Interface

The drop side transmit interface can be accessed through a generic 8-bit wide interface.

External circuitry is notified, using the TCA signal, when a cell may be written to the transmit FIFO. The cell is written to the FIFO as a byte wide stream (along with a bit marking the first byte of the cell) at instantaneous rates of up to 33 MHz.

Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-LITE. The register set is accessed as follows:

REGISTER MEMORY MAP

Address	Register
0x00	S/UNI-LITE Master Reset and Identity / Load Meters
0x01	S/UNI-LITE Master Configuration
0x02	S/UNI-LITE Master Interrupt Status
0x04	S/UNI-LITE Master Clock Monitor
0x05	S/UNI-LITE Master Control
0x06	S/UNI-LITE Clock Synthesis Control and Status
0x07	S/UNI-LITE Clock Recovery Control and Status
0x08-0x0B	Reserved
0x0C-0x0F	Reserved
0x10	RSOP Control/Interrupt Enable
0x11	RSOP Status/Interrupt Status
0x12	RSOP Section BIP-8 LSB
0x13	RSOP Section BIP-8 MSB
0x14	TSOP Control
0x15	TSOP Diagnostic
0x16-0x17	TSOP Reserved
0x18	RLOP Control/Status
0x19	RLOP Interrupt Enable/Status
0x1A	RLOP Line BIP-8/24 LSB
0x1B	RLOP Line BIP-8/24
0x1C	RLOP Line BIP-8/24 MSB
0x1D	RLOP Line FEBE LSB
0x1E	RLOP Line FEBE
0x1F	RLOP Line FEBE MSB
0x20	TLOP Control
0x21	TLOP Diagnostic
0x22-0x23	TLOP Reserved
0x24-0x27	Reserved
0x28-0x2B	Reserved
0x2C-0x2F	Reserved
0x30	RPOP Status/Control
0x31	RPOP Interrupt Status
0x32	RPOP Reserved
0x33	RPOP Interrupt Enable
0x34	RPOP Reserved
0x35	RPOP Reserved
0x36	RPOP Reserved
0x37	RPOP Path Signal Label

0x38	RPOP Path BIP-8 LSB
0x39	RPOP Path BIP-8 MSB
0x3A	RPOP Path FEBE LSB
0x3B	RPOP Path FEBE MSB
0x3C	RPOP Reserved
0x3D	RPOP Path BIP-8 Configuration
0x3E-0x3F	RPOP Reserved
0x40	TPOP Control/Diagnostic
0x41	TPOP Pointer Control
0x42	TPOP Reserved
0x43	TPOP Reserved
0x44	TPOP Reserved
0x45	TPOP Arbitrary Pointer LSB
0x46	TPOP Arbitrary Pointer MSB
0x47	TPOP Reserved
0x48	TPOP Path Signal Label
0x49	TPOP Path Status
0x4A	TPOP Reserved
0x4B-0x4F	TPOP Reserved
0x50	RACP Control/Status
0x51	RACP Interrupt Enable/Status
0x52	RACP Match Header Pattern
0x53	RACP Match Header Mask
0x54	RACP Correctable HCS Error Count
0x55	RACP Uncorrectable HCS Error Count
0x56	RACP Receive Cell Counter (LSB)
0x57	RACP Receive Cell Counter
0x58	RACP Receive Cell Counter (MSB)
0x59	RACP Configuration
0x5A-0x5F	RACP Reserved
0x60	TACP Control/Status
0x61	TACP Idle/Unassigned Cell Header Pattern
0x62	TACP Idle/Unassigned Cell Payload Octet Pattern
0x63	TACP FIFO Configuration
0x64	TACP Transmit Cell Counter (MSB)
0x65	TACP Transmit Cell Counter (MSB)
0x66	TACP Transmit Cell Counter (MSB)
0x67	TACP Configuration
0x68-0x7F	Reserved
0x80	S/UNI-LITE Master Test
0x81-0xFF	Reserved for Test

NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-LITE. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[7]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-LITE to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-LITE operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-LITE operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 0x00: S/UNI-LITE Master Reset and Identity / Load Meters

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	1
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision of the S/UNI-LITE to be read by software permitting graceful migration to support for newer, feature enhanced versions of the S/UNI-LITE. It also provides software reset capability.

Writing this register loads all the error counters in the RSOP, RLOP, RPOP, RACP and TACP blocks.

ID[3:0]:

The ID bits can be read to provide a binary S/UNI-LITE revision number.

TYPE[2:0]:

The TYPE bits distinguish the S/UNI-LITE from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-LITE to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-LITE is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-LITE out of reset. Holding the S/UNI-LITE in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise the effect of a software reset is equivalent to that of a hardware reset.

Register 0x01: S/UNI-LITE Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	AUTOFEBE	1
Bit 5	R/W	AUTOLRDI	1
Bit 4	R/W	AUTOPRDI	1
Bit 3	R/W	TCAINV	0
Bit 2	R/W	RCAINV	0
Bit 1	R/W	RXDINV	0
Bit 0		Unused	X

RXDINV:

The RXDINV bit selects the active polarity of the RXD+/- signals. The default configuration selects RXD+ to be active high and RXD- to be active low. When RXDINV is set to logic one, RXD+ to be active low and RXD- to be active high.

RCAINV:

The RCAINV bit selects the active polarity of the RCA signal. The default configuration selects RCA to be active high, indicating that a received cell is available when high. When RCAINV is set to logic one, the RCA signal becomes active low.

TCAINV:

The TCAINV bit selects the active polarity of the TCA signal. The default configuration selects TCA to be active high, indicating that a cell is available in the transmit FIFO when high. When TCAINV is set to logic one, the TCA signal becomes active low.

AUTOPRDI

The AUTOPRDI bit determines whether STS path remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOPRDI is set to logic one, STS path RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), line AIS, loss of pointer (LOP), STS path AIS or loss of cell delineation (LCD).

AUTOLRDI

The AUTOLRDI bit determines whether line remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is set to logic one, line RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF) or line AIS.

AUTOFEBE

The AUTOFEBE bit determines whether line and path far end block errors are sent upon detection of an incoming line and path BIP error events. When AUTOFEBE is set to logic one, one line or path FEBE is inserted for each line or path BIP error event, respectively. When AUTOFEBE is set to logic zero, incoming line or path BIP error events do not generate FEBE events.

Register 0x02: S/UNI-LITE Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R	TROOLI	X
Bit 6	R	LCDI	X
Bit 5	R	RDOOLI	X
Bit 4	R	TACPI	X
Bit 3	R	RACPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is high when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RACPI:

The RACPI bit is high when an interrupt request is active from the RACP block. The RACP interrupt sources are enabled in the RACP Interrupt Enable/Status Register.

TACPI:

The TACPI bit is high when an interrupt request is active from the TACP block. The TACP interrupt sources are enabled in the TACP Interrupt Control/Status Register.

TROOLI:

The TROOLI bit is the transmit reference out of lock interrupt status bit. TROOLI is set high when the TROOLV bit of the S/UNI-LITE Clock Synthesis

Control and Status register changes state. TROOLV indicates the clock synthesis phase locked loop is unable to lock to the reference on RRCLK+/- and is a logic one if the divided down synthesized clock frequency not within 244ppm of the TRCLK+/- frequency. TROOLI is cleared when this register is read.

LCDI:

The LCDI interrupt bit is set high when entering and exiting loss of cell delineation. This bit is reset immediately after a read to this register. The LCD interrupt is enabled in the S/UNI-LITE Master Control Register.

RDOOLI:

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the RDOOLV bit of the S/UNI-LITE Clock Recovery Control and Status register changes state. RDOOLV is a logic one if the divided down recovered clock frequency not within 244ppm of the RRCLK+/- frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods. RDOOLI is cleared when this register is read.

Register 0x04: S/UNI-LITE Master Clock Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RRCLKA	X
Bit 2	R	TRCLKA	X
Bit 1	R	RCLKA	X
Bit 0	R	TCLKA	X

This register provides activity monitoring on S/UNI-LITE clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

TCLKA:

The TCLK active (TCLKA) bit monitors for low to high transitions on the TCLK output. TCLKA is set high on a rising edge of TCLK, and is set low when this register is read.

RCLKA:

The RCLK active (RCLKA) bit monitors for low to high transitions on the RCLK output. RCLKA is set high on a rising edge of RCLK, and is set low when this register is read.

TRCLKA:

The TRCLK active (TRCLKA) bit monitors for low to high transitions on the TRCLK+ and TRCLK- inputs. TRCLKA is set high on a rising edge of TRCLK+, and is set low when this register is read.

RRCLKA:

The RRCLK active (RRCLKA) bit monitors for low to high transitions on the RRCLK+ and RRCLK- inputs. RRCLKA is set high on a rising edge of RRCLK+, and is set low when this register is read.

Register 0x05: S/UNI-LITE Master Control

Bit	Type	Function	Default
Bit 7	R/W	LCDE	0
Bit 6	R	LCDV	X
Bit 5	R/W	FIXPTR	1
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LLE	0
Bit 1	R/W	DLE	0
Bit 0	R/W	LOOPT	0

This register controls the timing and high speed loopback features of the S/UNI-LITE.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the S/UNI-LITE. When LOOPT is a logic zero, the transmitter timing is derived from inputs TRCLK+ and TRCLK-.

When LOOPT is a logic one, the transmitter timing is derived from the receiver inputs RXD+ and RXD- when clock recovery is enabled and from RRCLK+ and RRCLK- when clock recovery is disabled.

DLE:

The DLE bit enables the S/UNI-LITE diagnostic loopback. When DLE is a logic one, the transmit stream is connected to the receive stream. The DLE and the LLE bits should not be both set to a logic one simultaneously.

LLE:

The LLE bit enables the S/UNI-LITE line loopback. When LLE is a logic one, RXD+ and RXD- are connected internally to TXD+ and TXD-, respectively. The DLE and the LLE bits should not be both set to a logic one simultaneously.

FIXPTR:

The FIXPTR bit disables transmit payload pointer adjustments. If the FIXPTR bit is a logic 1, the transmit payload pointer is set at 522. If FIXPTR is a logic zero, the payload pointer is controlled by the contents of the TPOP Pointer Control register.

LCDV:

The LCDV bit reflects the current loss of cell delineation state. LCDV becomes a logic 1 when an out of cell delineation state has persisted for 4ms

without any lower level alarms (LOS, LOP, Path AIS, Line AIS) occurring. LCDV becomes logic 0 when the SYNC state has been maintained for 4ms.

LCDE:

The LCDE bit enables the loss of cell delineation (LCD) interrupt. When logic one, the S/UNI-LITE INTB output is asserted when there is a change in the LCD state. When logic zero, the S/UNI-LITE INTB output is not affected by the change in LCD state.

Register 0x06: S/UNI-LITE Clock Synthesis Control and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	TROOLV	X
Bit 2		Unused	X
Bit 1	R/W	TROOLE	0
Bit 0	R/W	TREFSEL	0

This register controls the clock synthesis and reports the state of the transmit phase locked loop.

TREFSEL:

The transmit reference select (TREFSEL) bit determines the expected frequency of TRCLK+/-. If TREFSEL is a logic 0, the correct line clock frequency is synthesized if the reference frequency is 19.44 MHz. If TREFSEL is a logic 1, the reference frequency must be 6.48 MHz. TREFSEL only has effect if the TBYP input is deasserted low.

TROOLE:

The TROOLE bit is an interrupt enable for the transmit reference out of lock status. When TROOLE is set to logic one, an interrupt is generated when the TROOLV bit changes state.

TROOLV:

The transmit reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference on TRCLK+/-. TROOLV is a logic one if the divided down synthesized clock frequency not within 244ppm of the TRCLK+/- frequency.

Register 0x07: S/UNI-LITE Clock Recovery Control and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	RROOLV	X
Bit 3	R	RDOOLV	X
Bit 2		Unused	X
Bit 1	R/W	RDOOLE	0
Bit 0	R/W	RREFSEL	0

This register controls the clock recovery and reports the state of the receive phase locked loop.

RREFSEL:

The receive reference select (RREFSEL) bit determines the expected frequency of RRCLK+/-. If RREFSEL is a logic 0, the reference frequency is 19.44 MHz. If RREFSEL is a logic 1, the reference frequency must be 6.48 MHz. RREFSEL only has effect if the RBYP input is deasserted low.

RDOOLE:

The RDOOLE bit is an interrupt enable for the receive data out of lock status. When RDOOLE is set to logic one, an interrupt is generated when the RDOOLV bit changes state.

RDOOLV:

The receive data out of lock status indicates the clock recovery phase locked loop is unable to lock to the incoming data stream. RDOOLV is a logic one if the divided down recovered clock frequency is not within 244ppm of the RRCLK+/- frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods.

RROOLV:

The receive reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the receive reference (RRCLK+/-). RROOLV should be polled after a power up reset to determine when the CRU PLL is operational. When RROOLV is a logic 1, the CRU is unable to lock to the receive reference. When RROOLV is a logic 0, the CRU is locked to the receive reference. The RROOLV bit may remain set at logic 1 for several hundred milliseconds after the removal of the power on reset as the CRU PLL locks to the receive reference clock.

Register 0x10: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out of frame alarm. When OOFE is set to logic one, an interrupt is generated when the out of frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit, register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the descrambling of the STS-3c (STM-1) stream. When DDS is a logic zero, descrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x11: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out of frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:

The OOFI bit is the out of frame interrupt status bit. OOFI is set high when a change in the out of frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x12: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x13: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (B1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP and RACP blocks.

Register 0x14: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET frame being set to 1 prior to scrambling except for the section overhead. The LAIS bit is logically ORed with the external TLAIS input.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-3c or STS-1 stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x15: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the transmit stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x18: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R	LAISV	0
Bit 0	R	RDIV	0

RDIV:

The RDIV bit is read to determine the remote defect indication state of the RLOP. When RDIV is high, the RLOP has declared line RDI.

LAISV:

The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 errors. When BIPWORD is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD is logic zero, the B2 error event counter is incremented for each B2 bit error that occurs during that frame (the counter can be incremented up to 8 times per frame for STS-1 and 24 times per frame for STS-3c).

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x19: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	RDIE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	RDII	X

RDII:

The RDII bit is the far end receive failure interrupt status bit. RDII is set high when a change in the line RDI state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (Z2) is detected. This bit is cleared when this register is read.

RDIE:

The RDIE bit is an interrupt enable for the far end receive failure alarm. When RDIE is set to logic one, an interrupt is generated when RDI changes state.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-24 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-24 error (B2) is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBE (Z2) is detected.

Register 0x1A: RLOP Line BIP-8/24 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x1B: RLOP Line BIP-8/24

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x1C: RLOP Line BIP-8/24 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-8/24 errors (B2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x1D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x1E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x1F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (Z2) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The error count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x20: TLOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RDI	0

RDI:

The RDI bit controls the insertion of line far end receive failure (RDI). When RDI is set to logic one, the TLOP inserts line RDI into the transmit SONET stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte of the transmit stream.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x21: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP	0

DBIP24:

The DBIP bit controls the insertion of bit errors continuously in the line BIP byte(s) (B2). When DBIP is set to logic one, the B2 byte(s) are inverted.

Register 0x30: RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	LOP	X
Bit 4		Unused	X
Bit 3	R	PAIS	X
Bit 2	R	PRDI	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	0

This register allows the status of path level alarms to be monitored.

PRDI, PAIS,LOP:

The PRDI, PAIS, and LOP bits reflect the current state of the corresponding path level alarms.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x31: RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI, BIPEI:

The BIPEI and FEBEI bits are set to logic one when the corresponding event, a path BIP-8 error or path FEBE is detected.

PRDII, PAISI, LOPI:

The PRDII, PAISI, and LOPI bits are set to logic one when a transition occurs in the corresponding alarm state.

PSLI:

The PSLI bit is set to logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register.

These bits (and the interrupt) are cleared when this register is read.

Register 0x33: RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

When a 1 is written to the FEBEE interrupt enable bit position, the reception of one or more FEBEs will activate the interrupt output.

BIPEE:

When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt output.

PRDIE, PAISE:

When a 1 is written to the PRDIE interrupt enable bit position, a change in the path remote defect indication state will activate the interrupt output. When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt output.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt output.

PSLE:

When a 1 is written to the PSLE interrupt enable bit position, a change in the path signal label will activate the interrupt output.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x37: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

This register allows the received path signal label byte to be read.

PSL[7:0]:

The PSL7 - PSL0 bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three consecutive frames.

Register 0x38: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x39: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

These registers allow path BIP-8 errors to be accumulated.

PBE[15:0]:

Bits PBE[15:0] represent the number of path BIP-8 errors (B3) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x3A: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE7	X
Bit 6	R	PFE6	X
Bit 5	R	PFE5	X
Bit 4	R	PFE4	X
Bit 3	R	PFE3	X
Bit 2	R	PFE2	X
Bit 1	R	PFE1	X
Bit 0	R	PFE0	X

Register 0x3B: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE15	X
Bit 6	R	PFE14	X
Bit 5	R	PFE13	X
Bit 4	R	PFE12	X
Bit 3	R	PFE11	X
Bit 2	R	PFE10	X
Bit 1	R	PFE9	X
Bit 0	R	PFE8	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

Bits PFE[15:0] represent the number of path FEBE errors (G1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The error count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x3DH: RPOP Path BIP-8 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated and reported to the return transmit path overhead processor if one or more of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated and reported on a bit basis.

Register 0x40: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

This register allows insertion of path level alarms and diagnostic signals.

PAIS:

The PAIS bit controls the insertion of STS path alarm indication signal. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.

DB3:

The DB3 bit controls the inversion of the B3 byte value. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted.

Register 0x41: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

NSE:

The NSE bit controls the insertion of negative pointer movements. A zero to one transition on this bit enables the insertion of a single negative pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the Arbitrary Pointer Registers. Normally, the Arbitrary Pointer Registers are written to set up the arbitrary new pointer value and a logic one is then written to this bit position to load the new pointer value.

If a legal value (i.e. $0 \leq$ pointer value ≤ 782) is transferred from the Arbitrary Pointer Registers, the transmit payload pointer will immediately change to the

corresponding byte position. If a value greater than 782 is transferred, the payload pointer remains unchanged.

This bit is automatically cleared after the new payload pointer has been loaded. This bit has no effect if the FIXPTR bit of the Master Control register is a logic 1.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the transmit stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated, although it is unlikely to be extracted by far end circuitry. If FTPTR is set to logic 1, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. At least one corrupted pointer is guaranteed to be sent. If FTPTR is a logic 0, a valid pointer is inserted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x45: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7], APTR[6], APTR[5], APTR[4], APTR[3], APTR[2], APTR[1], APTR[0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is transferred by writing a logic one to the PLD bit in the Pointer Control Register. A legal value (i.e. $0 \leq$ pointer value ≤ 782) results in the transmit payload pointer immediately changing to the corresponding byte position. If a value greater than 782 is transferred, the payload pointer remains unchanged.

If the FTPTR bit in the Pointer Control register is a logic 1, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

Register 0x46: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	0
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9], APTR[8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

S[1], S[0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer.

NDF[3], NDF[2], NDF[1], NDF[0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the Pointer Control Register) or when new data flag generation is enabled using the NDF bit in the TPOP Pointer Control Register.

Register 0x48: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	1
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	1
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label.

C2[7], C2[6], C2[5], C2[4], C2[3], C2[2], C2[1], C2[0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream.

Register 0x49: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

FEBE[3], FEBE[2], FEBE[1], FEBE[0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

PRDI:

The PRDI bit controls the insertion of the path remote defect indication (RDI). When a logic one is written to this bit position, the PRDI bit position in the path status byte (G1) is set high. If the AUTORDI bit is a logic one, an alarm state also sets the PRDI bit high. When a logic zero is written to this bit position, the PRDI bit position in the path status byte is set low provided AUTORDI is low or no alarms are currently active.

G1[2], G1[1], G1[0]:

The G1[2:0] bits are inserted in the unused bit positions in the path status byte .

Register 0x50: RACP Control/Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R/W	RXPTYP	0
Bit 5	R/W	PASS	0
Bit 4	R/W	DISCOR	0
Bit 3	R/W	HCSPASS	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DDSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell receive FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload. When DDSCR is a logic one, cell payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic zero, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic one, cells are passed to the receive FIFO regardless of errors detected in the HCS. In addition, the HCS verification finite state machine never exits the correction mode. Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

DISCOR:

The DISCOR bit disables the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single bit errors detected in the cell header are corrected. When DISCOR is a logic one, the

error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

PASS:

The PASS bit controls the function of the cell filter. When PASS is written with a logic zero, all cells matching the cell filter are dropped. When PASS is a logic one, the match header pattern registers are ignored and filtering of cells with VPI and VCI fields set to 0 is not performed. The default state of this bit together with the default states of the bits in the Match Mask and Match Pattern Registers enable the dropping of cells containing all zero VCI and VPI fields.

RXPTYP:

The RXPTYP bit selects even or odd parity for outputs RXPRTY. When it is set to logic one, output RXPRTY is the even parity bit for outputs RDAT[7:0]. When it is set to logic zero, RXPRTY is the odd parity bits for outputs RDAT[7:0].

OOCDV:

The OOCDV bit indicates the cell delineation state. When OOCDV is set high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states, and is hunting for the cell boundaries in the synchronous payload envelope. When OOCDV is set low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x51: RACP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	OOCDE	0
Bit 6	R/W	HCSE	0
Bit 5	R/W	FIFOE	0
Bit 4	R	OOCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register.

UHCSI:

The UHCSI bit is set high when an uncorrectable HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI:

The CHCSI bit is set high when a correctable HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set high when a change of cell delineation state has occurred. The OOCDI bit is set high when the RACP block transitions from the PRESYNC state to the SYNC state and from the SYNC state to the HUNT state. This bit is reset immediately after a read to this register.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FIFOE is set to logic one, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a correctable or an uncorrectable HCS error. When HCSE is set to logic one, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change of cell delineation state. When OOCDE is set to logic one, the interrupt is enabled.

Register 0x52: RACP Match Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

This register extends the cell filtering criteria beyond the all zeros pattern that must be present in the VPI and VCI fields of the idle or unassigned cell. The PASS bit in the RACP Control/Status Register must be set to logic zero to enable dropping of idle/unassigned cells matching the pattern defined by the contents of this register and the RACP Match Header Mask Register.

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third and fourth bits of the first octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register.

Register 0x53: RACP Match Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	0
Bit 6	R/W	MGFC[2]	0
Bit 5	R/W	MGFC[1]	0
Bit 4	R/W	MGFC[0]	0
Bit 3	R/W	MPTI2]	0
Bit 2	R/W	MPTI[1]	0
Bit 1	R/W	MPTI[0]	0
Bit 0	R/W	MCLP	0

The mask contained in this register is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third and fourth bits of the first octet of the 53 octet cell.

MPTI3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell.

MCLP:

The MCLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53 octet cell.

Register 0x54: RACP Correctable HCS Error Count

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

CHCS[7:0]:

The CHCS[7:0] bits indicate the number of correctable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the correctable HCS error count register address, or to the uncorrectable HCS error count register address.

The error count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x55: RACP Uncorrectable HCS Error Count

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

UHCS[7:0]:

The UHCS[7:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the correctable HCS error count register address, or to the uncorrectable HCS error count register address.

The error count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x56: RACP Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x57: RACP Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x58: RACP Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[18:0]:

The RCELL[18:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle/Unassigned cell matches are not counted. The counter should be polled every second to avoid saturating. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the

correctable HCS error count register addresses, the uncorrectable HCS error count register addresses or the receive cell counter register addresses.

The cell count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x59: RACP Configuration

Bit	Type	Function	Default
Bit 7	R/W	RGFCE[3]	1
Bit 6	R/W	RGFCE[2]	1
Bit 5	R/W	RGFCE[1]	1
Bit 4	R/W	RGFCE[0]	1
Bit 3	R/W	FSEN	1
Bit 2	R/W	RCALEVEL0	1
Bit 1	R/W	HCSFTR[1]	0
Bit 0	R/W	HCSFTR[0]	0

The Configuration Register is provided at RACP read/write address 9.

HCSFTR[1:0]:

The HCS filter bits, HSCFTR[1:0], indicate the number of consecutive error free cells required while in detection mode before reverting back to correction mode. Please refer to Fig. 4 for details.

HCSFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HCS before resumption of Cell acceptance. This cell is accepted.
01	Two ATM cells with correct HCS before resumption of Cell acceptance. The last cell is accepted.
10	Four ATM cells with correct HCS before resumption of Cell acceptance. The last cell is accepted.
11	Eight ATM cells with correct HCS before resumption of Cell acceptance. The last cell is accepted.

RCALEVEL0:

The RCA level 0 bit, RCALEVEL0, determines what output RCA indicates when it transitions low. When RCALEVEL0 is set to logic one, a high to low transition on output RCA indicates that the receive FIFO is empty. When RCALEVEL0 is set to logic zero, a high to low transition on output RCA indicates that the receive FIFO is near empty and contains four only bytes.

FSEN:

The active high fix stuff control enable bit FSEN selects the expected payload mapping of ATM cells when STS-1 mapping is selected. When FSEN is set to logic one, it is assumed columns 30 and 59 of the Synchronous Payload

Envelope (SPE) contain fixed stuff bytes. When FSEN is set to logic zero, it is assumed ATM payload fills the entire SPE except the path overhead column.

RGFCE[3:0]:

The receive GFC enable bits, RGFCE[3:0], determine which generic flow control bits are presented on the RGFC output. RGFCE[3] corresponds to the most significant GFC bit (first bit in the cell). If a RGFCE bit is a logic 1, the RGFC output presents in the appropriate bit location the state of the associated GFC bit in the current cell; otherwise, RFGC is deasserted low.

Register 0x60: TACP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	FIFOE	0
Bit 6	R	TSOCI	X
Bit 5	R	FOVRI	X
Bit 4	R/W	DHCS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope.

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any

position other than the first byte. The write address counter is reset to the first byte of the cell when TSOC is sampled high. This bit is reset immediately after a read to this register.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun error condition, or when the TSOC input is sampled high during any position other than the first byte. When FIFOE is set to logic one, the interrupt is enabled.

Register 0x61: TACP Idle/Unassigned Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

PTI[3:0]:

The PTI[3:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

Register 0x62: TACP Idle/Unassigned Cell Payload Octet Pattern

Bit	Type	Function	Default
Bit 7	R/W	ICP[7]	0
Bit 6	R/W	ICP[6]	1
Bit 5	R/W	ICP[5]	1
Bit 4	R/W	ICP[4]	0
Bit 3	R/W	ICP[3]	1
Bit 2	R/W	ICP[2]	0
Bit 1	R/W	ICP[1]	1
Bit 0	R/W	ICP[0]	0

ICP[7:0]:

The ICP[7:0] bits contain the pattern inserted in the payload octets of the idle or unassigned cell. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. Bit ICP[7] corresponds to the most significant bit of the octet, the first bit transmitted.

Register 0x63: TACP FIFO Control

Bit	Type	Function	Default
Bit 7	R/W	TXPTYP	0
Bit 6	R/W	TXPRTYE	0
Bit 5		Reserved	X
Bit 4	R	TXPRTYI	X
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	TCALEVEL0	0
Bit 0		Reserved	0

TCALEVEL0:

The active high TCA level 0 bit, TCALEVEL0 determines what output TCA indicates when it transitions low. When TCALEVEL0 is set to logic one, output TCA indicates that the transmit FIFO is full and can accept no more writes. When TCALEVEL0 is set to logic zero, output TCA indicates that the transmit FIFO is near full and can accept no more than four additional writes.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth. FIFO depth control may be important in systems where the cell latency through the TACP must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA is deasserted. TCA is asserted only after a complete cell has been read out; therefore, the current cell being read is included in the count. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

Note that FIFODP[1:0] only affects when TCA is asserted. All four cells of the FIFO may be filled before an over flow is declared.

It is not recommended that the FIFO depth be set to 1 cell. If a cell write is initiated only when TCA is asserted, half the bandwidth is lost to idle/unassigned cells. For minimum latency and maximum throughput, set the FIFO depth to 2 cells.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

TXPRTYI:

The TXPRTYI bit indicates if a parity error was detected on the TDAT[7:0] bus. This bit is cleared when this register is read. Odd or even parity is selected using the TXPTYP bit.

TXPRTYE:

The TXPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors on inputs TDAT[7:0] are indicated by the TXPRTYI bit and the INTB output. When set to logic zero, parity errors are indicated by the TXPRTYI bit but are not indicated on the INTB output.

TXPTYP:

The TXPTYP bit selects even or odd parity for input TXPRTY. When set to logic one input TXPRTY is the even parity bit for inputs TDAT[7:0]. When set to logic zero, inputs TXPRTY is the odd parity bit for inputs TDAT[7:0].

Register 0x64: TACP Transmit Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x65: TACP Transmit Cell Counter

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x66: TACP Transmit Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[15:0]:

The TCELL[18:0] bits indicate the number of cells read from the transmit FIFO and inserted into the SPE during the last accumulation interval. Idle/Unassigned cells inserted into the SPE are not counted.

A write to any one of the Transmit Cell Counter registers loads the registers with the current counter value and resets the internal 19 bit counter to 1 or 0.

The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid 200 ns after a transfer is triggered by a write to the transmit cell count register space.

The cell count can also be polled by writing to the S/UNI-LITE Master Reset and Identity / Load Meters register (0x00). Writing to register address 0x00 loads all the error counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x67: TACP Configuration

Bit	Type	Function	Default
Bit 7	R/W	TGFCE[3]	0
Bit 6	R/W	TGFCE[2]	0
Bit 5	R/W	TGFCE[1]	0
Bit 4	R/W	TGFCE[0]	0
Bit 3	R/W	FSEN	1
Bit 2	R/W	H4INSB	0
Bit 1	R/W	FIXBYTE[1]	0
Bit 0	R/W	FIXBYTE[0]	0

FIXBYTE[1:0]:

The FIXBYTE[1:0] bits identify the byte pattern inserted into fixed byte columns of the synchronous payload envelope.

FIXBYTE[1]	FIXBYTE[0]	BYTE
0	0	00H
0	1	55H
1	0	AAH
1	1	FFH

H4INSB:

The active low H4 insert enable, H4INSB bit determines the contents of the H4 byte in the outgoing SPE. If H4INSB is set to logic one, the H4 byte is set to the value of 00 hexadecimal. If H4INSB is set to logic zero, the H4 byte is set to the cell indicator offset value.

FSEN:

The active high fix stuff control enable, FSEN bit determines the payload mapping of ATM cells for STS-1 mapping. When FSEN is set to logic one, a fixed pattern is inserted into columns 30 and 59 of the Synchronous Payload Envelope (SPE). When FSEN is set to logic zero, ATM payload fills the entire SPE except the path overhead column.

TGFCE[3:0]:

The GFC enable bits, TGFCE[3:0], enable the insertion of the associated GFC bit by the TGFC serial input. If MFC[3] is a logic 1, first bit of the 4 bit serial sequence is inserted into the most significant GFC bit transmitted. Likewise, if MFC[0] is a logic 1, last bit of the sequence is inserted into the least significant GFC bit transmitted. If a bit is logic 0, the associated GFC bit value is derived from TDAT[7:0] in the case of an assigned cell, or from the Idle/Unassigned Cell Header Control register in the case of unassigned cells.

TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-LITE. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[7]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-LITE are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Test Mode Register Memory Map

Address	Register
0x00-0x7F	Normal Mode Registers
0x80	Master Test
0x81-0xFF	Reserved For Test

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x80: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-LITE test features. All bits, except PMCTST, are reset to zero by a reset of the S/UNI-LITE.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-LITE . While the HIZIO bit is a logic one, all output pins of the S/UNI-LITE except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-LITE for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-LITE to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit only has effect if the IOTST bit is a logic one. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-LITE for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-LITE microprocessor port becomes the test access port used to run the PMC

"canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic one.

Test Mode 0 Details

In test mode 0, the S/UNI-LITE allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register should be set to logic one.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one and the following addresses must be written with 00H: 91H, 95H, 99H, A1H, B1H, D1H and E1H. Reading the following address locations returns the values for the indicated inputs :

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
82H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
83H		TBYP	TGFC	XOFF	TSOC	TXPRTY	TWRENB	TFCLK
84H	RFCLK	RRDENB	TSEN	RATE[1]	RATE[0]	RBYP		

The following inputs can not be read using the IOTST feature: TRCLK+/-, RRCLK+/-, RXD+/-, ALOS+/-, D[7:0], A[7:0], ALE, CSB, WRB, RDB and RSTB.

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90H					RALM[2]	RFP[2]		
92H		INT[1]						
96H								TFPO
D0H	RSOC		RCA	RCP	RGFC		RXPRTY	INT[1]
D2H	RDAT[7]	RDAT[6]	RDAT[5]	RDAT[4]	RDAT[3]	RDAT[2]	RDAT[1]	RDAT[0]
E0H							RCP	

Notes:

1.) Bit INT corresponds to output INTB. INTB is an open drain output and should be pulled high for proper operation. Writing a logic one to the INT bit allows the S/UNI-LITE to drive INTB low. Writing a logic zero to the INT bit tristates the INTB output.

2.) RALM and RFP must be clocked by VCLK at least twice to become valid.

The following outputs can not be controlled using the IOTST feature: TXC+/-, TXD+/-, TCLK, RXDO+/-, RCLK, TCLK, D[7:0] and TCA.

OPERATION

Overhead Byte Usage

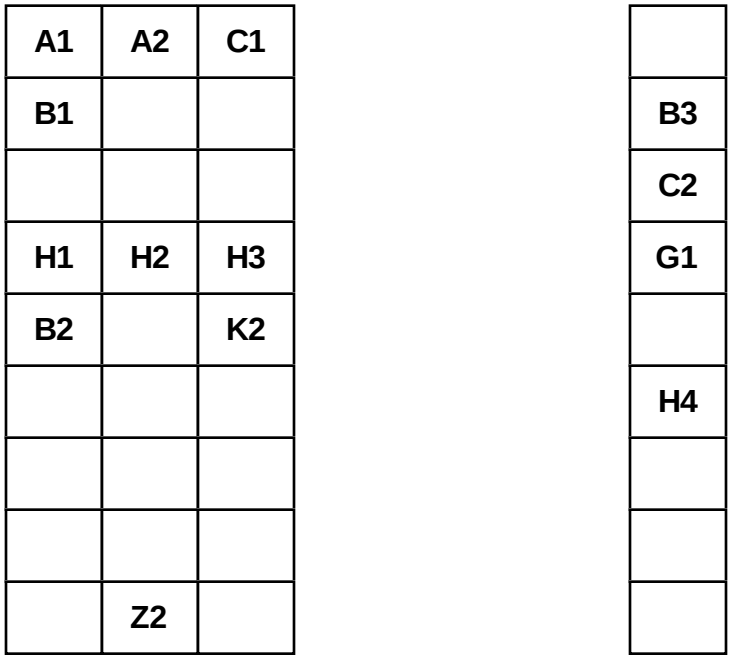
Under normal operating conditions, the S/UNI-LITE processes a subset of the complete transport overhead present in an STS-3c/STM-1 stream. The byte positions processed by the S/UNI-LITE are indicated in figures 8 and 9.

Fig. 8 STS-3c (STM-1) Overhead

A1	A1	A1	A2	A2	A2	C1	C1	C1	
B1									B3
									C2
H1	H1	H1	H2	H2	H2	H3	H3	H3	G1
B2	B2	B2				K2			
									H4
					Z2				

TRANSPORT OVERHEAD SOH | **PATH OVERHEAD POH**

Fig. 9 STS-1 Overhead



A1, A2: The frame alignment bytes (A1, A2) locate the SONET frame in the data stream. The transmitter inserts these bytes in the outgoing stream. The receiver searches for the A1, A2 bit sequence in the incoming stream. A1 and A2 are not scrambled by the frame synchronous SONET scrambler.

C1: The identification bytes identify the individual STS-1s in the byte interleaved STS-3c stream. The sequence 0x01, 0x02, 0x03 is inserted in the transmit direction. (Only 0x01 is transmitted in STS-1 mode.) These bytes are ignored in the receive direction. C1 is not scrambled by the frame synchronous SONET scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function. B1 is calculated over all bits of the previous frame after scrambling. B1 is placed in the current frame before scrambling. Receive B1 errors are accumulated in an error event counter.

H1, H2: The pointer value bytes locate the start of the synchronous payload envelope (SPE) in the SONET/SDH frame. In the transmit direction, a fixed pointer value of 522 decimal, with a normal new data flag indication, is inserted in the first H1-H2 pair. The concatenation indication is inserted in the remaining two H1-H2 pairs in STS-3c mode. In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function. B2 is calculated over all bits of the line overhead, and the SPE capacity of the previous frame before scrambling. B2 is placed in the current frame before scrambling. Receive B2 errors are accumulated in an error event counter.

K2: The K2 byte is used to identify line layer maintenance signals. In the transmit direction, line RDI is inserted by setting bits 6, 7, and 8 of the K2 byte to the pattern '110'. Line AIS is inserted by overwriting the line overhead (including bits 6, 7, and 8 of the K2 byte), and the SPE with the all ones pattern before scrambling. In the receive direction, bits 6, 7, and 8 of the K2 byte are examined to determine the presence of the line AIS, and the line RDI maintenance signals.

Z2: The growth byte provides a line far end block error function for remote performance monitoring. In the transmit direction, the number of B2 errors detected in the previous interval is inserted. This number has 25 legal values, namely 0 to 24 errors. In the receive direction, a legal Z2 byte value is added to the line FEBE event counter.

B3: The path bit interleaved parity byte provides a path error monitoring function. B3 is calculated over all bits of the SPE capacity of the previous frame before scrambling. B3 is placed in the current frame before scrambling. Receive B3 errors are accumulated in an error event counter.

C2: The path signal label byte indicates the content of the SPE. A hexadecimal value of 13 is transmitted, which indicates "Mapping for ATM."

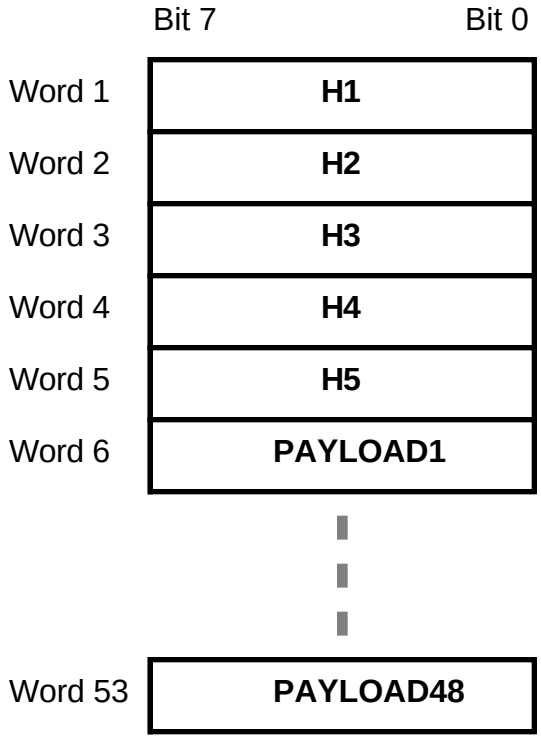
G1: The path status byte provides a path far end block error function, and provides control over the path remote defect indication maintenance signal. In the transmit direction, path remote alarm indication (RDI) and the number of B3 errors detected in the previous interval are inserted. This number has 9 legal values, namely 0 to 8 errors. In the receive direction, a legal G1 byte value is added to the path FEBE event counter. In addition, the path remote defect indication is detected.

H4: The cell offset indicator byte indicates the offset in bytes between itself, and the first cell boundary following the H4 byte. This byte is inserted correctly in the transmit direction, and is ignored in the receive direction.

Cell Data Structure

ATM cells may be passed to/from the S/UNI-LITE using a 9 bit data structure, consisting of a start of cell indication and an 8-bit wide word. The data structure is shown in the figure 10:

Fig. 10 Data Structure



Fifty-three 8-bit words are contained in this data structure. Bit 7 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first cell header octet). Word 5 of this structure contains the HCS octet.

In the receive direction, cells containing uncorrectable header errors are dropped while the HCSPASS bit in the RACP Control/Status Register is set to logic zero. No header status information is passed within this data structure; error free headers, and "corrected" headers are passed while HCSPASS is a logic zero. Error free headers, "corrected" headers, and headers containing uncorrectable errors are passed while HCSPASS is a logic one.

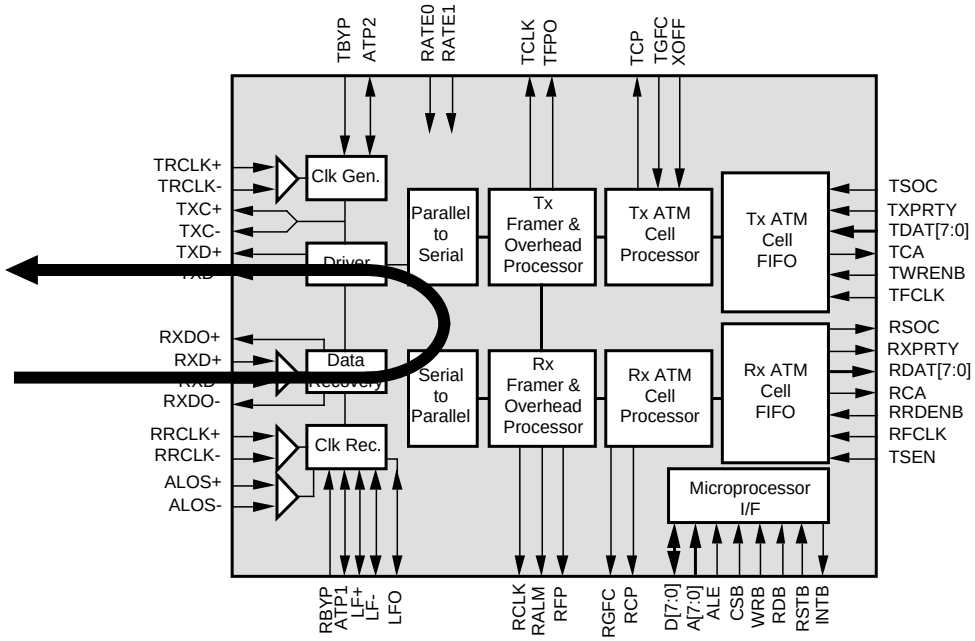
In the transmit direction, the HCS bit in the TACP Control Register determines whether the HCS is calculated internally, or is inserted directly from Word 5.

Loopback Operation

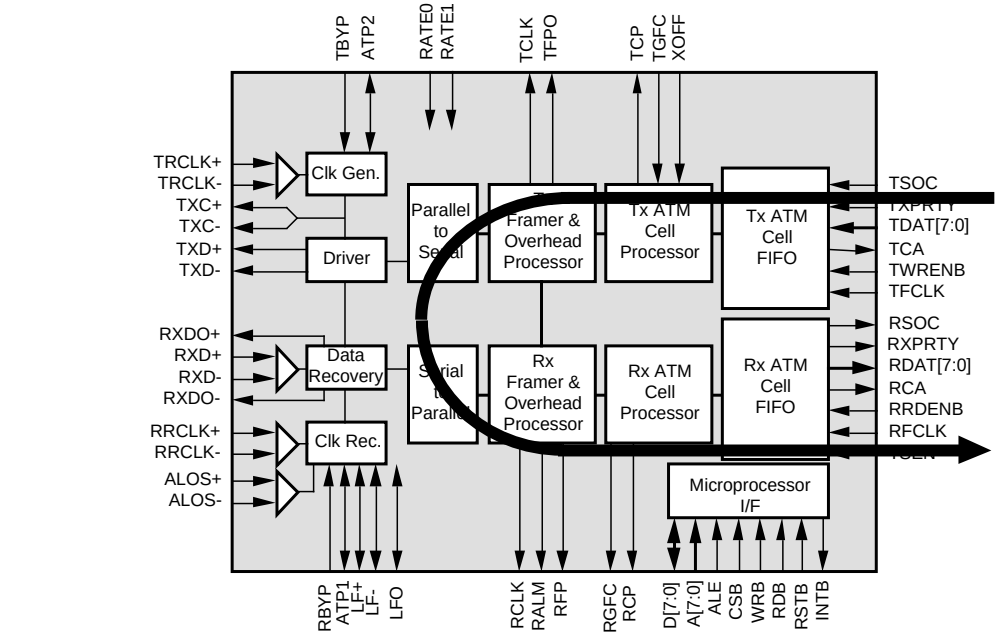
The S/UNI-LITE supports two loopback functions: line loopback, and diagnostic loopback. The diagnostic loopback connects the high speed transmit data and clock

to the high speed receive data and clock as shown in the partial block diagram in figure 11. The line loopback connects the high speed receive data and clock to the transmit data and clock. Diagnostic loopback and line loopback are activated by bits contained in the S/UNI-LITE Master Control Register.

Fig. 11 Loopback Operation



HIGH SPEED LINE LOOPBACK

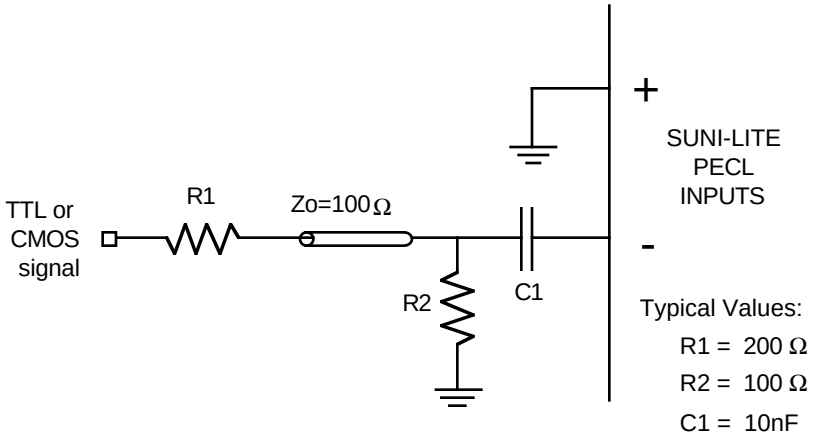


DIAGNOSTIC LOOPBACK

Driving Differential Inputs Single Ended

In some applications it may be more cost effective or technically desirable to drive the RRCLK+/-, TRCLK+/- or ALOS+/- inputs with a single ended TTL or CMOS signal. Figure 12 illustrates the suggested configuration to achieve this. Note that the RXD+/- inputs do not support single ended operation and must always be driven by a differential source.

Fig. 12 Single Ended Driving Differential Inputs



The positive input should be grounded. The negative input should be A.C. coupled to an attenuated TTL or CMOS signal. The peak to peak voltage should be between 800 mV and 2.5 V. The values of the components are not critical and may be modified for specific applications.

A similar arrangement can be used for single ended ECL or pseudo-ECL signals. Resistor R1 should be omitted. A pseudo-ECL signal may be D.C. coupled (as is required for ALOS) by replacing C1 with a short.

This configuration logically inverts the input signal.

Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines *must* be followed in order to ensure proper operation:

1.) Connect digital and analog grounds together at only one point close to the connector where ground is brought into the card.

2.) Provide separate +5 volt analog transmit, +5 volt analog receive, and +5 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +5 volts is brought to the card.

3.) Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

4.) Ferrite beads are recommended for TAVD1, TAVD2, RAVD1 and RAVD2.

5.) Separate high-frequency decoupling capacitors are recommended for each analog power (TAVD1, TAVD2, RAVD1 and RAVD2) pin as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into the reference circuitry powered by TAVD1 and RAVD1.

6.) The high speed serial streams (TXD+/- and RXD+/) must be routed with controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device.

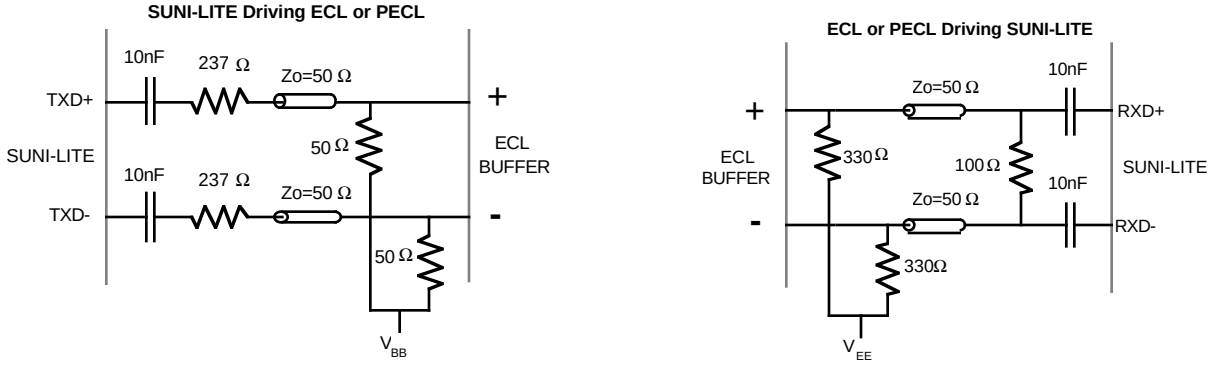
Interfacing to ECL or PECL Devices

Although the TXD+/- outputs are TTL compatible, only a few passive components are required to convert the signals to ECL (or PECL) logic levels. Figure 13 illustrates the recommended configuration. The capacitors AC couple the outputs so that the ECL inputs are free to swing around the ECL bias voltage (V_{BB}). The combination of the 237 Ω and 50 Ω resistors divides the voltage down to a nominally 800mV swing. The 50 Ω resistors also terminate the signals.

Similarly, the RXD+/- inputs to the S/UNI-LITE are AC coupled as shown in Figure 13. The S/UNI-LITE inputs are self-biasing to improve operating speed and waveform symmetry. For this reason, the DC blocking capacitors are always required, even when interfacing to PECL drivers. The only exception are the ALOS+/- inputs which must be DC coupled because of their low frequency content.

The D.C blocking capacitors shown in figure 13 should be ceramic in type. A minumum value of 10 nF is recommended.

Fig. 13 Interfacing S/UNI-LITE to ECL or PECL



Clock Recovery

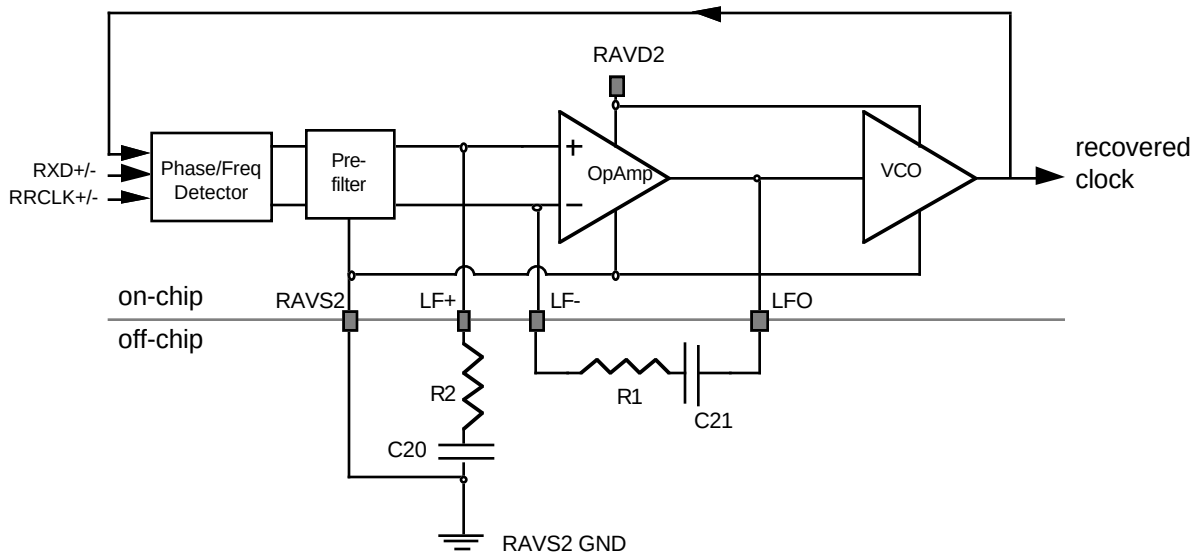
Figures 14a) and 14b) are abstractions of the clock recovery phase lock loop illustrating the connections to external components.

Figure 14a illustrates the asymmetrical loop filter application where the external passive components (R1, R2, C1, C2) are set to different values to account for the finite output impedance of the integral op-amp in the S/UNI-LITE. The asymmetrical loop filter circuit does not have good jitter transfer properties and is not recommended for new designs.

Figure 14b illustrates the unity gain buffer loop filter application where the integral op-amp output is buffered through a unity gain amplifier to minimize the effect of its finite output impedance on the transfer function of the PLL. The unity gain buffer loop filter circuit exceeds SONET/SDH jitter tolerance and jitter transfer specifications and is recommended for new designs.

Additional analysis of jitter transfer and jitter tolerance issues for the S/UNI-LITE can be found in PMC's ATM Design Notes "Meeting SONET/SDH WAN Interface Jitter Transfer Requirements with the S/UNI-LITE", PMC-950139

Fig. 14a Clock Recovery Circuit - Asymmetrical Loop Filter (recommended for designs requiring maximum jitter tolerance)

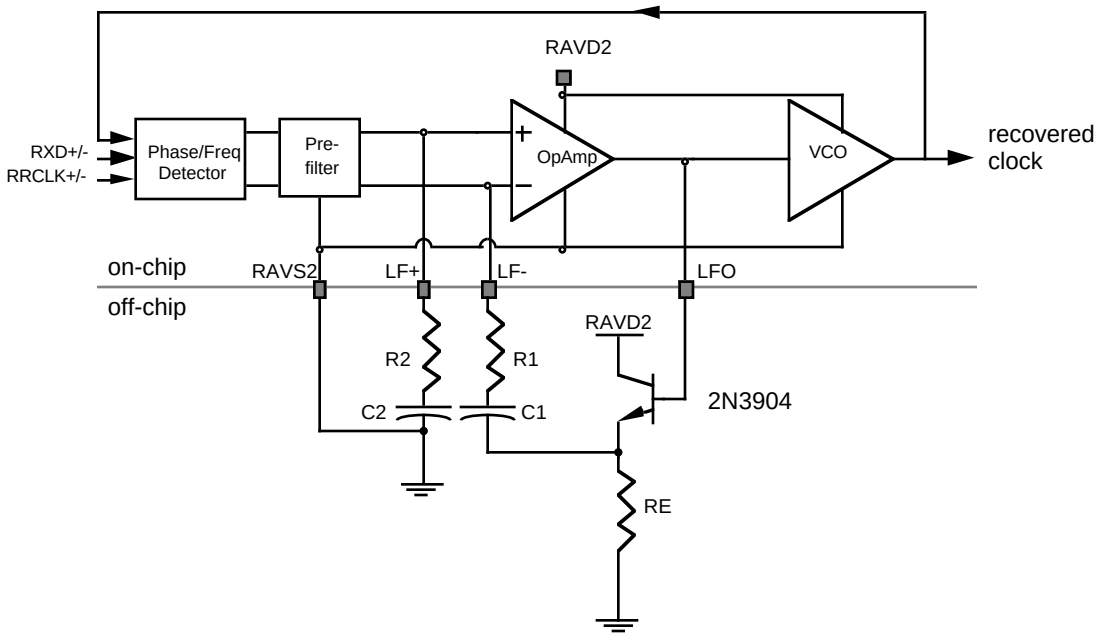


Different component values may be selected to optimize the loop behavior for each line rate:

Line Rate (Mbit/s)	R1 (Ω)	R2 (Ω)	C20, C21 (μF)
155.52 & 51.84	200	412	0.47
25.92 & 12.96	200	412	2.2

All resistors are 1% metal film (1/4 watt) resisters. Unpolarized capacitors are recommended.

Fig. 14b Clock Recovery Circuit - Unity Gain Buffer Loop Filter (recommended for designs requiring BISDN-UNI jitter transfer)



Line Rate (Mbit/s)	R1 (Ω±1%)	R2 (Ω±1%)	C1, C2 min (μF)	RE (Ω±1%)
155.52	68.1	90.9	4.7	100
51.84	68.1	90.9	15	100

The capacitors (C1, C2) determine the amount of "peaking" in the jitter transfer curve. The capacitor values can be ±10%. The capacitors should be non-polarized because when the S/UNI-LITE is held in reset, the capacitors are reverse-biased at approximately 2.0V. Also, for some process extremes, the capacitors may operate with a D.C. reverse-bias of up to 1.0V.

The recommended values for the capacitors are not readily available in non-polarized versions. Therefore, two polarized capacitors can be connected "back-to-back" (in series, anode-to-anode) to implement each capacitance in Figure 14b. Since these back-to-back capacitors will be in series, they should be of twice the value of the desired capacitance. This back-to-back configuration effectively creates a "bi-polar" capacitor.

Clocking Options

The S/UNI-LITE supports several clocking modes. Figure 16 is an abstraction of the clocking topology. The external connections and application for each of the options (A and B) is illustrated in Figure 17.

Fig. 16 Conceptual Clocking Structure

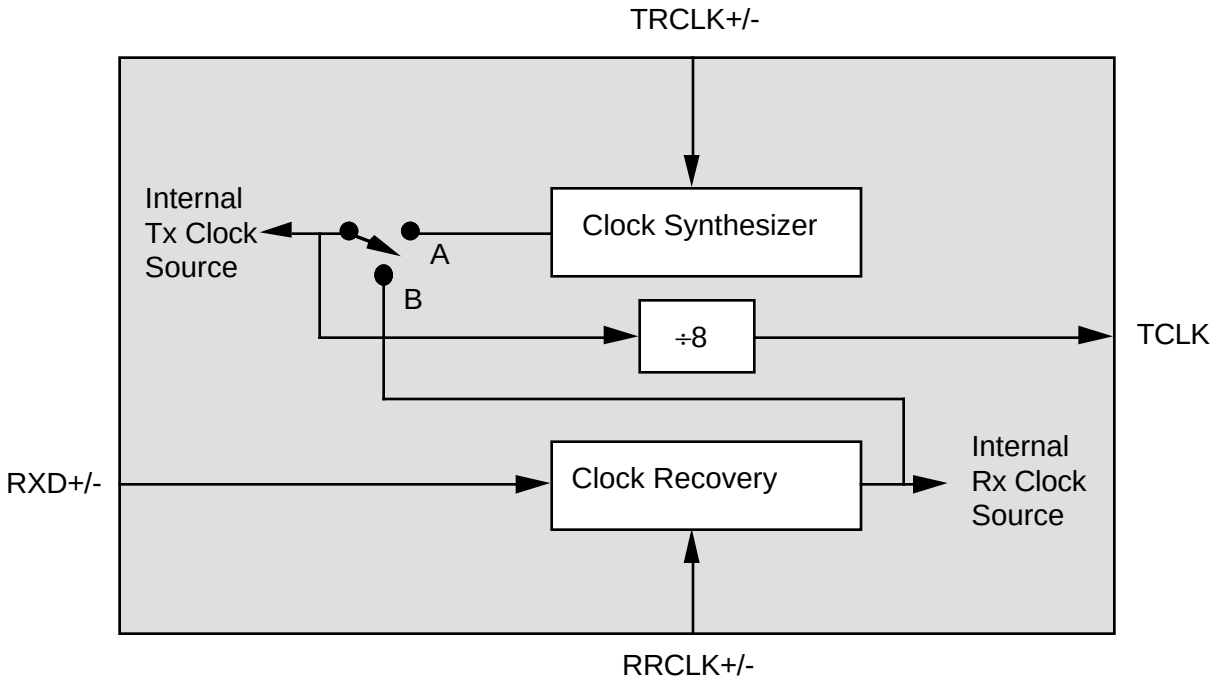
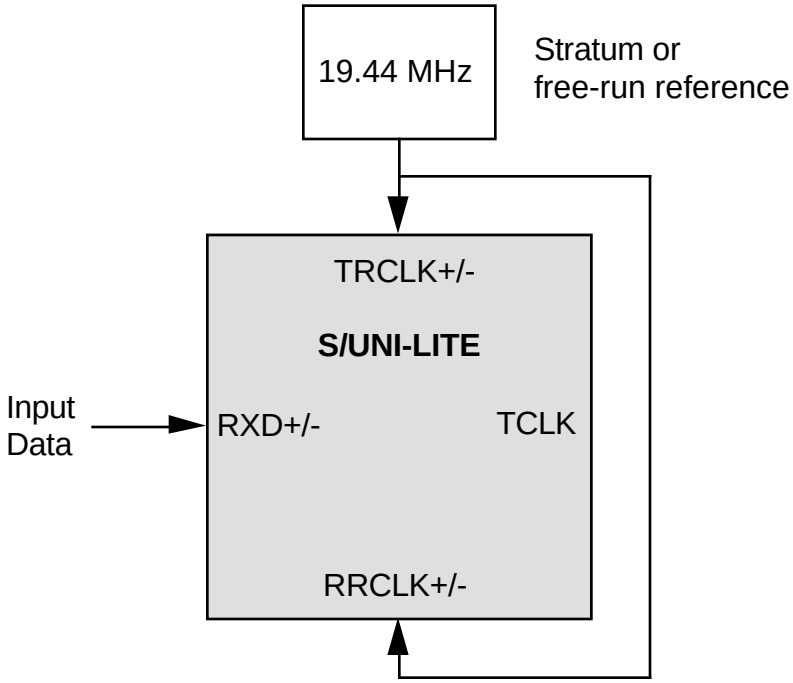


Fig. 17a Mode A: Clock Synthesis



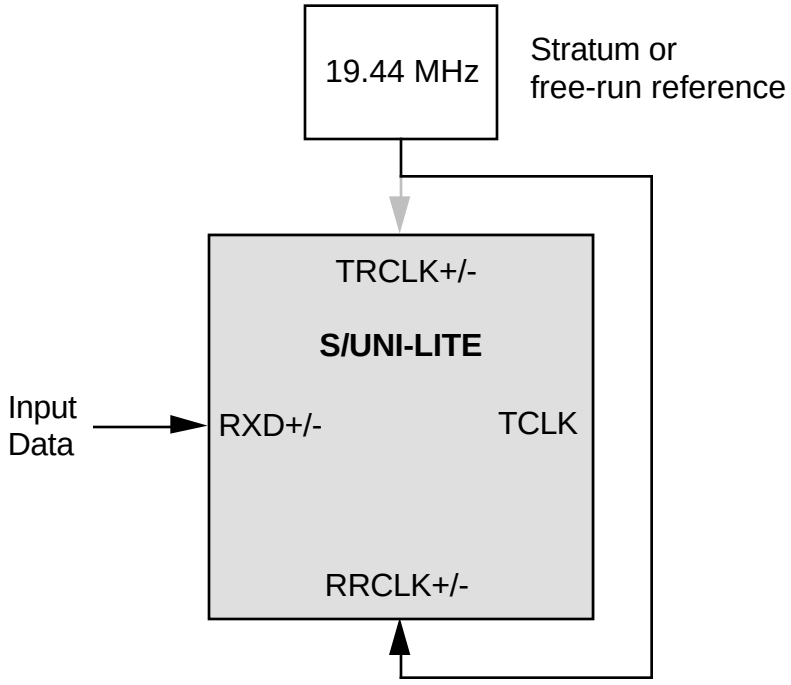
Mode A is recommended for all public user network interfaces (UNIs) and for private UNIs and private network node interfaces (NNIs) that are not synchronized to the recovered clock.

The transmit clock in a public UNI must conform to SONET Network Element (NE) requirements specified in Bellcore GR-253-CORE. These requirements include jitter generation, short term clock stability, phase transients during synchronization failure, and possibly holdover. The 19.44 MHz clock source is typically a VCXO (or temperature compensated VCXO) locked to a primary reference source for public UNI applications. The accuracy of this clock source should be within ±20 ppm of 19.44 MHz to comply with the SONET/SDH network element free-run accuracy requirements.

The transmit clock in a private UNI or a private NNI may be locked to an external reference or may free-run. The simplest implementation requires a free-running 19.44 MHz, ±50 ppm, oscillator.

Mode A is selected by clearing the LOOPT bit of the Master Control register. TRCLK+/- is multiplied by eight to become the 155.52 MHz transmit clock. The clock synthesizer does not attenuate jitter below 500 kHz, so TRCLK+/- must be jitter free. The source of TRCLK+/- may also be used as the clock recovery reference, RRCLK+/-.

Fig. 17b Mode B: Loop Timing



Mode B is recommended for private UNIs and private NNIs that require synchronization to the recovered clock. The clock recovery unit attenuates jitter above 130 kHz for STS-3c and above 40 kHz for STS-1.

Mode B is selected by setting the LOOPT bit of the Master Control register. The TRCLK+/- inputs are ignored. Normally, the transmit clock is locked to the receive data. In the event of a loss of signal condition, the transmit clock is synthesized from RRCLK+/-.

FUNCTIONAL TIMING

Drop Side Receive Interface

Fig. 18a Receive FIFO Empty Option (RCALEVEL0=1)

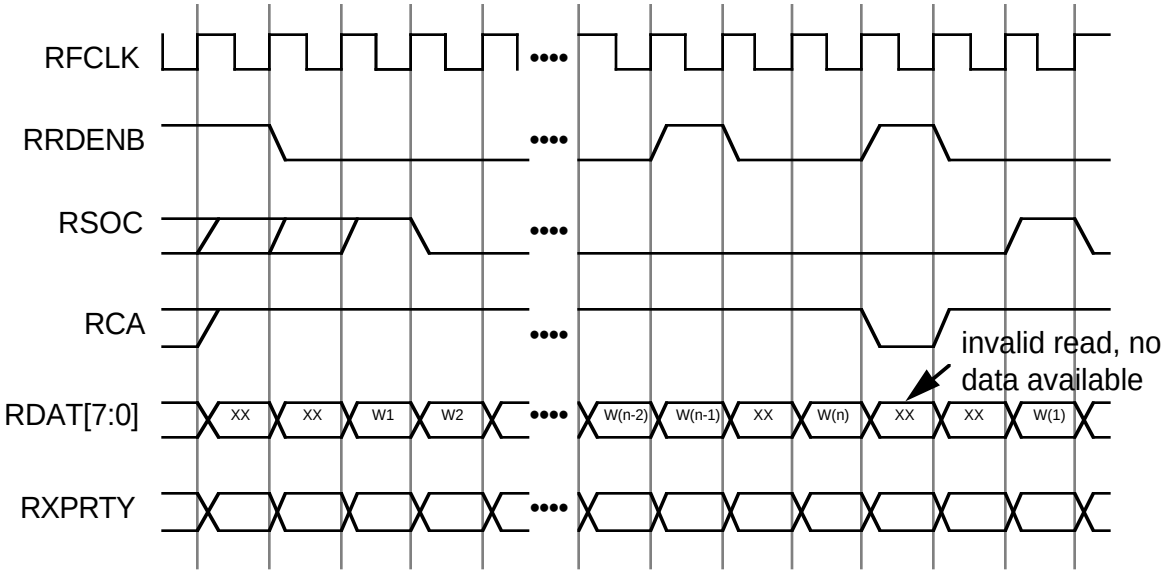
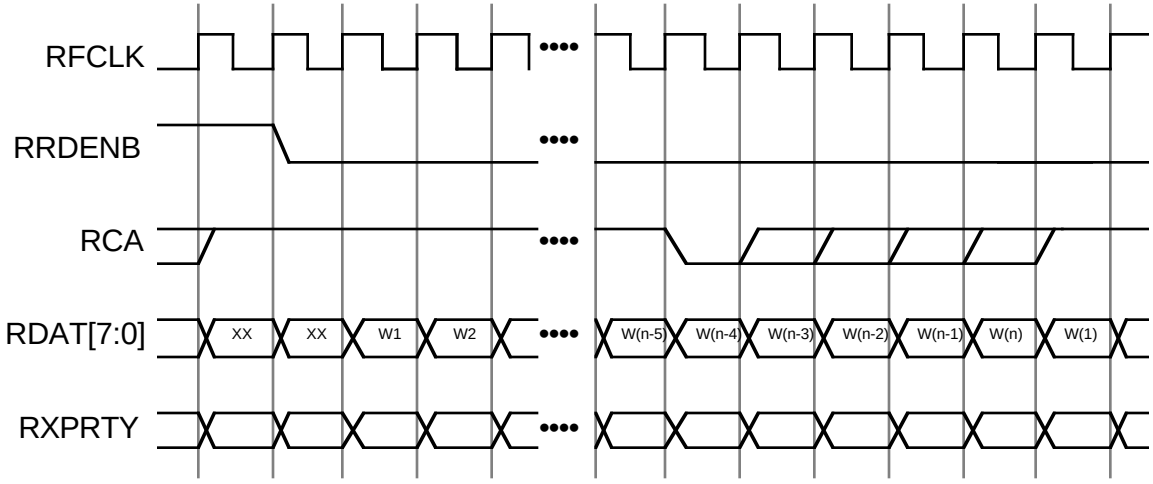


Fig. 18b Receive FIFO Near Empty Option (RCALEVEL0=0)



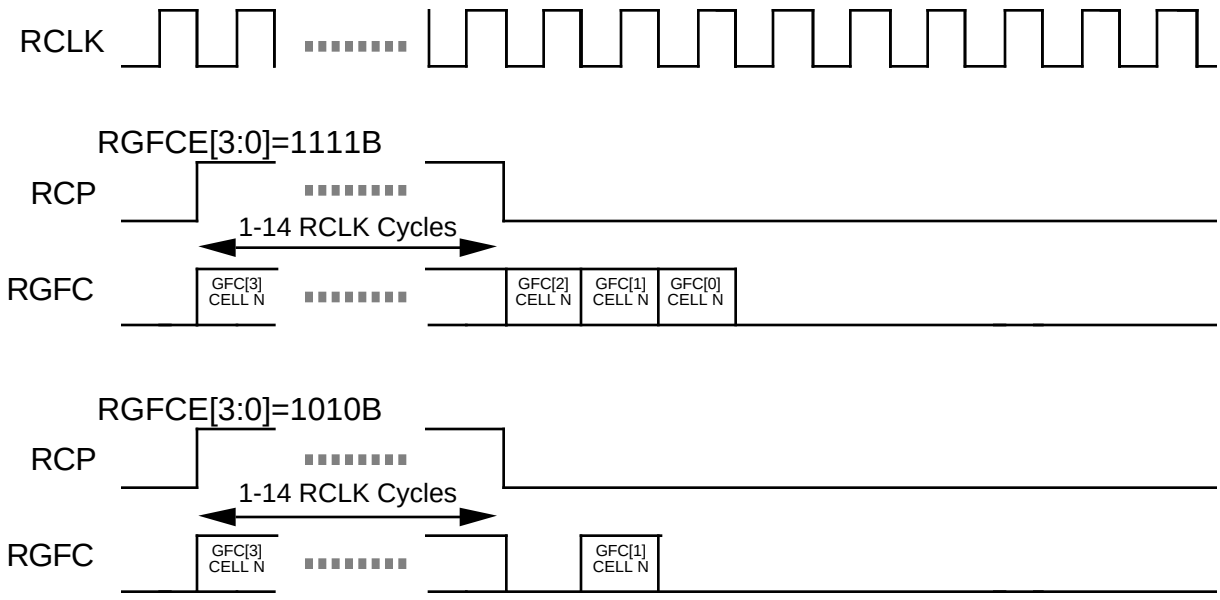
The S/UNI-LITE indicates that a cell is available by asserting the receive cell available signal, RCA. RCA remains high until the internal FIFO is near empty or empty. Near empty implies that the ATM Layer device can initiate at most four additional reads. The ATM Layer device indicates, by asserting the RRDENB signal, that the data on the RDAT[7:0] bus during the next RFCLK cycle will be read from the S/UNI-LITE.

Figure 18a illustrates the Receive FIFO empty option. RCA transitions low when the last word of the last cell is available on the RDAT[7:0] bus. The RDAT[7:0] bus, RXPRTY and RSOC are valid in cycles for which RCA is high and RRDENB was low is the previous cycle. If the ATM Layer device requests a read while RCA is deasserted, the PHY layer device will ignore the additional reads.

Figure 18b illustrates the Receive FIFO near empty option. RCA transitions low four words before the last word of the last cell is read from the S/UNI-LITE. RCA remains low for a minimum of one RFCLK clock cycle and then can transition high to indicate that there are additional cells available from the PHY layer device.

Once RCA is deasserted and has been sampled, the ATM Layer device can issue no more than four reads. If the ATM Layer device issues more reads than the allowable number, and RCA remains deasserted throughout, the PHY layer device will ignore the additional reads.

Fig. 19 Receive GFC Serial Link

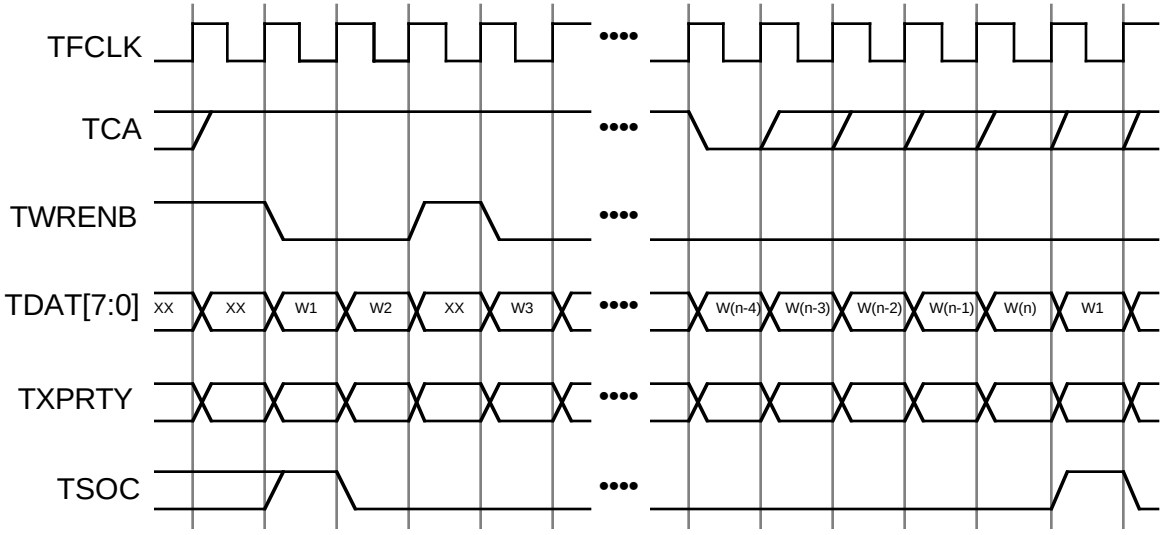


The Receive GFC Serial Link Diagram (Figure 19) illustrates the operation of the receive generic flow control, RGFC, and receive GFC control pulse, RCP, outputs. The first RGFC bit position, which is coincident with the RCP being high, contains the

first GFC bit received and corresponds to the first bit of the cell. The RCP pulse width varies between 1 and 14 RCLK cycles depending on the alignment of the ATM cell and the SONET/SDH transport and path overheads. Extraction of the GFC[3:0] bits is controlled by the four RGFC enable (RGFCE[3:0]) bits in the RACP Configuration register. The output value in each GFC bit position can be forced low by setting the corresponding RGFCE bit to zero. The serial link is inactive (forced low) if the S/UNI-LITE is out of cell delineation or if the current cell contains an uncorrectable header.

Drop Side Transmit Interface

Fig. 20 Transmit FIFO



As shown in Figure 20, the S/UNI-LITE indicates that there is space available for a full cell in its internal FIFO by asserting the transmit cell available signal, TCA. TCA remains asserted until the transmit FIFO is almost full. Almost full implies that the S/UNI-LITE can accept at most an additional four writes after the current write.

If TCA is asserted and the ATM Layer device is ready to write a byte, it should assert TWRENB low and present the byte on the TDAT[7:0] bus. If the presented byte is the first byte of a cell, the ATM Layer device should also assert signal TSOC. At any time, if the ATM Layer device does not have a byte to write, it can deassert TWRENB.

When TCA is deasserted and it has been sampled, the ATM Layer device can write no more than four bytes to the PHY layer device. If the ATM Layer writes more than four bytes and TCA remains deasserted throughout, the S/UNI-LITE will indicate an error condition and ignore additional writes until it asserts TCA again.

Fig. 21 Transmit GFC Serial Link

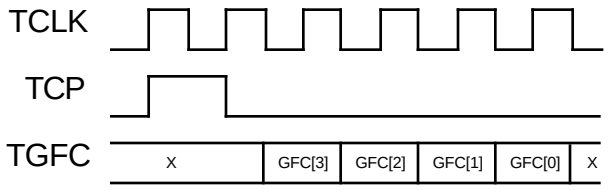


Figure 21 illustrates the transmit GFC serial link which provides the ability to insert flow control information downstream of the transmit FIFO. The TCP output pulses high once per transmitted cell to initiate the transfer on the GFC bits. GFC[3] is the most significant bit and is transmitted first. The TACP Configuration register controls the insertion of each serial bit. If the insertion is disabled, the default GFC value is inserted. For unassigned cells, the default is the contents of the TACP Idle/Unassigned Cell Header Pattern register. For assigned cells, the default is the value received from TDAT[7:0].

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±500 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C
Power Dissipation	1 W

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = 5 V ±5%
(Typical Conditions: T_A = 25°C, V_{DD} = 5 V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{PIL}	Input Low Voltage (ALOS+, ALOS- Only)	AVD -1.8		AVD -1.6	Volts	Guaranteed ALOS+, ALOS- Input LOW Voltage referenced to RAVD
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{PIH}	Input High Voltage (ALOS+, ALOS- Only)	AVD -1.0		AVD -0.8	Volts	Guaranteed ALOS+, ALOS- Input HIGH Voltage referenced to RAVD
$V_{PISWING}$	Input Swing (RRCLK+, RRCLK-, RXD+, RXD-, TRCLK+, TRCLK- Only)	0.6		1.0	Volts	Input swing assuming ECL/PECL signal AC coupled as illustrated in figure 13
V_{OL}	Output or Bidirectional Low Voltage (TTL Only)		0.1	0.4	Volts	V_{DD} = min, I_{OL} = -8 mA for RDAT[7:0], RXPRTY, RCP, RGFC, RSOC, RCA, TCA, TCP, TCLK, and RCLK, and 4 mA for all others, Note 3
V_{OH}	Output or Bidirectional High Voltage (TTL Only)	2.4	4.7		Volts	V_{DD} = min, I_{OH} = 8 mA for RDAT[7:0], RXPRTY, RCP, RGFC, RSOC, RCA, TCA, TCP, TCLK, and RCLK, and 4 mA for all others, Note 3

V_{TXOL}	Output or Bidirectional Low Voltage (TXD+, TXD-, TXC+, TXC- Only)			0.4	Volts	V_{DD} = min, I_{OL} = -6 mA for TXD+, TXD-, TXC+, and TXC-, Note 5
V_{TXOH}	Output or Bidirectional High Voltage (TXD+, TXD-, TXC+, TXC- Only)	3.9			Volts	V_{DD} = min, I_{OH} = 6 mA for TXD+, TXD-, TXC+, and TXC-, Note 5
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			1.0	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10		+10	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{ILPD}	Input Low Current	-10		+10	µA	V_{IL} = GND, Notes 4, 3
I_{IHPD}	Input High Current	-200	-83	-20	µA	V_{IH} = V_{DD}, Notes 4, 3
I_{IL}	Input Low Current	-10		+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10		+10	µA	V_{IH} = V_{DD}, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF

I_{DDOP}	Operating Current Processing Cells		156	185	mA	V_{DD} = 5.25 V, Outputs Unloaded, TXD+/- = RXD+/- =155.52 Mbit/s,
			85	110	mA	TXD+/- = RXD+/- =51.84 Mbit/s,

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bidirectional pin with internal pull-down resistor.
5. The values for V_{TXOL} and V_{TXOH} ensure a minimum 600 mV swing at the ECL buffer input when the circuit shown in figure 13 is used to attenuate TXD+, TXD-, TXC+, and TXC-.
6. Typical values are not production tested.

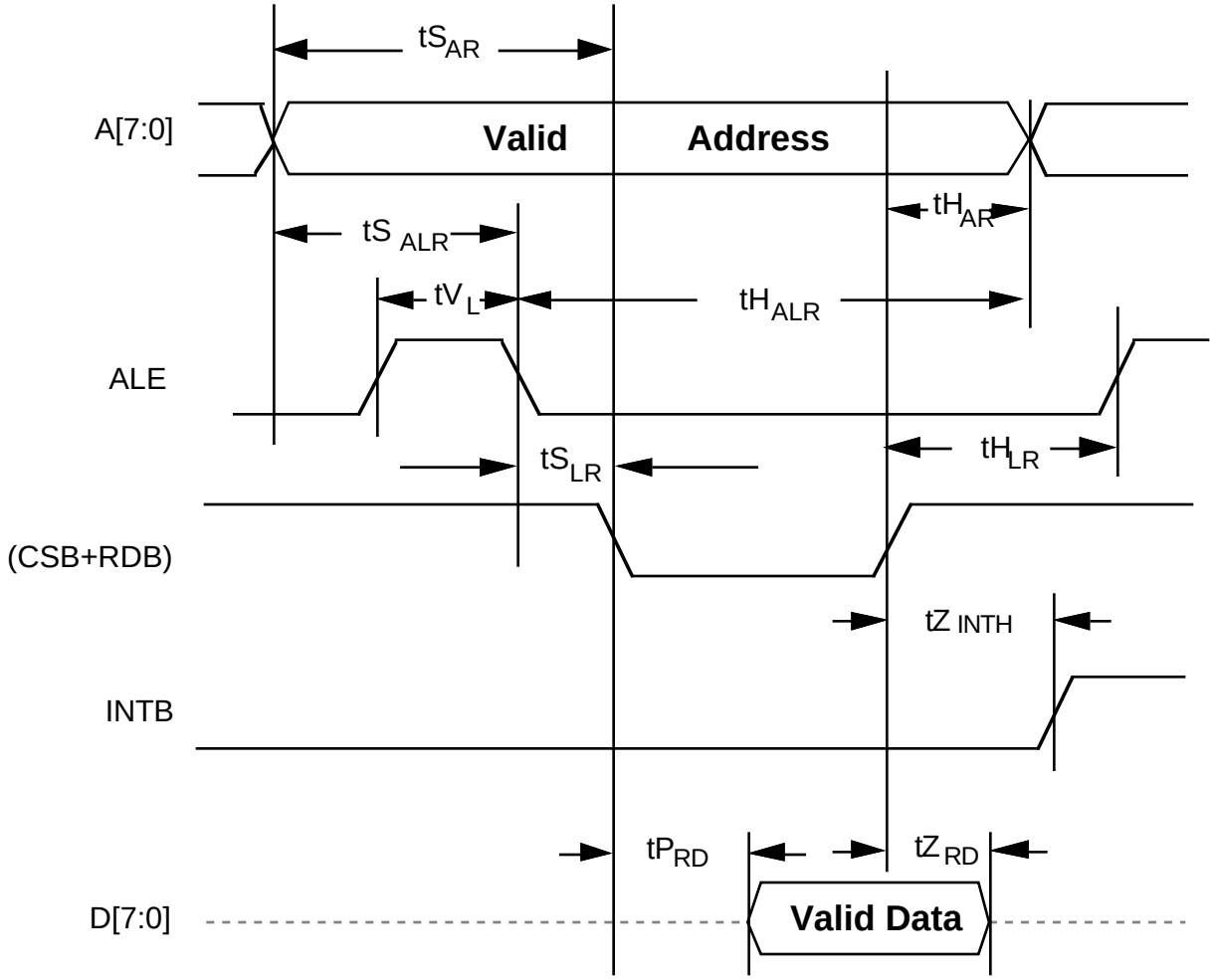
MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±5%)

Microprocessor Interface Read Access (Fig. 22)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Fig. 22 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.

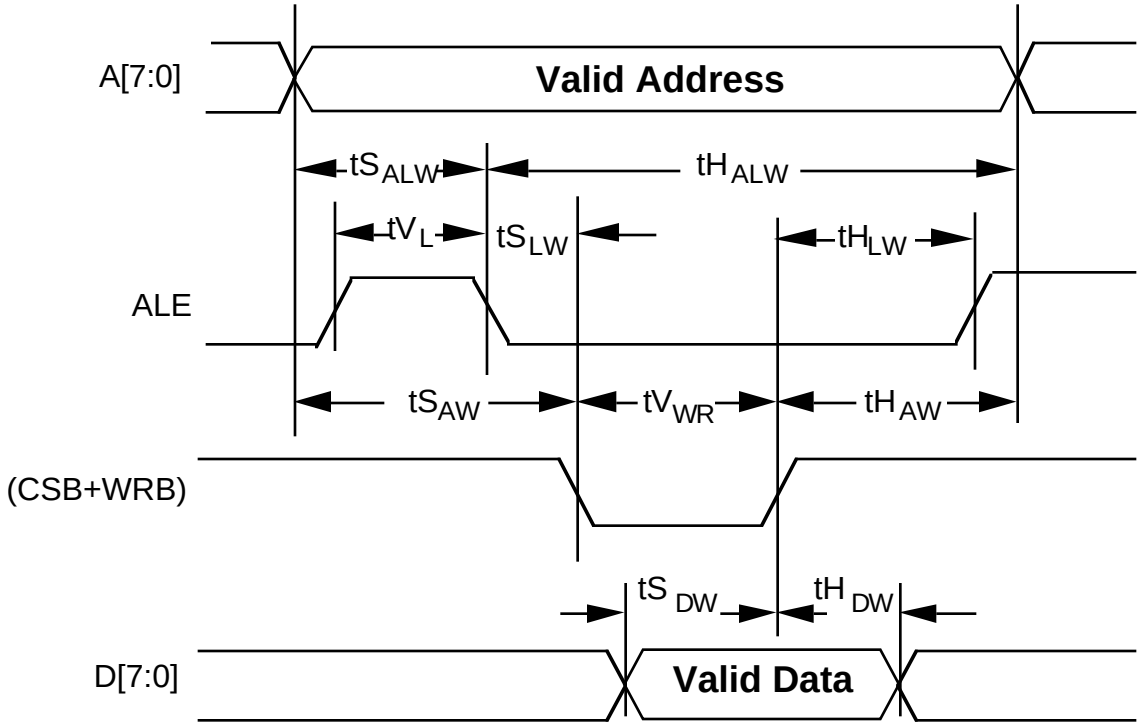
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Microprocessor Interface Write Access (Fig. 23)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 23 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

S/UNI-LITE TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±5%)

Line Side Receive Interface

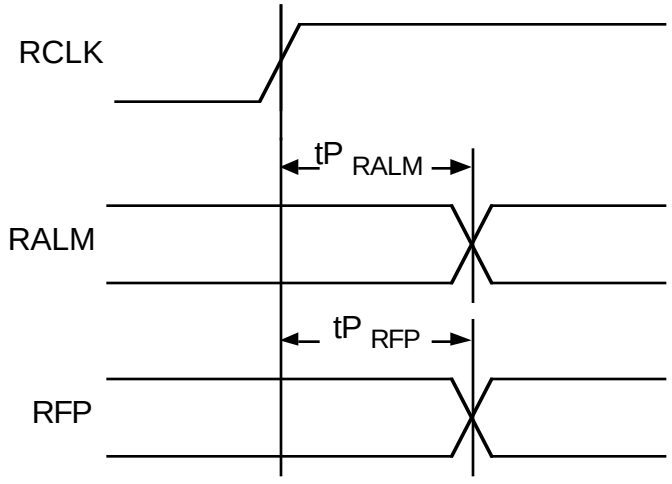
Symbol	Description	Min	Max	Units
	RRCLK+/RRCLK- Duty Cycle 19.44 or 6.48 MHz	30	70	%
	RRCLK+/RRCLK- Frequency Tolerance†	-20	+20	ppm

† The specification may be relaxed to +/- 50 ppm if the S/UNI-LITE is not loop timed, or for LAN applications that do not require this timing accuracy. If loop timing is enabled, the specified tolerance is required to meet the SONET free run accuracy specification under loss of signal conditions.

Receive Alarm Output (Fig. 24)

Symbol	Description	Min	Max	Units
tP_{RALM}	RCLK High to RALM Valid	2	20	ns
tP_{RFP}	RCLK High to RFP Valid	2	20	ns

Fig. 24 Receive Alarm Output Timing

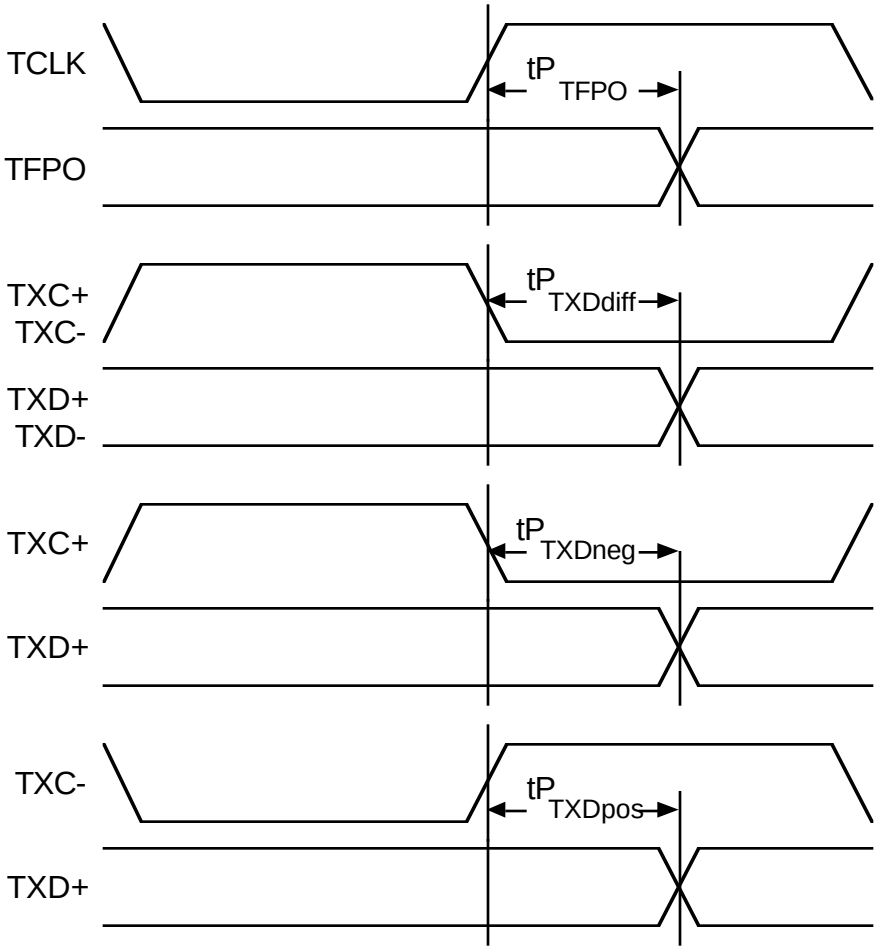


Line Side Transmit Interface (Fig. 25)

Symbol	Description	Min	Max	Units
	TRCLK+/TRCLK- Duty Cycle 19.44 or 6.48 MHz (TBYP low)	30	70	%
	TRCLK+/TRCLK- Frequency Tolerance†	-20	+20	ppm
tP_{TFPO}	TCLK High to TFPO Valid	3	20	ns
$tP_{TXDdiff}$	TXC+/TXC- Low to TXD+/TXD- Valid	-2	2	ns
tP_{TXDneg}	TXC+ Low to TXD+ Valid	-3	2	ns
tP_{TXDpos}	TXC- High to TXD+ Valid	-2	3	ns

† The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The specified tolerance is required to meet the SONET free run accuracy specification.

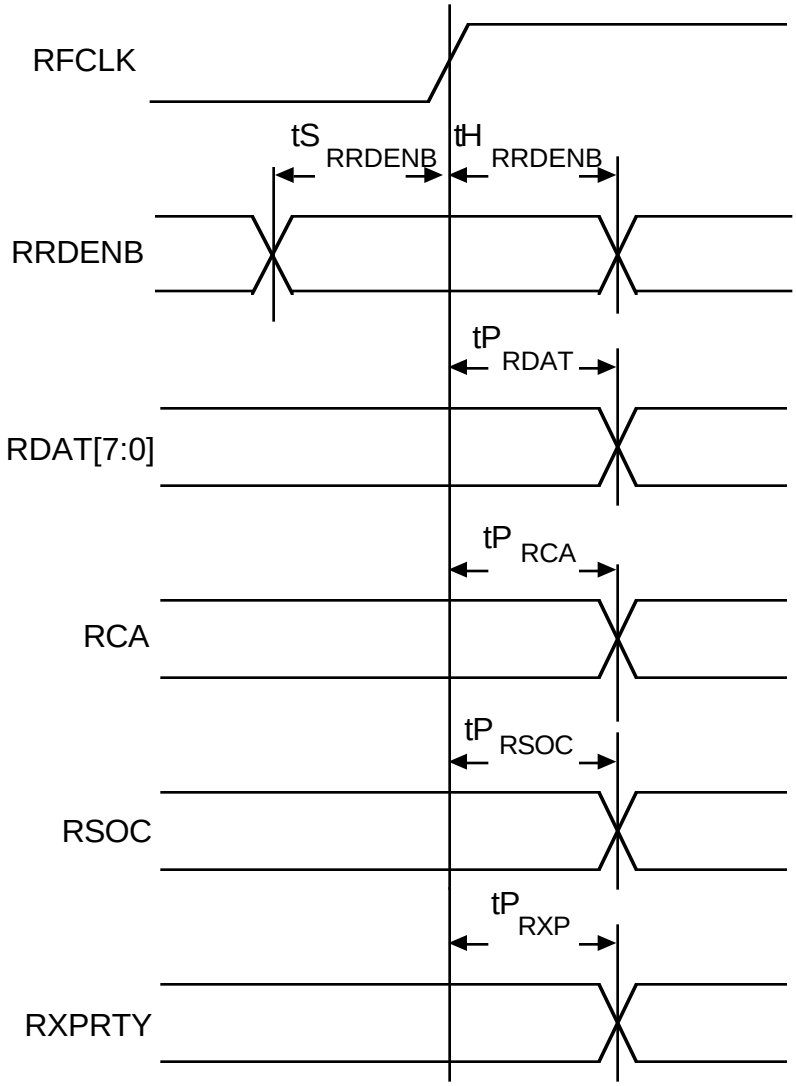
Fig. 25 Line Side Transmit Interface Timing



Drop Side Receive Synchronous Interface (Fig. 26)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		33	MHz
	RFCLK Duty Cycle	40	60	%
tS_{RRDENB}	RRDENB to RFCLK High Setup	10		ns
tH_{RRDENB}	RFCLK High to RRDENB Hold	1		ns
tP_{RDAT}	RFCLK High to RDAT[7:0] Valid	2	20	ns
tP_{RXP}	RFCLK High to RXPRTY Valid	2	20	ns
tP_{RCA}	RFCLK High to RCA Valid	2	20	ns
tP_{RSOC}	RFCLK High to RSOC Valid	2	20	ns

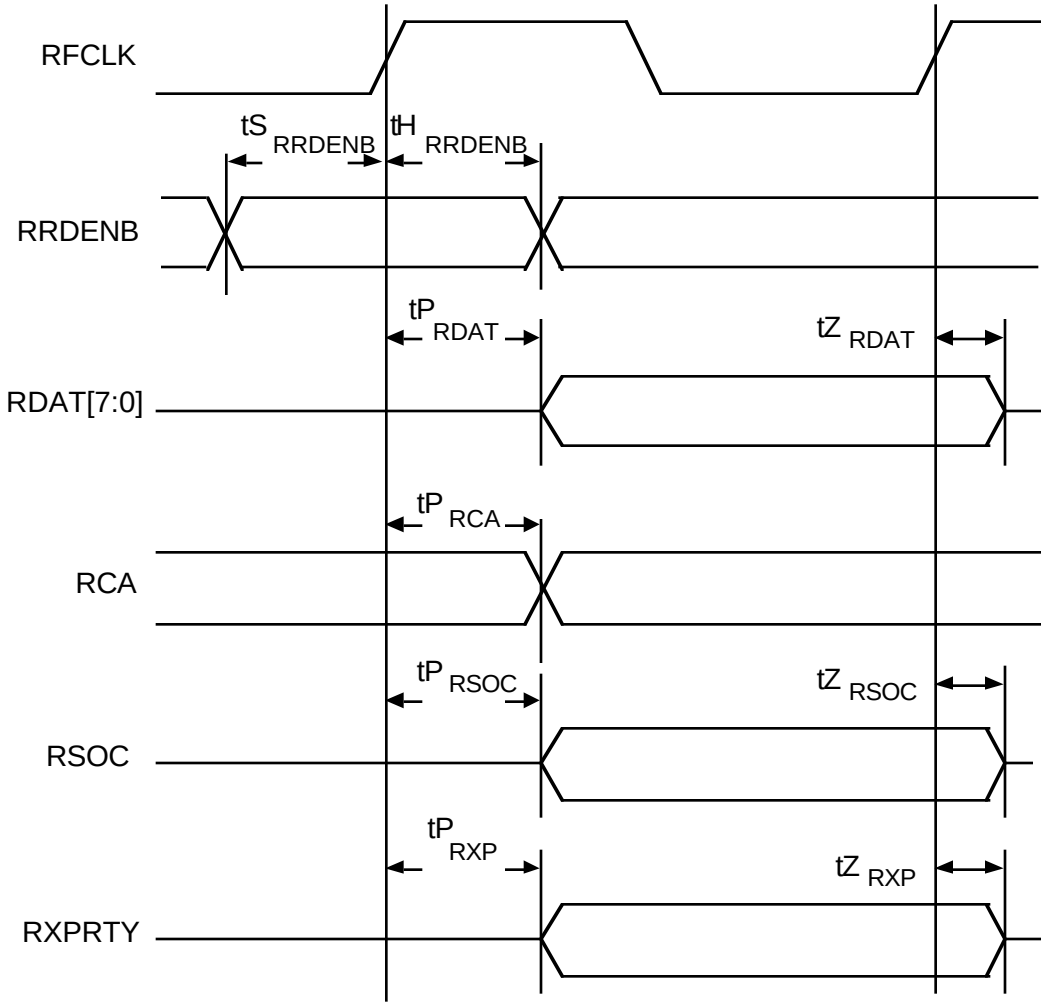
Fig. 26 Drop Side Receive Synchronous Interface Timing (TSEN = 0)



Drop Side Receive Synchronous Interface (Fig. 27)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		33	MHz
	RFCLK Duty Cycle	40	60	%
tS_{RRDENB}	RRDENB to RFCLK High Setup	10		ns
tH_{RRDENB}	RFCLK High to RRDENB Hold	1		ns
tP_{RDAT}	RFCLK High to RDAT[7:0] Valid	2	20	ns
tZ_{RDAT}	RFCLK High to RDAT[7:0] Tristate	2	20	ns
tP_{RXP}	RFCLK High to RXPRTY Valid	2	20	ns
tZ_{RXP}	RFCLK High to RXPRTY Tristate	2	20	ns
tP_{RCA}	RFCLK High to RCA Valid	2	20	ns
tP_{RSOC}	RFCLK High to RSOC Valid	2	20	ns
tZ_{RSOC}	RFCLK High to RSOC Tristate	2	20	ns

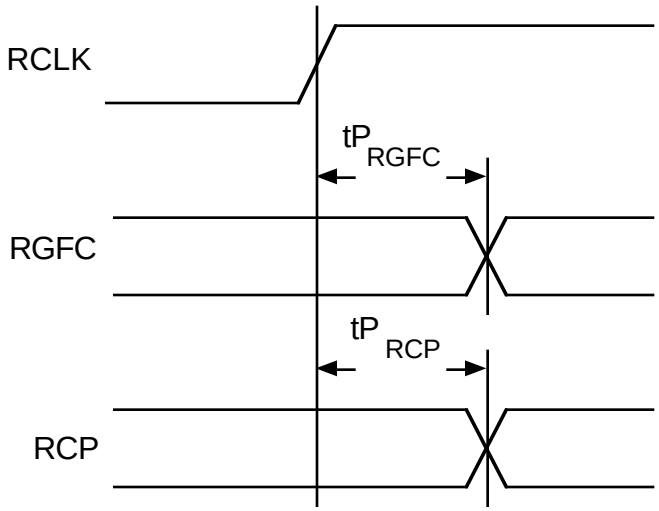
Fig. 27 Drop Side Receive Synchronous Interface Timing (TSEN = 1)



GFC Extract Port (Fig. 28)

Symbol	Description	Min	Max	Units
tP_{RGFC}	RCLK High to RGFC Valid	-1	10	ns
tP_{RCP}	RCLK High to RCP Valid	-1	10	ns

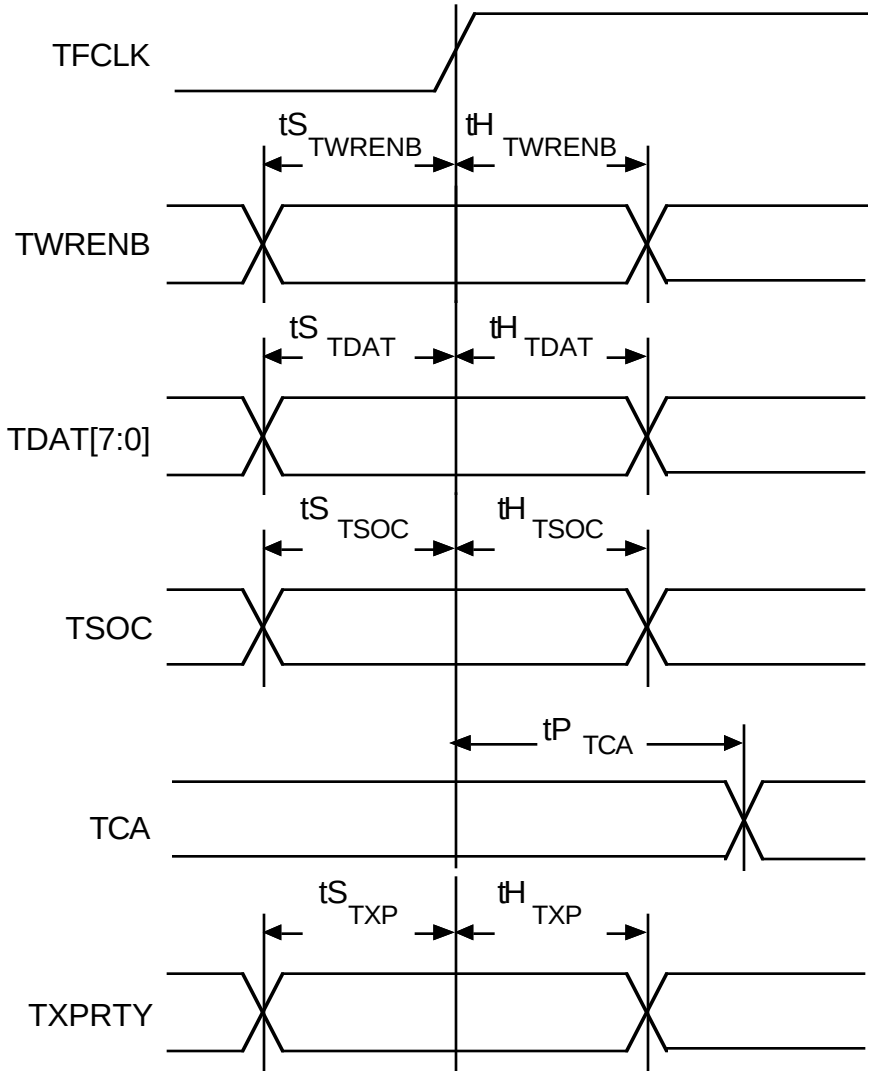
Fig. 28 GFC Extract Port Timing



Drop Side Transmit Synchronous Interface (Fig. 29)

Symbol	Description	Min	Max	Units
	TFCLK Frequency		33	MHz
	TFCLK Duty Cycle	40	60	%
tS_{TWRENB}	TWRENB Set-up time to TFCLK	10		ns
tH_{TWRENB}	TWRENB Hold time to TFCLK	1		ns
tS_{TDAT}	TDAT[7:0] Set-up time to TFCLK	10		ns
tH_{TDAT}	TDAT[7:0] Hold time to TFCLK	1		ns
tS_{TXP}	TXPRTY Set-up time to TFCLK	10		ns
tH_{TXP}	TXPRTY Hold time to TFCLK	1		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	10		ns
tH_{TSOC}	TSOC Hold time to TFCLK	1		ns
tP_{TCA}	TFCLK to TCA Valid	2	20	ns

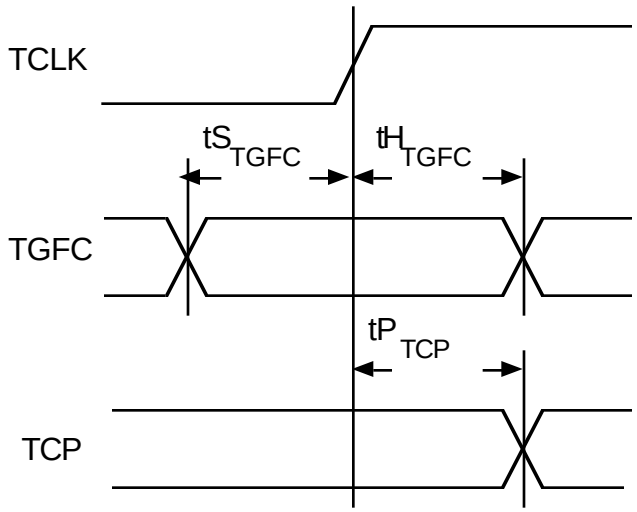
Fig. 29 Drop Side Transmit Synchronous Interface



GFC Insert Port (Fig. 30)

Symbol	Description	Min	Max	Units
tS_{TGFC}	TGFC Set-up time to TCLK	10		ns
tH_{TGFC}	TGFC Hold time to TCLK	1		ns
tP_{TCP}	TCLK High to TCP Valid	-1	10	ns

Fig. 30 GFC Insert Port Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. All output propagation delays are measured with a 50 pF load on the outputs.

3. Differential output propagation delay time is the time in nanoseconds from the crossing point of the reference signal to the crossing point of the output.

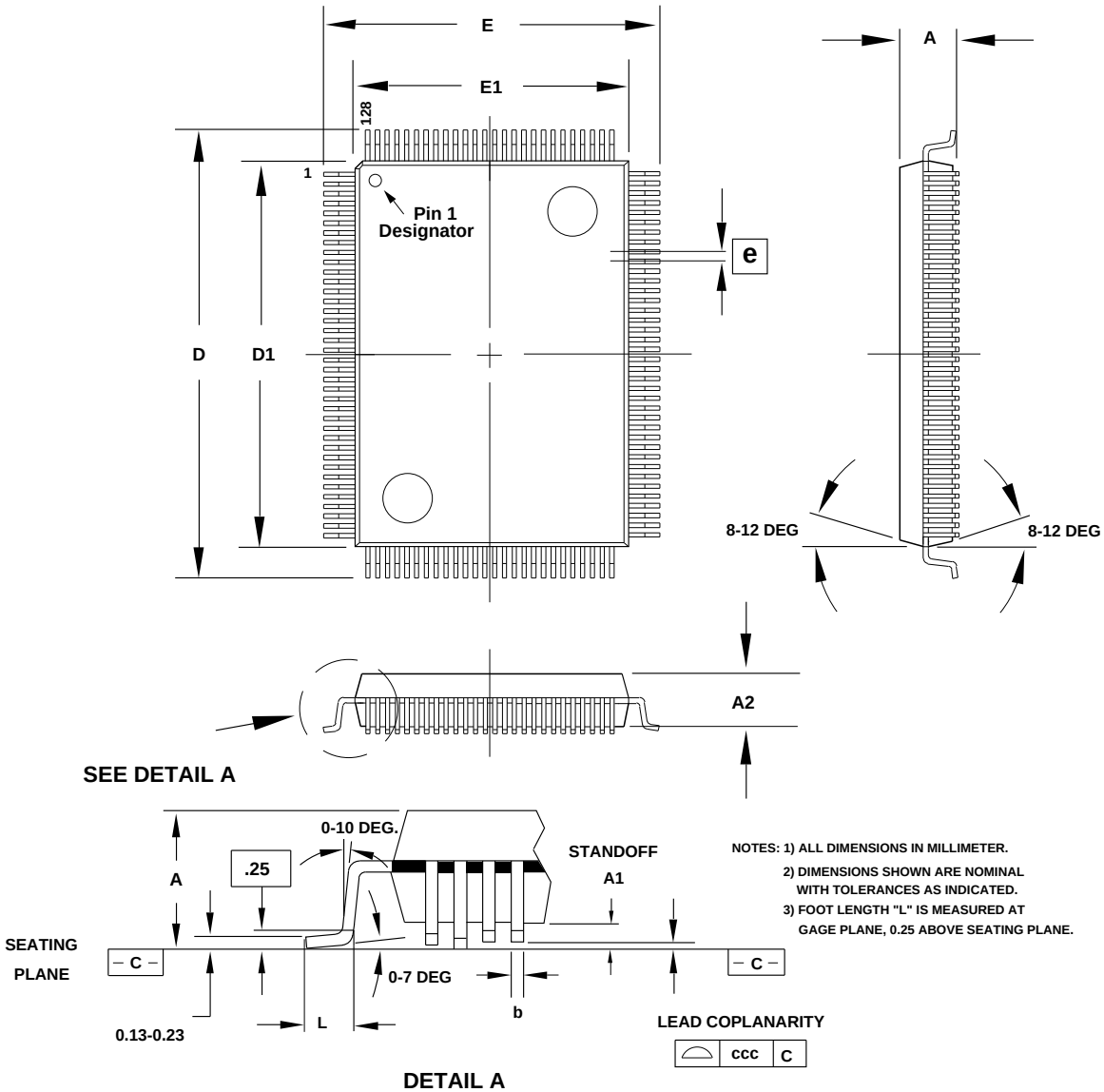
ORDERING AND THERMAL INFORMATION

PART NO.	DESCRIPTION
PM5346-RC	128 Pin Copper Leadframe Plastic Quad Flat Pack (PQFP)

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5346-RC	0°C to 70°C	60 °C/W	25 °C/W

MECHANICAL INFORMATION

128 Pin Copper Leadframe Rectangular Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 128 PIN METRIC RECTANGULAR PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 20 x 2.7 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.82	0.25	2.57	22.95	19.90	16.95	13.90	0.73		0.17	
Nom.			2.70	23.20	20.00	17.20	14.00	0.88	0.50	0.22	
Max.	3.40	0.53	2.87	23.45	20.10	17.45	14.10	1.03		0.27	0.10

NOTES

NOTES

NOTES

PMC-931110(R6) ref 931109(R8) Issue date: March, 1996.