STANDARD MICROSYSTEMS CORPORATION

PRELIMINARY
PRODUCT
SPECIFICATION

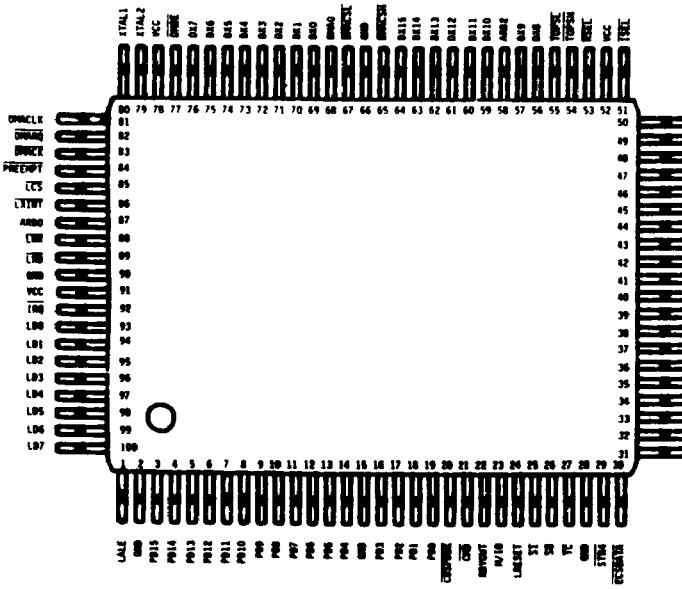
MICRO CHANNEL™ ESDI FIXED DISK DRIVE ADAPTER MSD95C10 (MIDAS)™

August 1989 – Rev. 1

FEATURES

* IBM Compatible ESDI Drive Interface
* Direct Connection to Micro Channel™ Bus
* Contains ESDI Drive Interface Logic
* 16-Bit DMA Transfers on Micro Channel at up to 5 Mbyte/sec
* IBM Register File Emulation
* Internal 26 Byte FIFO
* Supports 8- or 16-Bit Ring Buffers
* Up to 10 Mbyte/sec Ring Buffer DMA Rate
* Direct Connection to Local Processor over Separate Data Bus
* ROM and I/O Relocation Support
* Optional Wait State Generation for ROM Accesses
* DMA Configurable Between Micro Channel and Ring Buffer or Local Processor
* Firmware Programmable Card ID
* Directly Interfaces to the MSD95C01 for a High Integration ESDI Controller
* Low Power CMOS Technology

PIN CONFIGURATION



PACKAGE: 100-Pin Plastic Rectangular Flat Package
Ordering Information: MSD95C10 SMD

GENERAL DESCRIPTION

The Standard Microsystems MSD95C10 is a CMOS device containing all the functions required to implement an IBM compatible Micro Channel ESDI fixed disk drive adapter. Although it is optimized to interface to the MSD95C01 Hard Disk controller and a local processor like the 8031 or the 80188, it interfaces to the Micro Channel ensuring bit and register level compatibility with the IBM adapter regardless of the hard disk controller and local processor used.

By integrating all the interface functions into a single 100-pin device, the MSD95C10 reduces the number of components required on the adapter board. The 26 byte FIFO and the optimized DMA interface provide high performance with low arbitration overhead on the Micro Channel side.

The POS and DMA functions are Micro Channel conformant and furthermore bit compatible with the IBM adapter. Another level of flexibility is achieved by making so additional features (like fast vs. slow Mic Channel waiving on preemption) programmab from the local processor interface.

The I/O register file, as well as the Mic Channel to Local Processor handsha mechanism, are fully IBM compatible.

The 26-byte FIFO improves performance ensuring the traffic on the Micro Channel bursty. The FIFO can be programmed to fl between the Micro Channel on one side, whi the other side can be the ring buffer DMA up to 10 Mbyte/sec, or the local process I/O space. Burst length and fairness mo can be programmed in the POS registers as p the IBM specifications. Further tuning the system's throughput vs. bus latency achievable by programming the device throu its local processor interface to relinqui the Micro Channel immediately on preempti or on predefined transfer boundaries

The ESDI interface logic is also integrated, enhancing the ESDI command interface performance.

The local processor interface comprises a dedicated 8-bit multiplexed bus and the associated control lines from the processor. The MSD95C10 also provides the local processor with its reset and interrupt lines.

The ring buffer interface consists of a 16-bit data bus plus a DMA interface to the disk controller. The device can be programmed to use an 8-bit wide ring buffer for low-cost applications or slow Micro Channel embodiments (machines with built-in wait states), or a 16-bit interface for highest performance.

The MSD95C10 will interface to an 8-bit disk controller and transparently perform the appropriate byte swapping for the disk controller to access a 16-bit wide ring buffer.

The ring buffer DMA interface was optimized for the MSD95C01 stacked request mode, but it can also be programmed for a handshaked request/acknowledge as well.

The MSD95C10 includes a 20 MHz crystal oscillator which is used by the disk controller as well.

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Name	Symbol	Description
MICROCHANNEL INTERFACE			
37-34	Address 3-0	A3-A0	Input. Low order bits of address bus. Used to select the POS or internal register accessed. Directly connected to Micro Channel.
44,43,39	Address 16-14	A16-A14	Input. High order bits of address bus. Used to relocate the ROM chip select segment according to its POS value. Directly connected to Micro Channel.
19-16, 14-3	Data Bus	PD0-PD15	Input/Output. A 16-bit data bus used to access the POS registers, the internal I/O registers, and for DMA to and from the adapter.
46	$\overline{\text{System Byte}}$ High Enable	$\overline{\text{SBHE}}$	Input. Indicates valid data is being transferred on the high byte of the bus. Directly connected to Micro Channel.
23	Memory/$\overline{\text{IO}}$	M/$\overline{\text{IO}}$	Input. Distinguishes between memory and I/O cycles. Directly connected to Micro Channel.
25,26	$\overline{\text{Status 1-0}}$	$\overline{\text{S1}}$-$\overline{\text{S0}}$	Input. These signals define the type of access cycle (read/write) performed. Directly connected to Micro Micro Channel.
21	$\overline{\text{Command}}$	$\overline{\text{CMD}}$	Input. Defines a valid cycle on the bus. Directly connected to Micro Channel.

Pin No.	Name	Symbol	Description
MICROCHANNEL INTERFACE (continued)			
20	Card Selected Feedback	CD SFDBK	Output. Indicates the adapter recognized being addressed. Connected to two Micro Channel lines: -CD SFDBK(n) and -CD DS 16(n).
22	Ready Out	RDYOUT	Output. Used to extend ROM access cycles by connecting it to the CD CHRDY line of Micro Channel.
33,58, 42,87	Arbitration Priority	ARB3-ARB0	Input/Output. Open drain I/O lines used to drive drive and sense the DMA arbitration level. Directly connected to Micro Channel.
32	Arbitrate/ Grant	ARB/GNT	Input. Generated by the Central Arbitration Control Point to indicate the beginning and end of a DMA arbitration cycle.
84	Preempt	PREEMPT	Input/Output. Open drain signal driven by the device t request an arbitration cycle. Sensed to terminate transfers when another board is activating the line. Directly connected to Micro Channel.
38	Burst	BURST	Output. Open drain signal activated to indicate a bloc DMA transfer. Directly connected to Micro Channel.
27	Terminal Count	TC	Input. Indicates terminal count of a DMA transfer. Ends burst transfers. Directly connected to Micro Channel.
92	Interrupt	IRQ	Output. Open drain signal used as an interrupt request Directly connected to the appropriate Micro Channel interrupt.
45	Card Setup	CDSETUP	Input. Selects the board POS registers for access. Directly connected to Micro Channel.
31	Channel Reset	CHRESET	Input. Generated by the Micro Channel to reset all adapters. Directly connected to Micro Channel.
LOCAL PROCESSOR INTERFACE			
85	Chip Select	LCS	Input. Activated when the local processor needs to access the MSD95C10 registers.
93-100	Local Data Bus	LD0-LD7	Input/Output. An 8-bit address and data multiplexed bu used to access the MSD95C10 from the adapter local processor.
1	Address Latch Enable	LALE	Input. Its falling edge is used to latch a valid address on LD0-LD7.

Pin No.	Name	Symbol	Description
LOCAL PROCESSOR INTERFACE (continued)			
89	Local Read	$\overline{\text{LRD}}$	Input. Local processor read signal.
88	Local Write	$\overline{\text{LWR}}$	Input. Local processor write signal.
86	Local Interrupt	$\overline{\text{LXINT}}$	Output. Interrupt to the local processor. Set and cleared upon predefined register accesses.
24	Local Reset	LRESET	Output. Typically used to reset the adapter local processor. Combines the Micro Channel reset line and a software reset bit controlled by the host.
ESDI DRIVE INTERFACE			
50	ESDI Command Serial Output	ECDATA	Output. This pin provides the ESDI Command output serialized. It requires an external open collector inverting buffer.
30	ESDI Command Input	$\overline{\text{ECSDATA}}$	Input. Serialized ESDI Command data input from Serial the ESDI drive.
48	ESDI Request	ETREQ	Output. This pin provides the ESDI command transfer request. It is used in conjunction with ETACK in order to shift data between the MSD95C10 and an ESDI drive. Requires an external open collector inverting buffer.
49	ESDI Acknowledge	$\overline{\text{ETACK}}$	Input. Acknowledge provided by the ESDI drive for every bit of data shifted in or out.
RING BUFFER AND DISK CONTROLLER INTERFACE			
64-59, 57-56, 76-69	Ring Buffer Data Bus	DX15-DX0	Input/Output. 16 bit data bus connecting the ring buffer and the MSD95C10. Lower byte also connected to the disk controller.
82	DMA Request	$\overline{\text{DMARQ}}$	Output. Signal used to request a DMA cycle from the disk controller a DMA cycle into the ring buffer.
83	DMA Acknowledge	$\overline{\text{DMACK}}$	Input. Signal used by the disk controller to acknowledge a previously requested MSD95C10 ring buffer DMA cycle.
68	DMA Address 0	DMA0	Input. Determines whether a ring buffer cycle has an odd or even address. Used to swap high and low bytes for accesses from an 8-bit disk controller.

Pin No.	Name	Symbol	Description
RING BUFFER AND DISK CONTROLLER INTERFACE (continued)			
77	Output Enable	DMOE	Input. Activated by the disk controller when reading from the ring buffer. Used to generate high and low byte RAM chip select lines.
67 65	Chip Select Low Chip Select High	DMACSL DMACSH	Output. These are the chip select signals for the ring buffer low and high byte memory banks.
81	Clock Out	DMACLK	Output. Buffered version of the signal at XTAL1. Typically connected to the MSD95C01 to run its DMA circuitry on that clock.
MISCELLANEOUS			
51	I/O Selection	ISEL	Input. Selects the I/O registers of the MSD95C10 for host access. Supplied by external decode of Micro Channel address. Internally latched on falling CMD.
53	ROM Selection Input	RSEL	Input. Selects the board ROM for access. Internally latched on falling CMD and combined with the POS ROM relocation bits to generate XROM and RDYOUT.
47	ROM Selection Output	XROM	Output. Board ROM chip select.
29	POS 4 Strobe Output	STR4	Output. Strobe signal activated during a write to POS 4. Simplifies the external implementation of an additional POS register.
55 54	Driver control	TOPSL TOPSH	Output. Bus driver direction control signals. When low, the corresponding byte is driven into the Micro Channel.
80 79	Crystal 1 Crystal 2	XTAL1 XTAL2	An external crystal is connected to these pins. An external TTL clock may be connected instead to X1 with a 390 Ohm pullup resistor.
41,52, 78,91	Power Supply	VCC	+5V power supply pins.
2,15, 28,40, 66,90	Ground	GND	Ground pins.

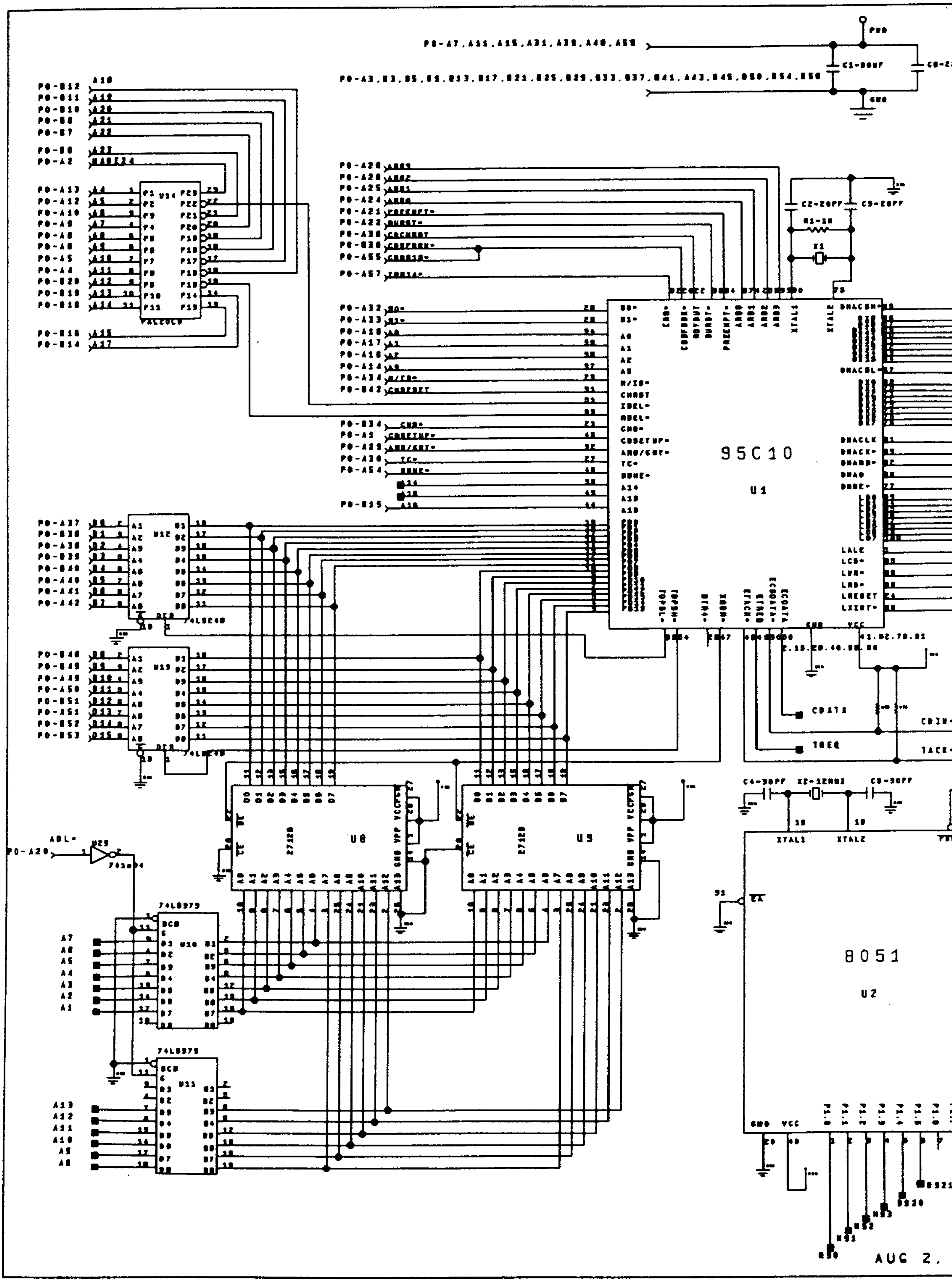
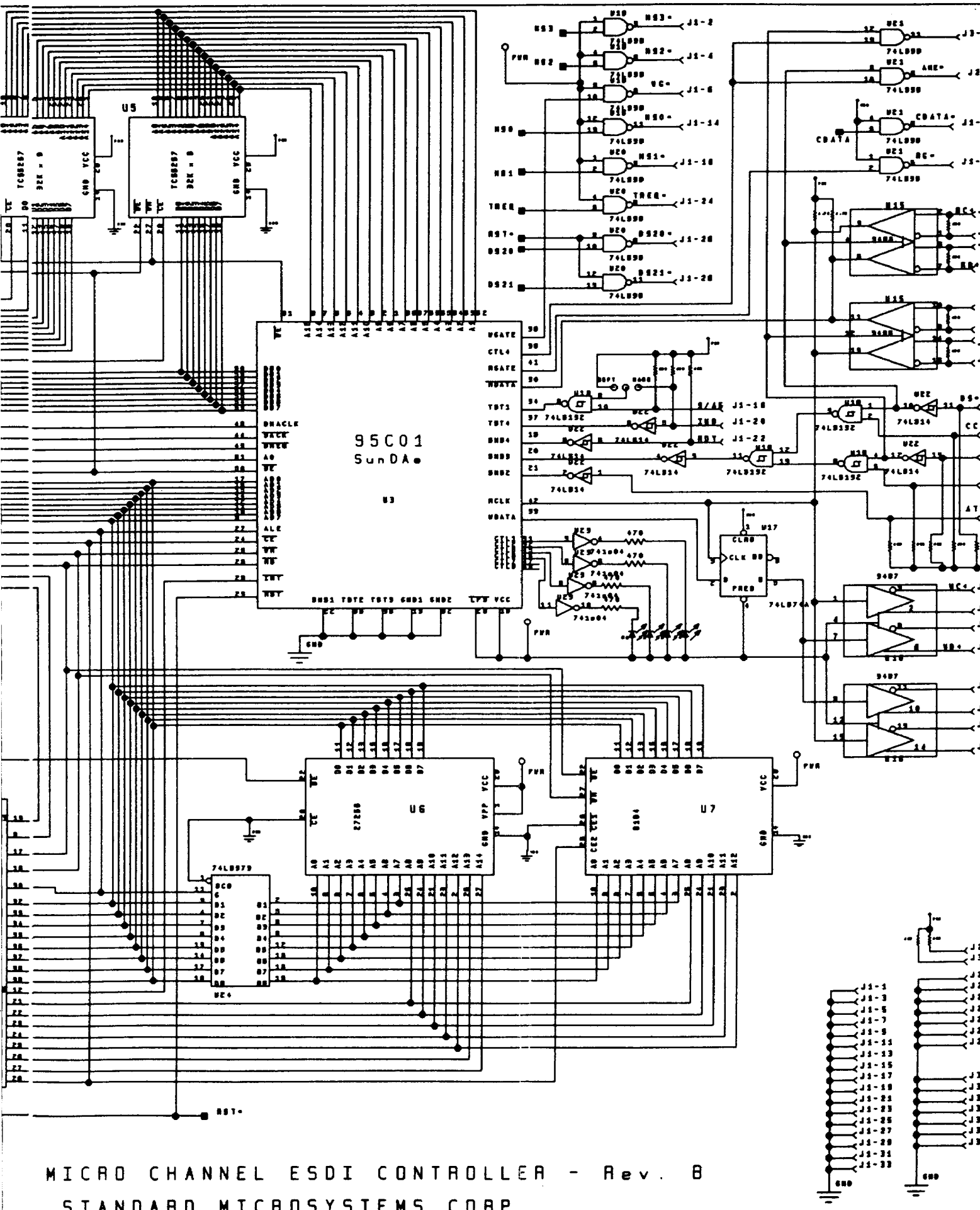


FIGURE 1


95C01
SunDAe
U3
U5
U6
U7
MICRO CHANNEL ESDI CONTROLLER - Rev. B
STANDARD MICROSYSTEMS CORP.

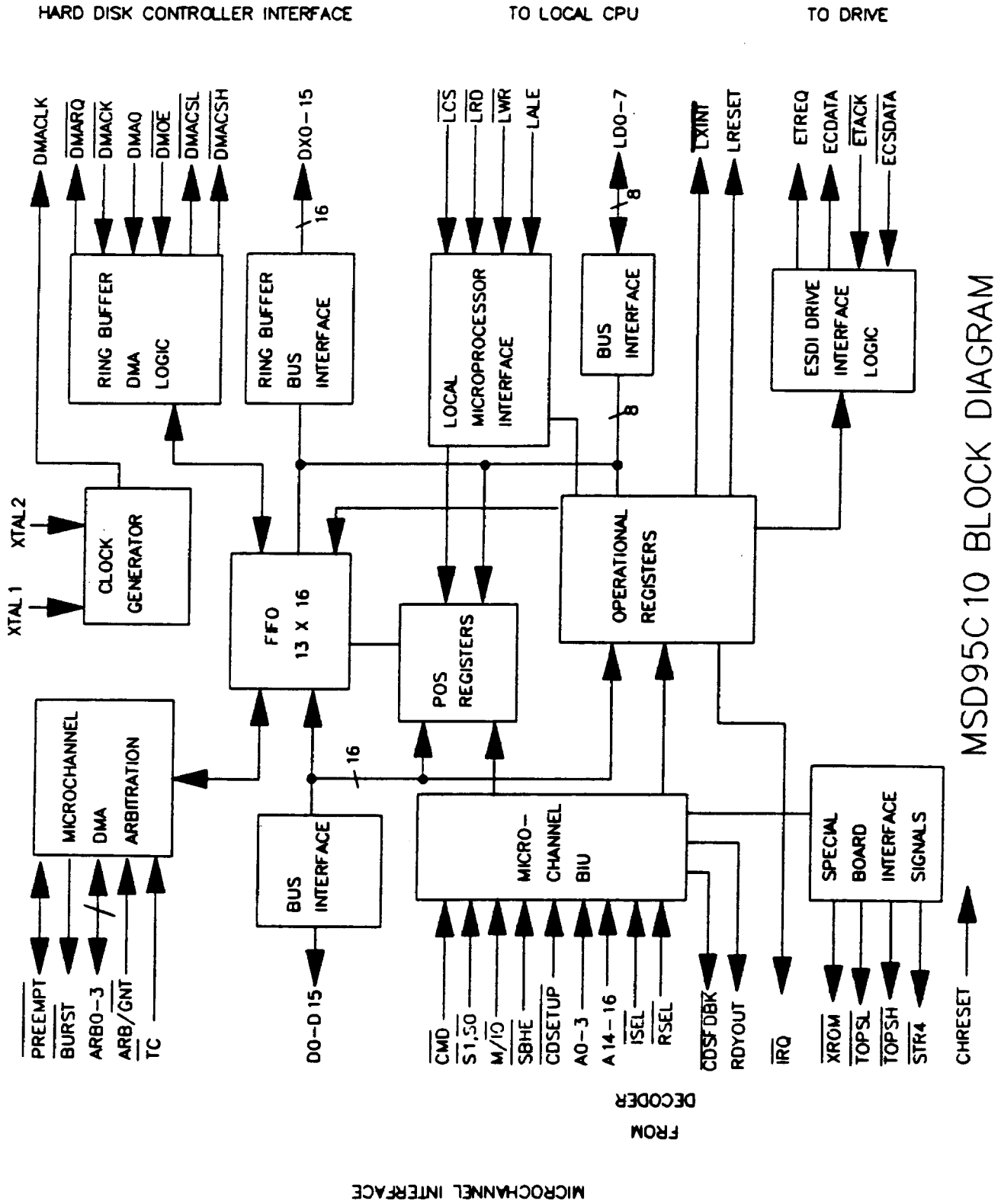


FIGURE 2 - INTERNAL BLOCK DIAGRAM

SYSTEM DESCRIPTION

The MSD95C10 is a Micro Channel interface device conceived to support single DMA channel intelligent adapter boards. For the typical application of a Micro Channel ESDI hard disk adapter, the MSD95C10 offers a high integration solution fully compatible with IBM's ESDI controller. Figure 1 illustrates the typical system block diagram.

The MSD95C10 is accessible by the host processor through various interfaces. Four POS registers (typically accessed by the IBM System Configuration Utilities) are used for adapter identification and configuration. A set of six I/O mapped registers represent the adapter to system interface and are used for initialization, control, and command/status handshaking. The last interface is the DMA port used for the data transfer to and from the adapter. An additional optional interface supported by the MSD95C10 is the access to an on-board BIOS ROM. The MSD95C10 generates the ROM chip select, supporting eight possible relocations and optional ROM wait states.

All the host interface registers are also accessible from the local processor side. Additional registers are accessible from the local processor only. These are used for functions transparent to the Micro Channel host. An example of these functions is the serial ESDI command interface included in the MSD95C10.

Communication between the host and the local processor is facilitated by a handshaked command/status scheme able to interrupt either one on demand.

Data transfers between the host and the adapter are buffered by a 26-byte FIFO. Both sides of the FIFO are able to work in a DMA mode to maximize throughput.

The Micro Channel DMA circuitry includes all the arbitration logic needed to gain control of the bus and request slave DMA transfers.

The local processor side includes the DMA logic necessary to request and handle ring buffer DMA transfers from the MSD95C01. Two DMA modes are supported, handshaked (for simplicity), and stacked (for highest performance).

A third option supported allows access to the FIFO through the local processor I/O space. Even in this case, FIFO hysteresis ensures bursty Micro Channel transfers regardless of the speed ratio between the local bus and the Micro Channel.

FUNCTIONAL DESCRIPTION

Adapter ID Storage and Retrieval

The MSD95C10 stores the two adapter ID bytes (POS registers 0 and 1). Their values are programmable by the local processor, allowing the designer to use any ID while saving external logic. If both ID registers are not programmed by the local processor, the MSD95C10 uses FFFFH, making the host believe the adapter is not present. POS registers 0 and 1 are write only for the local processor and read only on the Micro Channel.

Other POS Registers

POS registers 2 and 3 are used by the System Configuration Utilities to configure the board using its adapter description file. These are read/write registers on the Micro Channel, while they can also be read by the local processor to learn the configuration options in effect.

POS register 4 is not required for the ESDI adapter, but enhancements can be done by defining new functions and configuring through an external register POS 4. The MSD95C10 provides a strobe signal ($\overline{STR4}$) that can be used to write to such an external register. Possible applications of an external POS register may be to provide configurable interrupt mapping into more than one Micro Channel interrupt line, additional I/O space relocations, or even as a general purpose output port from the host into the adapter.

I/O Registers Seen by Host

The MSD95C10 I/O register file consists of the following:

Attention	8-bits Write only
Basic Control	8-bits Write only
Basic Status	8-bits Read only
Interrupt Status	8-bits Read only
Command Interface	16-bits Write only
Status Interface	16-bits Read only

The I/O space can be relocated to an alternate address using POS register 2.

ROM Support

The MSD95C10 can assist in providing an on-board ROM. It generates the chip select for the ROM based on the following:

* External ROM address partial decode ($\overline{\text{RSEL}}$ input)
* ROM Relocation programmed in POS register 3.
* ROM Enable programmed in POS register 3.

The device can also support slower memories by negating its RDYOUT during ROM accesses, thus resulting in Micro Channel synchronous extended cycles. If zero wait state ROM access is preferred, RDYOUT should be left unconnected.

Micro Channel DMA Arbitration

The MSD95C10 includes all the functionality to perform slave DMA transfers by direct connection of the relevant pins to the Micro Channel.

The Micro Channel DMA arbitration is done using the parameters selected in POS register 2 (arbitration level and arbitration method) and in POS register 3 (Burst Length). The arbitration level can be programmed to any of 15 valid levels; the arbitration method can be either fairness or linear priority. The burst length can be programmed to 24 transfers, 16 transfers, 8 transfers or burs disabled (single transfer mode).

The MSD95C10 would typically request the bu when its FIFO is empty on a write operation or when it is full on a read operation. Thi minimizes the arbitration overhead on th Micro Channel. If the device is configure for single transfer (burst disabled), thi rule is relaxed, allowing requests on an number of transfers.

The behavior of the device when it i preempted is determined by the immediat relinquish bit, programmed by the loca processor. If the immediate relinquish mod is used, the device will terminate its burs on the next transfer. Otherwise it wil release it on eight transfer boundaries This flexibility can be used by the designe to trade off system bus latency and dis performance.

After it relinquishes the bus on preemption the behavior of the MSD95C10 is the determined by the arbitration method bit i POS register 2.

When configured for fairness, it will no participate in a new arbitration cycle unti $\overline{\text{PREEMPT}}$ goes inactive (all requesters had th bus). If configured for linear priority, i will participate in any subsequen arbitration cycle, provided it is ready fo a full FIFO transfer.

Micro Channel Interrupts

The $\overline{\text{IRQ}}$ output is used as a Micro Channe interrupt. The status of this line is als available as a bit 0 in the Basic Statu Register. The command completion informatio coming from the adapter is available in th Interrupt Status Register. Reading th Interrupt Status Register will automaticall clear the interrupt. The interrupt is set b the local processor writing to the Interrup Status Register.

I/O Registers Seen by Local Processor

The register file seen by the local processor resides in the range 20H to 2FH. The registers accomplish the functions described below.

ADDRESS	WRITE FUNCTION	READ FUNCTION
20	POS 0	POS 2
21	POS 1	POS 3
22	Status Interface Low	Command Register Low
23	Status Interface High	Command Register High
24	Interrupt Status	Attention Register
25	UNUSED	Basic Control Register
26	Basic Status	Basic Status
27	ESDI Command Data Low	ESDI Config/Status Low
28	ESDI Command Data High	ESDI Config/Status High
29	ESDI Shift Control	Various Status Bits
2A-2B	UNUSED	UNUSED
2C	Transfer Count Low	Actual Transfer Count Low
2D	Transfer Count High	Actual Transfer Count High
2E	FIFO Access Port	FIFO Access Port
2F	Various Control Bits	Status and Control Readback

ESDI Interface

The output pins $\overline{\text{ECDATA}}$ and $\overline{\text{ETREQ}}$, and the input pins $\overline{\text{ECSDATA}}$ and $\overline{\text{ETACK}}$ of the MSD95C10 comprise the ESDI command, configuration and status interface.

The corresponding logic in the MSD95C10 enhances the solution integration and performance by doing the 16-bit serialization, parity checking, as well as the request-acknowledge handshake for the ESDI command and status serial transfers.

The local processor accesses those services through the MSD95C10 registers 27H through 29H.

Ring Buffer Interface

The adapter data storage area typically consists of a ring buffer managed by the hard disk controller (MSD95C01). The MSD95C10 requires sequential access to the ring buffer in order to DMA data to and from the Micro Channel.

The ring buffer data interface consists of a 16-bit bus (DX0-15), which can also be programmed to transfer only 8 bits at a time over DX0-7.

The DMA Request ($\overline{\text{DMARQ}}$) and DMA Acknowledge ($\overline{\text{DMACK}}$) signals are used by the MSD95C10 to provide a DMA interface to the ring buffer.

Paired with the MSD95C01, the MSD95C10 is able to improve ring buffer throughput by stacking up to 12 outstanding requests, while for a more conventional interface, the MSD95C10 also supports a fully handshaked request/acknowledge sequence. DMACLK is a buffered clock output connected as the MSD95C01 DMA clock.

Implementing a 16-bits wide ring buffer with the MSD95C10 does not require a 16-bit hard disk controller. The MSD95C10 would use two additional inputs, the DMA Address 0 (DMA0) and the ring buffer Output Enable ($\overline{\text{DMOE}}$) from the disk controller, to generate the appropriate Chip Select Low ($\overline{\text{DMACSL}}$) and Chip Select High ($\overline{\text{DMACSH}}$). It also swaps low and high bytes for disk controller odd address accesses.

Local Processor Interrupts

$\overline{\text{LXINT}}$ is the MSD95C10 interrupt to the local processor. It is set by the host writing into the attention register.

The adapter BUSY bit is logically equivalent to the local processor interrupt, and can be polled by reading the Basic Status Register bit 4. It is readable from either the host or local processor side. It is cleared by the local processor writing a zero to the bit.

Clock Generation

A crystal oscillator incorporated in the MSD95C10 is used to run some of the MSD95C10 internal circuitry. It is also available at the output pin DMACLK as a buffered MOS clock. DMACLK is connected to the MSD95C01 to serve as the clock for its DMA logic. A 15-20 MHz parallel resonant crystal, along with a 1.0 MOhm resistor, should be connected to the XTAL1 and XTAL2 pins, and a 22p capacitor should be connected from each p to ground.

Decoding Considerations

The signals that affect the decoding different functions are:

$\overline{\text{CDSETUP}}$ - Connected to the $\overline{\text{CDSETUP}}$ line the Micro Channel, serving as the chip sele signal for the POS registers.
$\overline{\text{ISEL}}$ - Chip select signal for the MSD95C internal registers. Only applicable for I/ space. A0-2 determine the register, A4 also used internally to provide the alternat I/O area.
$\overline{\text{RSEL}}$ - ROM select. Used to enable a relocate ROM accesses.
$\overline{\text{LCS}}$ - Chip select on the local process side. When active, the device occupie locations 20H through 2FH. The address latched from LD0-7 on LALE falling edges.

POS Registers Description

POS 0 - READ ONLY

ADAPTER ID LOW							

POS 1 - READ ONLY

ADAPTER ID HIGH							

POS 2 - READ/WRITE

0	ARBIT. METHOD	ARBITRATION		LEVEL		ALTER. ADDR.	CARD ENABLE

ARBITRATION METHOD - Fairness when cleared. Linear priority when set to one.
ARBITRATION LEVEL - Defines the adapter priority level for DMA operations.
ALTER. ADDRESS - When cleared the MSD95C10 I/O registers start at the base addres determined by the pin $\overline{\text{ISEL}}$ and A3-0 (3510H for a typical adapter), whe set to one the registers are shifted requiring A3-1 (typically 3518H)
CARD ENABLE - Enables the adapter when set. If kept low, all functions except th POS registers are disabled.

POS 3 - READ/WRITE

0	0	BURST LENGTH		ROM DISABLE		ROM SEGMENT	

BURST LENGTH - Determines the DMA burst length on the Micro Channel. The burst length ir
words is 8 times the value programmed.
ROM DISABLE - Disables the on-board ROM when set to one.
ROM SEGMENT - Relocates the ROM decode according to address lines A14 through A16. Supports
eight segments.

Host I/O Registers Description

ATTENTION REGISTER - 8 BITS - WRITE ONLY - ADDRESS OFFSET 3

DEVICE SELECT CODE			0	ATTENTION REQUEST CODE			

Writing the registers generates a local processor interrupt.

BASIC CONTROL REGISTER - 8 BITS - WRITE ONLY - ADDRESS OFFSET 2

HARD RESET	0	0	0	0	0	Enable DMA	Enable INT

HARD RESET - Generates a hardware reset for the device and the board.
Enable DMA - Enables request of DMA transfers on the Micro Channel.
Enable INT - Enables the device interrupt to the Micro Channel.

BASIC STATUS REGISTER - 8 BITS - READ ONLY - ADDRESS OFFSET 2

DMA ENABLED	INT PENDING	COMMAND IN PROG	BUSY	STATUS FULL	CIR FULL	XFER REQ.	INT

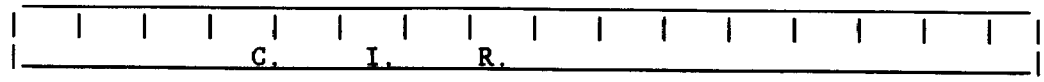
DMA ENABLED - High when enabled.
INT PENDING - High when INT about to come.
COMMAND IN PROG - Command in progress in the adapter.
BUSY - Last command to Attention Register being processed.
STATUS FULL - Status word available.
CIR FULL - Command word not read yet.
XFER REQ - Transfer request, the adapter is ready to DMA.
INT - Set means adapter interrupt.

INTERRUPT STATUS REGISTER - 8 BITS - READ ONLY - ADDRESS OFFSET 3

DEVICE SELECT			0	INTERRUPT ID			

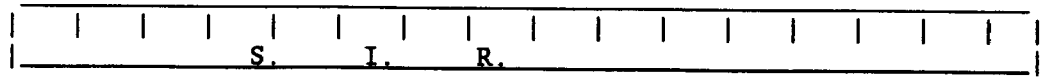
Generates an interrupt when written by the local processor. The interrupt is cleared upon reading the register.

COMMAND INTERFACE REGISTER - 16 BITS - WRITE ONLY - ADDRESS OFFSET 0



Writing the register sets CIR FULL bit.

STATUS INTERFACE REGISTER - 16 BITS - READ ONLY - ADDRESS OFFSET 0



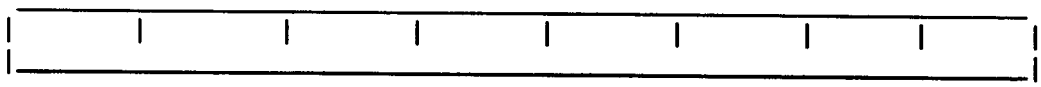
Contains valid data when STATUS FULL bit is set. STATUS FULL clears upon reading th register.

Local Processor I/O Registers Description

The local processor can access the host I/O registers according to an address table presente before. The bit arrangement is equivalent to the one seen by the host.

The registers presented below are only accessible by the local processor.

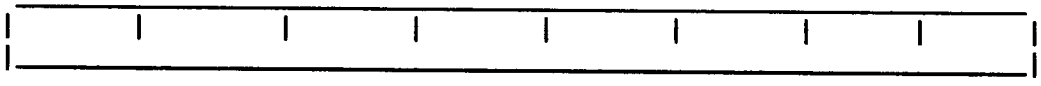
REGISTER 26 - BASIC STATUS REGISTER - READ/WRITE



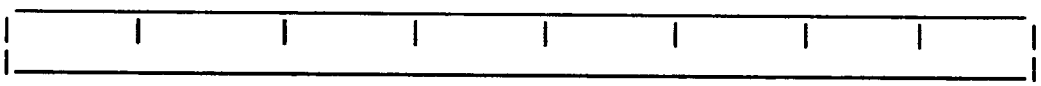
When written the bits act as follows:

BIT	USAGE
0	Not used/don't care
1	Not used/don't care
2	If on clears BASIC STATUS REGISTER bit 2.
3	If on clears BASIC STATUS REGISTER bit 3.
4	If on clears BASIC STATUS REGISTER bit 4.
5	Copied to BASIC STATUS REGISTER bit 5.
6	Copied to BASIC STATUS REGISTER bit 6.
7	Not used/don't care.

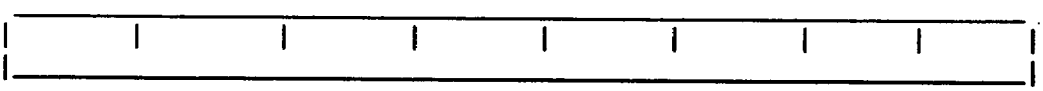
REGISTER 27 - ESDI COMMAND DATA LOW - WRITE ONLY



REGISTER 27 - ESDI CONFIGURATION/STATUS LOW - READ ONLY



REGISTER 28 - ESDI COMMAND DATA HIGH - WRITE ONLY



REGISTER 28 - ESDI CONFIGURATION/STATUS LOW - READ ONLY

REGISTER 29 - ESDI SHIFT CONTROL - WRITE ONLY

0	0	0	0	0	SHIFT CONTROL		

SHIFT CONTROL

0	NO OPERATION
1	Shift ESDI command data to ESDI drive
2	Shift data from ESDI drive to ESDI config/status registers.
4	Reset ESDI shift register logic

REGISTER 29 - ESDI STATUS BITS - READ ONLY

FIFO NOT EMPTY	FIFO NOT ALM EMPT	FIFO NOT FULL	FIFO NOT ALM FULL	TERM. COUNT	PARITY ERROR	ESDI READ	NO ESDI SHIFT

FIFO NOT EMPTY - Off when the FIFO is empty.
FIFO NOT ALM EMPTY - Off when the FIFO is almost empty (one word present).
FIFO NOT FULL - Off when the FIFO is full.
FIFO NOT ALM FULL - Off when the FIFO is almost full.
TERM. COUNT - Set when the transfer count is completed or when the FIFO is disabled.
PARITY ERROR - The ESDI config/status word received has a parity error.
ESDI READ - When set means the last ESDI command to shift register was a read.
NO ESDI SHIFT - When set, means the ESDI shift register is not shifting.

REGISTER 2C - TRANSFER COUNT LOW - READ/WRITE

REGISTER 2D - TRANSFER COUNT HIGH - READ/WRITE

The transfer count should be programmed with the number of transfers minus one. In the 16-bit ring buffer mode (or local processor access mode) the count is in words, while in the 8-bit ring buffer mode it is in bytes. When read, it provides the number of transfers yet to be requested.

REGISTER 2E - FIFO ACCESS PORT - READ/WRITE ACCORDING TO FIFO DIRECTION

REGISTER 2F - CONTROL BITS - WRITE ONLY

FAST RB DMA	BUS LATENCY			16 BIT RING B.	FIFO PORT	READ DIR	FIFO ENABLE
		0	0				

REGISTER 2F - STATUS AND CONTROL READBACK - READ ONLY

FAST RB DMA	BUS LATENCY	ODD ADD RB	ODD ADD LOCAL	16 BIT RING B.	FIFO PORT	READ DIR	FIFO ENABLE

FAST RB DMA - Determines the ring buffer DMA handshake. When set to 1, it uses t fast DMA scheme where up to 12 requests are stacked. Typically nee the MSD95C01 as the disk controller. When 0, it will only pulse t $\overline{\text{DMARQ}}$ line once until $\overline{\text{DMACK}}$ is asserted.

BUS LATENCY - Determines when to release the Micro Channel upon preemption. Wh set to 1 it only releases it at eight transfers boundaries. Otherwi it is released immediately on preemption.

ODD ADD RB - Set when the ring buffer odd byte is to be accessed next in the 8-b mode.

ODD ADD LOCAL - Set when the local processor will access the second byte (odd addres in the local processor FIFO access mode.

16-BIT RING B. - Selects between 8- and 16-bit ring buffer bus. A logic 1 means 1 bits.

FIFO PORT - Selects the access to the FIFO on the adapter side. When set, the FI is accessible by the local processor through address "2E". Otherwi the FIFO is accessed directly from the ring buffer DMA.

READ DIR - Selects the FIFO direction. When set it goes in the "read" directio namely the FIFO flows to the Micro Channel.

FIFO ENABLE - Enables the FIFO and ring buffer DMA logic. All other bits in th byte have to be set before enabling the FIFO.

Bit Level Interactions

Some register bits are modified on specific events. These are typically used to ensure a safe handshake mechanism between the host and the local processor.

Writing into the Attention Register by the host sets the BUSY bit (BASIC STATUS REGISTER bit 4) and activates the local processor interrupt $\overline{\text{LXINT}}$. The BUSY bit and the interrupt is cleared when the local processor writes to the BASIC STATUS REGISTER with bit 4 set.

Writing a word into the Command Interface Word register by the host sets the C.I.R. FULL bit (BASIC STATUS REGISTER bit 2). The C.I.R. FULL bit is cleared when the local processor writes to the BASIC STATUS REGISTER with bit 2 set.

Writing to the Interrupt Status register by the local processor sets the INTERRUPT bit (BASIC STATUS REGISTER bit 0). The INTERRUPT bit is cleared when the host reads the Interrupt Status Register. If the INTERRUPT ENABLE (Basic Control Register bit 0) and the CARD ENABLE (POS 2 bit 0) are set, the INTERRUPT bit will activate the $\overline{\text{IRQ}}$ interrupt line. Writing a pair of bytes to the Status Interface Register by the local processo sets the STATUS OUT FULL bit (BASIC STATU REGISTER bit 3). The sequence must writing the low byte first and then the hi byte. The high byte write sets the STATU OUT FULL. The STATUS OUT FULL automatically cleared by the host reading t Status Interface word register. The loc processor is also capable of clearing it writing to the BASIC STATUS REGISTER with bi 3 set.

The DMA ENABLE bit (Basic Control Registe bit 1) is typically set by the host after t DMA controller has been programmed and rese by the terminal count line $\overline{\text{TC}}$ going active It can also be cleared by the host.

The Reset bit (Basic Control Register bit 7 generates a hardware reset for the device a the local processor. The POS registers a not affected. The bit should be then writte low in order to terminate the reset.

NOTE: Except for the BASIC CONTROL REGISTE and the BASIC STATUS REGISTER, the registe usage is transparent to the device. Eve when the register content is transparent, fo simplicity purposes, the bit usage describe throughout the document corresponds to th IBM ESDI Fixed Disk Adapter/A.

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin, with respect to ground ..... V_{CC}+0.3V
Negative Voltage on any pin, with respect to ground ..... -0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=5.0V±5%)

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	COMMENTS
Low Input Voltage High Input Voltage	V_{IL} V_{IH}	 2.0		0.8	V V	TTL Levels TTL Levels
Low Output Voltage High Output Voltage	V_{OL} V_{OH}	 2.4		0.4	V V	
Input Leakage Current	I_L			±10	uA	$V_{SS}<V_{IN}<V_{CC}$
V_{CC} Supply Current	I_{CC}		150		mA	@ 20 MHz
Input Capacitance	C_{IN}			5	pf	
Pin Current Drive Capability 1 ($\overline{PREEMPT}$, $\overline{ARB0}$-$\overline{ARB3}$, $\overline{IRQ}$, $\overline{BURST}$)	I_{D1}			24	mA	sink
Pin Current Drive Capability 2 (CLKOUT, RDYOUT, $\overline{CDSFDBK}$)	I_{D2}			12	mA	
Pin Current Drive Capability 3 (All other output and bidirectional pins)	I_{D3}			2	mA	

A.C. PARAMETERS

Parameter	Min	Max
1) $\overline{S0}$ $\overline{S1}$ valid to RDYOUT falling		28ns
2) $\overline{CMD}$ active to RDYOUT rising		26ns
3) $\overline{ISEL}$ and address decode valid to $\overline{CDFBK}$ active		36ns
$\overline{RSEL}$ and address decode valid to $\overline{CDFBK}$ active		35ns
4) ARB\$\overline{GNT}$ falling to $\overline{PMPT}$ inactive		40ns
5) ARB\$\overline{GNT}$ falling to $\overline{BURST}$ active		40ns
6) $\overline{CMD}$ to $\overline{BURST}$ inactive (burst length reached or fifo exhausted)		40ns
7) $\overline{TC}$ active to $\overline{BURST}$ inactive		25ns
8) $\overline{CMD}$ active to data valid		45ns
9) Data setup time before $\overline{CMD}$ invalid	15ns	
Data hold time after $\overline{CMD}$ invalid	15ns	
10) $\overline{DMACK}$ active to data valid (for disk write direction)		30ns
11) Data setup time to $\overline{DMACK}$ inactive	15ns	
Data hold time after $\overline{DMACK}$ inactive (for disk read direction)	15ns	
12) $\overline{DMACK}$ active to $\overline{DMACSL}$, $\overline{DMACSH}$ active		16ns
13) DMA0 high to $\overline{DMACSH}$ active		20ns
DMA0 low to $\overline{DMACSL}$ active ($\overline{DMACK}$=1)		20ns
14) DMOE low to DX0-7 driven (byte swap for odd read) (DMA0=1, $\overline{DMACK}$=1)		45ns
DMA0 high to DX8-15 driven (byte swap for odd write) ($\overline{DMOE}$=1, $\overline{DMACK}$=1)		45ns
15) $\overline{LRD}$ and $\overline{LCS}$ active to valid data		55ns
16) Data hold time after $\overline{LWR}$ inactive	15ns	
17) Data setup time to $\overline{LWR}$ active	10ns	
18) $\overline{CMD}$ active to $\overline{TOPSH}$, $\overline{TOPSL}$ active		30ns
19) $\overline{CMD}$ inactive to $\overline{XROM}$, $\overline{TOPSH}$, $\overline{TOPSL}$ inactive	0	
20) $\overline{RSEL}$ active to $\overline{XROM}$ active		26ns
21) Byte swap delay for odd access (DX8-15 valid to DX0-7 valid) - read		18ns
(DX0-7 valid to DX8-15 valid) - write		

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