National Semiconductor

PRELIMINARY

DP8025 TROPIC™
Token-Ring Protocol Interface Controller

General Description

The Token-Ring Protocol Interface Controller (TROPIC) is a microCMOS VLSI device designed for easy implementation of IEEE 802.5 Token-Ring LAN interface adapters. The TROPIC chip includes integrated Analog and Digital Token-Ring interfaces and bus interface support for ISA and MicroChannel hosts. Transmit and receive buffers are implemented in shared RAM, with buffer arbitration and control provided by the TROPIC chip.

TROPIC provides full IEEE 802.5 compatibility, including Medium Access Control (MAC) and Logical Link Control (LLC) protocol handling, and is IBM 802.5 certified. Network performance exceeds current 802.5 Jitter Requirements. The TROPIC supports both 16 Mbps and 4 Mbps operation, which are chip-selectable.

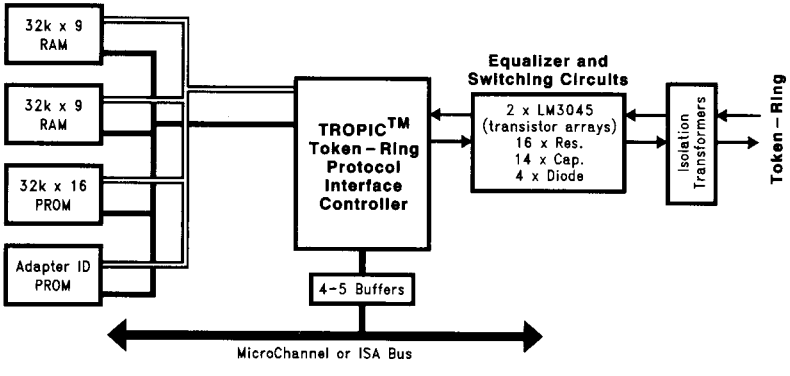
TROPIC integrates both digital and analog CMOS technologies in a single 175-pin, 1.48" (37.2 mm) module. Operation is driven by an integral Microprocessor Unit (MPU), which is microcoded for flexible functionality. The microcode controlling the MPU (provided with TROPIC) is stored in an external PROM, which allows simple PROM upgrades to remain current with any future changes to the IEEE 802.5 standard. External RAM is used for data, control, and scratch-pad storage. The TROPIC chip provides an interface for directly attaching the required external PROM and RAM devices.

Host Transmit and Receive buffers and control blocks are provided through a Shared RAM Interface, which is managed by a TROPIC integral controller. The control blocks are used to pass commands and messages between the Host system and TROPIC.

Features

- Complete Token-Ring Adapter solution
- Integrated Bus Interface support for ISA and MicroChannel, including MicroChannel POS registers
- MAC Layer 802.5 and LLC executed in integral microprocessor unit (MPU), minimizing Host software
- MPU microcode provided
- Chip-selectable 16/4 Mbps operation
- Minimal supporting hardware required
- Single +5V supply required
- CMOS for low power dissipation
- Configurable RAM size and Page size
- Optional Parity on Host interface
- Shared buffer memory using standard 8k by 9 or 32k by 9 RAM
- Support for IBM Source Routing Bridges
- Minimal Host memory space required

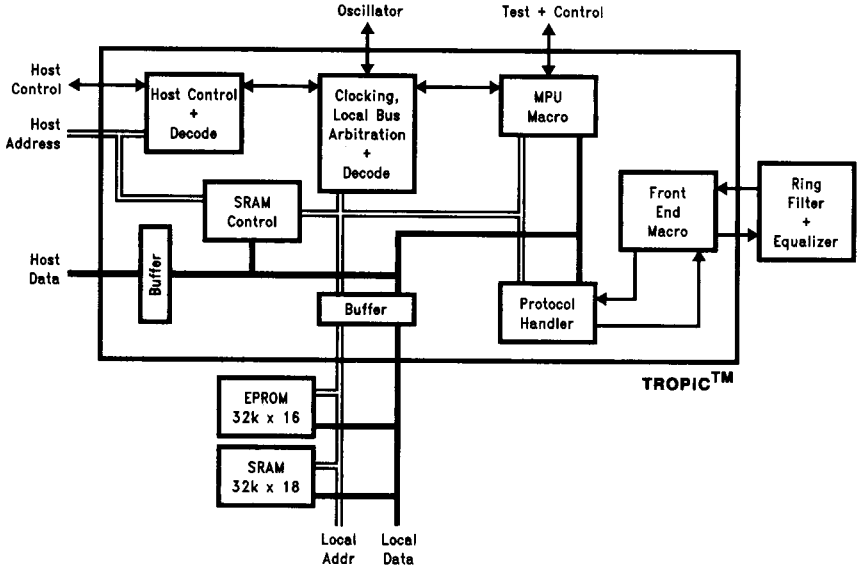
1.0 System Diagram



TL/F/11334-1

Table of Contents

2.0 Block Diagram



TL/F/11334–2

3.0 Functional Description

TROPIC provides three external interfaces (Token-Ring, Host Bus, and Local Storage). TROPIC also requires certain Host system resources.

TOKEN-RING INTERFACE

The Front End Macro within TROPIC supplies a Ring Interface. This provides signals and inputs for external equalization and transformer circuits that form the actual Token-Ring Serial interface. The external Token-Ring Serial Interface provides physical connection to the Token-Ring LAN Media. It must include appropriate filter circuits (one Transmit filter and two Receive filters, one each for 4 Mbps and 16 Mbps operation), switching circuitry to switch between the 4 Mbps and 16 Mbps Receive filters, and line protection and conditioning components.

HOST BUS INTERFACE

The Host Bus interface allows the Host system to transfer data to and from TROPIC. This interface includes a twenty-four bit address bus, a sixteen bit data bus with optional parity, and control signals to allow the TROPIC Host Bus interface to attach directly, as a bus slave, to ISA or MicroChannel. This makes TROPIC appear to be a memory device on the Host Bus that can be read or written using standard memory access and MMIO (Memory Mapped I/O) procedures.

LOCAL STORAGE INTERFACE

This interface provides direct attachment from TROPIC to local PROM and RAM devices, which TROPIC controls exclusively. This interface includes an eighteen bit data bus and sixteen bit address bus, plus control lines to choose proper memory devices and control read and write operations.

HOST SYSTEM RESOURCE REQUIREMENTS

TROPIC requires four Host system resources for MicroChannel and ISA bus Hosts as follows:

- One Interrupt
- 16k or 64k of memory address space for Shared RAM buffers and control blocks (which allow passing of high-level commands, frame data, and status codes between TROPIC and Host software)
- ROM/MMIO space (8k for MicroChannel/ISA)
- 5 bytes of I/O space for MicroChannel and ISA

Each of these resources is described in more detail later.

TROPIC INTERNAL ELEMENTS

TROPIC can be implemented with an understanding of just its external interfaces and Host requirements. However, some consideration of TROPIC's internal structure and data flow is useful.

TROPIC consists of four main logical blocks:

- Front End Macro (FEM)
- Protocol Handler
- Integral MPU
- Shared Memory Controller

The functions of each of TROPIC's internal logical elements is best understood by considering data flow through the device during reception and transmission of Token-Ring data, as described next (these discussions assume some understanding of Token-Ring message structures).

3.0 Functional Description (Continued)

TROPIC DATA FLOW—RECEPTION

Front End Macro

The Front End Macro (FEM), combined with external equalizer components, provides the interface needed to transmit and receive Manchester coded data over the Token-Ring media at either 4 Mbps or 16 Mbps. The provided functions include:

- Equalization of transmission channel
- Detection of receive signal
- Clock recovery and re-timing of received signal
- Transmission of output data
- Control functions, such as wrap test of interface circuit
- Ring Insertion and Wire Fault detection

The Front End Macro provides D-to-A and A-to-D signal conversion only. The Protocol Handler and MPU perform MAC and LLC processing, encoding, and decoding of data streams.

Received signals that have been decoded to NRZ clock and data form are sent to the Protocol Handler.

Protocol Handler

When data is received from the Front End Macro, the Protocol Handler first converts the serial data to byte parallel data usable by the MPU, and generates parity on the received data for subsequent internal validity checks.

At the proper time during the receive sequence, the Protocol Handler begins bit-wise CRC (Cyclic Redundancy Check) accumulation on the received data. At the proper point in the received message, the Protocol Handler extracts the Token-Ring destination address. It then compares it with the values loaded into the Protocol Handler to determine if the message should be copied by this station. If so, the Protocol Handler begins transferring the message to TROPIC's local RAM for additional MPU operations.

The Protocol Handler transfers, in order, the physical control field, the Token-Ring destination and source addresses, the data fields, and the message's CRC characters. When the CRC-protected portion of the message has been received, the received CRC characters are checked for validity.

If there is a CRC mismatch, the local RAM area used to store the message is released and the message is not processed. Otherwise, proper changes are made to the frame status byte after the end of frame delimiter. At this point, processing moves from the Protocol Handler to the MPU.

MPU

The MPU assembles the data transferred from the Protocol Handler into multi-byte segments. The areas where the message data has been stored are set up as valid for transfers to the Host Bus via the Shared Memory interface.

The actual mapping and management of data into the buffers is controlled by the MPU microcode, and is also affected by certain host-controlled parameters and status codes from the Protocol Handler.

Shared Memory Controller

When the transfer is complete, a status code is written to the appropriate buffer control block address in Shared RAM and an interrupt is issued to the Host. The Host software can then transfer the received data out of the Shared Memory area.

TROPIC DATA FLOW—TRANSMISSION

Transmissions from the Host are essentially the opposite of receptions. The Host software transfers data and an appropriate transfer command code to a free buffer in Shared RAM, and then signals TROPIC's MPU that a message is waiting. The MPU then sets up the Protocol Handler to begin a transfer from Shared Memory.

When the Protocol Handler senses a pending transmission, it begins transferring the data into its 32-byte FIFO. When enough data is buffered to allow continuous transmission through the Front End Macro, the Protocol Handler waits for a token on the LAN. When a token is acquired, it is converted to a frame. Applicable control characters are generated, encoded, and transmitted (via the FEM), and the transmission continues with destination and source addresses, followed by the information field. When the entire information field has been transferred, the Protocol Handler inserts the CRC characters that it has accumulated into the message, followed by the encoded delimiter and frame status byte.

4.0 Initialization

The TROPIC can be configured to work in a number of environments. The Power-On Reset configuration is initialized in three ways:

- by setting TROPIC configuration input pins to steady state levels via switches, jumpers, pullup/pulldown resistors, or hard-wiring of the input pins
- by Microcode setting of software control switches
- by loading configuration data into internal TROPIC registers (Configuration Registers). In MicroChannel Hosts, this is accomplished by writing to TROPIC's internal POS registers. For all other implementations, the TROPIC Configuration Registers are loaded from the Storage Data bus after reset (as described later in this section).

TROPIC CONFIGURATION PINS

Four input pins are used to configure TROPIC for the Host environment: DPEN, −CFG2, −CFG1, and −CFG0.

The DPEN pin enables/disables generaton and checking of parity of the Host dats bus. The Host Configuration pins −CFG2, −CFG1, and −CFG0 are used to identify the Host bus type, as shown below. This affects various operating aspects, including memory mapping and register usage.

4.0 Initialization (Continued)

Host Configuration Pins (0 = GND, 1 = V_{CC})

−CFG2	−CFG1	−CFG0	Bus Type Indicated
1	1	1	ISA 16-bit
0	1	1	ISA 8-bit
1	0	1	MicroChannel 16-bit
0	0	1	MicroChannel 8-bit
1	1	0	Reserved
0	1	0	Reserved
1	0	0	Reserved
0	0	0	Reserved

MICROCODE SETTINGS

Several TROPIC registers are initialized by PROM microcode. These control mostly memory mapping and management and internal parity functions, and are usually unavailable to the Host (even in Ready-only mode).

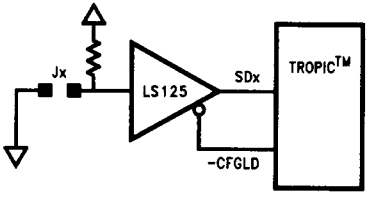
TROPIC CONFIGURATION REGISTERS

In MicroChannel host environments, the Configuration Registers are loaded directly from the host during POS. For all other host implementations, the Configuration Register is automatically loaded from the Storage data bus after reset. Access to the Configuration Registers is limited and varies according to Host bus type.

Besides Host Bus type (set by configuration pins), the following TROPIC aspects can also be configured:

- **ROM/MMIO Host Base Address**—Defines the base address (in the Host's memory space) for the ROM/MMIO control area
- **Host Interrupt Level**—For ISA and MicroChannel bus types, defines the IRQ level to be used
- **Ring Speed**—Selects 4 Mbps or 16 Mbps Ring Speed
- **RAM Type**—Indicates the type of storage RAM (static or dynamic) used on the TROPIC-based adapter
- **Shared RAM Page Size**—Selects the Shared RAM interface page (window) size in host memory space
- **Primary/Secondary Adapter**—For ISA and MicroChannel bus types, sets TROPIC to respond as either the Primary Adapter (x0A20) or the Secondary Adapter (x0A24h)

To facilitate the load of the configuraton data for ISA Host implementations, TROPIC provides the signal −CFGLD. This signal can be used to "gate" configuration data onto the storage data bus as illustrated below:



TL/F/11334–5

Storage Data bus signals during configuration load are defined as shown in the table on the next page.

4.0 Initialization (Continued)

Storage Data Bus Signals during ISA Configuration Load (0 = GND, 1 = V_{CC})

Data Bit(s)*	Configuration Description
SD15–SD9	**BIOS/MMIO Base Address**—Defines initial Host Base Address for the TROPIC ROM/MIO region of host memory (described in Section 5.0). Data Bits correspond to the inverted sense of host address lines HA19–HA13 respectively: 0000000 xFE000 • • 0010111 xD0000 • • 0011001 xCC000 • • 1111111 x00000
SD8–SD7	**Encoded IRQ Level (ISA ONLY):** Selects interrupt level for adapter, as follows: Bit 8 / Bit 7 / Selected IRQ 0 / 0 / IRQ7 0 / 1 / IRQ6 1 / 0 / IRQ3 1 / 1 / IRQ2
SD6	Reserved—**must** be set to 0.
SD5	**RAM Type:** Indicates the type of Storage RAM used on the TROPIC-based adapter. 0 = Static RAM, 1 = Dynamic RAM
SD4	Reserved—DO NOT drive
SD3–SD2	**Shared RAM Page Size:** Selects the shared RAM page (window) size, i.e., the amount of the Host's memory space that is allocated to shared RAM. These bits are coded as follows: SD3 / SD2 / Page Size 0 / 0 / 64 kB 0 / 1 / 32 kB 1 / 0 / 16 kB 1 / 1 / 8 kB This shared RAM page size may not be the total amount of shared RAM on the adapter. For example, an adapter with 64 kB of available shared RAM can be set for a 16 kB page size to allow shared RAM paging.
SD1	**TROPIC Ring Speed:** 0 = 16 Mbps, 1 = 4 Mbps
SD0	**Primary/Alternate Adapter Selection Bit:** 0 = Secondary (xA24), 1 = Primary (xA20)

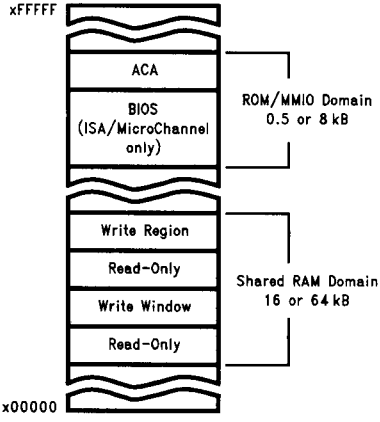
*TROPIC Storage Data Lines are internally pulled up to V_{CC}. Allowing a data line to "float" during configuration load will result in setting that bit/option to "1".

For more detailed descriptions of configuration register bit fields see Section 6.0.

5.0 Host Address Space Structure

TROPIC's Host Address Space is divided into two domains: Shared RAM and ROM/MMIO, shown below:

Shared Memory—Host Address Map



TL/F/11334–3

SHARED RAM DOMAIN

As discussed in the Functional Description, transmission and reception data and control blocks are transferred between TROPIC and the Host via the TROPIC Shared RAM area. This area can be either 16 kB or 64 kB, depending on the Host's upper memory area usage; its size and initial base address are configured during Reset initialization.

During operation, Shared RAM can be relocated and paged. Location and paging status are available through the Shared RAM address parameters defined in the RAM Relocation Register (RRR) and Shared RAM Paging Register (SRPR), as described in Section 6.0.

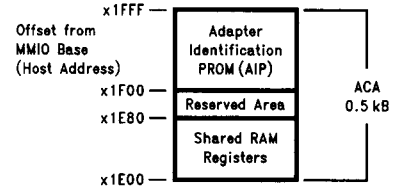
Mapping of the buffers and control blocks in Shared RAM is controlled by microcode. Buffer management and handshaking are summarized in Section 7.0. More complete details are beyond the scope of this document, and are covered in a separate programming document.

ROM/MMIO (MEMORY MAPPED I/O) DOMAIN

For MicroChannel and ISA Hosts, the ROM/MMIO domain is 8k and includes 7.5k for BIOS and 0.5k for an area called the Attachment Control Area (ACA).

The structure of the ACA is shown below.

Attachment Control Area (ACA)



TL/F/11334–4

The Adapter Identification PROM (AIP) area is a read-only region that contains unique adapter parameters, such as the IEEE node address and serial number.

The area from x1E80 to x1EFF is reserved and *should not* be accessed by the Host.

The MMIO Registers provide several important status and control registers that are accessible to the Host during operation. These are discussed in the next section.

6.0 Registers

The Host communicates with and controls TROPIC using three methods: Shared RAM, interrupts, and registers.

TROPIC supports three register areas:

- **MMIO Registers**—these are used by all Host bus types
- **Programmed I/O (PIO) Registers**—these are used only by ISA and MicroChannel hosts and are decoded during normal operation
- **MicroChannel Standard POS Registers**—these are used only by MicroChannel hosts and are decoded *only* during Setup

Note: POS Registers reside in PIO space, but are treated separately because they are only decoded during Setup.

REGISTER USAGE AND LOCATION BY BUS TYPE

Register usage varies by bus type, as shown below.

Register Usage by Bus Type

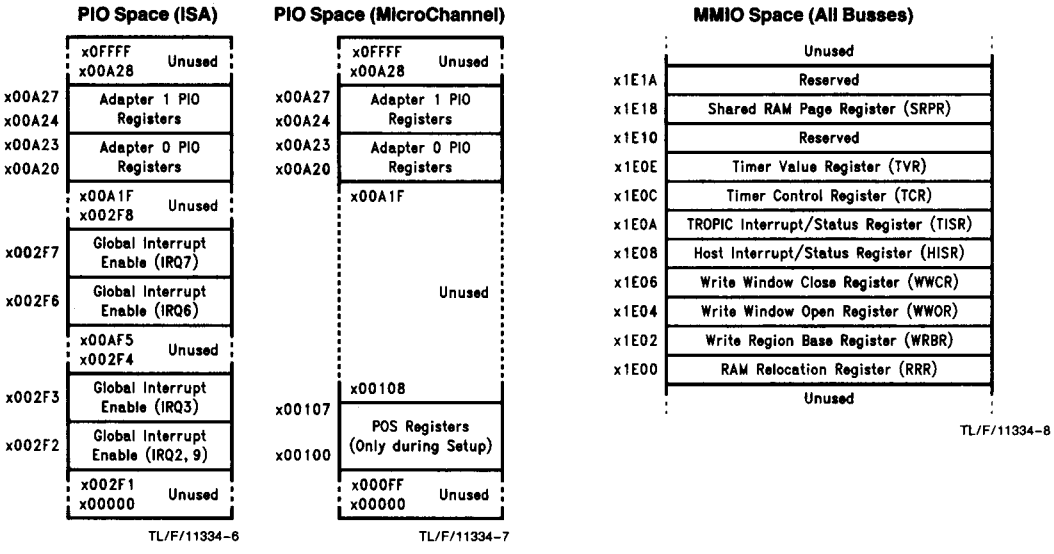
Bus Type	MMIO Registers	PIO Registers	MicroChannel POS Registers
MCS	Yes	Yes	Yes
ISA	Yes	Yes	No

4

6.0 Registers (Continued)

Memory allocation of registers is shown below.

Register Location by Bus Type



MMIO REGISTERS-GENERAL

The MMIO Registers are used by all bus types and are located within the ACA Host Address Space area. They include mostly read-only status registers, with a few Read/Write control registers. For ISA and MicroChannel buses, some of these registers are replicated in the PIO Registers; in such cases, one register is usually read-only while the alternative location is read/write.

All of the MMIO Registers consists of two-byte (word) registers, each having its low order byte at an even address and its high order byte at the following odd address. Note that addresses are relative to the ROM/MMIO Base Address.

MMIO REGISTERS—ISA AND MICROCHANNEL

This section describes MMIO Register usage in detail for ISA and MicroChannel Hosts.

RAM Relocation Register (RRR)

This register is used to relocate the Shared RAM region and indicate its page size and location. It also contains bits used to control different TROPIC operating modes.

Warning: Reserved bits (indicated by "—"), though readable, are controlled by TROPIC. These bits should not be changed.

6.0 Registers (Continued)

ISA BUS MODE:

x1E01								x1E00							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	RAM Size		—	—	AB19	AB18	AB17	AB16	AB15	AB14	AB13 (= 0)	—

MICROCHANNEL BUS MODE:

x1E01								x1E00							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	RAM Size		—	—	—	—	—	—	—	—	—	—

Bit(s)	Description
15–12	Reserved.
11–10	**Shared RAM Page Size:** Selects the shared RAM page (window) size, i.e., the amount of the Host's memory space that is allocated to shared RAM. These bits are coded as follows: 11 10 Page Size 0 0 8 kB 0 1 16 kB 1 0 32 kB 1 1 64 kB This shared RAM page size may not be the total amount of shared RAM on the adapter; instead, this value indicates the amount of shared RAM for the Host to map into its memory. For example, an adapter with 64 kB of available shared RAM can be set for a 16 kB page size to allow shared RAM paging. If the RRR bit 11 is set to 0 and bit 10 is set to 1, this would indicate 16 kB of shared RAM in the Host's memory map. **Note:** To use Shared RAM paging, Host software must also use the SRPR (Shared RAM Paging Register) correctly. See the later SRPR description for details.
9–8	Reserved.
7–1	**(FOR MICROCHANNEL BUS MODE) Reserved.** **(FOR ISA BUS MODE) Shared RAM Host Base Address:** For TROPIC adapters in ISA I/O Bus mode, bits 7 through 1 of the RRR register are used to set the shared RAM starting address. This location must be set before the Shared RAM can be accessed and must be set to a location in the memory map that does not cause a conflict. These register bits default to zero on power-up or after an adapter reset. If the register contains zero, the shared RAM is not mapped into the memory map. This register must be set to a correct address boundary as follows: • 8 kB shared RAM page should be on an 8 kB address boundary. • 16 kB shared RAM page should be on a 16 kB address boundary. • 32 kB shared RAM page should be on a 32 kB address boundary. • 64 kB shared RAM page should be on a 64 kB address boundary. For shared RAM paging, the address boundary can be on a 16 kB boundary since only 16 kB of PC address space is used. **Note:** To select a valid address boundary, RRR Bit 1 (AB13) should always be set to 0.
0	Reserved.

6.0 Registers (Continued)

Write Region Base Register (WRBR)—READ ONLY
Write Window Open Register (WWOR)—READ ONLY
Write Window Close Register (WWCR)—READ ONLY

WRBR (Read Only):

x1E03								x1E02							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB (Least Significant Byte) WRBR								MSB (Most Significant Byte) WRBR							

WWOR (Read Only):

x1E05								x1E04							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB (Least Significant Byte) WWOR								MSB (Most Significant Byte) WWOR							

WWCR (Read Only):

x1E07								x1E06							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB (Least Significant Byte) WWCR								MSB (Most Significant Byte) WWCR							

These management register pairs specify an offset into shared RAM. The offsets are 16-bit values. The even register contains the most significant byte of this value. For example:

WRBR(15–8) at x1E03 = 24 (LSB)

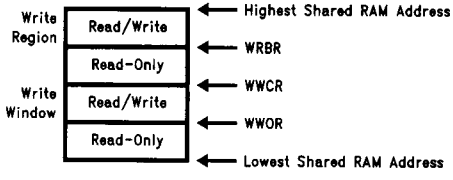
WRBR(7–0) at x1E02 = 47 (MSB)

WRBR full register value = 2447

In this example, a 16-bit Read of the WRBR (at x1E02) returns 2447; however, the logical (useable) address value is 4724.

IMPORTANT: To obtain a useable address, Host software **must** perform a byte-swap on 16-bit Reads from the WRBR, WWOR, and WWCR registers.

As illustrated below, TROPIC can concurrently define two separate and independent computer write areas within the Shared RAM domain: the *write region* and the *write window.* The size of each of these areas can be individually defined in word (2-byte) increments from 2 bytes to the maximum size of the shared RAM domain.



TL/F/11334–9

The two areas differ only in how they are bound. The write region always extends from the highest address of the shared RAM domain down to a variable origin specified by the WRBR. The write window extends from a variable base defined by the WWOR pair to a variable limit defined by the WWCR pair. Also, the low-order bit in each odd register is zero since all write boundaries are word (2-byte) aligned.

Any address in the shared RAM not given specific Host write access by the shared RAM management registers is given Host read-only access. A Host write to any of these read-only memory addresses or to any shared RAM management register MMIO address will not be completed and will activate the Host Access error interrupt condition (HISR bit 2). Since the origin of the write region (WRBR) and the write window (WWOR) must be greater than zero if either write area is to be defined, the first 2 bytes of the shared RAM domain are always read-only to the Host.

The interface mechanism allows the Host read-only access to the entire shared RAM domain until TROPIC is initialized and Host write-access areas are defined by TROPIC.

The WRBR contains either zero or the offset of the beginning of the write region. When this field is zero, no write region is available. The WWOR contains either zero or the offset of the beginning of the write window. This field contains zero until TROPIC is opened, and when it is zero, no write window is available. The WWCR contains either zero or the first offset after the last writeable offset. This field is reserved until TROPIC is opened, and when it is zero, no write window is available.

6.0 Registers (Continued)

HOST INTERRUPT/STATUS REGISTER (HISR)

This read/write register contains interrupt and control bits to allow TROPIC to issue interrupts to Host software.

x1E09								x1E08							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	TCHK	SRBR	ASBF	ARBC	SSBR	BFFC	—	CH/IR	INTE	—	TINT	EINT	AINT	IBLK	PR/AL

Bit(s)	Description
15	Reserved.
14	**TROPIC Check (TCHK):** TROPIC has encountered an unrecoverable error and is closed. The reason for the check may be read from the shared RAM using the address in the write window close management register pair in the attachment control area of the MMIO region. The information returned is defined in the separate programming reference document.
13	**SRB Response (SRBR):** TROPIC has recognized an SRB request and has set the return code in the SRB. A return code of: x00: Indicates successful completion of the SRB request. x01–xFD: Indicates unsuccessful completion of the SRB request. xFF: Indicates that the request has been accepted and is in process. A subsequent SSB response will be issued at the command completion. This interrupt bit is set for this return code only if the Host has set the "SRB Free Request" bit in the TISR.
12	**ASB Free (ASBF):** TROPIC has read the response provided in the ASB, and the ASB is available for another response. This interrupt bit is set only if the Host has set the "ASB Free Request" bit in the TISR or if an error has been detected in the response.
11	**ARB Command (ARBC):** The ARB contains a command for the Host to act on.
10	**SSB Response (SSBR):** The SSB contains a response to a previous SRB command from the Host.
9	**Bridge Frame Forward Complete (BRFC):** TROPIC has completed transmitting a frame forwarded by the bridge Host software.
8	Reserved
7	**CHCK/IRQ Steering Control (CH/IR):** This bit is used to control error interrupts. If 0, TROPIC will issue a CHCK. If 1, TROPIC will issue IRQ. CHCK is not supported in ISA and MicroChannel bus modes and, for those modes, this bit must be set to 1.
6	**Interrupt Enable (INTE):** When this bit is on, interrupt requests will be presented to the Host. When this bit is off, all interrupts are masked off. The bit can be set by either TROPIC or the Host.
5	Reserved.
4	**Timer Interrupt (TINT):** When this bit is on, the TVR(7–0) has expired.
3	**Error Interrupt (EINT):** TROPIC has had a machine check occur, the TROPIC deadman timer expire, or the TROPIC timer overrun.
2	**Access Interrupt (AINT):** When this bit is on, it indicates that a shared RAM access violation or an illegal MMIO operation by the Host to an Attachment Control Area register pair has occurred. The following conditions will set this bit: • Any Host write to a write-protected location in the shared RAM domain • Any Host write to a shared RAM management (WRBR, WWCR, WWOR) register • Any Host write to HISR(7–0) • Any Host write to a nonzero interrupt field of TISR(15–8) or HISR(15–8). Nonzero interrupt fields of TISR(15–8) and HISR(15–8) must be manipulated using OR and AND MMIO commands.
1	**1SA Bus Mode ONLY** **Interrupt Block Bit (IBLK):** Set by TROPIC to prevent interrupts until interrupts are re-enabled.
0	**Primary/Alternate Address (PR/AL):** This bit reflects the setting of the TROPIC primary/alternate setup information. If this bit is off, the primary adapter address is selected. If this bit is on, the alternate adapter address is selected.

6.0 Registers (Continued)

TROPIC INTERRUPT/STATUS REGISTER (TISR)

This read/write register provides interrupts (for Shared RAM management, errors, timeouts, and other events) and control values that allow Host software to issue interrupts to TROPIC (letting the Host and TROPIC communicate asynchronously). The Host software sets bits in TISR(14–8) to interrupt TROPIC.

x1E0B								x1E0A							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	BFFR	CSRB	RASB	SRBFR	ASBFR	ARBF	SSBF	IPE	TINTT	AINTT	DTEXP	TCHKT	—	THIM	TSIM

Bit(s)	Description
15	Reserved.
14	**Bridge Frame Forward Request (BRFR):** The Host software has placed a frame in the bridge transmit buffers and is requesting that the frame be forwarded.
13	**Command in SRB (CSRB):** The Host software has placed a command in the SRB and is informing TROPIC.
12	**Response in ASB (RASB):** The Host software has placed a response to an ARB request in the ASB and is informing TROPIC.
11	**SRB Free Request (SRBFR):** The Host software wants to use the SRB, but a previous request is still being processed by TROPIC. TROPIC will return an "SRB free" interrupt when the SRB return code field has been set.
10	**ASB Free Request (ASBFR):** The Host software wants to use the ASB, but a previous response is still being processed by TROPIC. TROPIC will return an "ASB free" interrupt when the ASB return code field has been set.
9	**ARB Free (ARBF):** The command in the ARB has been read by the Host software and the ARB is available. If the command requires a response from the Host software (receive and transmit only), it will be provided in the ASB later.
8	**SSB Free (SSBF):** The response in the SSB has been read by the Host software and the SSB is available.
7	**Internal Parity Error (IPE):** If this bit was on, there was a parity error on TROPIC's internal bus.
6	**Timer Interrupt—TROPIC (TINTT):** At least one of the TCR(15–8) timers has an interrupt to present to TROPIC.
5	**Access Interrupt—TROPIC (AINTT):** When this bit is on, it indicates that a shared RAM access violation or an illegal MMIO operation by TROPIC to an Attachment Control Area register has occurred.
4	**Deadman Timer Expired (DTEXP):** The deadman timer has expired, indicating an adapter microcode problem. This bit is one of the conditions that can set HISR bit 3.
3	**TROPIC Processor Check—TROPIC (TCHKT):** This bit does not latch on but follows the state of the TROPIC processor machine check indication. This bit is one of the conditions that can set HISR bit 3.
2	Reserved.
1	**TROPIC Hardware Interrupt Mask (THIM):** When this bit is on, it prevents adapter hardware interrupts (TISR bits 7 and 5) from being presented to the TROPIC processor.
0	**TROPIC Software Interrupt Mask (TSIM):** When this bit is on, it prevents Host software interrupts (TISR bits 14-8) from being presented to the TROPIC processor.

6.0 Registers (Continued)

TIMER CONTROL REGISTER (TCR)

This register controls both Host and ring timing. TCR(7–0) is used with the TVR register to control the Host programmable timer. TCR(15–8) controls the fixed-duration timers used by TROPIC's microcode timing routines, and is reserved.

x1E0D								x1E0C							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	PTIM	PTRM	PTCG	PTOS	PTCS	HLCK	—	—

Bit(s)	Description
15–8	Reserved (TROPIC MPU timer control).
7	**Host Programmable Timer Interrupt Mask (PTIM):** This bit controls the timer interrupt operation. When this bit is on, the timer interrupts the Host when the programmable count expires. When the bit is off, the timer will not interrupt the Host, and the timer status must be obtained by polling either HISR bit 4 or TVR(7–0). The timer interrupt, like all Host interrupts, is also subject to the interrupt enable bit (HISR bit 6).
6	**Host Programmable Timer Reload Mode (PTRM):** If this bit is on, the timer automatically reloads from TVR(15–8) when the countdown expires (reaches zero). When this bit is off, the timer must be reprogrammed or restarted after each countdown. Setting bit 6 while the count is counting reloads TVR(7–0) with the initial count in TVR(15–8).
5	**Host Programmable Timer Count Gate (PTCG):** This bit enables/disables timer counting and also allows reloading of the initial countdown from TVR(15–8). Setting the bit to 1 enables the timer and starts counting. Resetting to 0 disables the timer and halts decrementing of the timer count. The countdown may be resumed by writing a 1 back to this bit, since the count contained in the timer is not changed when the gate bit is cleared. However, if a gate set is received when the gate bit is already on and timer count is 0, the countdown value reloads from TVR(15–8) and a full countdown begins.
4	**Host Programmable Timer Overrun Status (PTOS):** This bit is set when an overrun condition is detected with the Host timer interrupt. If the timer interrupt has not been reset before the end of the next timing period, the overrun bit is set at the end of that period. Once set, this status bit remains active until reset to zero by the Host.
3	**Host Programmable Timer Count Status (PTCS):** This bit is **Host Read-only** and is set by TROPIC when the timer contains a nonzero countdown value (the timer is loaded but not necessarily counting). If this bit is 1, the nonzero timer counter value can be obtained by reading TVR(7–0). Otherwise, reads to the TVR(7–0) return zeroes. When the timer countdown is halted by clearing of TCR bit 5 and the count value is not zero, this bit will remain active (set to 1).
2	**Host Interlock (HLCK):** This interlock allows TROPIC's internal diagnostic routine to check the functional capability of the Host timing facility without interference from the Host. When set to 1, this bit prevents Host MMIO writes from updating the contents of the TVR register and the Host portion (except this bit) of TCR(7–0). This bit will be set only when TROPIC's internal diagnostic procedures require exclusive use of the Host programmable timer.
1–0	Reserved.

6.0 Registers (Continued)

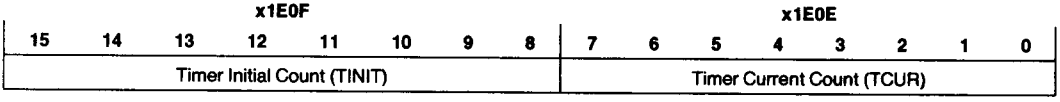
TIMER VALUE REGISTER (TVR)

This register contains the Host timer initial countdown value in TVR(15–8) and the current Host timer count in TVR(7–0) (referred to as "the timer"). Reading TVR(15–8) always returns the last value written to it (zero following initial power-on). Both TVR(15–8) and TVR(7–0) are cleared after power-on reset. For each byte, possible values range from 10 ms (x01) to 2.55 seconds (xFF) in 10 ms increments.

If the timer contains zeros, writing a byte to TVR(15–8) transfers that value to the timer. Counting is then subject to the state of the TCR(5) gate bit. A read of TVR(7–0) returns the actual contents of the Host timer counter at the time the read is received by TROPIC. Writes to TVR(7–0) are ignored.

If the counter is loaded (nonzero), a write to the TVR(15–8) register will not cause the timer to be reloaded. The loading of the new TVR(15–8) value to the timer is governed by the state of the TCR gate and reload bits (TCR bits 5 and 6).

The TCR(3) count status bit and the TCR(5) gate bit are used with TVR(7–0). When the timer is loaded (the TCR(3) count status bit is 1), the value returned from TVR(7–0) is the actual timer count at the time of the read. If the TCR(3) gate bit is 1, then the counter will be counting and the value returned will reflect the current instantaneous counting state.



Bit(s)	Description
15–8	**Host Programmable Timer Initial Count (TINIT):** See description above.
7–0	**Host Programmable Timer Current Count (TCUR):** See description above.

6.0 Registers (Continued)

SHARED RAM PAGE REGISTER (SRPR)

Through the SRPR register, TROPIC allows the Host system to use memory paging schemes to allocate a smaller Shared RAM domain (in the Host memory space) than the actual physical Shared RAM size on the TROPIC adapter. For example, if the adapter needs 64k of Shared RAM, but the Host system can allocate only 16k, the 64k adapter RAM can be mapped to the 16k Host space as four separate 16k pages, any one of which is "visible" at a given moment. Note that TROPIC always has full access to the entire 64k space even if the Host is using a smaller page size.

The SRPR register is only valid in Host bus modes that support RAM paging. It is used before initialization to communicate to TROPIC's microcode the total amount of RAM to use, and is also used after initialization to "page" the shared RAM into the Host's memory map.

Before TROPIC is initialized, the Host's software must write the appropriate value to the SRPR to communicate to TROPIC's microcode how much total shared RAM to use. If a value of x0000 is written to the SRPR, TROPIC uses only the amount of RAM indicated by the Shared RAM size bits in the RRR register (bits 10 and 11). If the RRR Shared RAM size bits are set to the page size indicated in the ID PROM under the RAM paging function, the Host software can write xC000 to the SRPR, (i.e., set bits 6 and 7 to a "11") and TROPIC's microcode will use all 64 kB of Shared RAM. The Host software can then access the entire 64 kB of shared RAM using RAM paging.

If RAM paging is selected, the SRPR can be used to "page" the Host "window" into the full 64 kB of Shared RAM after TROPIC is initialized. See the separate programming reference document for more details on Shared RAM paging procedures.

x1E19								x1E18							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	PS1	PS0	—	—	—	—	—	—

Bit(s)	Description
15–8	Reserved
7	**Page Select Bit 1 (PS1):** *Before initialization,* this bit and bit 6 indicated whether RAM Paging should be used, as follows: Value (PS1, PS0) — Meaning 00 — Use RRR (10,11) as total RAM, no paging 01 — Reserved 10 — Reserved 11 — Use 64k as total RAM, use paging *After initialization,* this bit and bit 6 are used to select the desired memory page, as follows: Value (PS1, PS0) — Meaning 00 — Map Page 1 into Host Memory Map 01 — Map Page 2 into Host Memory Map 10 — Map Page 3 into Host Memory Map 11 — Map Page 4 into Host Memory Map
6	**Page Select Bit 0 (PS0):** See PSI above.
5–0	Reserved.

6.0 Registers (Continued)

PIO REGISTERS (ISA AND MICROCHANNEL)

The PIO Registers provide access to certain MMIO Register data or controls that are unavailable to ISA and MicroChannel Hosts via the MMIO Registers. This includes Configuration Register information, Soft Reset Control, and ROM/MMIO Address information. The PIO registers also provide Shared RAM Address information for MicroChannel bus Hosts and Global Interrupt Enable registers for ISA bus Hosts.

There are four I/O addresses dedicated for PIO operations to each possible adapter type (primary or alternate). Read (IN) or write (OUT) operations to these addresses either cause an action or transfer data. The same address has different definitions based on whether Read or Write access is used, as described in the table below.

Note: The MicroChannel POS Registers also appear in Host I/O space, but are discussed separately in the next section.

PIO Registers (ISA)

	Read	Write	
x00A27	Reserved	Interrupt Enable	Secondary Adapter
x00A26	Reserved	Reset Release	
x00A25	Reserved	Reset Latch	
x00A24	Setup Read 1	Reserved	
x00A23	Reserved	Interrupt Enable	Primary Adapter
x00A22	Reserved	Reset Release	
x00A21	Reserved	Reset Latch	
x00A20	Setup Read 1	Reserved	
x00A1F – x002F8	Unused		
x002F7	Reserved	IRQ7	Global Interrupt Enable
x002F6	Reserved	IRQ6	
x002F5 – x002F4	Unused		
x002F3	Reserved	IRQ3	
x002F2	Reserved	IRQ2	

TL/F/11334–10

PIO Registers (MicroChannel)

	Read	Write	
x00A27	Reserved	Reserved	Secondary Adapter
x00A26	Setup Read 2	Reset Release	
x00A25	Reserved	Reset Latch	
x00A24	Setup Read 1	Reserved	
x00A23	Reserved	Reserved	Primary Adapter
x00A22	Setup Read 2	Reset Release	
x00A21	Reserved	Reset Latch	
x00A20	Setup Read 1	Reserved	

TL/F/11334–11

Global Interrupt enable (IRQn) **x0002F7 (WRITE)** **ISA ONLY**
x0002F6 (WRITE)
x0002F3 (WRITE)
x0002F2 (WRITE)

For ISA Bus mode, an I/O Write (OUT) to x002Fn issues a global interrupt enable. This resets interrupt generating circuits in *all* adapters sharing the Host interrupt facilities. The specific IRQ level is defined by the value of "n", as follows:

Write to	Enables
x0002F7	IRQ7
x0002F6	IRQ6
x0002F3	IRQ3
x0002F2	IRQ2, 9

This command performs no function for MicroChannel Bus mode.

6.0 Registers (Continued)

Setup Read 1 x00A20 (x00A24) READ ISA/MicroChannel

A read to this register returns all but the high-order bit of the 1 byte ROM/MMIO domain base address (in Host's memory space) and 2 bits of interrupt level information.

For MicroChannel Host bus adapters, this information must have been set during the setup function of POST. The address specifies where, in a 512 kB portion of 1 MB of MicroChannel Host-addressable memory, TROPIC registers will be located.

For ISA Host bus adapters, this information must be set (by jumpers, switches, etc.) when the adapter is installed, or using a proprietary software downloading scheme, to define where in the Host-addressable memory TROPIC registers will reside.

x00A20 (x00A24) READ

7	6	5	4	3	2	1	0
RAB18	RAB17	RAB16	RAB15	RAB14	RAB13	Encoded IRQ	

Bit(s)	Description
7–2	**ROM/MMIO Host Base Address:** (Address Bits 18–13, respectively): Used to determine all but the high order bit of the ROM/MMIO starting address, usually as part of Initialization handshaking (see Section 7.0), as follows:

Setup Read 1-Bit	Boundary	ROM/MMIO Address Bit
7	256 kB	18
6	128 kB	17
5	64 kB	16
4	32 kB	15
3	16 kB	14
2	8 kB	13

The ROM/MMIO domain is mapped to any contiguous 8 kB block within a 1 MB Host address space. If an optional BIOS module is installed on the adapter that executes at power-on time, the ROM/MMIO domain must be limited to the 96 kB of BIOS space in the Host (x0C8000–0DFFFF).

Note: For *MicroChannel Host.* See bit 0 of Setup Read 2 Register at x0A22 (x0A26) for the value of address bit 19 (512 kB). For *ISA Host:* Bit 19 is always equal to 1.

1–0 **Encoded IRQ Level:** Indicates interrupt level selected for adapter, as follows:

Bit 1	Bit 0	ISA Bus Mode	MicroChannel Bus Mode
0	0	IRQ2	IRQ2
0	1	IRQ3	IRQ3
1	0	IRQ6	IRQ10
1	1	IRQ7	IRQ11

TROPIC Reset Latch x00A21 (x00A25) WRITE ISA/MicroChannel

A Write to this register causes an unconditional TROPIC reset to be latched on. The entire TROPIC is held reset until a TROPIC Reset Release is received from the Host. The TROPIC reset state is similar to a power-on reset and is used to start TROPIC in a known state. While TROPIC is held reset, the Host cannot access either the Shared RAM or the MMIO region (except for the BIOS area).

TROPIC Reset Release x00A22 (x00A26) WRITE ISA/MicroChannel

A Write to this register turns off a TROPIC reset condition previously latched on by a TROPIC Reset Latch from the Host. Before TROPIC can be fully reset, at least 50 ms must elapse between a TROPIC Reset Latch and TROPIC Reset Release instruction. If TROPIC is not latched in a reset condition, the command is ignored.

6.0 Registers (Continued)

Setup Read 2 x00A22 (x00A26) READ MicroChannel ONLY

For MicroChannel Hosts only, a read to this register returns a 1-byte value containing the Shared RAM address *plus* the high-order bit of the ROM/MMIO domain base address. This information must have been set during the setup function of POST. The address specifies where, in a 1M space of MicroChannel Host-addressable memory, the Shared RAM on the adapter will be located. The ROM/MMIO address bit specifies which 512 kB portion of 1 MB MicroChannel Host-addressable memory the ROM/MMIO domain is in.

Note: For ISA Hosts, the Shared RAM domain is set by Host software using the RRR register (see earlier discussion of MMIO Registers).

x00A22 (x00A26) READ—MicroChannel ONLY

7	6	5	4	3	2	1	0
SAB19	SAB18	SAB17	SAB16	SAB15	SAB14	SAB13	RAB19

Bit(s)	Description
7–1	**MicroChannel Hosts Only** **Shared RAM Host Base Address:** (Address Bits 19–13, respectively): Used by MicroChannel Hosts to determine the Shared RAM starting address, usually as part of Initialization handshaking (see Section 7.0), as follows:
0	**MicroChannel Hosts Only** **ROM/MMIO Host Base Address: Bit 19:** Used by MicroChannel Hosts to determine bit 19 of the ROM/MMIO domain base address (see Setup Read 1 Register above for more information)

Setup Read 2-Bit	Boundary	Shared RAM Address Bit
7	512 kB	19
6	256 kB	18
5	128 kB	17
4	64 kB	16
3	32 kB	15
2	16 kB	14
1	8 kB	13

Adapter Interrupt Enable x00A23 (x00A27) WRITE ISA ONLY

A Write to this register Resets and re-enables *only* the TROPIC-based adapter's interrupt generation circuitry. Since this leaves all other Host adapters disabled, the TROPIC adapter is able to monopolize the interrupt facilities.

MicroChannel POS REGISTERS (MicroChannel Only)

During Setup *only,* TROPIC provides PIO-addressable POS registers for polling and initializing adapters in MicroChannel Hosts, in keeping with MicroChannel architecture, these registers let configuration information be written from the non-volatile POS memory on the MicroChannel motherboard to TROPIC during Setup. However, these registers *are not* available during TROPIC operations after Setup. (During normal operation, refer instead to the Setup Read 1 and Setup Read 2 PIO Registers for adapter information.) The POS Register region of PIO space has the following structure:

MicroChannel POS Register Locations (only available during Setup)

x00107	Channel Check/Status Register (High Byte)—READ ONLY
x00106	Channel Check/Status Register (Low Byte)—READ ONLY
x00105	Status/Check Register
x00104	Configuration Register (High Byte)
x00103	Configuration Register (Low Byte)
x00102	Card Enable
x00101	MicroChannel Card ID (High Byte)—READ ONLY
x00100	MicroChannel Card ID (Low Byte)—READ ONLY

6.0 Registers (Continued)

MicroChannel Card ID Register Pair (Read Only)

This read-only register pair provides the unique MicroChannel Card ID (as stored in the Adapter Identification PROM). Bits 15–4 of the ID are always set at xE00, so the range of unique Card ID values are xE0000 to xE000F.

x00101								x00100							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CARD ID High Byte (Hardwired to xE0)								Upper 4 Bits of CARD ID Low Byte (Hardwired to x0)				Lower 4 Bits of CARD ID Low Byte (Unique to Adapter)			

Bit(s)	Description
15-8	**Card ID High Byte:** This is always "hardwired" to xE0.
7–4	**Card ID Low Byte (Most Significant 4 bits):** This is always "hardwired" to x0.
3–0	**Card ID Low Byte (Least Significant 4 bits):** These bits are card-specific.

Card Enable Register

This register contains the MicroChannel Card Enable bit and the Shared RAM Base Address (which is loaded from Configuration Register bits 15–9 during POST).

x00102							
7	6	5	4	3	2	1	0
AB19	AB18	AB17	AB16	AB15	AB14	AB13 (= 0)	CENA

Bit(s)	Description
7–1	**Shared RAM Host Base Address:** (Address Bits 19–13): Used to set the shared RAM page starting address during Setup. This location must be set before the Shared RAM can be accessed and must be set to a location in the memory map that does not cause a conflict. These register bits default to the same setting as Configuration Register Bits 15–9 on power-up or after an adapter reset. If the register contains this value, the shared RAM page is not mapped into the memory map. This register must be set to a correct address boundary as follows: • 8 kB shared RAM page should be on an 8 kB address boundary. • 16 kB shared RAM page should be on a 16 kB address boundary. • 32 kB shared RAM page should be on a 32 kB address boundary. • 64 kB shared RAM page should be on a 64103 address boundary. For RAM paging, the address boundary can be on a 16 kB boundary since only 16 kB of PC address space is used. **Note:** To select a valid address boundary, RRR Bit 1 (AB 13) should always be set to 0.
0	**Card Enable Bit (CENA):** This bit, when set to 1, enables all MMIO and PIO operations along with the card Data Bus and return signal drivers. If set to 0, the card is disabled.

6.0 Registers (Continued)

Configuration Register Pair

This register pair provides an alternative to hardware jumpers at Setup.

x00104								x00103							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMA19	RMA18	RMA17	RMA16	RMA15	RMA14	RMA13	Encoded IRQ Level	—	—	—	RAM Size		RATE	PR/AL	

Bit(s)	Description
15–9	**ROM/MMIO Host Base Address:** (Address Bits 19–13): Used to set the ROM/MMIO starting address during Setup. This location must be set before the ROM/MMIO can be accessed and must be set to a location in the memory map that does not cause a conflict. The ROM/MMIO domain is mapped to any contiguous 8 kB block within a 1 MB Host address space.
8–7	**Encoded IRQ Level:** Selects interrupt level for adapter, as follows: Bit 8 / Bit 7 / Selected IRQ 0 / 0 / IRQ2 0 / 1 / IRQ3 1 / 0 / IRQ10 1 / 1 / IRQ11
6–4	Reserved.
3–2	**Shared RAM Page Size:** Bits 3 and 2 select the shared RAM page (window) size, i.e., the amount of the Host's memory space that is allocated to shared RAM. These bits are coded as follows: Bit 3 / Bit 2 / Page Size 0 / 0 / 8 kB 0 / 1 / 16 kB 1 / 0 / 32 kB 1 / 1 / 64 kB This shared RAM page size may not be the total amount of shared RAM on the adapter. For example, an adapter with 64 kB of available shared RAM can be set for a 16 kB page size to allow shared RAM paging. If bit 3 is set to 1 and bit 2 is set to 0, this would indicate 16 kB of shared RAM in the Host's memory map.)
1	**TROPIC Data Rate:** 0 = 4 Mbps, 1 = 16 Mpbs
0	**Primary/Alternate Adapter Selection Bit:** 0 = Primary, 1 = Alternate

Status/Check Register

This register contains the MicroChannel Status and I/O Channel Check indicator bits.

x00105							
7	6	5	4	3	2	1	0
CHCK	CSTAT	—	—	—	—	—	—

Bit(s)	Description
7	**Channel Check:** Reflects the true value of −CHCK, TROPIC's I/O Channel Check Signal (0 = Active, 1 = Inactive).
6	**Channel Check Status:** Only valid if Channel Check is active (0 = Present, 1 = Not Present).
5–0	Reserved.

Channel Check Status Registers (Read Only)

This read-only register pair holds the MicroChannel Channel Check Status bits. It should be considered a reserved area.

7.0 Software Operation of TROPIC

As mentioned earlier, once TROPIC initialization is complete, the Host software communicates with and controls TROPIC through three methods: Shared RAM, interrupts, and registers. This section briefly describes procedures for using those methods to operate TROPIC. More complete details are provided in a separate programming reference document.

SHARED RAM CONTROL BLOCKS

One use of Shared RAM is to provide buffers for passing Token-Ring data between TROPIC and the Host. A second, equally important use of the Shared RAM is to allow the passing of specialized data between TROPIC and the Host software in *Control Blocks.* Control Blocks are used to pass *Commands* (i.e. requests), and the status of requests between TROPIC and the Host software. There are four Control Blocks:

- **System Request Block (SRB)**—used to pass a command from the Host software to TROPIC and to pass return codes back to the Host software
- **System Status Block (SSB)**—if an SRB command requires further processing, this block is used to pass the ultimate results of the command from TROPIC to the Host software
- **Adapter Request Block (ARB)**—used to pass a command or information from TROPIC to the Host software
- **Adapter Status Block (ASB)**—used by the Host software to respond to an ARB command received from TROPIC, usually with an indication of successful or unsuccessful completion

These Control Blocks are used in conjunction with interrupts to provide event-driven, asynchronous operation of TROPIC, as described later.

Control Block Commands include high level requests from the Host software to TROPIC for MAC (Media Access Control) and LLC (Logical Link Control) services, which are provided within TROPIC by its MPU and Protocol Handler. The Host software is therefore relieved from having to manage MAC, or LLC services, greatly reducing Host program size and complexity.

SHARED RAM BUFFERS

Shared RAM includes two types of buffers for passing Token-Ring data between TROPIC and the Host:

- Transmit Buffers (also called Data Holding Buffers, or DHBs)
- Receive Buffers

Transmit Buffers (DHBs)

TROPIC assembles and transmits frame data from the Transmit Buffers (based on transmit commands issued through the SRB [System Request Block] by the Host software).

The number and size of the Transmit Buffers is determined when TROPIC is issued an Open Adapter command (as described later).

RECEIVE BUFFERS

TROPIC takes frame data from the Token-Ring and writes it into Receive Buffers in Shared RAM. It then places a Receive command in the ARB and issues an interrupt to the Host software. Among other things, the Receive command information will include the starting address of the Receive buffer.

The total size of the Receive Buffers is determined indirectly when TROPIC is issued an Open Adapter command (described later); all Shared RAM that is not needed for work areas, control blocks, communication areas, and Transmit Buffers is configured as Receive Buffers. Multiple Receive Buffers may be chained together to hold a complete frame, in which case each buffer will contain a pointer to the next buffer in the chain (and the Receive command will indicate the starting address of the first Receive Buffer).

INITIALIZATION HANDSHAKING

Before beginning an operating session with TROPIC, the Host software must first perform an initialization to ensure a known starting point. The typical method is as follows:

1. Invoke a Reset condition on TROPIC (using an Adapter Reset PIO Register access for MicroChannel and ISA.
2. Delay for at least 50 ms.
3. Invoke a Reset Release (using a Reset Release PIO Register access for MicroChannel and ISA.
4. If Shared RAM is to be paged, request paging by writing xC000 to SRPR (Shared RAM Page Register).
5. Set the Enable Interrupt bit of the HISR register (Host Interrupt/Status Register).
6. Wait for 1 to 3 seconds until TROPIC sets the "SRB Response" bit of the HISR register (indicating initialization and TROPIC's Adapter Diagnostics Program are complete).
7. Read the WRBR (Write Region Base Register) and the Shared RAM Segment address. Use the offset in the WRBR and the Shared RAM Segment Address to calculate the initial location of the SRB where TROPIC has posted the results of the initialization (including any diagnostics failure messages).
8. Read and evaluate the results in the SRB and store important parameters. If diagnostics code indicates successful completion, proceed with operations.
9. If Fast Path Transmission will be used, fill out the SRB with CONFIG.FAST.PATH.RAM command information and interrupt TROPIC. Read the response in the SRB to get the new SRB address.

7.0 Software Operation of TROPIC (Continued)

HOST-TO-TROPIC COMMAND HANDSHAKING

Commands that Host software can issue to TROPIC using the SRB are summarized later in this section. The general procedure for issuing a command to TROPIC is:

1. Host software writes the appropriate Command code and related parameters into the SRB.
2. Host software sets the TISR register's "Command in SRB" bit to issue an interrupt to TROPIC.
3. TROPIC checks the validity of the SRB contents and either:
   — completely processes the command, sets a return code other than xFF in the SRB, and issues an interrupt to the Host software (by setting the HISR register's "Response in SRB" bit).
   — performs initial processing only, sets the return code to xFF in the SRB, and provides a "command correlator". TROPIC issues an interrupt to the Host software (by setting the HISR register's "Response in SRB" bit) *only* if an SRB Free Request Interrupt is issued by the Host software (by setting the TISR register's "SRB Free Request" bit).
4. Depending on the command, TROPIC may request more data using the ARB (Adapter Request Block) and DHB (i.e., the Transmit Buffer). The Host software uses the ASB (Adapter Status Block) to indicate that the requested data has been moved to the appropriate Shared RAM location. After reading the ARB, the Host software interrupts TROPIC by setting the TISR "ARB Free" bit.
5. When processing is completed for a command in process (i.e., return code is xFF in Step 3), TROPIC puts the final return code in the SSB (System Status Block) and interrupts the Host software by setting HISR "SSB Response" bit).
6. After the Host software reads the return code from the SSB, it interrupts TROPIC by setting the TISR "SSB Free" bit.

TROPIC-TO-HOST COMMAND HANDSHAKING

The commands which can be issued from TROPIC to the Host software using the ARB are summarized in a table later in this section. The general procedure for issuing a command to the Host software is as follows:

1. TROPIC writes the appropriate Command code and related parameters into the ARB.
2. TROPIC sets the HISR register's "ARB Command" bit to issue an interrupt to the Host software.
3. The Host software reads the ARB contents and issues an interrupt to TROPIC by setting the TISR register's "ARB Free" bit (to acknowledge command receipt and to indicate that TROPIC can re-use the ARB).
4. If a response is required based on the command, the Host software writes the response information into the ASB (Adapter Status Block) and issues an interrupt to TROPIC by setting the TISR register's "Response in ASB" bit.
5. After TROPIC reads the ASB response, it either:
   — sets a return code of xFF in the SRB, and issues an interrupt to the Host software by setting the HISR register's "ASB Free" bit *only* if the "ASB Free Request" interrupt bit is set.
   — sets an error return code indicating that an error has been detected, and issues an interrupt to the Host software by setting the HISR register's "ASB Free" bit, regardless of the status of the "ASB Free Request" interrupt bit.

SRB (Host-to-TROPIC) COMMAND SUMMARY

Direct Interface Commands

These commands affect TROPIC as a whole, rather than specific SAPs (Service Access Points) or link stations, and do not involve LLC processing.

Command Name	Code (Hex)	Description
DIR.CLOSE.ADAPTER	04	Closes the adapter, terminating all Ring communications (or Open Wrap test, if in process)
DIR.CONFIG.FAST.PATH.RAM	12	Tells adapter to use Fast Path interface techniques and sets values for the amount of shared RAM to allocate for the transmit interface and the size of the Fast Path buffers to be used; this command can only be issued when the adapter is in a Closed state
DIR.INTERRUPT	00	Forces a TROPIC interrupt; has no effect on Ring communications
DIR.MODIFY.OPEN.PARMS	01	Modifies adapter options previously set by DIR.OPEN.ADAPTER
DIR.OPEN.ADAPTER	03	Opens adapter with specified options, preparing adapter for normal ring operations (in automatic receive mode) or adapter wrap test
DIR.READ.LOG	08	Reads and resets adapter error counters
DIR.RESTORE.OPEN.PARMS	02	Modifies adapter options set by DIR.OPEN.ADAPTER
DIR.SET.FUNCT.ADDRESS	07	Sets the functional address for the adapter to receive Ring messages
DIR.SET.GROUP.ADDRESS	06	Sets the Group address for the adapter to receive Ring messages

7.0 Software Operation of TROPIC (Continued)

DLC (IEEE 802.2 SAP and Station Interfaces) Commands

These commands affect SAPs (Service Access Points) or link stations, and make use of LLC protocols.

Command Name	Code (Hex)	Description
DIC.CLOSE.SAP	16	Closes (deactivates) an SAP and frees associated control block(s)
DLC.CLOSE.STATION	1A	Closes one link station; will not complete while Ring is "beaconing"
DLC.CONNECT.STATION	1B	Initiates a SABME_UA exchange to place the local and remote link stations in a data transfer state, or completes such an exchange that has been initiated by the remote station
DLC.FLOW.CONTROL	1D	Controls the flow of data across a specified link station on an SAP, or every link on an SAP
DLC.MODIFY	1C	Modifies selected working values on an open link station or the default values of an SAP
DLC.OPEN.SAP	15	Opens (activate) an SAP and allocates an individual SAP control block
DLC.OPEN.STATION	19	Allocates resources to support a logical link connection
DLC.REALLOCATE	17	Removes a given number of link station control blocks from a SAP and returns them to the adapter pool, or removes a given number of link station control blocks from the adapter pool and returns them to a SAP
DLC.RESET	14	Resets one SAP and all associated link stations, or all SAPs and all associated link stations
DLC.STATISTICS	1E	Reads statistics for a specific link station

Transmit Commands and the Fast Path Interface

There is actually only one transmit command with various subcommands to indicate the type of data to be transmitted. All the commands have the same format with the only difference being the actual command code.

The Fast Path interface provides a pool of transmit buffers that Host software can fill asynchronously to the TROPIC MPU's processing. Host software moves Transmit commands and related data together to these buffers and then signals TROPIC that the pools have been updated. TROPIC then processes frames according to each data block's associated command.

The Fast Path transmit interface is activated by issuing a "DIR.CONFIG.FAST.PATH.RAM" SRB command to TROPIC. TROPIC subsequently processes transmit commands based on Fast Path interface procedures. Fast Path handshaking and operations are covered in detail in a separate programming document.

Note: If Fast Path Transmit is not activated, then TROPIC operates in a less efficient transmission mode that requires the Host software to first issue a transmit command *only*, wait for a TROPIC response, and *then* move transmission data to the Transmit buffer. This mode exists primarily for compatibility with earlier drivers, and it should not be used in new software.

Command Name	Code (Hex)	Description
TRANSMIT.DIR.frame	0A	Requests transmission of a Direct transmission; the application must assemble the entire message, leaving room for the source address, which TROPIC inserts; no LLC protocol assistance is provided in this mode
TRANSMIT.I.frame	0B	Requests transmission of I-format (Information transfer format) frame
TRANSMIT.UI.frame	0D	Requests transmission of UI-format (Unsequenced Information transfer format) frame
TRANSMIT.XID.CMD	0E	Requests transmission of XID-format (Exchange Identification format) Command frame
TRANSMIT.XID.RESP.FINAL	0F	Requests transmission of XID-format final Response frame (in response to an XID Command being received)
TRANSMIT.XID.RESP.NOT.FINAL	10	Requests transmission of XID-format non-final Response frame (in response to an XID Command being received)
TRANSMIT.TEST.CMD	11	Requests transmission of TEST-format Command frame

7.0 Software Operation of TROPIC (Continued)

ARB (TROPIC-to-Host) COMMAND SUMMARY

Command Name	Code (Hex)	Description
DLC.STATUS	83	Indicates a change in DLC status to the Host
RECEIVED.DATA	81	Informs the Host that data for a particular STATION-ID has been received; the Host must move the data from the Shared RAM Receive buffers to buffers in Host memory
RETRANSMIT.DATA	86	Lets adapter request a retransmission of frames by the Host due to changes in link station status; the Host responds by moving frames to the transmit buffer Pool starting at the frame with the correlator in the ARB
RING.STATUS.CHANGE	84	Indicates a change in network status to the Host
TRANSMIT.DATA.REQUEST	82	When Fast Path is *not* used, informs the Host that TROPIC now needs data for a Transmit command previously issued by the Host

BRIDGE OPERATION AND COMMANDS

By using two TROPIC-based adapters in the same workstation, each connected to a separate Ring, a bridge application program can forward frames between the two Rings. This capability is supported by some additional resources:

- two additional SRB commands
- one additional ARB command
- two additional Shared RAM areas—a Bridge Transmit Control area and Bridge Transmission buffers
- two additional interrupt register bits, one in the HISR and one in the TISR

Bridge handshaking and operations are covered in detail in a separate programming document. The commands are summarized below:

Command Name	Code (Hex)	Description
DIR.CONFIG.BRIDGE.RAM	0C	Tells adapter how much shared RAM to allocate for bridge transmit control areas and buffers
DIR.SET.BRIDGE.PARMS	09	Lets Host set values and conditions for adapter to use when copying frames for forwarding
RECEIVED.BRIDGE.DATA	85	Informs Host that adapter has received frame that requires forwarding

8.0 Pin Descriptions

Note: **I** = Input-only digital, **O** = Output only digital, **B** = Bidirectional digital, **A** = Analog
I-PU = Input-only digital with internal pullup*, **I-PD** = Input-only digital with internal pulldown*
B-PU = Bidirectional digital with internal pullup*
– = Active low signal
*Internal polysilicon resistor with nominal value of 15k ±30%

Pin Name	Pin No.	Type	Description
TOKEN RING INTERFACE PINS			
-4 MBPS	N09	O	**4 MBPS** RING SPEED: This output is connected to an external 16 Mbps equalizer. It is driven low if the ring speed is set to 4 Mbps and can sink 8.0 mA at 0.3V. If the ring speed is set to 16 Mbps, this output is set to TRI-STATE® with a maximum leakage current of 10 mA.
-16 MBPS	N08	O	**16 MBPS** RING SPEED: This output is connected to an external 4 Mbps equalizer. It is driven low if the ring speed is set to 16 Mbps and can sink 8.0 mA at 0.3V. If the ring speed is set to 4 Mbps, this output is set to TRI-STATE with a maximum leakage current of 10 mA.
PHANTA	P07	A	**PHANT**OM DRIVE **A**—This pin and PHANTOM DRIVE B are the outputs for the Phantom Drive signal. These Pins are connected via resistors to the line side of the transmit pulse transformer. The Phantom Drive signal inserts the station into the wiring concentration unit.
PHANTB	P06	A	**PHANT**OM DRIVE **B**—see PHANTA.
PLL4	P09	A	**PLL** FILTER—4 MBPS: The resistor and capacitors attached to the A pin control how responsive PLL oscillator is to phase changes in the received data at 4 Mbps.
PLL16	P10	A	**PLL** FILTER—16 MBPS: The capacitor attached to the B pin controls how responsive the PLL oscillator is to phase changes in the received data at 16 Mbps.
RINA	N07	A	**Ring IN A:** One of the two lines on which differential data is received from the Token Ring through the receive transformer and equalizer circuits.
RINB	P08	A	**Ring IN B:** See RINA above.
ROUTA	P05	A	**Ring OUT A:** One of the two lines on which differential data is driven to the Token Ring through the transmit transformer and equalizer circuits.
ROUTB	N05	A	**Ring OUT B:** See ROUTA above.
POWER SUPPLY PINS (DIGITAL)			
GND	D07, E06, E07, E08, F04, G04, G10, H10, J04, J10, L05, L08, L09		
V_{CC}	D06, D08, E05, G03, G11, H04, J03, J11, K10, M05, M08		
POWER SUPPLY PINS (ANALOG) **Care should be taken to reduce noise in these pins since they supply analog elements of TROPIC.**			
GND	M07 (PLL Filter Return), N06		
V_{CC}	L06, L07, M06		
NO CONNECT PINS			
NC All Busses For ISA	 E01, F01, F09, F11, G13, H12, J01, L11, L12, M01, M11, M12, M13, M14, N01, N11, N12, N13, N14, P13, P14 C01, D01		
CLOCK INTERFACE PINS			
32 MHZ	F14	I	**32 MHZ** IN: This input line must be driven from a 32 MHz ±0.005% signal source with a duty cycle of 40–60% of total cycle.

8.0 Pin Descriptions (Continued)

Note: **I** = Input-only digital, **O** = Output only digital, **B** = Bidirectional digital, **A** = Analog
I-PU = Input-only digital with internal pullup*, **I-PD** = Input-only digital with internal pulldown*
B-PU = Bidirectional digital with internal pullup*
− = Active low signal
+ = Active high signal
*Internal polysilicon resistor with nominal value of 15k ±30%

Pin Name	Pin No.	Type	Description
TROPIC LOCAL STORAGE INTERFACE PINS			
−RAS +CO/−DAT	E12	O	−**ROW ADDRESS STROBE** / (+**CODE**/−**DATA**): For Dynamic RAM, this output is the Row Address Strobe (RAS). It is activated on any access by TROPIC to the DRAM, and also during refresh cycles. If static RAM is used, this signal is high during accesses to the Code Block and low during accesses to the Data Block.
−CASHI −SRAMHI	D12	O	**COLUMN ADDRESS STROBE HI**/−**SRAM SELECT HI**: This output is used to select the dynamic or static RAM devices on the HI byte of the storage bus. When this signal is activated for a read access, good parity must be provided by the external devices.
−CASLO −SRAMLO	D11	O	**COLUMN ADDRESS STROBE LO**/−**SRAM SELECT LO:** This output is used to select the dynamic or static RAM devices on the LO byte of the storage bus. When this signal is activated for a read access, good parity must be provided by the external devices.
−ROM	G12	O	**ROM** SELECT: This output is used to select ROM devices on the storage bus. All reads and writes to the ROM are word (two-byte) operations.
−AIP	F13	O	**AIP** SELECT: This output is activated by TROPIC during any MPU or Host read cycle that references the AIP. This signal is also activated for MicroChannel accesses to the Card ID. When this line is active, only the low-order 4 bits of the data bus need to be driven. The high-order 12 data bits and the parity bits are ignored by TROPIC. No WRITE logic is enabled during AIP Select cycles; therefore, writing to the AIP is not allowed.
−DRAMWE	E13	O	**DRAM WRITE ENABLE**: This output line is activated by TROPIC during any write access to RAM or DRAM. This signal is conditioned by timing logic to provide the correct Write Enable signal for DRAMs selected by the CAS lines.
−SRAMOE	E11	O	**SRAM OUTPUT ENABLE**: This output signal has meaning only when static RAM is used. It is activated by TROPIC on any RAM read access from either byte of the storage bus.
−SWRITE	E14	B	**STORAGE WRITE**: This bidirectional line is activated by TROPIC whenever the current storage bus operation is a "write" from TROPIC's perspective. The signal is not conditioned by timing logic.
−SD15 to −SD8 −SDP1	(Note 1)	B-PU	**STORAGE DATA**(bits 15 through 8) and **Storage Data Parity 1** (MSB): This bidirectional bus carries the high-order data for all storage devices on the Local Storage Interface.
−SD7 to −SD0 −SDP0	(Note 1)	B-PU	**STORAGE DATA**(bits 7 through 0) and **Storage Data Parity 0** (LSB): This bidirectional bus carries the low-order data for all storage devices on the Local Storage Interface. If a separate BIOS module is used, it must be attached to this byte of the storage bus. Also, for accesses to a separate BIOS module, parity does not need to be provided, and TROPIC inverts the data so it is considered to be positive active.
−SA14 to −SA0	(Note 1)	B	**STORAGE ADDRESS**(bits 14 through 0): This bidirectional bus carries the address for all storage devices on the Local Storage Interface and is valid when one of the storage select lines is activated.
−SMI	P12	I-PU	**STORAGE MEMORY INHIBIT**: For normal operation, this input pin MUST be tied inactive or left unconnected; it has an integrated pullup resistor in its receiver.
−MIP	P11	I-PU	**MIP** TEST: For normal operation, this input pin MUST be tied inactive or left unconnected; it has an integrated pullup resistor in its receiver.

Note 1: See the Connection Diagrams and Pinout Tables in Section 12.0 for Pin Numbers.

8.0 Pin Descriptions (Continued)

Note: **I** = Input-only digital, **O** = Output only digital, **B** = Bidirectional digital, **A** = Analog
I-PU = Input-only digital with internal pullup*, **I-PD** = Input-only digital with internal pulldown*
B-PU = Bidirectional digital with internal pullup*
− = Active low signal
+ = Active high signal
*Internal polysilicon resistor with nominal value of 15k ±30%

Pin Name	Pin No.	Type	Description
HOST INTERFACE PINS FOR ALL BUS TYPES			
RESET	A01	I	HOST **RESET**: Input used to reset TROPIC. Positive active on ISA and MicroChannel hosts.
−CFGLD	E10	O	**CONFIG**URATION **LOAD**: Held low to "gate" settings from physical jumpers (or equivalent) to TROPIC's internal Configuration Register. Low level when RESET is active.
−CFG2	M09	I-PU	HOST **CONFIG**URATION **2**: This pin and pins CFG1 and CFG0 are used together to indicate the bus type to TROPIC during reset; for more information, see Section 4.0.
−CFG1	M10	I-PD	HOST **CONFIG**URATION **1**: see CFG2
−CFG0	N10	I-PU	HOST **CONFIG**URATION **0**: see CFG2
HD15 to HD0	(Note 1)	B	**HOST DATA**(bits 15 through 0)—These bidirectional, positive active pins are used to transfer data across the Host data bus. TRI-STATE when RESET is active.
HDP1	B03	B	**Host Data Parity 1** (MSB): Bidirectional, positive active pin used to transfer parity bit for most significant Host Data byte.
HDP0	A03	B	**Host Data Parity 0** (LSB): Bidirectional, positive active pin used to transfer parity bit for least significant Host Data byte.
HA19 to HA0	(Note 1)	I	**HOST ADDRESS**(bits 19 through 0)—These positive active pins are connected to the Host address bus.
−EHDH	A07	O	**ENABLE HOST DATA HIGH**: External buffer enable for high byte (driven high when RESET is active).
−EHDL	B07	O	**ENABLE HOST DATA LOW**: External buffer enable for low byte (driven high when RESET is active).
−EHPI	A02	O	**ENABLE HOST PARITY IN**: Enables Host Parity In for Data Bus buffer hardware. Driven high when RESET is active.
HDDIR	C07	O	**HOST DATA DIR**ECTION: Direction signal source for Host Data buffer hardware. Low for Host Reads, high for Host Writes. Driven high when RESET is active.

Note 1: See the Connection Diagrams and Pinout Tables in Section 12.0 for Pin Numbers.

8.0 Pin Descriptions (Continued)

Note: **I** = Input-only digital, **O** = Output only digital, **B** = Bidirectional digital, **A** = Analog
I-PU = Input-only digital with internal pullup*, **I-PD** = Input-only digital with internal pulldown*
B-PU = Bidirectional digital with internal pullup*
− = Active low signal
+ = Active high signal
*Internal polysilicon resistor with nominal value of 15k ±30%

Pin Name	Pin No.	Type	Description
HOST INTERFACE PINS FOR ISA HOSTS			
+AEN	C04	I	**A**DDRESS **EN**ABLE
+RDY	C02	O	CHANNEL **READY**: High level when RESET is active.
−BHE	B01	I	**B**YTE **H**IGH **E**NABLE
−BIOS	F10	O	**BIOS** ACCESS: Activated by TROPIC when Host addresses the BIOS ROM. High level when RESET is active.
−CHCK	E03	O	I/O CHANNEL **CHECK**: High level when RESET is active.
+DPEN	F02	I	**DATA PARITY ENABLE:** TROPIC checks data parity on Host writes when this signal is tied high.
−IOR	E04	I	**I/O R**EAD: If this signal and IOW are active, IOR is not recognized and TROPIC goes into Card Test mode.
−IOW	F03	I	**I/O W**RITE: If this signal and IOR are active, IOW is not recognized and TROPIC goes into Card Test mode.
−MEMR	D04	I	**MEM**ORY **R**EAD
−MEMW	D05	I	**MEM**ORY **W**RITE
−REF	B02	I	**REF**RESH
IRQ2I	P02	I	INTERRUPT **REQ**UEST **2** INPUT
IRQ2O	C03	O	INTERRUPT **REQ**UEST **2** OUTPUT: High level when RESET is active.
IRQ3I	P01	I	INTERRUPT **REQ**UEST **3** INPUT
IRQ3O	E02	O	INTERRUPT **REQ**UEST **3** OUTPUT: High level when RESET is active.
IRQ6I	N02	I	INTERRUPT **REQ**UEST **6** INPUT
IRQ6O	D03	O	INTERRUPT **REQ**UEST **6** OUTPUT: High level when RESET is active.
IRQ7I	L04	I	INTERRUPT **REQ**UEST **7** INPUT
IRQ7O	D02	O	INTERRUPT **REQ**UEST **7** OUTPUT: High level when RESET is active.
TH	P03, P04	I	**T**IE **H**IGH—These pins must be pulled High using a nominal value external pullup resistor.
HOST INTERFACE PINS FOR MICROCHANNEL HOSTS			
MIO	C04	I	+**M**EMORY/ −**I/O** CYCLE
+CHRDY	C02	O	CARD **CH**ANNEL **READY**: High level when RESET is active.
−SBHE	B01	I	**S**YSTEM **B**YTE **H**IGH **E**NABLE
−BIOS	F10	O	**BIOS** ACCESS: Activated by TROPIC when Host addresses the BIOS ROM. High level when RESET is active.
−CHCK	E03	O	I/O CHANNEL **CHECK**: High level when RESET is active.
−DPENI	F02	I	**DATA PARITY ENABLE IN:** TROPIC checks data parity on Host writes when this signal goes low.
−CMD	E04	I	**COMMAND**
−ADL	F03	I	**AD**DRESS LATCH
−S1	D04	I	**S**TATUS BIT **1**
−S0	D05	I	**S**TATUS BIT **0**
−REF	B02	I	**REF**RESH

8.0 Pin Descriptions (Continued)

Note: **I** = Input-only digital, **O** = Output only digital, **B** = Bidirectional digital, **A** = Analog
I-PU = Input-only digital with internal pullup*, **I-PD** = Input-only digital with internal pulldown*
B-PU = Bidirectional digital with internal pullup*
− = Active low signal
+ = Active high signal
*Internal polysilicon resistor with nominal value of 15k ±30%

Pin Name	Pin No.	Type	Description
HOST INTERFACE PINS FOR MICROCHANNEL HOSTS (Continued)			
+A23	P02	I	SYSTEM **A**DDRESS BIT **23** (MSB)
−IRQ2	C03	O	INTERRUPT **REQ**UEST **2**: High level when RESET is active.
+A22	P01	I	SYSTEM **A**DDRESS BIT **22**
−IRQ3	E02	O	INTERRUPT **REQ**UEST **3**: High level when RESET is active.
+A21	N02	I	SYSTEM **A**DDRESS BIT **21**
−IRQ6	D03	O	**I**NTERRUPT **REQ**UEST **6**: High level when RESET is active.
+A20	L04	I	SYSTEM **A**DDRESS BIT **20**
−IRQ7	D02	O	INTERRUPT **REQ**UEST **7**: High level when RESET is active.
+MA24	P03	I	**M**EMORY **A**DDRESS ENABLE **24**
−DS16	C01	O	CARD **D**ATA **S**IZE **16**: High level when RESET is active.
−SETUP	P04	I	**SETUP** SIGNAL
−SFBK	D01	O	**S**ELECT **FEEDBACK**: High level when RESET is active.

9.0 Hardware Interface

Because TROPIC has a limited number of I/O pins and its drivers cannot directly drive the loads encountered on many of the Host interface signals, some support components ("glue") must be added to each adapter, as described in this section.

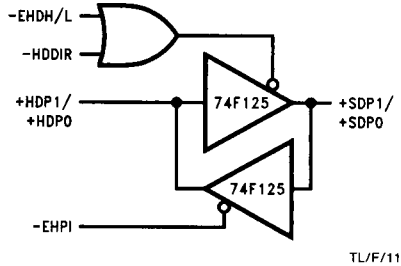
FOR ISA BUS HOSTS

- Bidirectional TRI-STATE buffer module(s), such as a 74ALS245, to buffer data bits. HDB [Host Data Bus] (15–0) is buffered as D15–D0 for a 16-bit adapter, HDB(7–0) is buffered as D7–D0 for an 8-bit adapter. Its direction pin is attached to the HDDIR signal from TROPIC; its enable pin is attached to the EHDH/L signals from TROPIC.
- Open collector drivers for the CHCK and RDY signals.
- Open collector drivers for the IRQ2/3/6/7O signals. The outputs of the glue from these signals attach directly to the IRQ2/3/6/7I signals.

FOR MICROCHANNEL BUS HOSTS

- Bidirectional TRI-STATE buffer module(s), such as a 74ALS245, to buffer data bits. The direction pins are attached to the HDDIR signal from TROPIC; each enable pin is attached to the EHDH/L signals from TROPIC. Each byte has its own enable pin, as required by MicroChannel architecture.
- TRI-STATE drivers like the 74F125 for the data parity bits and an OR gate like the 74AS32. Each parity bit requires two TRI-STATE gates and an OR gate (as shown below). TROPIC provides the EHPI signal.

TROPIC Pins



TL/F/11334–12

- An open collector driver for the CHCK signal.
- An open collector driver for the DPAREN signal. A 74F125 with both input pins tied to the HDDIR signal should be used, with its DPAREN output tied to the DPENI signal.
- An open collector driver for the IRQn signals.

10.0 Interface Considerations

This section discusses additional considerations for TROPIC's External Storage and Host Interfaces.

EXTERNAL STORAGE INTERFACE CONSIDERATIONS

TROPIC provides a flexible interface to external storage devices. These devices include static or dynamic RAM and a PROM containing microcode and possibly BIOS data. External storage may also include a separate Adapter Identification PROM (AIP) and/or separate BIOS PROM.

On MicroChannel Bus adapters, the AIP PROM also contains four bits of the Card ID. The AIP SELECT signal is used to select the PROM for both types of accesses. For AIP cycles, address bits 6 and 7 are active; for Card ID accesses, bits 6 and 7 are forced inactive.

In cases where the BIOS resides in the microcode PROM, the ROM SELECT signal is activated and the three highest order storage address bits are forced high for BIOS accesses. Thus, the BIOS must reside logically in the top 8 kB region of the PROM.

In cases where the BIOS resides in a separate PROM, the BIOS SELECT signal, along with 13 bits of the storage address bus, are used for BIOS accesses.

TROPIC supports dynamic RAM with a single Row Address Strobe (RAS) and two Column Address Strobes (CAS), and uses the upper eight address lines for the multiplexed 16-bit address. The CAS signals each select one of the bytes (HI or LO) and the RAS signal is common to both bytes. Refresh is accomplished by distributed RAS-only cycles. One refresh cycle is taken every 15 μs, so all 256 rows are refreshed in 3.84 ms.

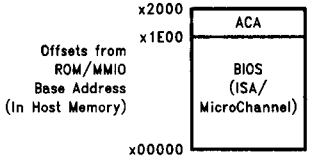
INTERFACING A SEPARATE BIOS ROM MODULE

In ISA and MicroChannel Hosts, LAN adapters typically provide support for a BIOS ROM device. The BIOS ROM usually contains code to support remote loading of the operating system on diskless workstations.

In TROPIC's default configuration, BIOS code is stored in an 8 kB portion of the microcode PROM. However, TROPIC does provide integrated support for storing BIOS code in a separate BIOS ROM device, eliminating the need for additional buffers and decoding logic.

Specifically, TROPIC supports an 8k x 8 BIOS ROM device (2764). TROPIC decodes and maps the ROM into Host memory space via the 8 kB ROM/MMIO region. Because TROPIC maps the ACA (Attachment Control Area) into the top 0.5 kB of the ROM/MMIO Host memory region (see below), the Host can access only the lower 7.5 kB of the BIOS ROM; BIOS code must therefore be stored in the lower 7.5 kB of the BIOS ROM.

BIOS/MMIO Host Memory Map

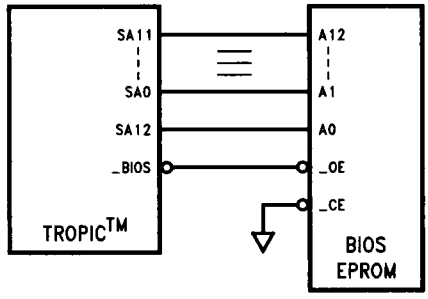


TL/F/11334–14

The ROM/MMIO base address is loaded from the Host into the TROPIC Configuration registers during initialization, either via the Storage Data Bus (for ISA) or POS registers (for MicroChannel); see Section 4.0 for details. For BIOS data access details, see the TROPIC programming reference document.

A BIOS ROM device is connected to TROPIC's Storage bus. The nature of TROPIC's Storage Interface requires the connection of the Storage Address lines (SAx lines) as shown below. The Storage Data lines SD0–7 are connected to the BIOS ROM Data pins D0–7 respectively.

Separate BIOS PROM Connection



TL/F/11334–15

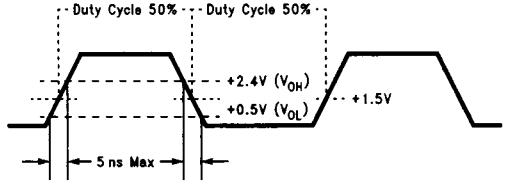
During initialization, TROPIC must be configured to utilize the separate BIOS ROM. This is accomplished by driving the SDP1 line low (0V) during configuration load. See Section 4.0 for more initialization details.

OSCILLATOR REQUIREMENTS

Frequency	32.0 MHz (TTL)
Supply Voltage	5.0V ±10%
Frequency Stability	±10 PPM (±0.01%)
Output Specifications:	
Load	5 TTL Gates Max
Duty Cycle	50% ±10% (Note 1)
Rise Time	5 ns Max (Note 2)
Fall Time	5 ns Max (Note 2)
V_{OH}	2.4V Min
V_{OL}	+0.5V Min

Note 1: Measured at +1.5V level. See diagram below.

Note 2: Measured between the +0.5V (V_{OL}) and +2.4V (V_{OH}) levels. See diagram below.



TL/F/11334–16

11.0 DC and AC Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range (T_{STG})	−40°C to +60°C
Power Dissipation (PD)	@ V_{CC} = 5.5V (@ 4 Mbps) 800 mW (@ 16 Mbps) 990 mW
Lead Temp (TL) (Soldering, 10 sec.)	(@ Pin Head) 185°C
ESD Rating	1000V (Human Body Model)

DC Specifications (@ 0°C–60°C, V_{CC} = +5.0V ±10%)

Symbol	Parameter	Min	Max	Units
V_{OH}	High Level Output Voltage (@ −1 mA)	2.4		V
V_{OL}	Low Level Output Voltage (@ 4 mA)		0.5	V
V_{IH}	Minimum High Level Input Voltage	2.0		V
V_{IL}	Minimum Low Level Input Voltage		0.8	V
I_L	Input Leakage Current V_{CC} = 5.5V, V_{IL} = 0V[1] V_{CC} = 5.5V, V_{IL} = 0V[2] V_{CC} = 5.5V, V_{IL} = 5.5V		 −10 −200 10	 μA
C_{IN}	Input Capacitance		5.0	pF

Note 1: No internal pullup.

Note 2: With internal pullup.

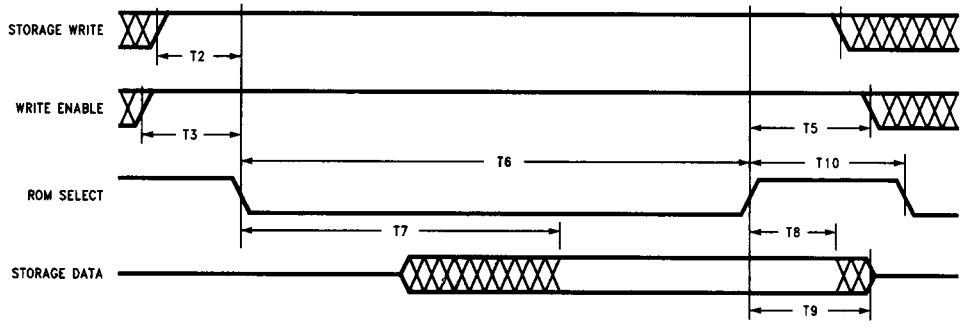
AC Specifications

EXTERNAL STORAGE INTERFACE TIMING

Timing diagrams in this section reflect the timing requirements at the TROPIC pins and assume a capacitive load of 75 pF for address and data busses and 25 pF for control signals.

After each External Storage access, there is a "dead" period during which no selects are active and TROPIC data drivers are placed in TRI-STATE. This period allows external devices that were accessed to return to TRI-STATE before other external devices or TROPIC begins driving the data bus. This "dead" period is 60 ns maximum, and all external devices must be able to return their drivers to TRI-STATE within this amount of time.

ROM Read Cycle

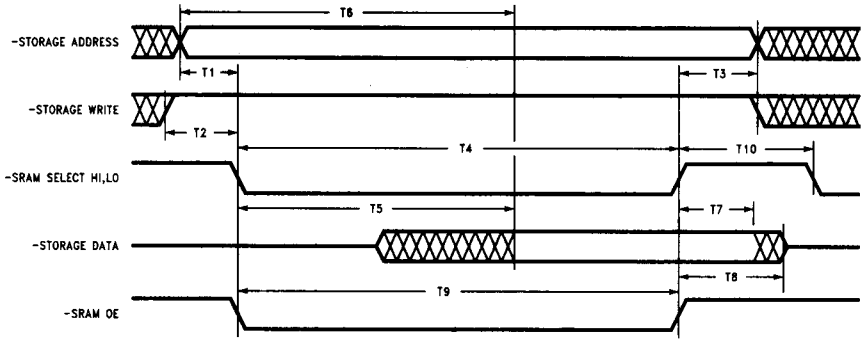


TL/F/11334–17

Symbol	Parameter	Min	Max	Units
T1	STORAGE ADDRESS setup time	20		ns
T2	STORAGE WRITE setup time	25		ns
T3	WRITE ENABLE setup time	60		ns
T4	STORAGE ADDRESS and STORAGE WRITE hold time	0		ns
T5	WRITE ENABLE hold time	60		ns
T6	ROM SELECT pulse width	120	130	ns
T7	STORAGE DATA VALID after ROM SELECT active		75	ns
T8	STORAGE DATA hold time	0		ns
T9	ROM SELECT inactive to STORAGE DATA TRI-STATE		60	ns
T10	ROM SELECT inactive	60		ns

11.0 DC and AC Specifications (Continued)

Static RAM Read Cycle

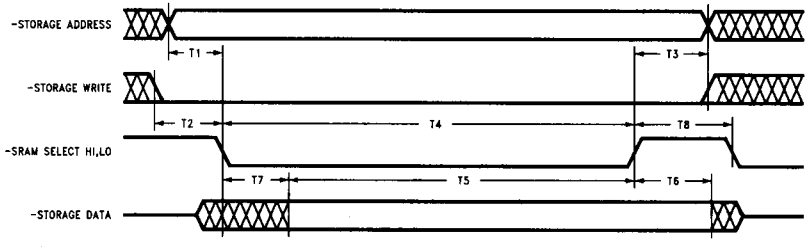


Note: – = Active low signal.

TL/F/11334–18

Symbol	Parameter	Min	Max	Units
T1	STORAGE ADDRESS setup time	20		ns
T2	STORAGE WRITE setup time	25		ns
T3	STORAGE ADDRESS and STORAGE WRITE hold time	0		ns
T4	RAM SELECT pulse width	120	130	ns
T5	STORAGE DATA VALID after RAM SELECT active		85	ns
T6	STORAGE DATA VALID after STORAGE ADDRESS valid		100	ns
T7	STORAGE DATA hold time	0		ns
T8	RAM SELECT inactive to STORAGE DATA TRI-STATE		60	ns
T9	SRAM OE pulse width	120	130	ns
T10	SRAM SELECT inactive	60		ns

Static RAM Write Cycle



Note: – = Active low signal.

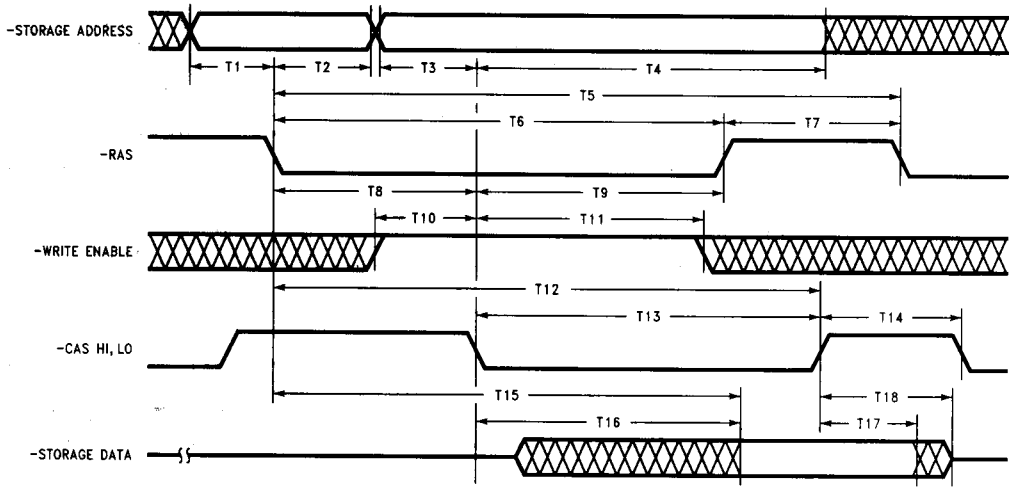
TL/F/11334–19

Symbol	Parameter	Min	Max	Units
T1	STORAGE ADDRESS setup time	20		ns
T2	STORAGE WRITE setup time	25		ns
T3	STORAGE ADDRESS and STORAGE WRITE hold time	25		ns
T4	RAM SELECT pulse width	90	100	ns
T5	STORAGE DATA setup time, MicroChannel™ STORAGE DATA setup time, ISA	80 70		ns
T6	STORAGE DATA hold time	25		ns
T7	STORAGE DATA valid after RAM SELECT active, MicroChannel STORAGE DATA valid after RAM SELECT active, ISA		10 20	ns
T8	SRAM SELECT inactive	60		ns

Note: The Storage Data timing changes depending on which bus type is selected on the host configuration pins. Differences in data timing for ISA vs MicroChannel require differences in the local memory sequencing to maximize performance.

11.0 DC and AC Specifications (Continued)

Dynamic RAM Read Cycle



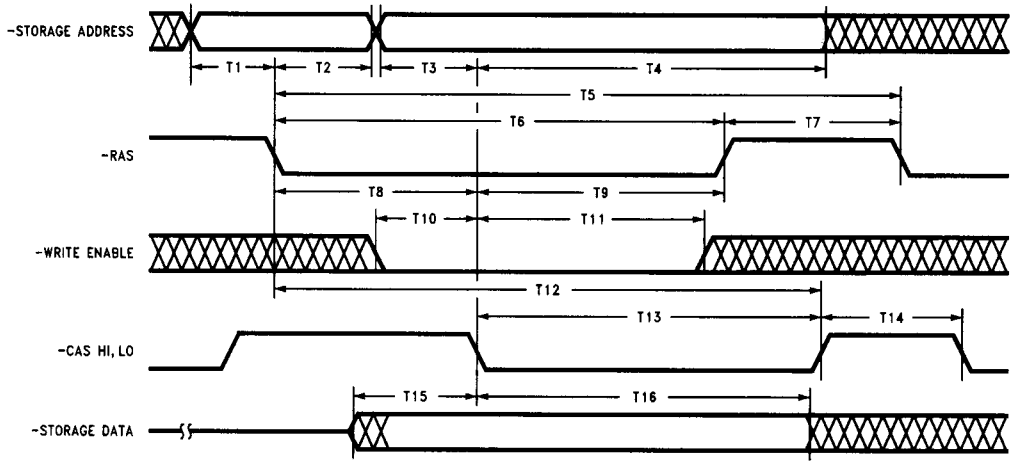
TL/F/11334-20

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	STORAGE ROW ADDRESS setup time	5		ns
T2	STORAGE ROW ADDRESS hold time	15		ns
T3	STORAGE COLUMN ADDRESS setup time	5		ns
T4	STORAGE COLUMN ADDRESS hold time	100		ns
T5	Cycle time	185		ns
T6	RAS pulse width	105		ns
T7	RAS precharge time	75		ns
T8	RAS to CAS delay time	30		ns
T9	RAS hold time from CAS	75		ns
T10	WRITE ENABLE setup time	10		ns
T11	WRITE ENABLE hold time	75		ns
T12	CAS hold time from RAS	135		ns
T13	CAS pulse width	105		ns
T14	CAS precharge time	75		ns
T15	STORAGE DATA valid from RAS		95	ns
T16	STORAGE DATA valid from CAS		65	ns
T17	STORAGE DATA hold time from CAS	0		ns
T18	CAS inactive to STORAGE DATA TRI-STATE		60	ns

11.0 DC and AC Specifications (Continued)

Dynamic RAM Write Cycle

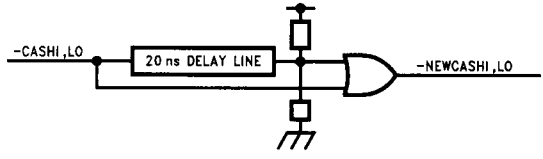


TL/F/11334-21

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	STORAGE ROW ADDRESS setup time	5		ns
T2	STORAGE ROW ADDRESS hold time	15		ns
T3	STORAGE COLUMN ADDRESS setup time	5		ns
T4	STORAGE COLUMN ADDRESS hold time	100		ns
T5	Cycle time	185		ns
T6	RAS pulse width	105		ns
T7	RAS precharge time	75		ns
T8	RAS to CAS delay time	30		ns
T9	RAS hold time from CAS	75		ns
T10	WRITE ENABLE setup time	10		ns
T11	WRITE ENABLE hold time	75		ns
T12	CAS hold time from RAS	135		ns
T13	CAS pulse width	105		ns
T14	CAS precharge time	75		ns
T15	STORAGE DATA setup time, MicroChannel STORAGE DATA setup time, ISA	35 −17		ns
T16	STORAGE DATA hold time, MicroChannel STORAGE DATA hold time, ISA	105 90		ns

Note: The Storage Data timing changes depending on which bus type is selected on the host configuration pins. Differences in data timing for ISA vs MicroChannel require differences in the local memory sequencing to maximize performance. In ISA mode some external circuitry will be required with most DRAMs. The following circuit is recommended:

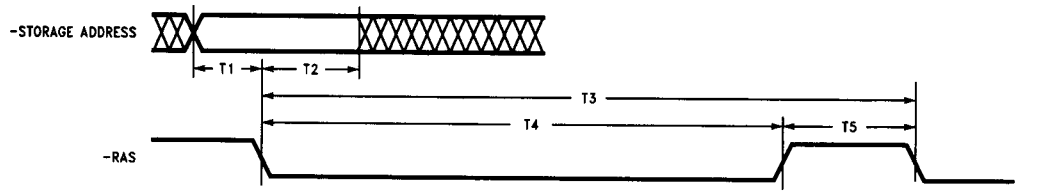


TL/F/11334-37

This trims the leading edge of −CAS and will meet the timing requirements of most DRAMs.

11.0 DC and AC Specifications (Continued)

Dynamic RAM Refresh Cycle

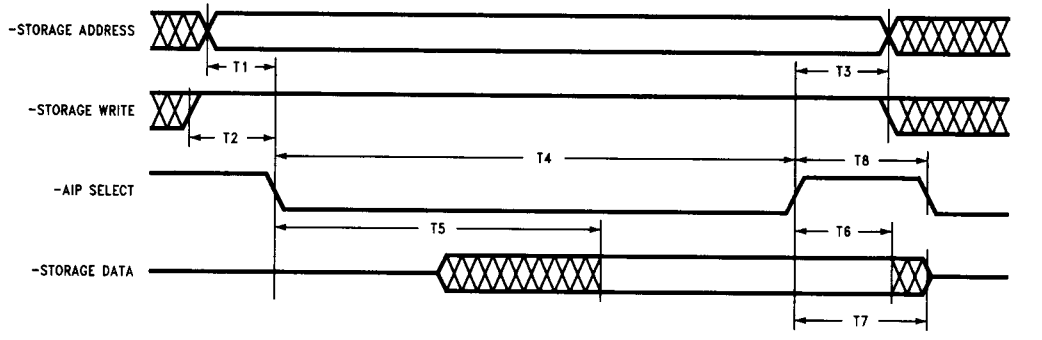


TL/F/11334–22

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	STORAGE ROW ADDRESS setup time	5		ns
T2	STORAGE ROW ADDRESS hold time	15		ns
T3	Cycle time	185		ns
T4	RAS pulse width	105		ns
T5	RAS precharge time	75		ns

AIP Read Cycle



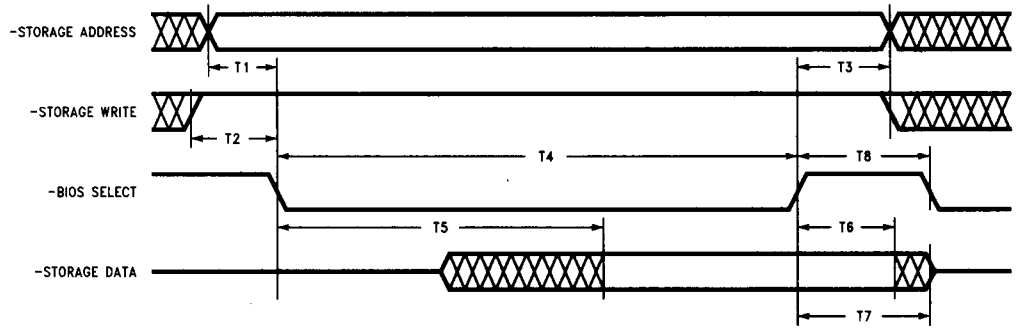
TL/F/11334–23

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	STORAGE ADDRESS setup time	20		ns
T2	STORAGE WRITE setup time	25		ns
T3	STORAGE ADDRESS and STORAGE WRITE hold time	0		ns
T4	AIP SELECT pulse width	120	130	ns
T5	STORAGE DATA VALID after AIP SELECT active		75	ns
T6	STORAGE DATA hold time	0		ns
T7	AIP SELECT inactive to STORAGE DATA TRI-STATE		60	ns
T8	AIP SELECT inactive	60		ns

11.0 DC and AC Specifications (Continued)

BIOS Read Cycle



TL/F/11334-24

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	STORAGE ADDRESS setup time	20		ns
T2	STORAGE WRITE setup time	25		ns
T3	STORAGE ADDRESS and STORAGE WRITE hold time	0		ns
T4	BIOS SELECT pulse width	490	510	ns
T5	STORAGE DATA VALID after BIOS SELECT active		450	ns
T6	STORAGE DATA hold time	0		ns
T7	BIOS SELECT inactive to STORAGE DATA TRI-STATE		60	ns
T8	BIOS SELECT inactive	60		ns

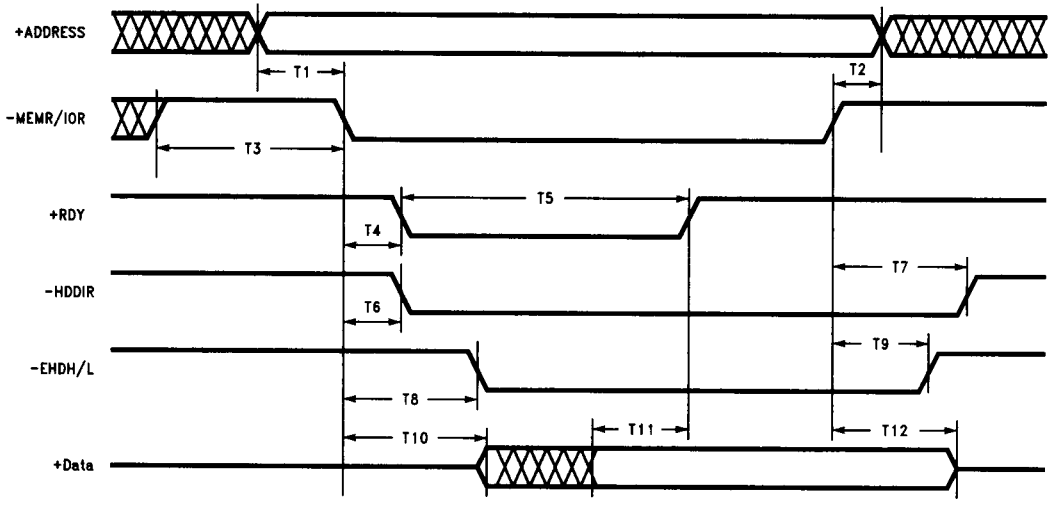
11.0 DC and AC Specifications (Continued)

HOST INTERFACE TIMING

The Host Interface provides interfaces between TROPIC and the Host Bus for interrupt signals and register access. This interface makes TROPIC appear to the Host as a memory-I/O slave.

As shown in this section, timing requirements vary according to the type of Host Bus used (ISA or MicroChannel). All timing diagrams in this section reflect the timing requirements at the TROPIC pins and assume a capacitive load of 50 pF for data lines and 25 pF for control signals and address lines.

ISA Host—Read Timing



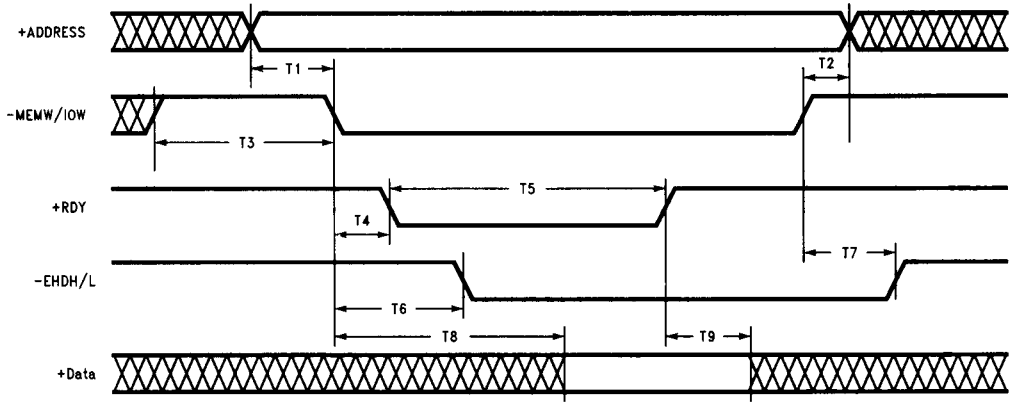
TL/F/11334–25

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	Address valid to MEMR/IOR active REF inactive to MEMW/IOW active	0 0		ns
T2	MEMR/IOR inactive to ADDRESS not valid	5		ns
T3	MEMR/IOR inactive	70		ns
T4	MEMR/IOR active to RDY low	15	40	ns
T5	RDY low normal access SRAM normal access DRAM access error	 215 215 60	 835 1210 180	ns
T6	MEMR/IOR active to HDDIR active	10	30	ns
T7	MEMR/IOR inactive to HDDIR inactive	25	70	ns
T8	MEMR/IOR active to EHDH/L active	40	135	ns
T9	MEMR/IOR inactive to EHDH/L inactive	10	25	ns
T10	MEMR/IOR active to DATA TRI-STATE off	40	135	ns
T11	DATA valid to RDY high	15		ns
T12	MEMR/IOR inactive to DATA TRI-STATE	20	50	ns

11.0 DC and AC Specifications (Continued)

ISA Host—Write Timing

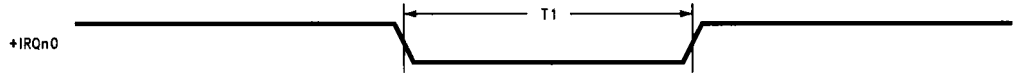


TL/F/11334–26

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	Address valid to MEMW/IOW active REF inactive to MEMW/IOW active	0 0		ns
T2	MEMR/IOW inactive to ADDRESS not valid	5		ns
T3	MEMW/IOW inactive	70		ns
T4	MEMW/IOW active to RDY low	15	40	ns
T5	RDY low normal access SRAM normal access DRAM access error	 215 215 60	 835 1210 180	 ns
T6	MEMW/IOW active to EHDH/L active	40	135	ns
T7	MEMW/IOW inactive to EHDH/L inactive	10	25	ns
T8	MEMW/IOW active to DATA valid		180	ns
T9	RDY high to DATA invalid	0		ns

ISA Host—Interrupt Request Timing



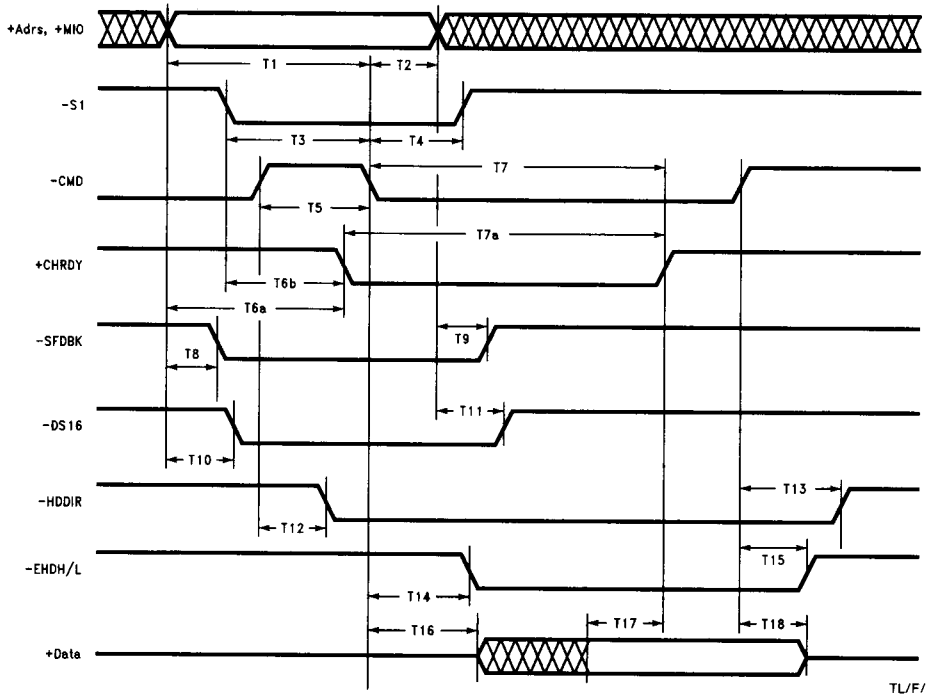
TL/F/11334–27

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	Interrupt Request n pulse width	125	440	ns

11.0 DC and AC Specifications (Continued)

MicroChannel Host—Read Timing



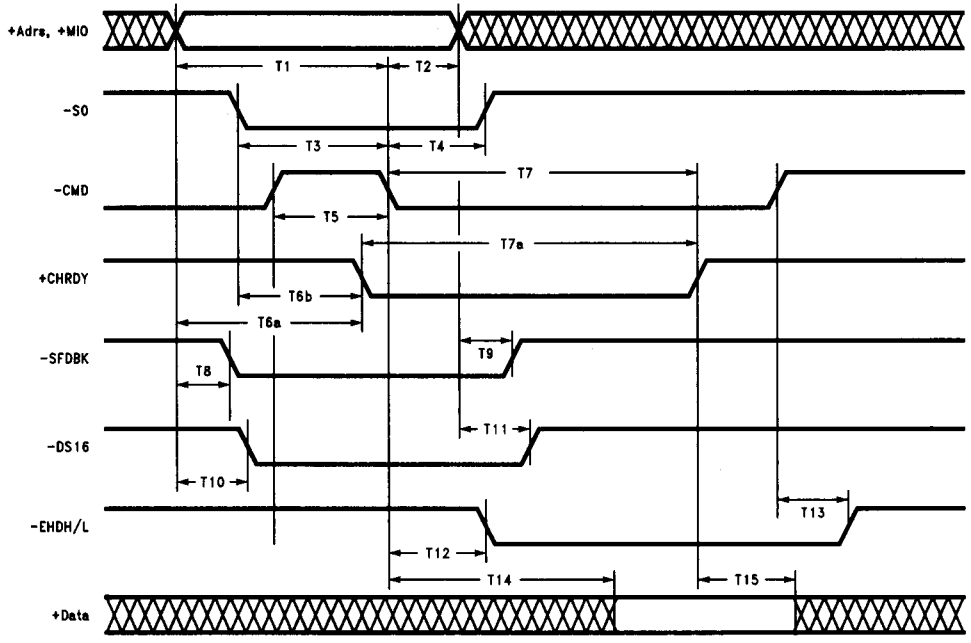
TL/F/11334-28

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	Address and MIO valid to CMD active	5		ns
T2	CMD active to Address and MIO not valid	5		ns
T3	S1 active to CMD active	10		ns
T4	CMD active to S1 inactive	5		ns
T5	CMD inactive	70		ns
T6a T6b	Address valid to CHRDY low (b met) S1 active to CHRDY low (a met)	15 10	40 29	ns
T7	CMD low to CHRDY high normal access SRAM normal access DRAM	 140 140	 835 1210	ns
T8	Address and MIO valid to SFDBK active	10	30	ns
T9	Address and MIO not valid to SFDBK inactive	10	30	ns
T10	Address and MIO valid to DS16 active	10	30	ns
T11	Address and MIO not valid to DS16 inactive	10	30	ns
T12	CMD inactive to HDDIR active	20	50	ns
T13	CMD inactive to HDDIR inactive	20	50	ns
T14	CMD active to EHDH/L active	10	25	ns
T15	CMD inactive to EHDH/L inactive	10	25	ns
T16	CMD active to DATA TRI-STATE off	10	30	ns
T17	DATA valid to CHRDY high	5		ns
T18	CMD inactive to DATA TRI-STATE	10	30	ns

11.0 DC and AC Specifications (Continued)

MicroChannel Host—Write Timing



TL/F/11334–29

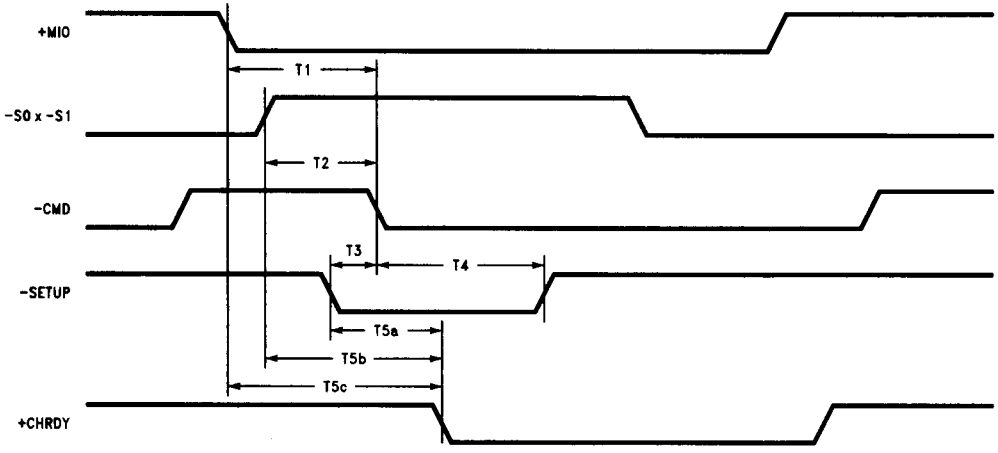
Note: HDDIR remains high throughout cycle.

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	Address and MIO valid to CMD active	5		ns
T2	CMD active to Address and MIO not valid	5		ns
T3	S0 active to CMD active	10		ns
T4	CMD active to S0 inactive	5		ns
T5	CMD inactive	70		ns
T6a	Address valid to CHRDY low (b met)	17	40	ns
T6b	S0 active to CHRDY low (a met)	11	29	
T7	CMD low to CHRDY high normal access SRAM normal access DRAM	 140 140	 835 1210	ns
T7a	CHRDY low—access error	60	80	ns
T8	Address and MIO valid to SFDBK active	10	30	ns
T9	Address and MIO not valid to SFDBK inactive	10	30	ns
T10	Address and MIO valid to DS16 active	10	30	ns
T11	Address and MIO not valid to DS16 inactive	10	30	ns
T12	CMD active to EHDH/L active	10	25	ns
T13	CMD inactive to EHDH/L inactive	10	25	ns
T14	CMD active to DATA valid		90	ns
T15	CHRDY high to DATA not valid	0		ns

11.0 DC and AC Specifications (Continued)

MicroChannel Host—Setup Timing



TL/F/11334–30

Note: – = Active low signal.

Symbol	Parameter	Min	Max	Units
T1	MIO low to CMD active	5		ns
T2	S0 x S1 active to CMD active	5		ns
T3	SETUP active to CMD active	5		ns
T4	CMD active to SETUP inactive	10		ns
T5a	SETUP to CHRDY low (b, c met)	10	30	
T5b	(S0 x S1) valid to CHRDY low (a, c met)	15	35	ns
T5c	MIO low to CHRDY low (b, c met)	15	35	

12.0 Connection Diagrams

PIN DEFINITIONS

Note: Some pins have different definitions depending on the host bus type used, as indicated in the table.

I = Input-only digital, **O** = Output only digital,

B = Bidirectional digital, **A** = Analog

I-PU = Input-only digital with internal pullup*, **I-PD** = Input-only digital with internal pulldown*

B-PU = Bidirectional digital with internal pullup*

*Internal polysilicon resistor with nominal value of 15k ±30%

NC = No Connect (*should not* be connected for normal operation)

Pin No.	Pin Name	Type
A01	RESET	I
A02	−EHPI	O
A03	HDP0	B
A04	HD0 (LSB)	B
A05	HD2	B
A06	HD5	B
A07	−EHDH	O
A08	HD8	B
A09	HD11	B
A10	−SD4	B-PU
A11	−SD1	B-PU
A12	−SDP1	B-PU
A13	−SD8	B-PU
A14	−SD12	B-PU
B01 (ISA) (MicroChannel)	 −BHE −SBHE	 I I
B02 (ISA) (MicroChannel)	 −REF −REF	 I I
B03	HDP1	B
B04	HD1	B
B05	HD3	B
B06	HD6	B
B07	−EHDL	O
B08	HD9	B
B09	HD12	B
B10	−SD5	B-PU
B11	−SD2	B-PU
B12	−SDP0	B-PU
B13	−SD9	B-PU
B14	−SD13	B-PU
C01 (ISA) (MicroChannel)	 NC −DS16	 O
C02 (ISA) (MicroChannel)	 +RDY +CHRDY	 O O

Pin No.	Pin Name	Type
C03 (ISA) (MicroChannel)	 IRQ2O −IRQ2	 O O
C04 (ISA) (MicroChannel)	 +AEN MIO	 I I
C05	HD4	B
C06	HD7	B
C07	HDDIR	O
C08	HD10	B
C09	HD13	B
C10	−SD6	B-PU
C11	−SD3	B-PU
C12	−SD0 (LSB)	B-PU
C13	−SD10	B-PU
C14	−SD14	B-PU
D01 (ISA) (MicroChannel)	 NC −SFBK	 O
D02 (ISA) (MicroChannel)	 IRQ7O −IRQ7	 O O
D03/ (ISA) (MicroChannel)	 IRQ6O −IRQ6	 O O
D04 (ISA) (MicroChannel)	 −MEMR −S1	 I I
D05 (ISA) (MicroChannel)	 −MEMW −S0	 I I
D06	V_{CC}	
D07	GND	
D08	V_{CC}	
D09	HD14	B
D10	−SD7	B-PU
D11	−CASLO −SRAMLO	O

Pin No.	Pin Name	Type
D12	−CASHI −SRAMHI	O
D13	−SD11	B-PU
D14	−SD15 (MSB)	B-PU
E01	NC	
E02 (ISA) (MicroChannel)	 IRQ3O −IRQ3	 O O
E03 (ISA) (MicroChannel)	 −CHCK −CHCK	 O O
E04 (ISA) (MicroChannel)	 −IOR −CMD	 I I
E05	V_{CC}	
E06	GND	
E07	GND	
E08	GND	
E09	HD15 (MSB)	B
E10	−CFGLD	O
E11	−SRAMOE	O
E12	−RAS +CO/−DAT	O
E13	−DRAMWE	O
E14	−SWRITE	B
F01	NC	
F02 (ISA) (MicroChannel)	 +DPEN −DPEN1	 I I
F03 (ISA) (MicroChannel)	 −IOW −ADL	 I I
F04	GND	
F05	HA12	I
F09	NC	
F10 (ISA) (MicroChannel)	 −BIOS −BIOS	 O O

12.0 Connection Diagrams (Continued)

PIN DEFINITIONS (Continued)

Note: Some pins have different definitions depending on the host bus type used, as indicated in the table.

I = Input-only digital, **O** = Output only digital,
B = Bidirectional digital, **A** = Analog
I-PU = Input-only digital with internal pullup*, **I-PD** = Input-only digital with internal pulldown*
B-PU = Bidirectional digital with internal pullup*
*Internal polysilicon resistor with nominal value of 15k ±30%
NC = No Connect (*should not* be connected for normal operation)

Pin No.	Pin Name	Type
F11	NC	
F12	−SA14 (MSB)	B
F13	−SIP	O
F14	32MHZ	I
G01	HA13 (LSB)	I
G02	HA0 (LSB)	I
G03	V_{CC}	
G04	GND	
G10	GND	
G11	V_{CC}	
G12	−ROM	O
G13	NC	
G14	−SA12	B
H01	HA14	I
H02	HA1	I
H03	HA2	I
H04	V_{CC}	
H10	GND	
H11	−SA13	B
H12	NC	
H13	−SA11	B
H14	−SA10	B
J01	NC	
J02	HA15	I
J03	V_{CC}	
J04	GND	
J10	GND	
J11	V_{CC}	
J12	−SA9	B
J13	−SA8	B
J14	−SA7	B
K01	HA16	I
K02	HA3	I
K03	HA17	I
K04	HA4	I
K05	HA5	I

Pin No.	Pin Name	Type
K09	−SA6	B
K10	V_{CC}	
K11	−SA5	B
K12	−SA4	B
K13	−SA3	B
K14	−SA2	B
L01	HA18	I
L02	HA19 (MSB)	I
L03	HA6	I
L04 (ISA) (MicroChannel)	IRQ7I +A20	I I
L05	GND	
L06	V_{CC}	
L07	V_{CC}	
L08	GND	
L09	GND	
L10	V_{CO}	O
L11	NC	
L12	NC	
L13	−SA1	B
L14	−SA0 (LSB)	B
M01	NC	
M02	HA7	I
M03	HA8	I
M04	HA9	I
M05	V_{CC}	
M06	V_{CC}	
M07	GND	
M08	V_{CC}	
M09	−CFG2	I-PU
M10	−CFG1	I-PD
M11	NC	
M12	NC	
M13	NC	
M14	NC	
N01	NC	

Pin No.	Pin Name	Type
N02 (ISA) (MicroChannel)	IRQ6I +A21	I I
N03	HA10	I
N04	HA11	I
N05	ROUTB	A
N06	GND	
N07	RINA	A
N08	−16MBPS	O
N09	−4MBPS	O
N10	−CFG0	I-PU
N11	NC	
N12	NC	
N13	NC	
N14	NC	
P01 (ISA) (MicroChannel)	IRQ3I +A22	I I
P02 (ISA) (MicroChannel)	IRQ2I +A23	I I
P03 (ISA) (MicroChannel)	TH +MA24	I I
P04 (ISA) (MicroChannel)	TH −SETUP	I I
P05	ROUTA	A
P06	PHANTB	A
P07	PHANTA	A
P08	RINB	A
P09	PLL4	A
P10	PLL16	A
P11	−MIP	I-PU
P12	−SMI	I-PU
P13	NC	
P14	NC	

12.0 Connection Diagrams (Continued)

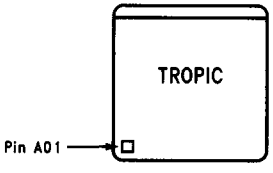
TROPIC Pin Maps

ISA Bus Mode Pin Definitions (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
	RESET	-BHE	NC	NC	NC	NC	HA13	HA14	NC	HA16	HA18	NC	NC	IRQ3I
1	O	-O	-O	-O	O	O	O	O	O	O	O	O	O	O
	1	15	29	43	57	71	85	99	113	127	141	155	169	183
	-EHPI	-REF	+RDY	IRQ7O	IRQ3O	+DPEN	HA0	HA1	HA15	HA3	HA19	HA7	IRQ6I	IRQ2I
2	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	2	16	30	44	58	72	86	100	114	128	142	156	170	184
	HDP0	HDP1	IRQ2O	IRQ6O	-CHCK	-IOW	V_{CC}	HA2	V_{CC}	HA17	HA6	HA8	HA10	TH
3	O	O	O	O	-O	O	O	O	O	O	O	O	O	O
	3	17	31	45	59	73	87	101	115	129	143	157	171	185
	HD0	HD1	+AEN	-MEMR	-IOR	GND	GND	V_{CC}	GND	HA4	IRQ7I	HA9	HA11	NC
4	O	O	O	O	-O	O	O	O	O	O	O	O	O	O
	4	18	32	46	60	74	88	102	116	130	144	158	172	186
	HD2	HD3	HD4	-MEMW	V_{CC}	HA12				HA5	GND	V_{CC}	ROUTB	ROUTA
5	O	O	O	O	O	O				O	O	O	O	O
	5	19	33	47	61	75				131	145	159	173	187
	HD5	HD6	HD7	V_{CC}	GND						V_{CC}*	V_{CC}*	GND*	PHANTB
6	O	O	O	O	O						O	O	O	O
	6	20	34	48	62						146	160	174	188
	-EHDH	-EHDL	HDDIR	GND	GND						V_{CC}*	GND*	RINA	PHANTA
7	O	O	O	O	O						O	O	O	O
	7	21	35	49	63						147	161	175	189
	HD8	HD9	HD10	V_{CC}	GND						GND	V_{CC}	-16MBPS	RINB
8	O	O	O	O	O						O	O	O	O
	8	22	36	50	64						148	162	176	190
	HD11	HD12	HD13	HD14	HD15	NC				-SA6	GND	-CFG2	-4MBPS	PLL4
9	O	O	O	O	O	O				O	O	O	O	O
	9	23	37	51	65	79				135	149	163	177	191
	-SD4	-SD5	-SD6	-SD7	-CFGLD	-BIOS	GND	GND	GND	V_{CC}	V_{CO}	-CFG1	-CFG0	PLL16
10	O	O	O	O	O	-O	O	O	O	O	O	O	O	O
	10	24	38	52	66	80	94	108	122	136	150	164	178	192
	-SD1	-SD2	-SD3	-CASLO	-SRAMOE	NC	V_{CC}	-SA13	V_{CC}	-SA5	NC	NC	NC	-MIP
11	O	O	O	-O	O	O	O	O	O	O	O	O	O	O
	11	25	39	53	67	81	95	109	123	137	151	165	179	193
	-SDP1	-SDP0	-SD0	-CASHI	-RAS	-SA14	-ROM	NC	-SA9	-SA4	NC	NC	NC	-SMI
12	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	12	26	40	54	68	82	96	110	124	138	152	166	180	194
	-SD8	-SD9	-SD10	-SD11	-DRAMWE	-AIP	NC	-SA11	-SA8	-SA3	-SA1	NC	NC	NC
13	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	13	27	41	55	69	83	97	111	125	139	153	167	181	195
	-SD12	-SD13	-SD14	-SD15	-SWRITE	32 MHz	-SA12	-SA10	-SA7	-SA2	-SA0	NC	NC	NC
14	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	14	28	42	56	70	84	98	112	126	140	154	168	182	196

* Indicates Analog Supply Source

Orientation - Top View



TL/F/11334-33

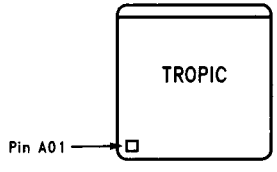
12.0 Connection Diagrams (Continued)

MicroChannel Bus Mode Pin Definitions (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
	RESET	-SBHE	-DS16	-SFBK	NC	NC	HA13	HA14	NC	HA16	HA18	NC	NC	+A22
1	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	1	15	29	43	57	71	85	99	113	127	141	155	169	183
	-EHPI	--REF	+CHRDY	-IRQ7	-IRQ3	-DPENI	HA0	HA1	HA15	HA3	HA19	HA7	I+A21	I+A23
2	O	O	O	O	O	-O	O	O	O	O	O	O	O	O
	2	16	30	44	58	72	86	100	114	128	142	156	170	184
	HDP0	HDP1	-IRQ2	-IRQ6	-CHCK	-ADL	V_{CC}	HA2	V_{CC}	HA17	HA6	HA8	HA10	+MA24
3	O	O	O	O	-O	O	O	O	O	O	O	O	O	O
	3	17	31	45	59	73	87	101	115	129	143	157	171	185
	HD0	HD1	MIO	--S1	-CMD	GND	GND	V_{CC}	GND	HA4	I+A20	HA9	HA11	-SETUP
4	O	O	O	-O	O	O	O	O	O	O	O	O	O	O
	4	18	32	46	60	74	88	102	116	130	144	158	172	186
	HD2	HD3	HD4	-S0	V_{CC}	HA12				HA5	GND	V_{CC}	ROUTB	ROUTA
5	O	O	O	-O	O	O				O	O	O	O	O
	5	19	33	47	61	75				131	145	159	173	187
	HD5	HD6	HD7	V_{CC}	GND						V_{CC}*	V_{CC}*	GND*	PHANTB
6	O	O	O	O	O						O	O	O	O
	6	20	34	48	62						146	160	174	188
	-EHDH	-EHDL	HDDIR	GND	GND						V_{CC}*	GND*	RINA	PHANTA
7	O	O	O	O	O						O	O	O	O
	7	21	35	49	63						147	161	175	189
	HD8	HD9	HD10	V_{CC}	GND						GND	V_{CC}	-16MBPS	RINB
8	O	O	O	O	O						O	O	O	O
	8	22	36	50	64						148	162	176	190
	HD11	HD12	HD13	HD14	HD15	NC				-SA6	GND	-CFG2	-4MBPS	PLL4
9	O	O	O	O	O	O				O	O	O	O	O
	9	23	37	51	65	79				135	149	163	177	191
	-SD4	-SD5	-SD6	-SD7	-CFGLD	-BIOS	GND	GND	GND	V_{CC}	V_{CO}	-CFG1	-CFG0	PLL16
10	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	10	24	38	52	66	80	94	108	122	136	150	164	178	192
	-SD1	-SD2	-SD3	-CASLO	-SRAMOE	NC	V_{CC}	-SA13	V_{CC}	-SA5	NC	NC	NC	-MIP
11	O	O	O	-O	O	O	O	O	O	O	O	O	O	O
	11	25	39	53	67	81	95	109	123	137	151	165	179	193
	-SDP1	-SDP0	-SD0	-CASHI	-RAS	-SA14	-ROM	NC	-SA9	-SA4	NC	NC	NC	-SMI
12	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	12	26	40	54	68	82	96	110	124	138	152	166	180	194
	-SD8	-SD9	-SD10	-SD11	-DRAMWE	-AIP	NC	-SA11	-SA8	-SA3	-SA1	NC	NC	NC
13	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	13	27	41	55	69	83	97	111	125	139	153	167	181	195
	-SD12	-SD13	-SD14	-SD15	-SWRITE	32 MHz	-SA12	-SA10	-SA7	-SA2	-SA0	NC	NC	NC
14	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	14	28	42	56	70	84	98	112	126	140	154	168	182	196

* Indicates Analog Supply Source

Orientation - Top View



TL/F/11334–34