T-52-33-49

TVP9520/25 DATA SHEET

Trident

TVP9520/25
VIDEO PROCESSING CHIPSET

Overview

- Supports 8, 16, 24, and 32 **bits/pixel**
- Supports display resolutions for **NTSC/PAL**(Overscan/ Underscan), **VGA & Enhanced VGA**
- Hardware supports **scalable full motion** video; **window clipping functions**
- Multiple **frame capture** and **hidden Capture**
- Live **multi-picture**
- VGA/XGA graphics/text **overlay**
- Advanced **chroma keying**
- Digital **special effects** processing (crossfading, linear blending, solarization, etc.)
- Advanced **genlock** circuit allows overlay from multiple video sources
- Software controlled **contrast, brightness, saturation** and **hue**
- Supports **interlaced input** and **interlaced or non-interlaced output; programmable sync polarity**
- Supports up to 4MB of 256Kx4 or 256Kx8 enhanced page mode VRAM. **Minimum memory configuration is four 256Kx4 or two 256Kx8 VRAMs**
- Displayable memory maps of 512x512, 512x1024, 1024x512, and 1024x1024
- **TARGA+®** register compatible
- Compatible with **ISA, EISA,** and **MCA** bus
- T1 160 Pin **PQFP**; T2 184 Pin **PQFP** Package

General Description

Trident's TVP9520/25 Video Processing Chipset offers scalable full motion video windowing, multiple frame capture, VGA/XGA graphics and text overlay, digital special effects processing, advanced chroma keying and up to 16.7 million displayable colors. TVP9520/25 is the new standard for high quality, cost effective, live video production on the PC desktop.

TVP9520/25 offers advanced proprietary functions and performance beyond its 8, 16, 24, or 32 bits of TARGA+® compatibility. Unique features include enhanced zoom, panning and mosaic, XGA overlay, linear scalable window operations (full screen to single pixel), plus the ability to perform real-time overlay and special effects.

TVP9520/25 can combine VGA/XGA text and graphics with input from one of two software selectable sources, such as video camera, laser disk, VCR, TV tuner, RGB Camera, or one of two frame buffer images. It can then be output to a VGA monitor, TV monitor, projection TV or recorded to videotape. Figure 1 is a high level TVP9520/25 functional flow diagram.

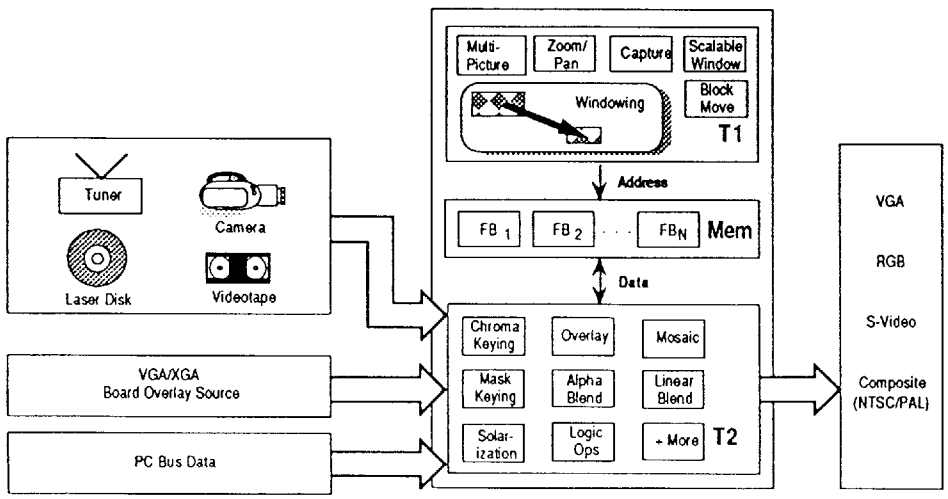

Figure 1. TVP9520/25 Functional Flow Diagram

Functional Block Description

TVP9520/25 chipset consists of two VLSI ASICs: T1 and T2. Figure 2 shows their application in a typical board design.

The TVP9520/25 chipset can be used with ISA or EISA bus PCs (PC/AT) or with Micro Channel Adapter (MCA) bus PCs (PS/2). The chipset is configured at the board level for a bus type using a simple pullup/pulldown technique described in the next section.

All internal functions and functional blocks in the TVP9520/25 chipset are controlled through a set of internal registers which are accessed through the PC's I/O space. The TVP9520/25 register set is a superset of the Truevision TARGA+® register set.

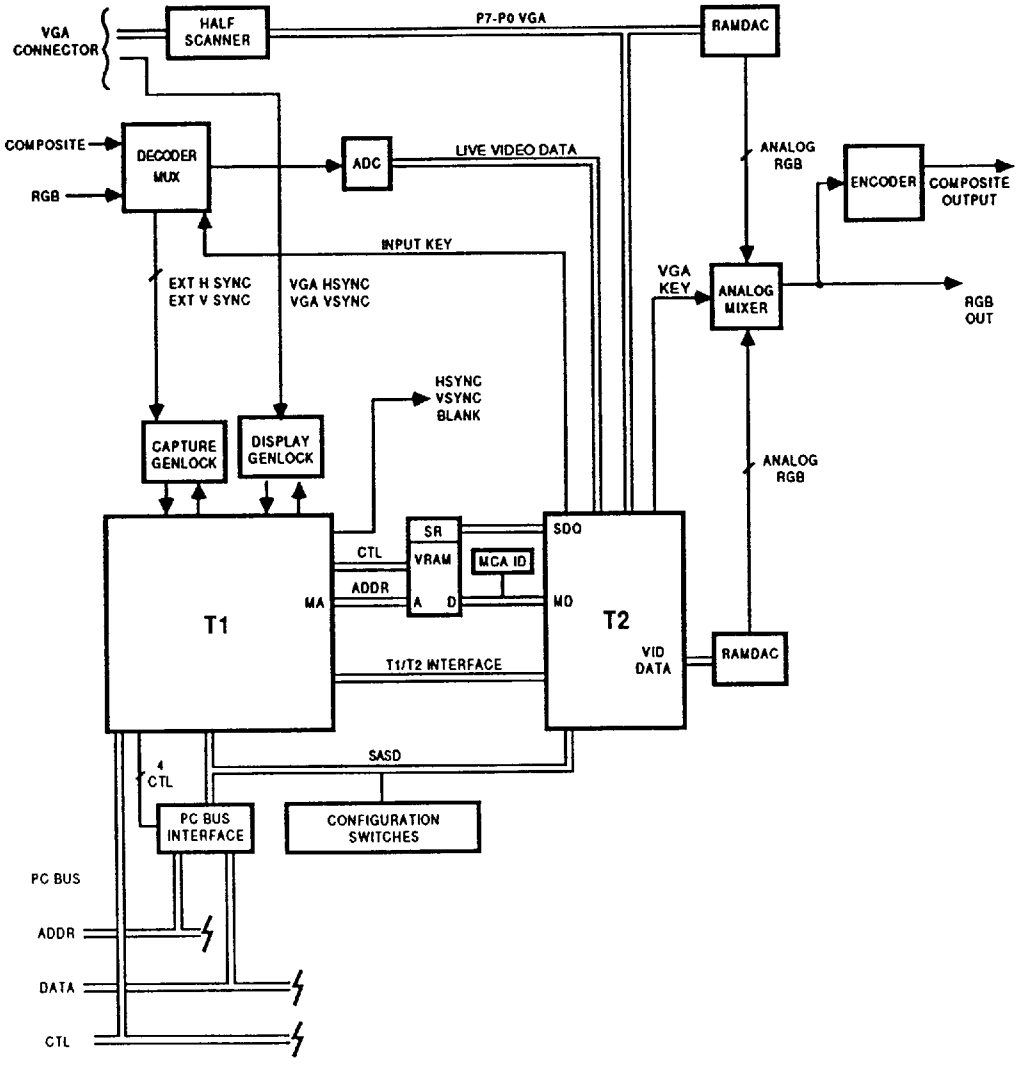

Figure 2. TVP9520/25 Chipset Application Diagram

T1

T1's main functional blocks, shown in Figure 3, are the PC System Interface, the CRT Controller (CRTC), the Arbitration and VRAM Controller, and T1/T2 Control/Interface block.

PC System Interface

The PC System Interface functional block in T1 has three elements: (1) Command/Address Decoder, (2) the PC Bus Interface Controller, and (3) the T1 ADMUX Interface.

Command/Address Decoder

The Command/Address Decoder analyzes PC bus address and control signals and generates TVP9520/25 internal control signals. The decoder has five multifunction pins which can be connected to either AT bus signals or MCA bus signals. The function of the pins is determined by the bus type for which T1 has been configured. (See later section, Configuring the TVP9520/25 Chipset).

PC Bus Interface Controller

The TVP9520/25 chipset is designed to communicate with the PC bus through external components in a PC Bus Interface that multiplexes 16 address bits and 16 data bits between the PC system bus and TVP9520/25's inter-chip 16 bit SASD bus. Typically, only four chips are needed for the PC Bus Interface: two address buffers and two bidirectional data buffers. As shown in Figure 5, the PC Bus Interface Controller provides four signals needed to control these external interface components.

On both T1 and T2 is an interface(ADMUX interface) that handles and synchronizes flow of multiplexed data between the chip's internal address/data bus and the external interchip SASD bus. In addition, T1's ADMUX interface supports auto-configuration by reading the logic status of SASD bus lines immediately after reset and providing the values to the SYSCONFIG register where they are latched. (Reference Configuring the TVP9520/25 Chipset section).

CRT Controller (CRTC)

The CRT Controller block provides display and video input handling functions including genlocking. It generates all necessary timing and control signals, including equalization and serration, and provides horizontal sync, vertical sync, blanking, and composite sync outputs. It also handles synchronization with outside video sources so that TVP9520/25 images may be merged with display information from a seperate VGA or XGA board.

In TARGA+® mode, the CRTC1 provides TARGA+® control functions. In this mode, CRTC1 is used for all video input and display timing functions.

In Trident mode, the CRTC block provides separate controllers for capture and display, and allows use of two separate timebases. Each controller has its own genlock circuitry which interfaces with a minimal number of external components to form a complete genlock subsystem. CRTC2's genlock handles inputs separately and independently from CRTC1's genlock, which provides pixel clocks for use with a VGA or XGA board or outside video sources.

TVP9520/25's two independent CRTCs allow operation in a variety of genlock and scanning modes. For compatibility, TVP9520/25 provides TARGA® and TARGA+® genlock and scan modes, which use a single timebase. However, TVP9520/25 Trident modes offer enhanced operation with dual timebases for more complex applications. For example, interlaced input may be handled while non-interlaced video is output.

Arbitration and VRAM Controller

The Arbitration unit handles prioritization and arbitration of memory requests. It controls operations such as refresh, CPU requests, access to memory for video capture, block move, and window operations.

The VRAM Controller unit provides the basic control signals needed by VRAM, such as $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The Controller also generates VRAM addressing for memory access, display under various display modes, and windowing. It controls memory data transfers between VRAM and T2. It supports up to 4MB of memory without an external decoder.

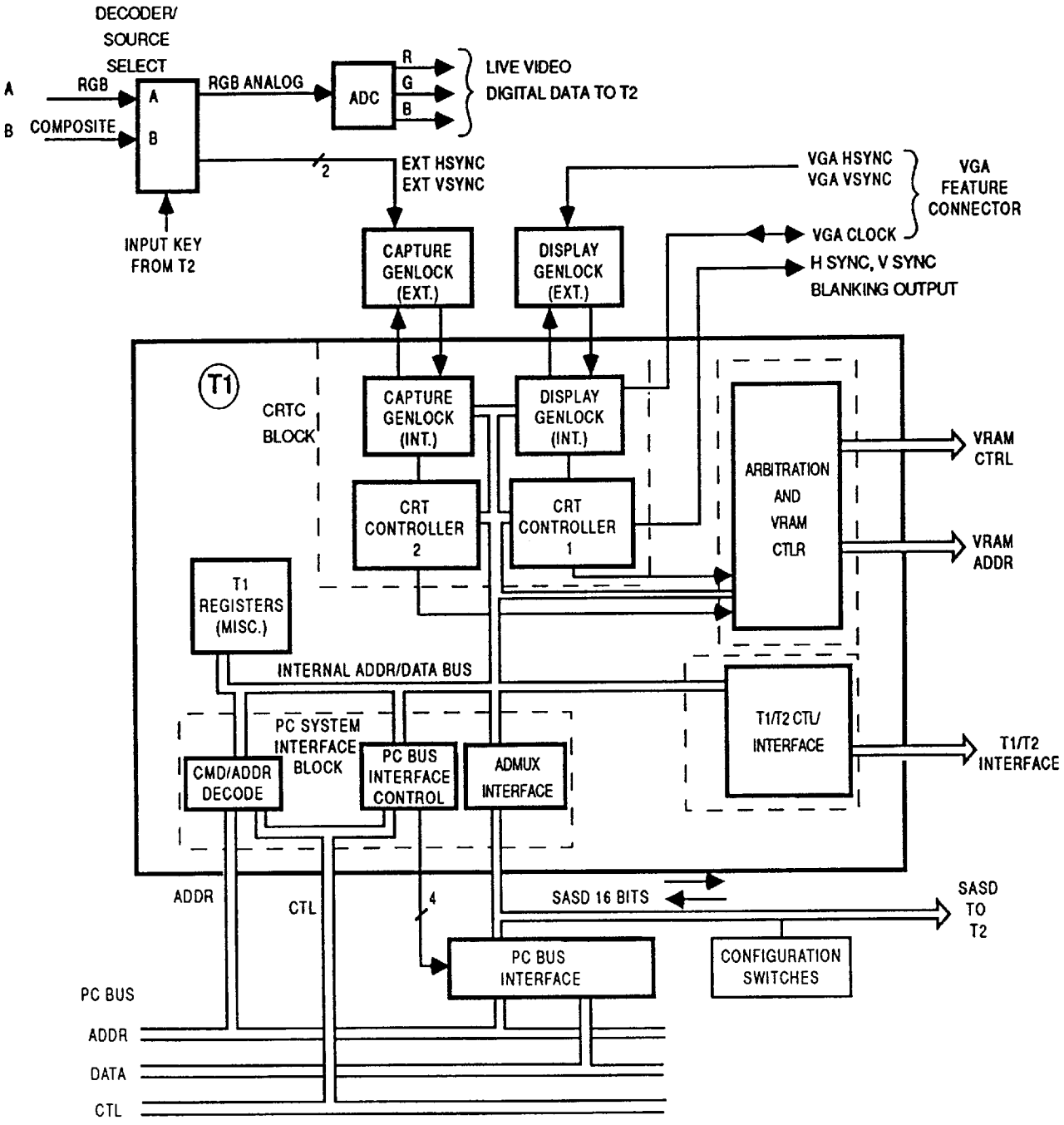

Figure 3. T1 Functional Block Diagram

T1/T2 Control/Interface

This functional block manages the T1/T2 control/ interface bus.

T2

The main functional blocks of T2, shown in Figures 4a & 4b, are the Input Processing block, the VRAM Interface block, the Mixer, the Overlay Controller, and the VGA Interface.

Input Processing

This block contains a live data input mask, a foreground processor used in blue channel processing, a chroma keyer, the capture data channel multiplexer, and a processor for creation of monochrome data from color data.

VRAM Interface

The VRAM Interface block contains interfaces for the interchip buses, a FIFO for data from the capture mux, a capture data mask, and a VRAM interface that routes data to/from the random-access part of the VRAM, and which also contains a mask (NEWMASK) usable with the VRAM data path.

Mixer Block

The Mixer provides a variety of pixel data manipulation functions. Its elements support 8, 16, 24, and 32 bit pixel operations including linear blending, alpha blending, logic operations, scalable full motion video, and many more features. All TARGA+® functions are supported.

For additional information on digital special effects, see Detailed Chipset Feature Information on later pages.

Overlay Controller

The Overlay Controller provides control for an external analog output signal mixer. It supports a wide range of advanced forms of keying, including: keying between two sources, chroma keying, luminance keying, keying on a bitplane, and VGA overlay. Chromakeying may be based on a single color, blue channel data, or a color range. TVP9520/25's advanced chroma processing allows shadows against a blue background to be preserved. The Overlay Controller supports using VGA overlay functions with other forms of keying; this allows many combinations of live video, frame buffer data, and VGA/XGA graphics (from a separate VGA/XGA board).

VGA Interface

The VGA Interface in T2 handles data input from a separate VGA or XGA board. It provides VGA keying control to the Overlay Controller.

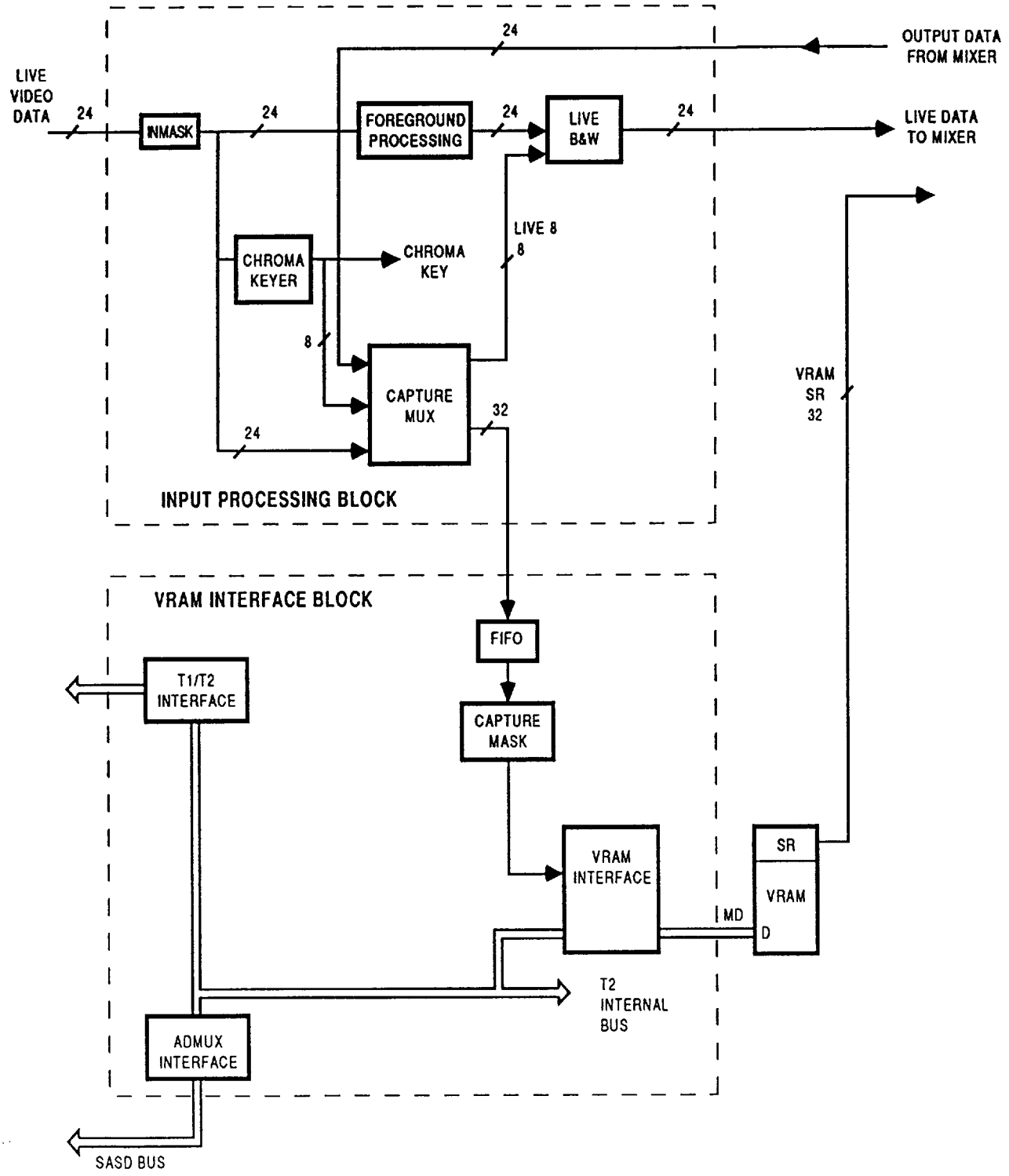

Figure 4a. T2 Functional Block Diagram

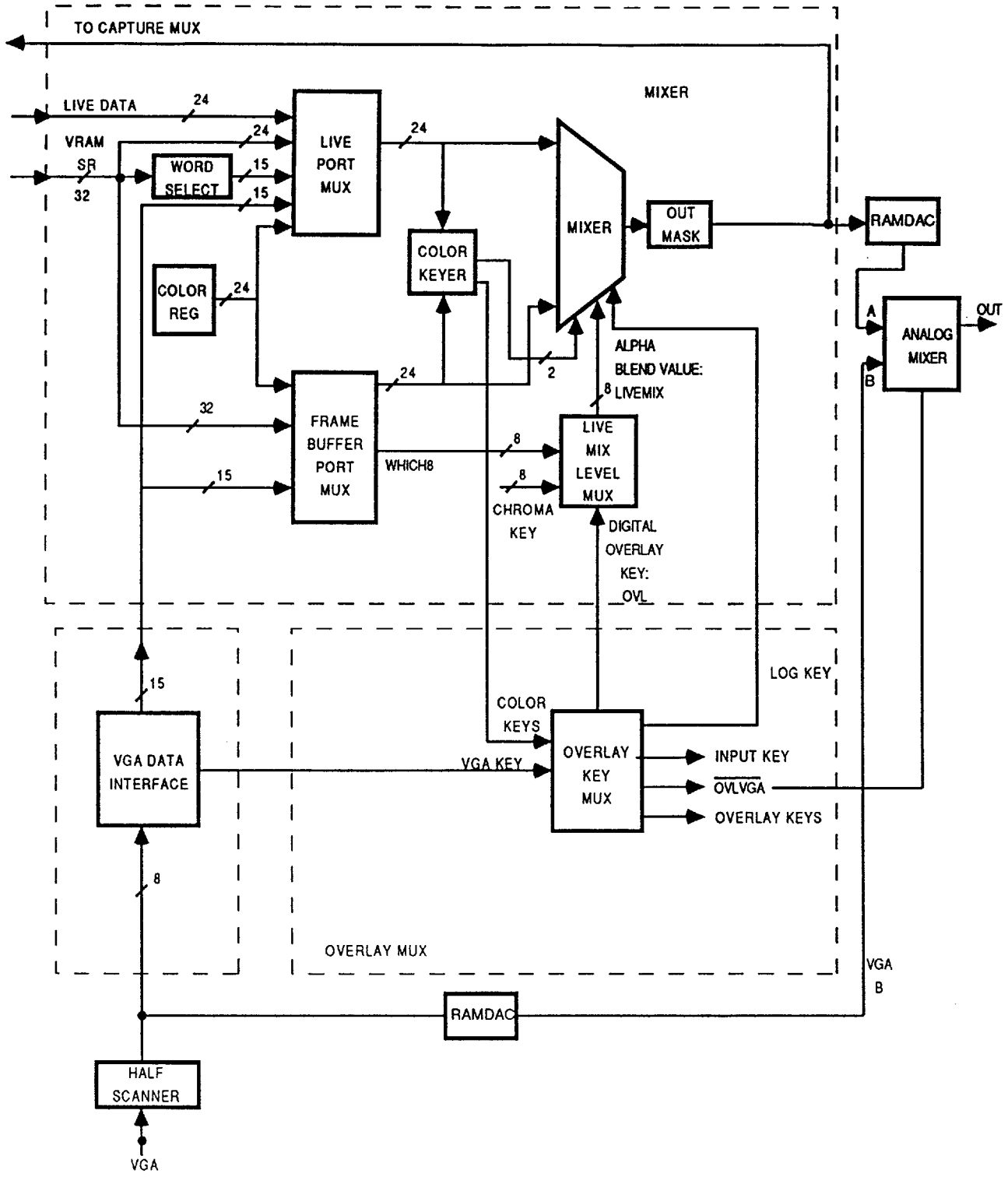

Figure 4b. T2 Functional Block Diagram

Configuring the TVP9520/25

Board-level configuration of the TVP9520/25 chipset is performed using a simple technique, illustrated in Figure 5. There are 10 board-level configuration parameters, each mapped to a bit on the SASD bus. A parameter is configured by connecting the bit to which it is mapped either high or low through a 4.7K to 10K pullup or pulldown resistor. This does not affect normal bus activity, but furnishes a logic state that can be read at initialization time. After reset, the SYSCONFIG register reads and latches the state of each SASD bus bit. The bit values are then used by T1 and T2 to determine required configuration. The SYSCONFIG register can also be read by software, providing a means for applications to determine board configuration.

Table 1. Board-Level Configuration Parameters

NAME	SASD BIT #	DESCRIPTION
cio	15	contiguous or non-contiguous I/O address. 0 = non-contiguous; 1 = contiguous
baseIO	14:12	these three bits set base I/O address
busSize	11	0 = 8-bit slot; 1 = 16-bit slot
AT/MCA	10	0 = MCA bus; 1 = AT bus
testconf	9	Set this bit = 1 for normal use
switch	8	General purpose input
biosEnb	7	0 = enable BIOS; 1 = disable BIOS (default)
biosSize	6:5	Value of bits 6 and 5 selects BIOS size of 4K, 8K, 16K, or 32K
biosBase	4	Sets BIOS base address of 0C000H or 0D000H
biosStart	3:0	Bits 3-0 set BIOS starting address

The board-level parameters and SASD bit values are readable as corresponding bits in the SYSCONFIG register (index 59H). For more information, see TVP9520/25 Technical Reference Manual.

Configuring for AT Bus

1. Set the AT/MCA bit = 1 with a pullup on SASD bus bit 10. This causes the following pins of T1 to assume the functions listed in Table 2:

Table 2. AT Bus Configuration

T1 PIN #	AT BUS FUNCTION
5	$\overline{\text{MEMR}}$
3	$\overline{\text{MEMW}}$
18	$\overline{\text{IOR}}$
19	$\overline{\text{IOW}}$
23	AEN

Configuring for MCA Bus

1. Set the AT/MCA bit = 0 with a pulldown on SASD bit 10 . This causes the following pins of T1 to assume the functions listed in Table 3:

Table 3. MCA Bus Configuration

T1 PIN #	MCA BUS FUNCTION
5	M/$\overline{\text{IO}}$
3	$\overline{\text{S0}}$
18	$\overline{\text{S1}}$
19	$\overline{\text{CMD}}$
23	$\overline{\text{CDSETUP}}$

2. For Micro Channel applications, TVP9520/25 supports MCA auto-configuration card IDs, which are four-byte values. When a card is enabled for an ID read by $\overline{\text{CDSETUP}}$, the PC may read the contents of I/O byte registers at 101H and 100H.

The high order four bits of register 101H are hardwired with a value of 8 (the first nibble of a video device ID). The low order nibble of register 101H and the byte in register 100H may be configured by using pullups/

pulldowns as described before, but in this case by placing them on the data bus lines <MD11:MD0> which connect T2 and VRAM.

For example:

to set card ID: 80CFH or 1000 0000 1100 1111
---MSB-- ---LSB--

set register 101= 80H = 1000 0000
set register 100 = CFH = 1100 1111

This is done by wiring pullups/pulldowns on the MD bus lines as follows:

<MD15:MD12>= pullups are already internally hardwired inside T2 to value of 8; no external configuration is needed.
<MD11:MD8> =0 0 0 0 pulldown all bits
<MD7:MD4> =1 1 0 0 pullup <MD7:MD4>
pulldown <MD5:MD4>
<MD3:MD0> =1 1 1 1 pullup all bits
<MD3:MD0>

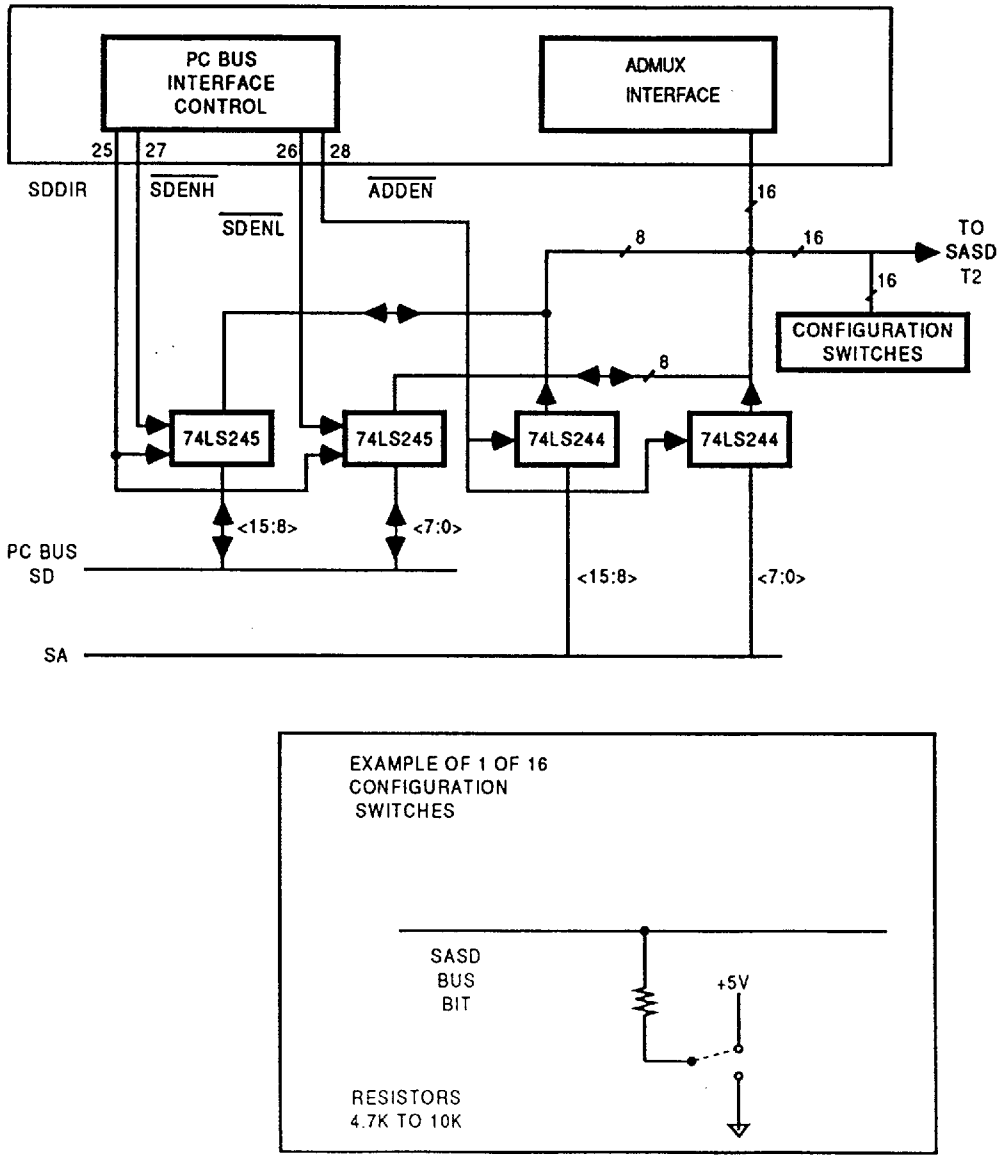

Figure 5. Board Level Configuration Of TVP9520/25 Chipset

Pixel Depth

Table 4 lists the pixel depths and associated colors available for the TVP9520/25.

Table 4. Pixel Depth Information

Depth	Color
8 bits/pixel	256
16 bits/pixel	32,768 (five bits each R, G, B; one overlay bit)
24 bits/pixel	16,777,216 (eight bits each R, G, B)
32 bits/pixel	16,777,216 (eight bits each R, G, B plus eight bits alpha channel)

Display Resolution

Table 5 lists typical display resolutions available. All may be converted to non-interlaced display.

Table 5. Display Resolution

Output Format	Resolution x Bits/Pixel	Minimum Memory
NTSC Underscan	512x400x16	512K
	512x400x32	1MB
	640x480x16	1MB
	640x480x32	2MB
NTSC Overscan	512x486x16	512K
	512x486x32	1MB
	648x486x16	1MB
	720x486x16	1MB
	756x486x16	1MB
PAL Underscan	512x476x16	512K
	512x476x32	1MB
	720x576x16	2MB
PAL Overscan	512x576x32	2MB
	768x576x16	2MB
VGA Compatible	512x400x16	512K
	512x496x16	512K
	640x400x16	1MB
	640x496x16	1MB
Enhanced VGA Compatible	800x600x16	2MB
	1024x768x16	2MB

TVP9520/25 Applications

The TVP9520/25 can be used in the following applications:

- Animation
- Titling
- Inspection
- Security
- Advertising
- Image Database
- Desktop Publishing
- Home Video Production
- Business Presentation
- Medical Imaging
- Video Training
- Military Applications
- Computer-Aided Instruction and Training

Design Kits

A design kit is available for RGB in-out board with S-Video PAL, NTSC daughter boards. Boards based on the Philips digital TV chipset are also available.

Detailed Chipset Feature

Video Windowing

- Provides source and destination capture windows. The destination window may be scaled linearly to pixel boundaries. Window locations can be defined arbitrarily.
- Provides two programmable CPU hardware windows (x,y independent). The windows may be programmed as read or write. Real time Multiple 90-degree rotation and mirror rotation effects available. Windows are bit maskable.
- Supports mixer effects within a window

Frame Capture

- Capture multiple frames
- Location and size programmable
- Live input video capture is independent of what is displayed on screen
- Overlay results may be captured
- Hidden capture live images may be captured in a frame buffer while another captured image is displayed on-screen
- In real mode, pixels in the frame buffer can be accessed through either of two page windows (4K, 8K, 16K, or 32K). In protected mode, memory can be mapped outside the first 1MB system memory for direct access.

VGA Overlay

- Overlay live video, with two frame buffers and VGA/XGA (can all be simultaneously displayed on a single screen)
- Digital wipe effects between live display and frame buffers
- Overlay video input in background or foreground
- Built-in 1, 2 or 8 bit overlay or alpha channel

Chroma Keying

- Multiple simultaneous chroma key sources for video and VGA/XGA
- Chroma key based on a color range
- Chroma key based on a fixed color
- Chroma key based on blue component of live input
- Preserves shadows during chroma keying

Digital Special Effects

- Selectable **border color or background color** via R, G, B color registers
- **Linear minifying** (or shrinking) of live video and captured frames. Size and location programmable. Mirror effect and real time trailing effects available.
- Realtime **inverse video** (complement of selected pixels).
- Offers **color filter** to generate real time effects between live/frame buffer, two frame buffers, live and fixed pattern.
- **Zoom.** Pixels on the selected screen area enlarged by the given X and Y zoom factors(1X to 64X). X and Y axis processing is independent.
- **Mosaic.** Mosaic quantizes an image into blocks of size on an axis of (resolution divided by mosaic factor on that axis of 1X to 64X). X and Y axis processing is independent. Also known as **tile effect.**
- **Panning.** Move displayed image area along X and (or) Y axis on pixel boundaries. X and Y axis independent.
- Real-time **logic operations** (AND, OR, NOR, etc.) between live video and frame buffer
- **Transparency effect.** Places a user defined transparency mask shape of a given color or color range over an image
- **Solarization.** Reduces the color shades in a given image. Three hardware masks are provided : CPU, Capture and Display. Color reduction performed through a color mask.
- **Multiple screens.** Supports hidden capture, screen swap, fading effects, etc.
- **Live multi-picture.** Multiple versions of a live image or portion of the live image frame buffer are displayed on screen
- **Pseudo color.** Convert given color index to a different RGB color via RAMDAC Color Look Up Table (CLUT)
- **Linear blending.** 256 levels. Two sources. Levels may be chosen in software or with alpha channel. For software method, the same value is used for entire image. For alpha channel method, blending level is defined on a pixel by pixel basis.
- **Smooth crossfading.** 256 levels. Fade in and out between two sources. Same method for choosing levels as linear blending.
- High speed **block move** between programmable CPU hardware windows
- VGA/XGA pass through and **overlay**

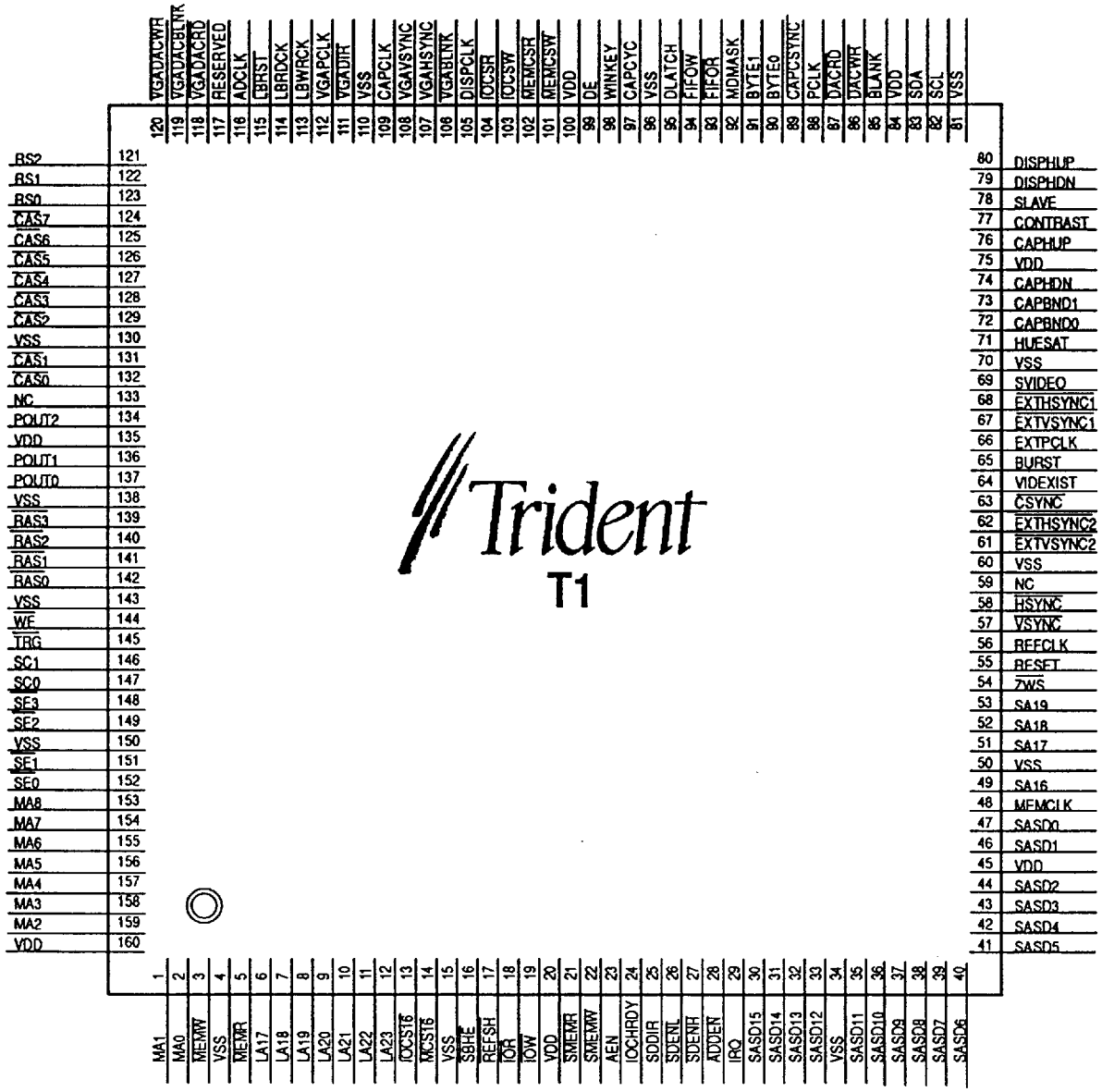

Figure 6. T1 Pinout Diagram

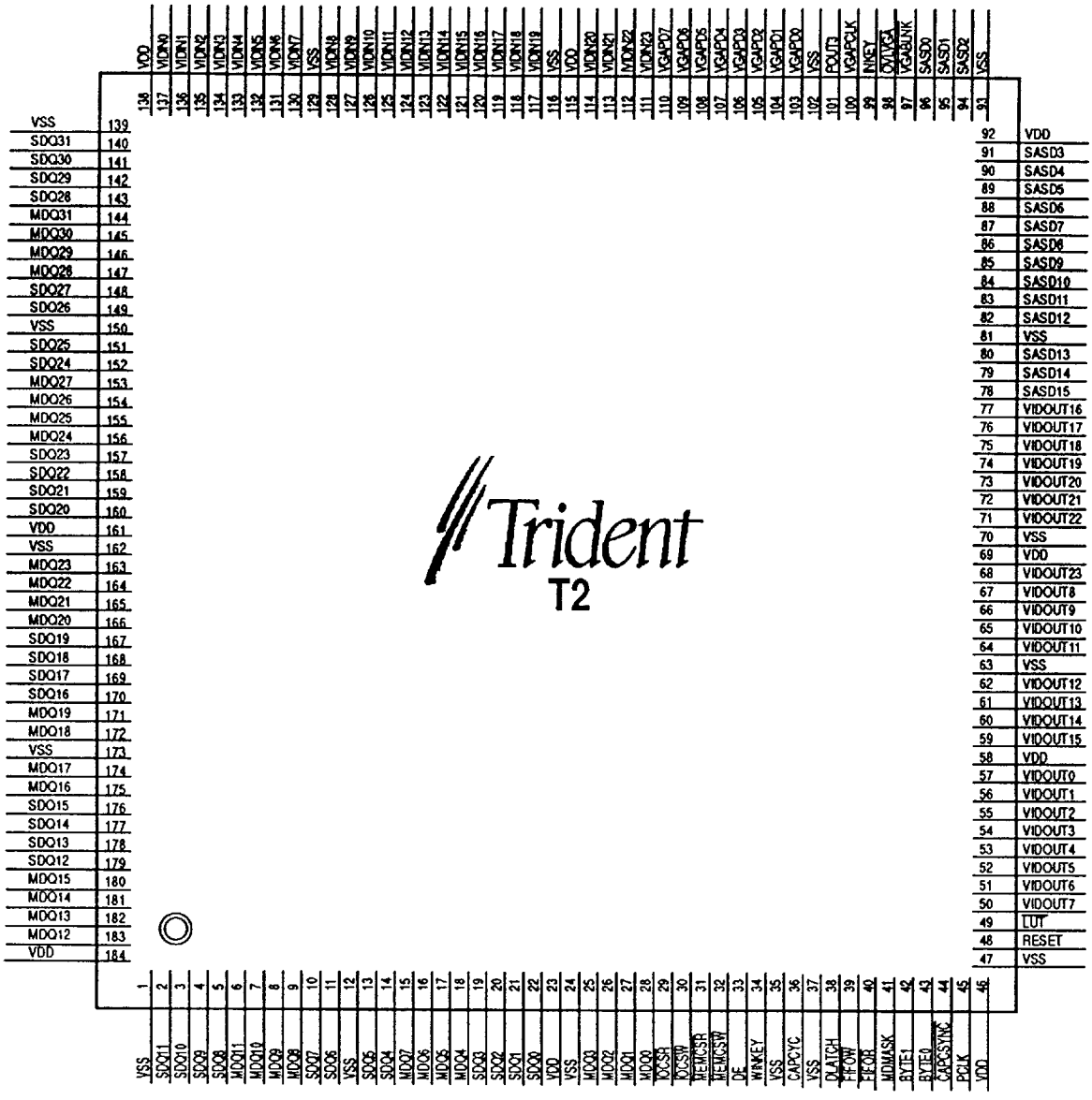

Figure 7. T2 Pinout Diagram

Table 6. T1 Pin Description

Pin	Pin Type	Pin Number	Description
Host Interface			
a. AT Bus Signals			
$\overline{\text{MEMR}}$	I	5	Memory read strobe for AT bus. Signal used during a memory read cycle to request the video processing board drive data onto the bus.
$\overline{\text{MEMW}}$	I	3	Memory write strobe for AT bus. Signal used during a memory write cycle to request the video processing board accept the data on the system data lines.
$\overline{\text{IOR}}$	I	18	I/O read strobe for AT bus. Signal used during an I/O read cycle to request the video processing board drive data onto the bus.
$\overline{\text{IOW}}$	I	19	I/O write strobe for AT bus. Signal used during an I/O write cycle to request the video processing board accept the data on the system data lines.
AEN	I	23	Address enable
IOCHRDY	O	24	Open drain output. Connected to IOCHRDY signal on AT Bus. Logical 0 informs CPU that a memory operation is in progress and that additional CPU wait states are required.
$\overline{\text{SMEMR}}$	I	21	System memory read strobe for AT bus. Signal has same functionality as $\overline{\text{MEMR}}$, except it is active only within the first 1MB of system address space.
$\overline{\text{SMEMW}}$	I	22	System memory write strobe for AT bus. Signal has same functionality as $\overline{\text{MEMW}}$, except it is active only within the first 1MB of system address space.
b. *MCA Bus Signals*			
M/$\overline{\text{IO}}$	I/O	5	M/$\overline{\text{IO}}$ indicates memory cycle or I/O cycle. A logical 1 indicates a memory cycle is in progress. A logical 0 indicates an I/O cycle is in progress.
$\overline{\text{S1}}$, $\overline{\text{S0}}$	I	18, 3	The logical values of $\overline{\text{S0}}$ and $\overline{\text{S1}}$, along with the logical value of M/$\overline{\text{IO}}$, indicate the start of a Microchannel bus cycle. Reference table below.
$\overline{\text{CMD}}$	I	19	Connected to $\overline{\text{CMD}}$ signal on Micro Channel bus. Signal used to indicate when data bus information valid. For write operations, data is valid throughout the active $\overline{\text{CMD}}$ period. For read operations, data

M/$\overline{\text{IO}}$	$\overline{\text{S0}}$	$\overline{\text{S1}}$	Definition
0	0	0	Reserved
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved

Table 6. T1 Pin Description- Continued

Pin	Pin Type	Pin Number	Description
			is valid after the leading edge of $\overline{CMD}$ but before the trailing edge of $\overline{CMD}$. Tri-state output.
$\overline{CD\ SETUP}$	I	23	This signal is driven active during the system configuration period. When activated, the signal is used to obtain the ID and configuration data of an adapter located in the specified Micro Channel slot.
CD CHRDY	O	24	Channel Ready signal. A logical 0 informs CPU that a memory or I/O operation is in progress and that additional CPU wait states are required.
c. Common Bus Signals For AT & MCA			
RESET	I	55	System reset (active high). At the falling edge of Reset configuration information is latched to the internal TVP9520/25 registers (SYSCONFIG (Index=59h) and Micro Channel ID register). The information is carried on SASD15-SASD0 & MD11-MD0 during the reset period.
IRQ	O	29	Interrupt Request. IRQ indicates an interrupt service request to the CPU.
ZWS	O	54	Zero Wait-State. Pin should be connected to the system zero-wait state enable signal.
$\overline{MCS16}$	O	14	Memory Chip Select 16. Open drain output. Indicates the current memory cycle is a 16-bit operation.
$\overline{IOCS16}$	O	13	I/O Chip Select 16. Indicates the current I/O cycle is a 16-bit operation.
$\overline{SBHE}$	I	16	Bus High Byte Enable. Decoded together with SA0 to enable 16-bit data transfer. Input from PC AT Bus. $\overline{SBHE}$ SA0 Transfer 0 0 Word transfer 0 1 High byte transfer 1 0 Low byte transfer 1 1 Reserved
$\overline{REFSH}$	I	17	Memory Refresh. Signal is driven by the system refresh controller and indicates a system memory refresh cycle is in process.
$\overline{ADDEN}$	O	28	Address Enable. Enables the two address buffers, which are part of the system bus interface.
SDDIR	O	25	System Data Direction. Controls the direction of data through the two data transceivers. The transceivers are part of the system bus interface.
$\overline{SDENH}$	O	27	System Data High Byte Enable. Enables the high byte of data transceiver of the system bus interface.
$\overline{SDENL}$	O	26	System Data Low Byte Enable. Enables the low byte of data transceiver of the system bus interface.
SASD15-SASD0	I/O	30-33, 35-44, 46-47	Multiplexed system address and data bus bits 15 - 0.

Table 6. T1 Pin Description - Continue

Pin	Pin Type	Pin Number	Description
SA19-SA16	I	53-51,49	System address bits 19-16.
LA23-LA17	I	12-6	Unlatched address bits 23 - 17.
Video Memory Interface			
$\overline{RAS3}$-$\overline{RAS0}$	O	139-142	Memory row address strobes.
$\overline{CAS7}$-$\overline{CAS0}$	O	124-129,131-132	Memory column address strobes.
$\overline{SE3}$-$\overline{SE0}$	O	148-149,151-152	Serial Port Enable. Activates VRAM serial port.
$\overline{TRG}$	O	145	Shift register transfer
SC1-SC0	O	146-147	Serial Clock 1 and Serial Clock 0
$\overline{WE}$	O	144	Memory Write Enable. Write data available at falling edge of $\overline{WE}$.
MA8-MA0	O	153-159,1-2	Multiplexed VRAM address bits 8 - 0.
MEMCLK	I	48	VRAM Memory clock.
CRT Control			
CSYNC	O	63	Composite sync. Provides sync to video encoder.
$\overline{EXTHSYNC1}$	I	68	External horizontal sync from a live source (e.g. camera).
$\overline{EXTVSYNC1}$	I	67	External vertical sync from a live source.
$\overline{EXTHSYNC2}$	I	62	External horizontal sync from a second live source
$\overline{EXTVSYNC2}$	I	61	External vertical sync from a second live source
$\overline{HSYNC}$	O	58	Horizontal sync output.
$\overline{VSYNC}$	O	57	Vertical sync output.
$\overline{BLANK}$	O	85	Video blanking signal to the RAMDAC. The signal is latched on the rising edge of PCLK. A logical 0 drives the analog RGB outputs to the blanking level. When BLANK is at a logical 0, the digital pixel input information and the overlay inputs are ignored.
BURST	O	65	Color burst gate. Used for composite video encoding.
DISPCLK	I	105	Main clock for the Display CRTC. Used as base clock to generate all Display CRTC timing.
CAPCLK	I	109	Main clock for the Capture CRTC. Used as base clock to generate all Capture CRTC timing.
ADCLK	O	116	A/D sampling clock . Connects to A/D convertor.
SLAVE	O	78	Genlock Master/Slave mode select. A logical 0 selects Master mode. In Master mode, T1 generates its own video timing. A logical 1 selects Slave mode. In slave mode, T1 uses video timing from the input source.
VIDEXIST	I	64	Indicate existence of input video source. A logical 1 indicates video from a live source exists.
REFCLK	I	56	Reference clock input. Connected to a 13.5MHz oscillator. Serves as base clock for entire chip operation
CONTRAST	O	77	Write enable clock for external register VIDCON (Index=E4h).
HUESAT	O	71	Write enable clock for external register HUESAT (Index=E6h).
SVIDEO	O	69	Super video select. Connected to external decoder. A logical 1 selects S-Video input. A logical 0 selects composite video input

Table 6. T1 Pin Description - Continued

Pin	Pin Type	Pin Number	Description.
PCLK	O	88	Pixel clock output.
EXTPCLK	O	66	Pixel clock from external live source
T2 Interface			
$\overline{\text{IOCSR}}$	O	104	I/O read signal for T2. A logical 0 selects a read of the T2 I/O registers.
$\overline{\text{IOCSW}}$	O	103	I/O write signal for T2. A logical 0 selects a write to the T2 I/O registers.
$\overline{\text{MEMCSR}}$	O	102	Memory read signal for T2. A logical 0 selects a memory data read from the VRAM to T2.
$\overline{\text{MEMCSW}}$	O	101	Memory write to T2. A logical 0 selects a memory data write from the SASD to T2.
DE	O	99	Composite data enable. Signal is a combination of HDE and VDE.
WINKEY	O	98	Hardware window key. Signal used to indicate window location. A logical 1 indicates the window area.
CAPCYC	O	97	Indicates T1 has commenced a capture operation.
DLATCH	O	95	VRAM data latch clock.
FIFOW	O	94	FIFO write clock. FIFO located in VRAM interface block of T2.
$\overline{\text{FIFOR}}$	O	93	FIFO read clock. FIFO located in VRAM interface block of T2.
$\overline{\text{CAPCSYNC}}$	O	89	Composite sync for capture.
MDMASK	O	92	Indicates when to send mask data to the VRAM.
BYTE1, BYTE0	O	91, 90	Byte indicator for CPU access. Reference table below.

8-bit Mode:

BYTE1	BYTE0	Byte
0	0	0
0	1	1
1	0	2
1	1	3

16-bit Mode:

BYTE1	BYTE0	16-bit
0	X	Least Significant 16-bit
1	X	Most Significant 16-bit

32/24-bit Mode:

BYTE1	BYTE0	32/24-bit
X	X	X

Table 6. T1 Pin Description - Continued

Pin	Pin Type	Pin Number	Description
VGA Interface			
VGABLNK	I	106	VGA Blank Signal. Signal is input from the VGA feature connector interface to the external display genlock circuitry. A Logical 0 indicates video blanking period.
VGAPCLK	I/O	112	VGA Pixel Clock. Signal is input from/output to the VGA feature connector interface to/from the external display genlock circuitry. Pixel clock direction is determined by signal VGADIR.
VGADIR	O	111	VGA Pixel Clock Direction. Determines direction of signal VGAPCLK. A logical 0 means the VGA card uses the pixel clock provided by the TVP9520/25 chipset. A logical 1 means the TVP9520/25 chipset uses the VGA pixel clock.
VGAHSYNC	I	107	VGA Horizontal Sync. Signal is input from the VGA feature connector interface to the external display genlock circuitry.
VGAVSYNC	I	108	VGA Vertical Sync. Signal is input from the VGA feature connector interface to the external display genlock circuitry.
Video DAC Chipset Interface			
RS2 - RS0	O	121-123	Video DAC register address bits 2-0. These bits indicate the type of read or write operation being performed from the RAMDAC.
DACRD	O	87	Video DAC read strobe. Connected to video data output bits VIDOUT23 to VIDOUT0. Accesed in indirect I/O operating mode, using indices DBh -D8h registers.
DACWR	O	86	Video DAC write strobe. Connected to video data output bits VIDOUT23 to VIDOUT0. Accesed in indirect I/O operating mode, using indices DBh -D8h registers.
VGADACRD	O	118	VGADAC read strobe. Accessed in indirect I/O operating mode, using indicies 97h-94h for both read & write.
VGADACWR	O	120	VGADAC write strobe. Accessed in indirect I/O operating mode, using indicies 97h-94h for both read & write. The direct I/O operating mode uses addresses from 0x3c9-0x3c6 for write only, which activates VGADACWR and video DACWR.
VGADACBLNK	O	119	Blank Signal to VGA DAC.
Other External Interface			
SCL	O	82	I^2C serial bus clock.
SDA	I/O	83	I^2C serial bus data bit.
LBRST	O	115	Line Buffer Reset. Connected to reset pin of Half Scanner.

Table 6 T1 Pin Description - Continued

Pin	Pin Type	Pin Number	Description
LBWRCK	O	113	Half Scanner write clock.
LBRDCK	O	114	Half Scanner read clock.
Programmable Pins			
POUT0	O	137	Programmable Output 0. Bit can be programmed via bit 0 of Trident Enhanced Register POUT (Index=54). Pin may be used as $\overline{\text{CD SFDBK}}$ for Microchannel applications. In this case, pin should be connected to $\overline{\text{CD SFDBK}}$ pin on the Microchannel bus.
POUT1	O	136	Programmable Output 0. Bit can be programmed via bit1 of Trident Enhanced Register POUT (Index=54).
POUT2	O	134	Pin may be used as $\overline{\text{BIOSEN}}$, to enable an on-boardBIOS. Programmable OUTPUT 2. Bit can be programmed via bit 2 of Trident Enhanced Register POUT (Index=54h)
PLL Support Logic			
CAPHUP	O	76	Phase detector output of capture PLL. Used to increase the capture PLL's frequency. A logical 1 causes the frequency to increase.
CAPHDN	O	74	Phase detector output of capture PLL. Used to decrease the capture PLL's frequency. A logical 0 causes the frequency to decrease.
DISPHUP	O	80	Phase detector output of display PLL. Used to increase the display PLL's frequency. A logical 1 causes the frequency to increase.
DISPHDN	O	79	Phase detector output of display PLL. Used to decrease the display PLL's frequency. A logical 0 causes the frequency to decrease.
CAPBND1, 0	O	73, 72	Capture VCO band select. Bits 7 and 6 of CAPBANDCTRL (Index=2B) select the capture band range.
Power Pins			
VSS	GND	4, 15, 34, 50, 60,70, 81, 96, 130, 138 110, 143, 150,	Ground
VDD	PWR	20, 45, 75, 84, 100, 135, 160	+5VDC

Table 7. T2 Pin Description

Pin	Pin Type	Pin Number	Description
Data Ports			
SDQ31- SDQ28	I	140-143	VRAM shift register data bits 31-0.
SDQ27-SDQ26	I	148-149	
SDQ25-SDQ24	I	151-152	
SDQ23-SDQ20	I	157-160	
SDQ19-SDQ16	I	167-170	
SDQ15-SDQ12	I	176-179	
SDQ11-SDQ8	I	2-5	
SDQ7-SDQ6	I	10-11	
SDQ5-SDQ4	I	13-14	
SDQ3-SDQ0	I	19-22	
VIDOUT23	O	68	Video data output (RGB) bits 23-0. Connected to digital input of RAMDAC.
VIDOUT22-VIDOUT16	O	71-77	
VIDOUT15-VIDOUT12	O	59-62	
VIDOUT11-VIDOUT8	O	64-67	
VIDOUT7-VIDOUT0	O	50-57	
VIDIN23-VIDIN20	I	111-114	Digitized live video input data (RGB) bits 23-0. Connected to the digital output of an A/D convertor.
VIDIN19-VIDIN8	I	117-128	
VIDIN7-VIDIN0	I	130-137	
MDQ31-MDQ28	I/O	144-147	VRAM data pins 31-0.
MDQ27-MDQ24	I/O	153-156	
MDQ23-MDQ20	I/O	163-166	
MDQ19-MDQ18	I/O	171-172	
MDQ17-MDQ16	I/O	174-175	
MDQ15-MDQ12	I/O	180-183	
MDQ11-MDQ8	I/O	6-9	
MDQ7-MDQ4	I/O	15-18	
MDQ3-MDQ0	I/O	25-28	
Host Interface			
RESET	I	48	System reset (active high). At the falling edge of Reset configuration information is latched to the internal TVP9520/25 registers (SYSCONFIG (Index=59h) and Micro Channel ID register). The information is carried on SASD15-SASD0 & MD11-MD0 during the reset period.
SASD15-SASD13	I/O	78-80	Multiplexed system address and data bus bits 15 - 0.
SASD12-SASD3	I/O	82-91	
SASD2-SASD0	I/O	94-96	
Control Output			
INKEY	O	99	Input source overlay key. Connected to the Decoder/Mux. Selects composite or analog RGB input to the A/D convertor. A logical 1 selects analog RGB input.

Table 7. T2 Pin Description - Continued

Pin	Pin Type	Pin Number	Description
$\overline{\text{OVLVGA}}$	O	98	Output overlay key. Connected to the Analog Mixer. Selects video data from T2 or VGA data from an external VGA controller to be ouput to the display. A logical 0 selects VGA.
Video Control Signal			
PCLK	I	45	Pixel clock input from T1.
T1 Interface			
$\overline{\text{IOCSR}}$	I	29	I/O read signal for T2. A logical 0 selects a read of the T2 I/O registers.
$\overline{\text{IOCSW}}$	I	30	I/O write signal for T2. A logical 0 selects a write to the T2 I/O registers.
$\overline{\text{MEMCSR}}$	I	31	Memory read signal for T2. A logical 0 selects a memory data read from the VRAM to T2.
$\overline{\text{MEMCSW}}$	I	32	Memory write to T2. A logical 0 selects a memory data write from the SASD to T2.
DE	I	33	Composite data enable. Signal is a combination of HDE and VDE.
WINKEY	I	34	Hardware window key. Signal used to indicate window location. A logical 1 indicates the window area.
CAPCYC	I	36	Indicates T1 has commenced a capture operation.
DLATCH	I	38	VRAM data latch clock.
$\overline{\text{FIFOW}}$	I	39	FIFO write clock. FIFO located in VRAM interface block of T2.
$\overline{\text{FIFOR}}$	I	40	FIFO read clock. FIFO located in VRAM interface block of T2.
$\overline{\text{CAPCSYNC}}$	I	44	Composite sync for capture. Also used for FIFO reset.
MDMASK	I	41	Indicates when to send mask data to the VRAM.
BYTE1, BYTE0	I	42, 43	Byte indicator for CPU access. Reference table below.

BYTE1	BYTE0	Byte
0	0	0
0	1	1
1	0	2
1	1	3

16-bit Mode:

BYTE1	BYTE0	16-bit
0	X	Least Significant 16-bit
1	X	Most Significant 16-bit

32/24-bit Mode:

BYTE1	BYTE0	32/24-bit
X	X	X

Table 7. T2 Pin Description - Continued

Pin	Pin Type	Pin Number	Description
VGA Interface			
VGAPD7-VGAPD0	I	110-103	VGA pixel data bits 7-0. Connected to Half Scanner output and VGA RAMDAC pixel data input.
$\overline{\text{VGABLNK}}$	I	97	VGA Blank Signal. Signal is input from the VGA feature connector interface to the external display genlock circuitry.
VGAPCLK	I	100	VGA Pixel Clock. Signal is input from/output to the VGA feature connector interface to/from the external display genlock circuitry Pixel clock direction is determined by signal $\overline{\text{VGADIR}}$.
Video DAC Chipset Interface			
LUT	O	49	Color mode select input . A logical 0 selects 24-bit true color operation mode. A logical 1 selects 24-bit true color bypass mode
Programmable Output			
POUT3	O	101	Programmable output 3. Bit can be programmed via bit 3 of Trident Enhanced Register POUT (Index=54).
Power Pins			
VSS	GND	1, 12, 24, 35, 37, 47, 63, 70, 81, 93, 102, 116, 129, 139, 150, 162, 173	Ground .
VDD	PWR	23, 46, 58, 69, 92, 115, 138, 161, 184	+5V.

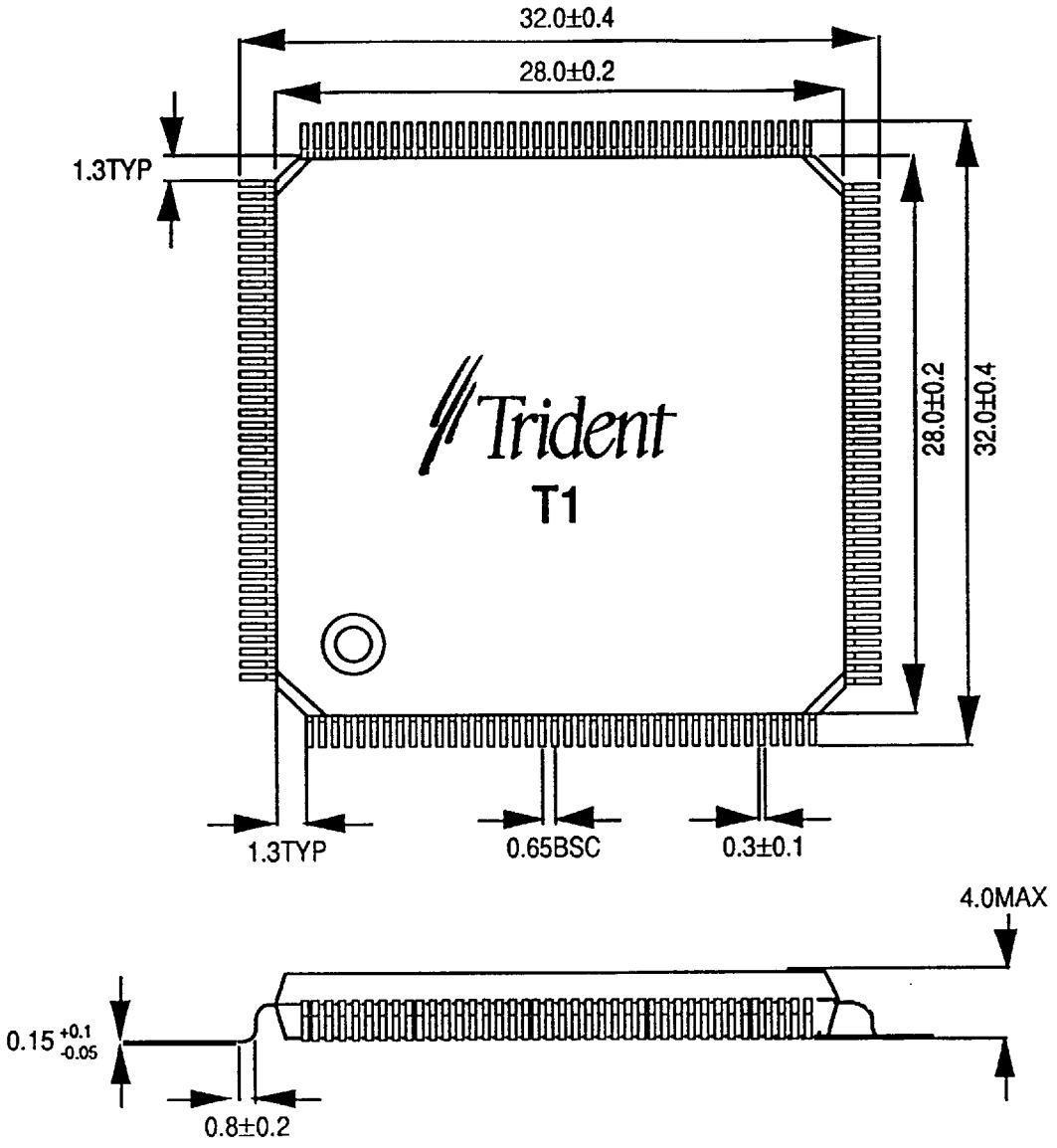

Figure 8. T1 Packaging Diagram

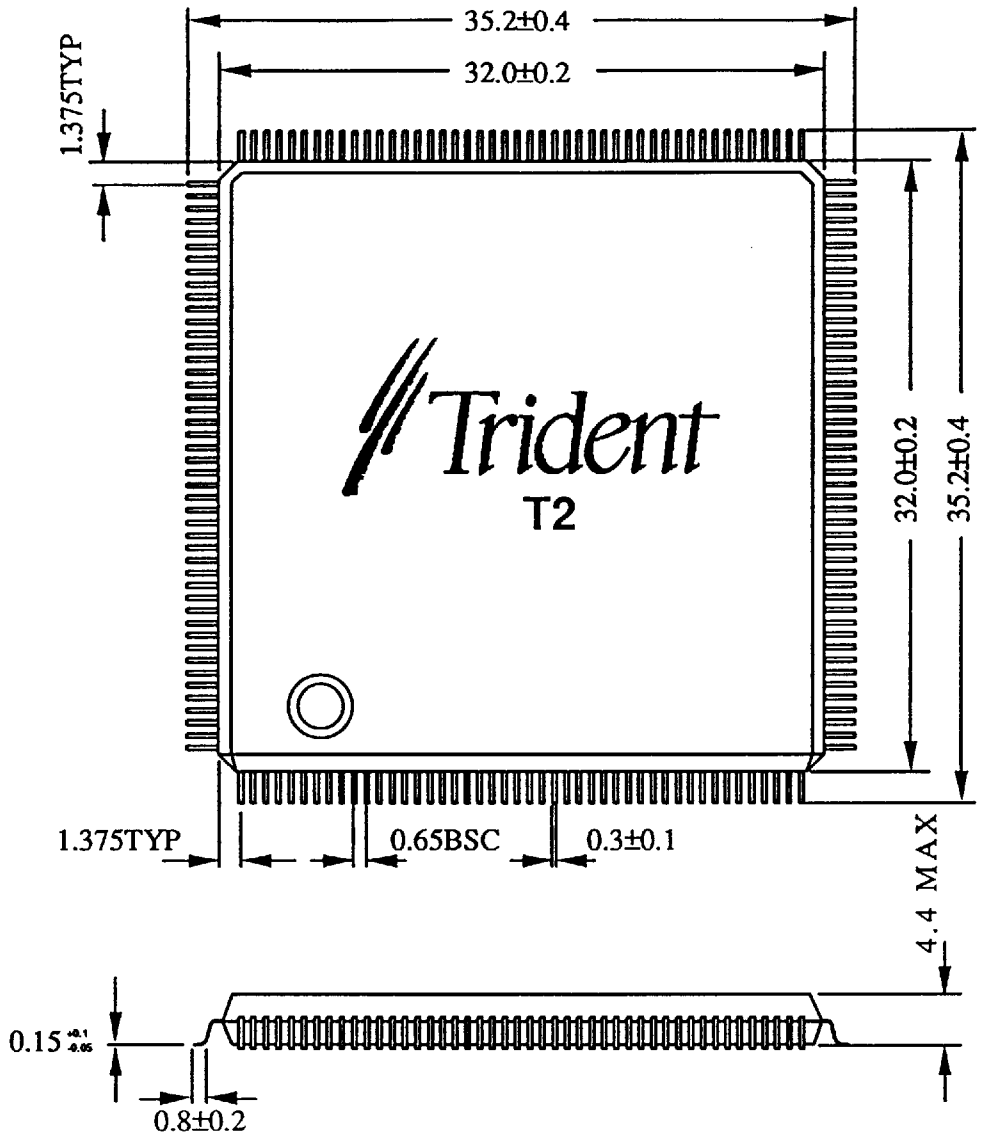

Figure 9. T2 Packaging Diagram

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