FE6030
Cache/DRAM and Channel Control Device

- Complete compatibility with the IBM* Personal System/2* Models 70 and 80
- Direct-Mapped Cache Controller
  Includes the following:
  Page Mode DRAM Controller
  Memory Configuration Registers
  Channel Controller
  Channel Buffer Controls
- Complete 256K, 1 MB, and 4 MB DRAM Support
- Ability to mix DRAM sizes in different banks
- Support for up to four banks (up to 64 MBytes) of Memory
- Programmable Wait States
- Shadow RAM for fast BIOS Execution
- Extended Setup Facility™ (ESF)™
- Low Power 1.25 Micron CMOS Technology

The FE6030 integrated circuit forms part of Western Digital's ® innovative FE6500 chip set, which facilitates the design and implementation of Model 70/80-compatible system boards. It decreases design complexity and saves space by combining the functions of many discrete arrays and components, also reducing system cost and increasing system reliability.

The Extended Setup Facility or ESF is a Western Digital enhancement, designed to allow more functionality such as a Winchester Controller, LAN Adapter or additional Serial Port to be added on to the system board. It provides product differentiation at the system level and helps reduce costs. The block diagram in Figure 1 illustrates a typical system utilizing the FE6500 chip set. Devices with bold outlines are available from Western Digital Corporation.

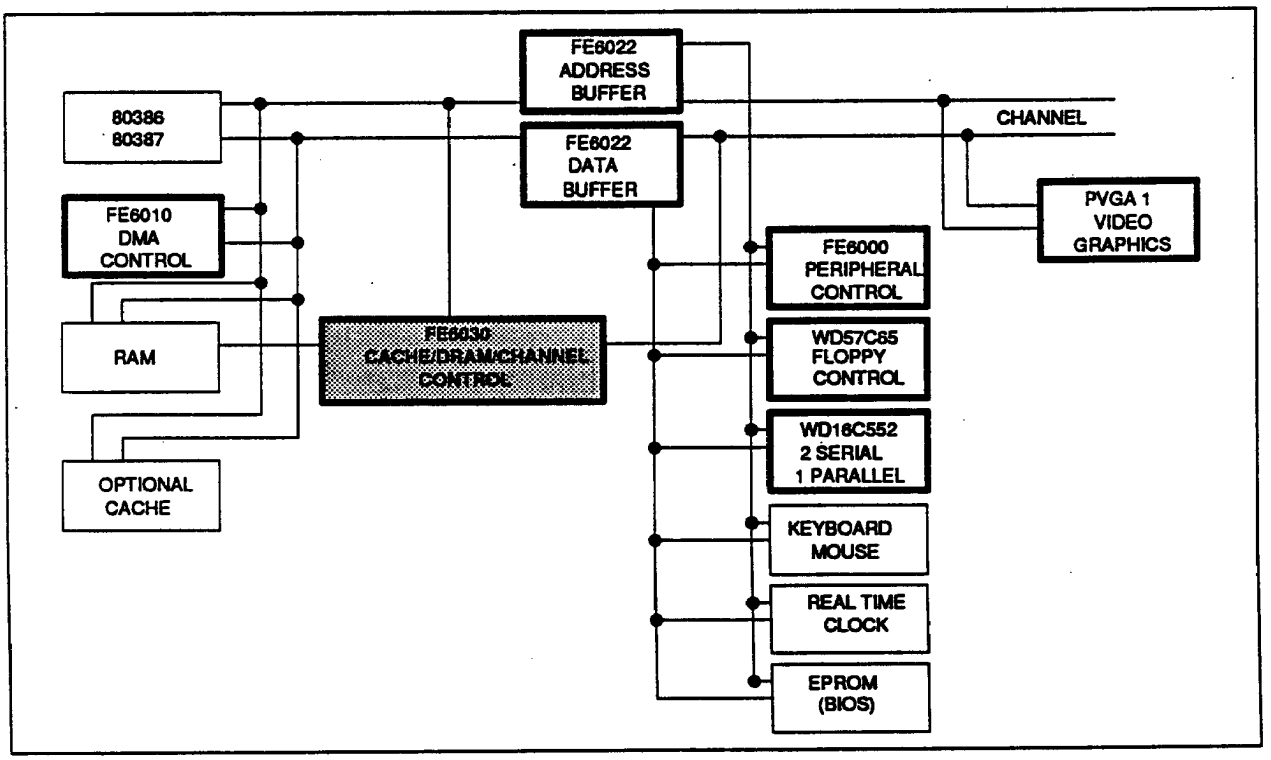

Figure 1. System Block Diagram

Additional References

IBM PS/2 Model 70 Technical Reference Manual
IBM PS/2 Model 80 Technical Reference Manual
Intel* Microprocessor and Peripheral Handbook

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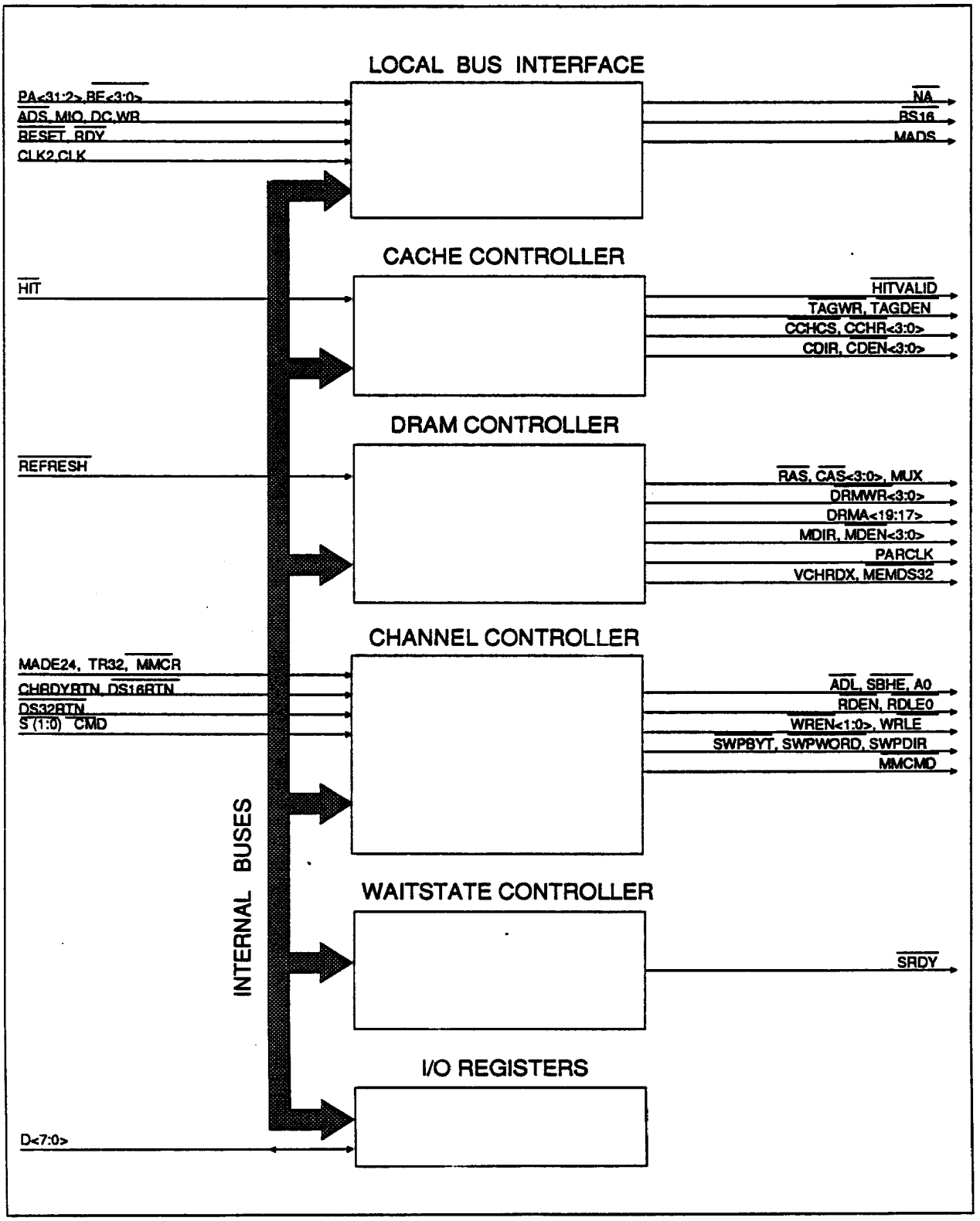

Figure 2. FE6030 Block Diagram

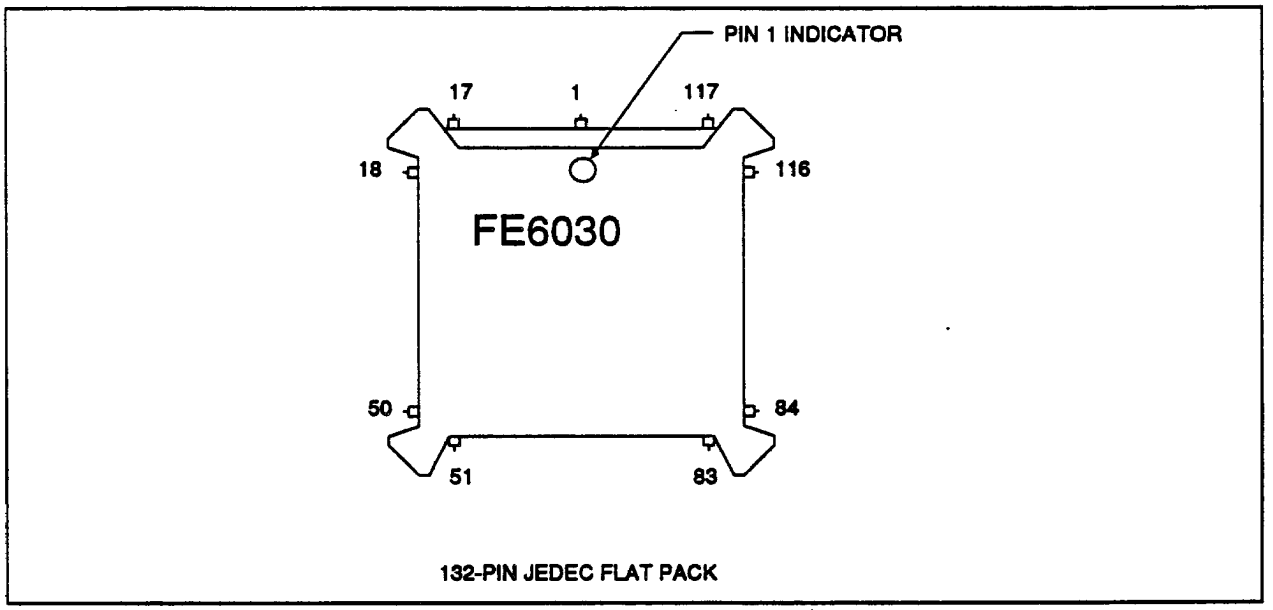

Figure 3. Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	PA2	34	RESERVED	67	$\overline{\text{WREN1}}$	100	$\overline{\text{CDEN2}}$
2	PA3	35	TR32	68	$\overline{\text{WRENH}}$	101	$\overline{\text{CDEN1}}$
3	PA4	36	CHRDYRTN	69	$\overline{\text{WRLE}}$	102	$\overline{\text{CDEN0}}$
4	PA5	37	$\overline{\text{DS16RTN}}$	70	$\overline{\text{SWPWORD}}$	103	CDIR
5	PA6	38	$\overline{\text{DS32RTN}}$	71	V_{SS}	104	$\overline{\text{TAGWR}}$
6	PA7	39	V_{DD}	72	$\overline{\text{SWPBYT}}$	105	$\overline{\text{TAGDEN}}$
7	PA8	40	$\overline{\text{MEMDS32}}$	73	SWPDIR	106	V_{SS}
8	PA9	41	UCHRDY	74	$\overline{\text{RAS}}$	107	$\overline{\text{HITVALID}}$
9	PA10	42	$\overline{\text{S0}}$	75	$\overline{\text{CAS0}}$	108	$\overline{\text{SRDY}}$
10	PA11	43	$\overline{\text{S1}}$	76	$\overline{\text{CAS1}}$	109	MADS
11	PA12	44	V_{SS}	77	$\overline{\text{CAS2}}$	110	$\overline{\text{RDY}}$
12	PA13	45	$\overline{\text{CMD}}$	78	$\overline{\text{CAS3}}$	111	$\overline{\text{HIT}}$
13	PA14	46	A0	79	$\overline{\text{DRMWR0}}$	112	MADE24
14	PA15	47	$\overline{\text{SBHE}}$	80	$\overline{\text{DRMWR1}}$	113	$\overline{\text{BE0}}$
15	PA16	48	$\overline{\text{ADL}}$	81	$\overline{\text{DRMWR2}}$	114	$\overline{\text{BE1}}$
16	PA17	49	RESERVED	82	$\overline{\text{DRMWR3}}$	115	$\overline{\text{BE2}}$
17	V_{SS}	50	V_{SS}	83	V_{SS}	116	V_{SS}
18	PA18	51	PARCLK	84	DRMA19	117	$\overline{\text{BE3}}$
19	PA19	52	$\overline{\text{NA}}$	85	DRMA18	118	WR
20	PA20	53	$\overline{\text{BS16}}$	86	MUX	119	DC
21	PA21	54	D0	87	$\overline{\text{MDEN3}}$	120	MIO
22	PA22	55	D1	88	$\overline{\text{MDEN2}}$	121	$\overline{\text{ADS}}$
23	PA23	56	D2		$\overline{\text{MDEN1}}$	122	V_{DD}
24	V_{DD}	57	D3		$\overline{\text{MDEN0}}$	123	$\overline{\text{REFRESH}}$
25	PA24	58	V_{SS}	91	MDIR	124	$\overline{\text{RESET}}$
26	PA25	59	D4	92	V_{DD}	125	HLDA
27	PA26	60	D5	93	$\overline{\text{CCHCS}}$	126	UCHMSTR
28	V_{SS}	61	D6	94	$\overline{\text{CCHWR3}}$	127	A20GTX
29	PA27	62	D7	95	V_{SS}	128	RESERVED
30	PA28	63	$\overline{\text{RDEN}}$	96	$\overline{\text{CCHWR2}}$	129	$\overline{\text{TEST}}$
31	PA29	64	$\overline{\text{RDLE0}}$	97	$\overline{\text{CCHWR1}}$	130	CLK
32	PA30	65	$\overline{\text{WREN0}}$	98	$\overline{\text{CCHWR0}}$	131	CLK2
33	PA31	66	V_{DD}	99	$\overline{\text{CDEN3}}$	132	V_{SS}

1.0 PIN DESCRIPTION

The signals assigned to the different pins are grouped according to their function, and discussed individually in the following table.

❑ LOCAL BUS INTERFACE SIGNALS

The FE6030 sits directly on the 80386 bus, controlling the 80386/DMA accesses to local memory, I/O and the Channel, and the Channel master accesses to the local memory.

❑ CACHE CONTROLLER SIGNALS

The Cache Controller on the FE6030 implements a direct-mapped cache for the 80386, which improves performance significantly by allowing the majority of memory cycles to be run at zero wait states. These signals form part of the interface between the cache controller and the external cache and TagRAMs. See Section 2.0 for a detailed description of the cache controller.

❑ DRAM CONTROLLER SIGNALS

The DRAM Controller supports Page Mode, and allows DRAMs of different sizes to be used together. 80386 pipelined operation, which allows fast accesses to the DRAMs, is also supported.

❑ CHANNEL CONTROLLER SIGNALS

The Channel controller implements the interface to the system board. The FE6030 generates the Channel interface signals whenever the 80386 or the DMA controller accesses any resource on the Channel.

❑ CHANNEL BUFFER CONTROL SIGNALS

The Channel Buffer signals control the data buffers between the local processor data bus and the Channel data bus. The data buffers are integrated in the FE6022 device; these signals provide the interface to that device. Note that the FE6022 must be strapped in the data buffer mode.

❑ MISCELLANEOUS SIGNALS

This set of signals include the V_{SS} and V_{DD} signal pins as well as the reserved pins, which should not be connected, but left open in the system.

Table 1. Pin Signals

PIN NO.	NAME	TYPE	FUNCTION
			LOCAL BUS INTERFACE
126	UCHMSTR (F1)	I	CHANNEL MASTER This signal has two functions. At power-up, the state of this signal is latched at the trailing edge of $\overline{\text{RESET}}$, and, in conjunction with F0, determines the frequency at which the FE6030 will operate. The following table lists the clock frequencies. FREQUENCY / F1 (UCHMSTR) / F0 (A20GTX) 16 MHz / 0 / 0 20 MHz / 0 / 1 25 MHz / 1 / 1
			At all other times UCHMSTR functions in its normal capacity as a signal from the CACP on the FE6010. When it is active, it indicates that a Channel master has the bus. The system designer should use a 10 K resistor to pull up/down this signal.
125	HLDA	I	HOLD ACKNOWLEDGE When the HLDA signal from the 80386 is active, it indicates that the 80386 has relinquished control of the bus.
124	$\overline{\text{RESET}}$	I	$\overline{\text{SYSTEM RESET}}$ This System Reset signal is driven by the FE6010, and is active at power-on. It initializes all internal state machines and registers to the power-on default stage.
131 130	CLK2 CLK	I I	SYSTEM CLOCKS CLK2 frequency is twice the operating frequency of the 80386. The FE6030 shares this CMOS-level signal with the 80386. CLK is another CMOS-level signal, whose frequency corresponds to the operating frequency of the processor. When the system is reset, it has the same phase relationship with CLK2 as the internal CLK of the 80386.

PIN NO.	NAME	TYPE	FUNCTION
33 32 31 30 29 27 26 25 23 22 21 20 19 18 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	PA31 PA30 PA29 PA28 PA27 PA26 PA25 PA24 PA23 PA22 PA21 PA20 PA19 PA18 PA17 PA16 PA15 PA14 PA13 PA12 PA11 PA10 PA9 PA8 PA7 PA6 PA5 PA4 PA3 PA2	I	PROCESSOR ADDRESS LINES These processor address lines are driven by the 80386, the DMA controller, or the Channel master.
117 115 114 113	$\overline{BE3}$ $\overline{BE2}$ $\overline{BE1}$ $\overline{BE0}$	I	$\overline{80386\ BYTE\ ENABLES}$ These 80386 Byte-Enable signals are driven by the 80386, the FE6010 DMA controller, or the Channel master.
127	A20GTX (F0)	I/O	ADDRESS WRAP-AROUND This signal has two functions. At power-on, it carries the encoding of the frequency at which the system will operate. It is latched by the trailing edge of $\overline{RESET}$. See the table in the UCHMSTR description for the configurations for different frequencies. After power-on, it performs a different function: it is used to wrap around addresses in the Real and Virtual 8086 modes of the 80386 processor. The signal is generated in the FE6010, and is a combination of the A20GATE generated by the 8742 and the Alternate Gate A20 signal from Port 0092H, Bit 1. The FE6030 uses this signal internally to generate the correct address for memory accesses. Depending on the frequency configuration required, the system designer should pull up/down this signal with a 10K resistor.

PIN NO.	NAME	TYPE	FUNCTION
62 61 60 59 57 56 55 54	D7 D6 D5 D4 D3 D2 D1 D0	I/O	CHANNEL DATA LINES These Channel data lines allow the internal registers of the FE6030 to be programmed through the Channel data bus. These registers can be accessed through 8-bit operations only. When they are accessed, a Channel cycle ($\overline{S0}$, $\overline{S1}$, $\overline{CMD}$, and so on) is initiated, and the controls for the Channel buffers are activated to complete the cycle.
121	$\overline{ADS}$	I	$\overline{ADDRESS\ STROBE}$ The FE6030 uses this signal to keep track of bus cycles on the 80386 bus. Both pipelined and non-pipelined cycles are supported by the FE6030. The Channel master cycles are controlled by the $\overline{CMD}$ signal.
110	$\overline{RDY}$	I	$\overline{80386\ READY}$ The Ready signal to the 80386 is used to track the bus cycles on the 80386 local bus. It is generated externally, by discrete components.
53	$\overline{BS16}$	O	$\overline{80386\ BS16}$ This is the BS16# signal to the 80386, and is asserted whenever the 80386 or the FE6010 accesses a 16-bit or 8-bit port. When accessing an 8-bit port, the FE6030 splits the 16-bit cycle into two 8-bit cycles.
52	$\overline{NA}$	O	$\overline{NEXT\ ADDRESS}$ The Next Address signal to the 80386 and the FE6010 is asserted whenever a pipelined cycle can be supported by the system. The FE6030 requests a pipelined cycle whenever a cycle other than a Cache-Read-Hit occurs.
120 119 118	MIO DC WR	I	BUS CYCLE TYPE The MIO line is tied to MIO signal from the 80386. For accesses to and from the Channel, it is buffered by the FE6022(Address Buffer Mode) to form Channel signal MMIO. DC and WR are tied directly to the 80386 D/C#, and W/R# signals. Together with MIO, they indicate the type of bus cycle being executed on the 80386 bus. Refer to the 80386 Data Sheet for the encoding of the bus cycles.
108	$\overline{SRDY}$	O	$\overline{SYSTEM\ READY}$ The FE6030 generates a Ready signal for system resources not on the local bus, including the local DRAM. The System Ready signal generates a Ready whenever the 80386/DMA performs a bus cycle that is not an access to the numeric coprocessor (80387 or Weitek 3167), nor a memory access resulting in a cache hit. The signal is logically ORed on the system board with the other sources of READY to generate a $\overline{RDY}$ to the 80386. Note that the default for the READY signal to the 80386/DMA is a "not-ready" interface.
			CACHE CONTROLLER
111	$\overline{HIT}$	I	$\overline{CACHE\ HIT}$ The external tag subsystem sends this signal to indicate that the current cycle resulted in a match of the Tag. Depending on whether or not the DRAM cycle can be cached, this signal is internally qualified to generate a cache hit indication. If a cache hit occurs on a memory read cycle, a zero wait state operation is accomplished. The following figure shows Ready Generation in an FE6500 system.
107	$\overline{HITVALID}$	O	$\overline{CACHE\ HIT\ QUALIFIER}$ This signal is sent out from the FE6030 to indicate that the $\overline{HIT}$ signal from the tag subsystem is valid and can be sampled by the external logic. $\overline{HIT}$ and $\overline{HITVALID}$ are logically ANDed to generate a READY signal to the 80386/DMA, which results in a zero wait state cycle on a cache read hit.

PIN NO.	NAME	TYPE	FUNCTION
			For a cycle requiring a cache update, $\overline{HIT}$ may be inactive in the early part of the cycle and become active in the latter part, when the Tag is updated. $\overline{HITVALID}$ is inactive in the latter part of the cycle, so as to prevent a spurious READY signal to the 80386 from being generated.
93	$\overline{CCHCS}$	O	$\overline{DATA\ CACHE\ CHIP\ SELECT}$ This is the Chip Select signal to the Data Cache. This signal is always active at the beginning of a cycle, permitting the slowest SRAMs to be used. It is only de-asserted for a cache update operation.
94 96 97 98	$\overline{CCHWR3}$ $\overline{CCHWR2}$ $\overline{CCHWR1}$ $\overline{CCHWR0}$	O	$\overline{DATA\ CACHE\ WRITE}$ This write signal writes individual bytes to the data cache. The FE6030 asserts the write signal corresponding to the byte enables asserted during the cycle.
104	$\overline{TAGWR}$	O	$\overline{TAG\ WRITE}$ This write signal updates the Tag in the TagRAM for a Cache Update cycle. Whenever a cache miss occurs, a pipelined cycle is requested and $\overline{TAGWR}$ updates the Tag value.
105	$\overline{TAGDEN}$	O	$\overline{TAG\ DATA\ ENABLE}$ This signal opens a "Tag buffer" such as the F244 during a Tag update cycle. Tag updates occur on a Cache Miss cyle on cachable memory areas.
103	CDIR	O	CACHE BUFFER DIRECTION CDIR determines the direction of the data flow for the F245 buffers, between the Processor Data (PD) and Cache Data (CD) buses. The F245 buffers minimize the loading on the 80386 local bus and permit more relaxed timings on the Data Cache SRAMs. They also permit SRAMs that do not require the Output Enable function to be used in the design. CDIR =0; CD (31:0) to PD (31:0) =1; PD (31:0) to CD (31:0)
99 100 101 102	$\overline{CDEN3}$ $\overline{CDEN2}$ $\overline{CDEN1}$ $\overline{CDEN0}$	O	$\overline{CACHE\ BUFFER\ ENABLES}$ $\overline{CDEN}$ provides the enable signals for the F245 buffers between the PD and CD busses. Each data byte has a separate enable. The signals are qualified internally by the byte enables from the 80386/DMA. Figure 4 illustrates a typical cache cycle with page hits.
			DRAM CONTROLLER
74	$\overline{RAS}$	O	$\overline{DRAM\ RAS\ SIGNAL}$ $\overline{RAS}$ connects to the RAS inputs of all the DRAMs. Depending on the load that is to be driven by the signal, $\overline{RAS}$ may have to be buffered by an external AS1832. This signal is active in Page Mode, as long as the accesses remain within the same row. It will remain active even if the accesses are made to addresses in different memory banks which share the same row address, because the row addresses are shared by the different memory banks. In normal RAS/CAS Mode, a RAS precharge takes place for every DRAM access.
86	MUX	O	ADDRESS MULTIPLEXER This pin interfaces with the external address multiplexers, and controls the generation of the row and column addresses the DRAM. MUX = 0; Row Address = 1; Column Address

PIN NO.	NAME	TYPE	FUNCTION
78 77 76 75	$\overline{CAS3}$ $\overline{CAS2}$ $\overline{CAS1}$ $\overline{CAS0}$	O	$\overline{DRAM\ CAS\ SIGNALS}$ There are four $\overline{CAS}$ signals to the DRAM, one for each bank. The bank being accessed has its $\overline{CAS}$ signal active during a cycle. At the end of the cycle, all $\overline{CAS}$ signals are inactive. This signal may have to be buffered with external AS1832s, depending on the load that is to be driven by this signal. Since the FE6030 de-asserts this signal at the end of each cycle, Page Mode DRAMs can be employed. Static Column DRAMs may also be used; however, they will operate in Page Mode.
82 81 80 79	$\overline{DRMWR3}$ $\overline{DRMWR2}$ $\overline{DRMWR1}$ $\overline{DRMWR0}$	O	$\overline{DRAM\ WRITE}$ The four write signals to the DRAM, one for each data byte, may have to be buffered by external AS1832s, depending on the load that is to be driven by this signal.
51	PARCLK	O	PARITY ERROR CLOCK This signal is used as a clock to latch in parity error information during DRAM read cycles. At the rising edge of this signal, the parity error information is latched in. The Parity Error Latch function is implemented on the system board.
84 85	DRMA19 DRMA18	O	DRAM SPLIT MEMORY ADDRESS These signals provide Address Bits 18 and 19 for DRAM accesses, which are sent to the external DRAM address multiplexors. These signals implement the split addressing memory feature.
123	$\overline{REFRESH}$	I	$\overline{REFRESH}$ This FE6010 signal indicates that a Refresh cycle is in progress and a Memory Read cycle is being run on the local bus. When this signal is active, the DRAM controller initiates a RAS-only cycle with the address supplied by the FE6010. Simultaneously, it initiates a Memory Read cycle on the Channel. A Ready signal is generated when both the cycles have been completed.
91	MDIR	O	DRAM BUFFER DIRECTION MDIR controls the direction of the F657 data between the Processor Data Bus (PD), and the DRAM Data Bus (MD). MDIR =0; MD (31:0) to PD (31:0) =1; PD (31:0) to MD (31:0)
87 88 89 90	$\overline{MDEN3}$ $\overline{MDEN2}$ $\overline{MDEN1}$ $\overline{MDEN0}$	O	$\overline{DRAM\ BUFFER\ ENABLES}$ These signals are the output enables for the F657 buffers between the PD and MD busses, with one enable signal for each byte. During a cycle, the enable signal corresponding to the active byte enables are asserted.
109	MADS	O	MEMORY ADDRESS STROBE The Memory Address Strobe signal for the external address latch latches all addresses to the External Data Cache and the DRAM. Figures 5 and 6 illustrate a typical cycle to the DRAM.
			CHANNEL CONTROLLER
43 42	$\overline{S1}$ $\overline{S0}$	I/O	$\overline{CHANNEL\ BUS\ STATUS\ LINES}$ The Channel Bus Status lines interface directly with the Channel, and, together with MIO, indicate the type of cycle being run on the Channel bus. They are input lines during a Channel Master cycle.
48	$\overline{ADL}$	O	$\overline{CHANNEL\ ADDRESS\ LATCH}$ This Channel Address Latch signal interfaces directly to the Channel NADL signal.
45	$\overline{CMD}$	I/O	$\overline{CHANNEL\ COMMAND}$ This Channel Command signal interfaces directly with the $\overline{CMD}$ signal from the Channel. This is an input signal during a Channel master cycle.

PIN NO.	NAME	TYPE	FUNCTION
46	A0	O	CHANNEL ADDRESS BIT 0 Address Bit 0 on the Channel directly interfaces with the A0 signal from the Channel.
47	$\overline{\text{SBHE}}$	O	$\overline{\text{CHANNEL BYTE HIGH ENABLE}}$ The Channel Byte High Enable signal interfaces directly with the $\overline{\text{SBHE}}$ signal on the Channel. The 16-bit slaves on the Channel use this signal to determine the bytes containing data during the current bus cycle, as shown in following table: A0 SBHE DATA AVAILABLE 0 0 D (15:0) 0 1 D (7:0) 1 0 D (15:8) 1 1 Reserved Note that this signal is not used by 8-bit or 32-bit slaves. The latter uses $\overline{\text{BE}}$ signals (Byte Enables) to perform the same function. $\overline{\text{SBHE}}$ is output only from the FE6030.
112	MADE24	I	MEMORY DATA ENABLE 24 This signal is the same as the Channel MADE24 signal, and interfaces directly with the Channel. If the signal is inactive during Channel memory cycles, it indicates that an address greater than 16 M is being presented. The FE6022 in Address Buffer Mode drives this signal inactive whenever the 80386 or the DMA performs a Channel memory access above the 16 M boundary.
36	CHRDYRTN	I	CHANNEL READY The Channel CHRDYRTN signal interfaces directly with the Channel. It is an external AND on the system board of all the READY sources present on the Channel, namely, the individual Channel slots, the PVGA, the FE6000 (IORDY), and the system board DRAM (UCHRDY). A Channel slave uses this signal to extend the bus cycle.
37	$\overline{\text{DS16RTN}}$	I	$\overline{\text{DATA SIZE 16}}$ This signal corresponds to the $\overline{\text{DS16RTN}}$ signal on the Channel and directly interfaces with it. It is generated by ORing all the $\overline{\text{CDDS16N}}$ signals on the Channel. When $\overline{\text{DS16RTN}}$ is active during a Channel cycle, it indicates that the slave being addressed is capable of transferring data in 16-bit quantities.
38	$\overline{\text{DS32RTN}}$	I	$\overline{\text{DATA SIZE 32}}$ This signal corresponds to the $\overline{\text{DS32RTN}}$ signal on the Channel and directly interfaces with it. It is generated by ORing all the $\overline{\text{CDDS32N}}$ signals on the Channel. When $\overline{\text{DS32RTN}}$ is active during a Channel cycle, it indicates that the slave being addressed is capable of transferring data in 32-bit quantities.
35	TR32	I	TRANSLATE 32 The Translate 32 signal on the Channel interfaces directly with the TR32 signal. When driven high, it indicates that a 16-bit master has the bus and that the Central Translator function should be turned on. This function facilitates communication between a 16-bit master and a 32-bit slave, providing for swapping data and generating the necessary control signals. It is driven low by the FE6022 whenever the 80386 or the DMA controller in the FE6010 makes an access to the Channel, since they are 32-bit masters.
40	$\overline{\text{MEMDS32}}$	O	$\overline{\text{LOCAL DRAM MEMORY SIZE 32}}$ The Memory Size 32 signal is used in the external logic to generate the $\overline{\text{DS16RTN}}$ and $\overline{\text{DS32RTN}}$ signals. It is driven by the FE6030 when a Channel master accesses the System board memory, and indicates that the memory accessed is thirty-two bits wide.
41	UCHRDY	O	LOCAL DRAM CHANNEL READY This Ready signal to the Channel is used to extend cycles when a Channel master accesses the system board RAM. It is also used in the external logic to generate CHRDYRTN. Figures 7 and 8 indicate typical master cycles to the system board DRAM.

PIN NO.	NAME	TYPE	FUNCTION
			CHANNEL BUFFER CONTROLS
63	$\overline{\text{RDEN}}$	O	$\overline{\text{READ ENABLE}}$ When data flows from the Channel to the processor bus, this signal serves as a read enable signal that enables the lower (15:0) and upper words (31:16) of the buffer. This signal is active when the 80386 or the DMA performs a Read from the Channel, or when a Channel master writes to the system board DRAM. The signal is also activated when the 80386/DMA accesses the registers on the FE6030 device.
64	$\overline{\text{RDLE0}}$	O	$\overline{\text{READ LATCH ENABLE 0}}$ This signal, Read Latch Enable 0, is the latch enable signal for Byte 0 (7:0). When the 80386 or the DMA performs a cycle to an 8-bit device on the Channel, the cycle is split into two, with this signal latching the data during the first cycle.
67 65 68	$\overline{\text{WREN1}}$ $\overline{\text{WREN0}}$ $\overline{\text{WRENH}}$	O	$\overline{\text{WRITE ENABLE}}$ These signals enable the buffer for a write operation when the data flow is from the processor bus to the Channel bus. The $\overline{\text{WREN0}}$ and $\overline{\text{WREN1}}$ signals control Bits 7-0 of Byte 0, and Bits 15-8 of Byte 1, respectively. $\overline{\text{WRENH}}$ controls the upper word, (Bits 31-16). The signals become valid when the 80386 or the DMA performs a Write operation to the Channel or when a Channel master performs a Read operation from the system board RAM. The signals are also activated when the 80386 or the DMA accesses any of the registers on the FE6030 device.
69	$\overline{\text{WRLE}}$	O	$\overline{\text{WRITE LATCH ENABLE}}$ The Write Latch Enable signal latches the Write data during a write operation by the 80386 or the DMA to the Channel. It provides the write-data-hold timing during these operations. The signal also latches data when either the 80386 or the DMA writes to an 8-bit port. In such a case, the cycle is split into two cycles on the Channel.
72	$\overline{\text{SWPBYT}}$	O	$\overline{\text{BYTE SWAP}}$ When the 80386 or the DMA accesses an 8-bit port, the cycle is split into two on the Channel. This signal is used to swap data to the correct bytes: **(7:0) to (15:8) for a Read operation** **(15:8) to (7:0) for a Write operation**
70	$\overline{\text{SWPWORD}}$	O	$\overline{\text{WORD SWAP}}$ This signal performs a word swap when a 16-bit Channel master talks to an 32-bit slave. Known as "Data Steering", the function is actually performed in the FE6022 device when it is configured in Data Buffer Mode. For a Channel Master read operation, it swaps D(31:16) to D(15:0); for a Channel Master write operation, it swaps D(15:0) to D(31:16).
73	SWPDIR (NCOPRES)	I/O	BYTE SWAP DIRECTION This signal serves two functions. At reset time, this signal detects the presence or absence of the 80387, and is latched by the trailing edge of $\overline{\text{RESET}}$. Reset State = 0; Numeric coprocessor present 1; Numeric coprocessor absent
			Its normal function at all other times is to determine the direction of the byte swap and word swap buffers. Depending on the configuration desired for the 80387, the designer should pull up/down this signal with a 10K resistor. **BYTE SWAP** **WORD SWAP** SWPDIR = 0 D (7:0) to D (15:8) D (15:0) to D (31:16) =1 D (15:8) to D (7:0) D (31:16) to D (15:0)

PIN NO.	NAME	TYPE	FUNCTION
			MISCELLANEOUS
129	$\overline{\text{TEST}}$	I	$\overline{\text{TEST PIN}}$ This is an active low pin to facilitate board-level testing. When low, this signal tristates all outputs and bi-directional signal lines, so that an ATE tester can drive these signal lines. When high, the outputs and bi-directional signal lines are enabled by the chip.
24, 39, 66, 92, 122	V_{DD}	I	+5 V Power Supply
17, 28, 44, 50, 58, 71, 83, 95, 106, 116, 132	V_{SS}	I	0 V Ground
34, 49, 128	Reserved	-	Should not be connected

Table 2 details the state of the pins on the FE6030 after a reset.

SIGNAL	BUS STATE AFTER RESET
D (7:0)	Z*
$\overline{\text{NA}}$, $\overline{\text{BS16}}$	High
$\overline{\text{S (1:0)}}$, $\overline{\text{ADL}}$, $\overline{\text{CMD}}$	High
$\overline{\text{SBHE}}$, A0	High
$\overline{\text{MEMDS32}}$	High
UCHRDY, $\overline{\text{SRDY}}$	High
MADS	High
$\overline{\text{HITVALID}}$	High
$\overline{\text{CCHCS}}$	High
CDIR, MDIR	Low
MCCHWR (3:0), $\overline{\text{CDEN (3:0)}}$	High
$\overline{\text{TAGWR}}$, $\overline{\text{TAGDEN}}$	High
$\overline{\text{RAS}}$, $\overline{\text{CAS (3:0)}}$	High
MUX, PARCLK	Low
$\overline{\text{DRMWR (3:0)}}$	High
DRMA (19:18)	High
$\overline{\text{MDEN (3:0)}}$	High
$\overline{\text{RDEN}}$	High
$\overline{\text{RDLE0}}$	Low
$\overline{\text{WREN (1:0)}}$, $\overline{\text{WRENH}}$	High
$\overline{\text{WRLE}}$	Low
$\overline{\text{SWPBYT}}$, $\overline{\text{SWPWORD}}$	High
SWPDIR	High

* Z = High Impedance

Table 2. Pin State After Reset

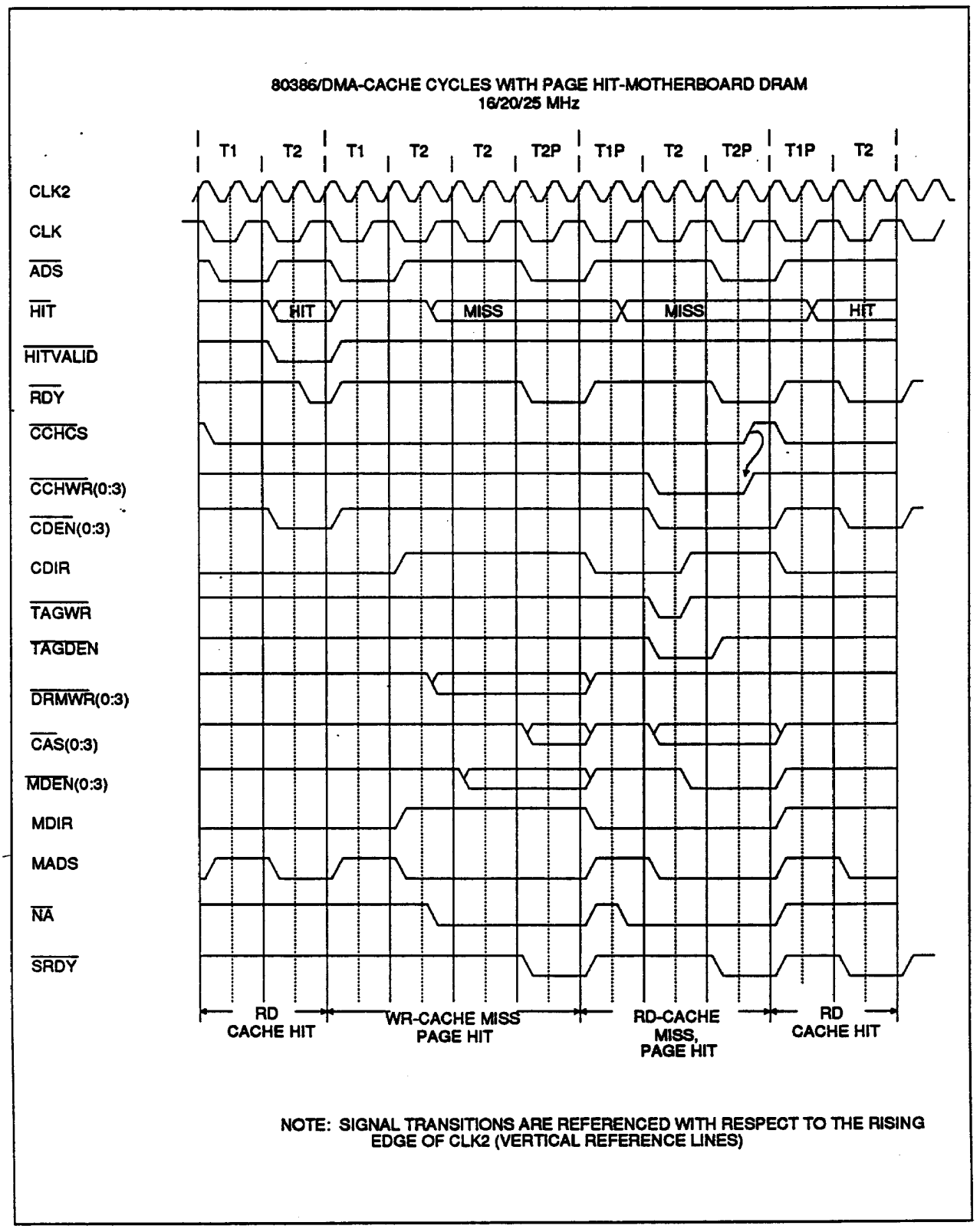

Figure 4. Cache Cycle with Page Hits

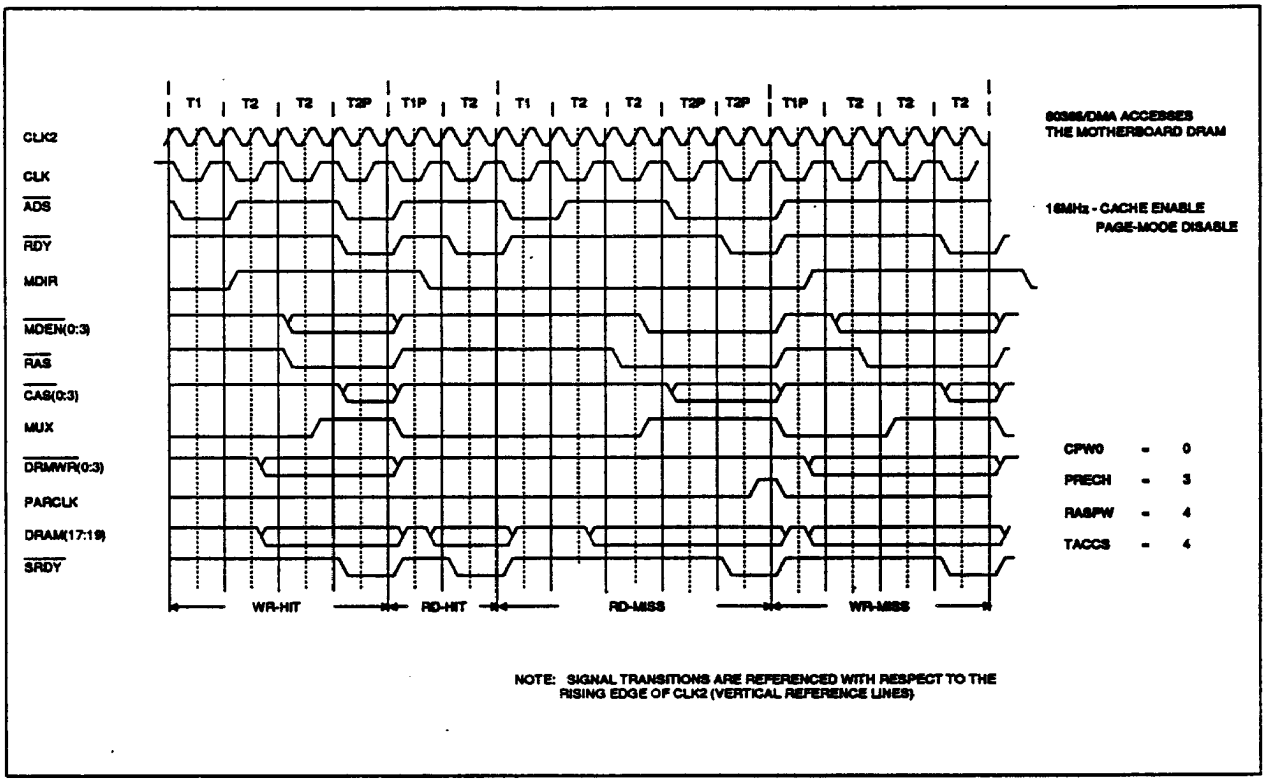

Figure 5. Channel Master Accesses to System Board DRAM-I

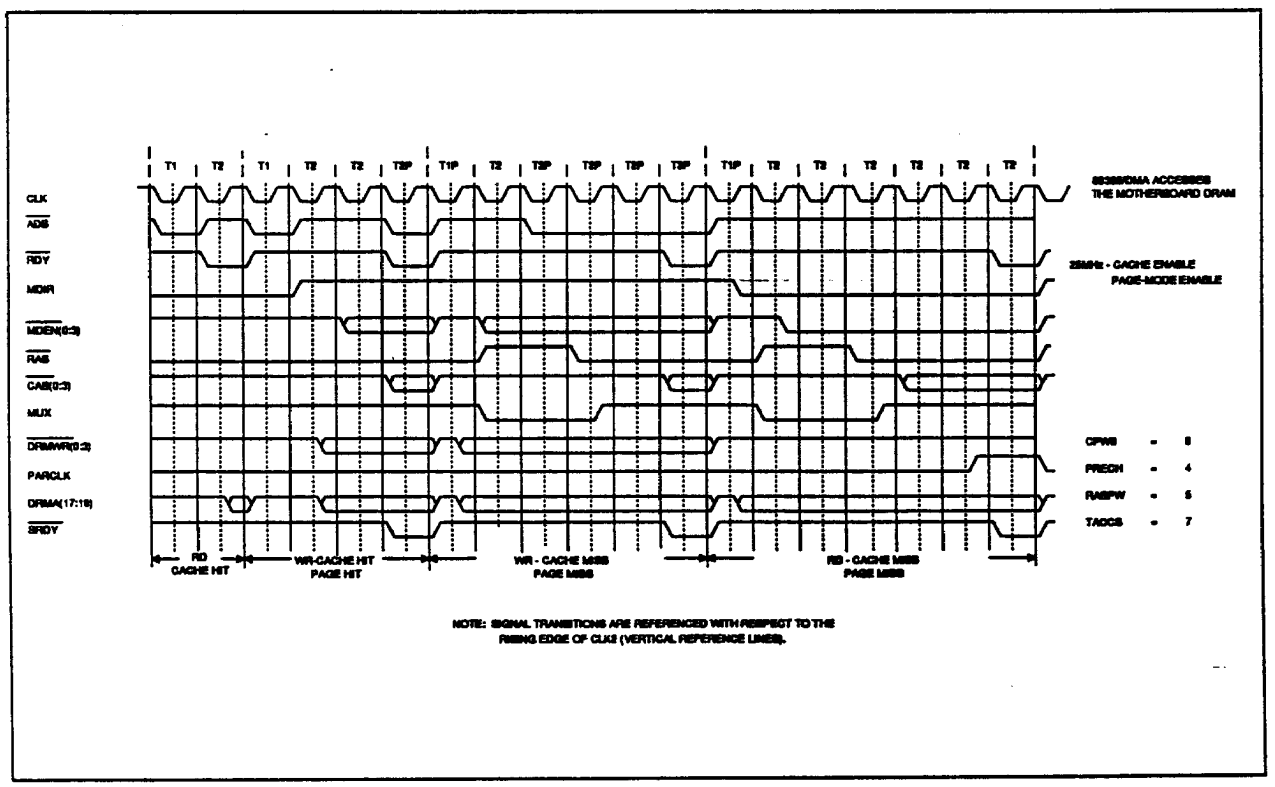

Figure 6. 80386/DMA Access to DRAM -I

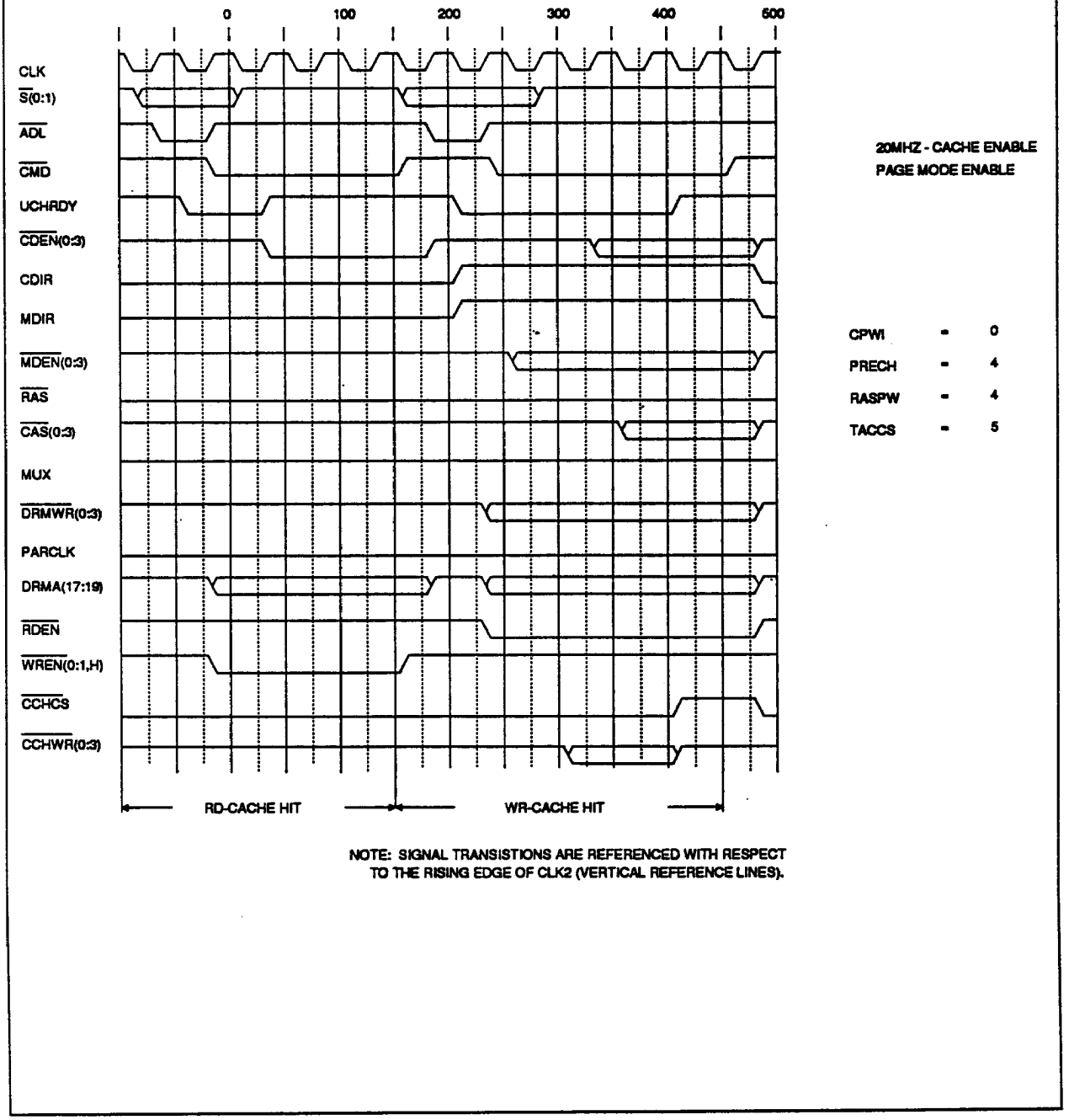

Figure 7. Channel Master Accesses to System Board DRAM-II

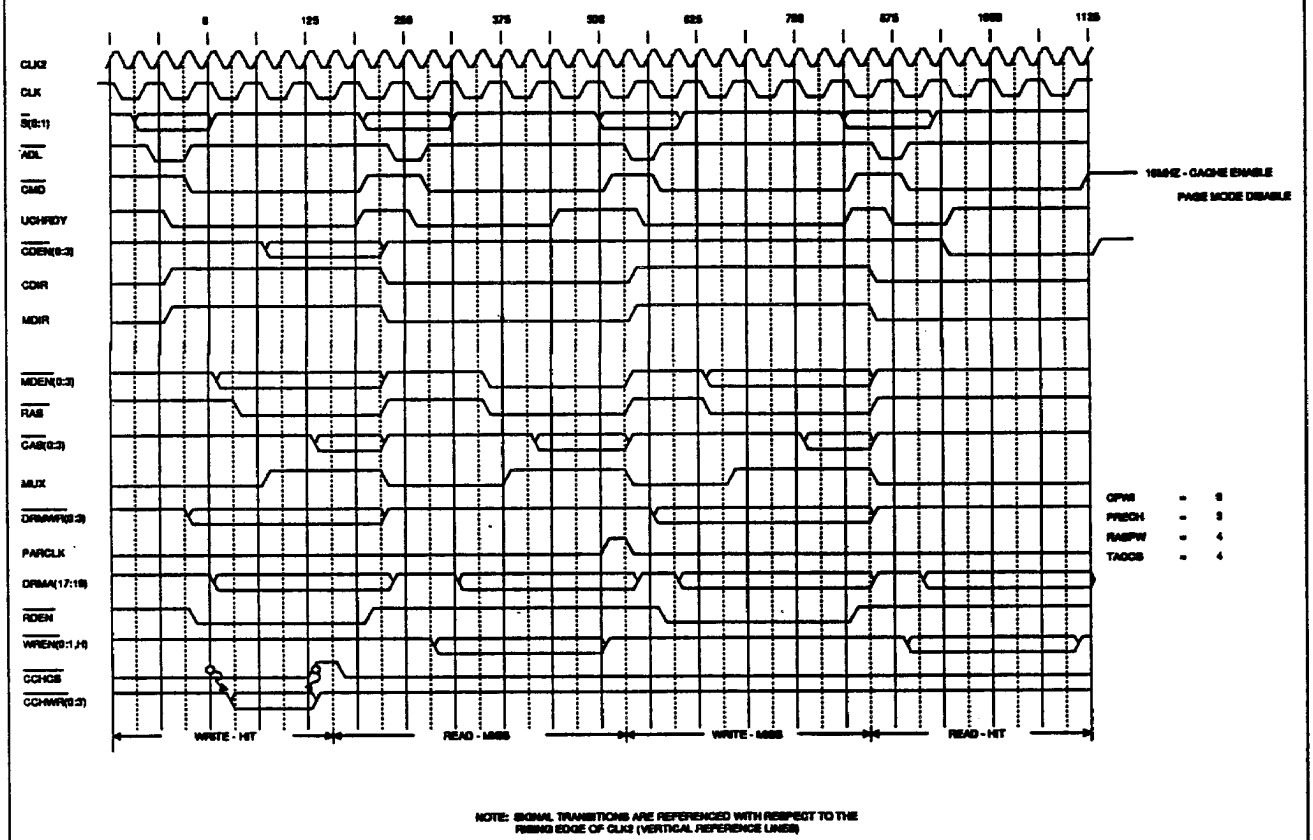

Figure 8. Channel Master Accesses to System Brd DRAM-III

2.0 DRAM CONTROLLER

2.1 MEMORY ORGANIZATION

The FE6030 supports up to four banks of DRAMs, each consisting of thirty-six bits, with each byte having an associated parity bit. The total memory capacity on the system board is dependent on the type of memory used and the number of banks populated, and could range from 1 MB to 64 MB. Table 3 lists the memory size options that are available.

DRAM TYPE	MEMORY CAPACITY
256K x 1	1 MB x (Number of Banks)
1 M x 1	4 MB x (Number of Banks)
4 M x 1	16 MB x (Number of Banks)

Table 3. Memory Size Options

The Model 80-071 provides two banks, each with 1 MB of memory. The Model 80-111 has two banks of 2 MB each. The FE6030 default setting at power-up is compatible with the Model 80-071 and Model 80-111: two 1 MB memory banks. The Extended Setup Facility feature can be used to enable more memory on the board.

Each of the banks can be enabled or disabled by programming the Memory Configuration register. In addition, banks can be swapped, in order to map around defective memory banks.

The FE6030 permits DRAMs of different sizes to be used in the four banks. However, all the DRAMs within a bank should be of the same size. For example, if Bank 0 were composed of 1 M x 1 DRAMs, Bank 1 of 256 K x 1 DRAMs, and Banks 2 and 3 were unpopulated, this would be a valid use of different-sized DRAMs. Certain restrictions that apply to mixing DRAM sizes should be noted carefully:

- The FE6030 does not support Page Mode operation when DRAMs of different sizes are used in different banks; therefore, in such cases, the DRAMs must be set in Forced Row Misses Mode through the Memory Configuration register. This will result in degraded performance when compared to Page Mode operation for the DRAMs.
- When using a mixture of DRAM sizes, always place the larger-sized DRAMs in the lower banks, or the system will not function. A system populating three banks with 4 M x 1, 1 M x 1, and 256 K x 1 DRAMs should organize them such that Bank 0 consists of 4 M x 1, Bank 1 of 1 M x 1, and Bank 2 of 256 K x 1 DRAMs, with Bank 3 unpopulated.
- When DRAMs of different sizes are used together and the Split RAM is placed in the memory map, the BIOS must ensure that the split RAM starting address is located at an address that is a multiple of the largest DRAMs. Thus, for 4 M x 1 DRAMs, it should be located at a 16 Mbyte boundary, for 1 M x 1 DRAMs at a 4 Mbyte boundary, for 256K x 1 DRAMs on a 1 Mbyte boundary. See Section 2.1.2.4 for further information.

When the DRAMs are used in Page Mode, the following address assignments should be used for the external multiplexers. REF refers to the addresses for Refresh Cycles. The DA bus is the address bus for the physical DRAM. RAS, CAS, and REF are from the MA or Latched Memory Addresses Bus.

256 K x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8		
CAS	2	3	4	5	6	7	9	10	8		
RAS	11	12	13	14	15	16	17	18	19		
REF	2	3	4	5	6	7	0	1	X		
1 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	
CAS	2	3	4	5	6	7	8	10	11	9	
RAS	20	21	13	14	15	16	17	18	19	12	
REF	2	3	4	5	6	7	8	0	1	X	
4 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	10
CAS	2	3	4	5	6	7	8	9	10	11	12
RAS	20	21	13	14	15	16	17	18	19	22	23
REF	2	3	4	5	6	7	8	9	0	1	X

Table 4. Page Mode DRAM Address Assignments

When DRAMs of different sizes are used in the banks, the following address assignments are recommended for use with the external multiplexers. Other address assignments may be used; however, care should be taken to ensure that the addressing for the smaller DRAMs is a subset of the addressing for the larger DRAMs, so that the DRAMs are addressed correctly even though different sizes are used in different banks.

The DA bus is the address bus for the physical DRAMs. The address bits for RAS, CAS, and REF are from the MA bus. REF refers to the addresses for Refresh cycles.

2.1.1 Memory Maps

The first 640 K of memory is used for system RAM. Additional banks of RAM are mapped in contiguous blocks, starting at 1 MB. The 256/384 K of extra RAM from the first 1 MB is the Split RAM, and is remapped to the top of the last block of memory on the system after the BIOS has determined the total memory size. Tables 6 to 15 provide memory maps for a typical system. In tables 6 through 13, A represents the amount, in Mbytes, of system board memory installed and enabled, starting at 00000000H; B represents the amount, in Mbytes, of memory available on the Channel, starting at or above 000100000H.

256 K x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8		
CAS	2	3	4	5	6	7	9	10	8		
RAS	11	12	13	14	15	16	17	18	19		
REF	2	3	4	5	6	7	0	1	X		
1 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	
CAS	2	3	4	5	6	7	9	10	8	20	
RAS	11	12	13	14	15	16	17	18	19	21	
REF	2	3	4	5	6	7	0	1	8	X	
4 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	10
CAS	2	3	4	5	6	7	9	10	8	20	22
RAS	11	12	13	14	15	16	17	18	19	21	23
REF	2	3	4	5	6	7	0	1	8	9	X

Table 5. Addresses For Different Sized DRAMs

ENSPLIT = 1 **640 = 1.** **ROMEN = 1** **Split Address = Disabled**	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0007FFFFH	512 K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128 K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 6. Memory Map 1

ENSPLIT = 1 640 = 0 ROMEN = 1 Split Address = Disabled	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0009FFFFH	640 K System Board RAM
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128 K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 7. Memory Map 2

ENSPLIT = 0 640 = 1 ROMEN = 1 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0007FFFFH	512 K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+384K)	384 K System Board RAM
(00100000+A+B+384K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128 K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 8. Memory Map 3

ENSPLIT = 0 640 = 0 ROMEN = 1 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0009FFFFH	640 K System Board RAM
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+256K)	256 K System Board RAM
(00100000+A+B+256K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128 K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 9. Memory Map 4

ENSPLIT = 1 640 = 1 ROMEN = 0 Split Address = Disabled	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0007FFFFH	512 K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128 K System Board ROM

Table 10. Memory Map 5

ENSPLIT = 1 640 = 0 ROMEN = 0 Split Address = Disabled	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0009FFFFH	640 K System Board RAM
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128 K System Board ROM

Table 11. Memory Map 6

ENSPLIT = 0 640 = 1 ROMEN = 0 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0007FFFFH	512 K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board RAM
00100000 - (00100000+A)	System Board RAM
0100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+384K)	384 K System Board RAM
(00100000+A+B+384K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128 K System Board ROM

Table 12. Memory Map 7

ENSPLIT = 0 640 = 0 ROMEN = 0 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	FUNCTION
00000000 - 0009FFFFH	640 K System Board RAM
000A0000 - 000BFFFFH	128 K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128 K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+256K)	256 K System Board RAM
(00100000+A+B+256K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128 K System Board ROM

Table 13. Memory Map 8

2.1.2 MEMORY CONFIGURATION

The tables in this section describe the format of the ESF and I/O registers that are used to configure memory on the system board. Note that the registers on the FE6030 can only be accessed by the 80386 microprocessor. In this description of the registers that can be written to, bits marked RESERVED should always be written with zeros; this will ensure compatibility with future Western Digital products.

2.1.2.1 Memory Control Register 0103H (W/O)

The Memory Control Register is implemented in the FE6000. At power-on, a refresh rate compatible with that of the Model 80, 0.8 µs refreshes, is selected, but the BIOS later changes this to 15.1 µs.

Bit 0	Reserved
Bit 1	$\overline{\text{FREF}}$ Fast Refresh 0 = Refresh of 0.8 µs 1 = Refresh of 15.1 µs
Bits 2-7	Reserved

(Power-on Default = 00000000)

Table 14. Memory Control Register

2.1.2.2 Memory Card Definition Register 0103H (R/O)

In the Western Digital chip set, this register is implemented in the FE6000. The power-on default, 256 K x 1 DRAMs, is compatible with both the 80-071 and the 80-111.

Bits 0, 1	R1, T1 00 - 1 MB RAM in Connector 1 10 - 2 MB RAM in Connector 1 X1 - No RAM (Should be at least 1 MB)
Bits 2, 3	R2, T2 00 - 1 MB RAM in Connector 1 10 - 2 MB RAM in Connector 1 X1 - No RAM
Bits 4-7	1 = Reserved

(Power-on Default = 11110000)

Table 15. Memory Card Definition Register

The IBM Memory Card Definition register is implemented on the Model 80 to detect the presence of two memory modules on the system board.

This register treats memory on the system board as being installed in two connectors. The Model 80-071 has connectors with 1 MB each; the Model 80-111 connectors can have up to 2 MB. Bits T1 and R1 are the encodings for Connector 1, and Bits T2 and R2 are the encodings for Connector 2. Some bits that were reserved on the 80-071 have been coded on the 80-111, but are compatible with the 80-071.

There are certain differences between the Western Digital and IBM implementations of this register. The Western Digital Memory Card Definition register does not support the detection of memory connectors, so it always indicates 11110000. Further, it views the system

board memory sequentially in four banks of 1 MB, 4 MB, or 16 MB each. However, to maintain compatibility with the Model 80, at power-up the 256 K x 1 DRAMs are mapped to correspond to the IBM connector mappings. In Model 80 Compatibility Mode (256K x 1 DRAMs), the following mapping is used:

W D-Implementation	IBM Model 80 Implementation
Bank 0	Lower 1 MB of Connector 1
Bank 2	Upper 1 MB of Connector 1
Bank 1	Lower 1 MB of Connector 2

Table 16. Model 80 Compatibility Mode

Bit 0	ENPLRPCH 0 - Enable Parity Checking of DRAM 1 - DisableParityCheckingof DRAM
Bit 1	ROMEN 0 - ROM Address Space (E0000-FFFFFH) in DRAM 1 - ROM Address Space in ROM
Bit 2	SIX40 0 - First Meg Split at 640 K 1 - First Meg Split at 512 K
Bit 3	ENSPLIT 0 -Split Memory Mapped by Split Address Register 1 - Split Memory Disabled
Bits 4-5	$\overline{EN01}$, $\overline{EN02}$ 00 - 2 MB Enabled in Connector 1 10 - First 1 MB Disabled in Connector 1 01 - 1 MB Enabled in Connector 1 11 - Invalid (Memory Disabled in Connector 1)
Bits 6-7	- Reserved

(Power-on Default = 11101011)

Table 17. Memory Encoding Register 1

2.1.2.3 Memory Encoding Register 1 00E1H And Shadow RAM

The bit encodings of this register on the 80-071 and the 80-111 differ, requiring several extra I/O writes to make the 80-111 compatible with the 80-071.

Western Digital implements this register on the FE6030 with all the bits being read/write. The register is compatible with the 80-111. Bit 0, ENPLRPCH, is duplicated on the FE6010, where it is a write-only bit used to control the ENPCHK signal. Table 17 shows the bit assignment for this register.

This register implements the Shadow RAM function and controls the copying of ROM to RAM, and the subsequent execution out of RAM.

When ROMEN is one, all read accesses are directed to the ROM, and all write accesses are directed towards the RAM. When it is zero, all read accesses are directed to the RAM, and write accesses are directed to the Channel, where they are ignored. Physical RAM locations E0000H-FFFFFH are always reserved for this purpose.

To use the Shadow RAM, execute the following steps:

1. Set ROMEN to one.

2. Read Locations E0000 - FFFFFH, and write to the same locations. This copies the ROM code to the RAM.

3. Set ROMEN to zero. The code will now execute out of RAM.

NOTE
Do not perform any ESF operations while these three steps are being executed, as the ESF register may be corrupted.

Table 18 details different memory configurations generated under the combinations of ENSPLIT, SIX40 and ROMEN.

ENSPLIT	ROMEN	SIX40	CONFIGURATION
0	0	0	ROM Disabled. 256 KB at Split Address
0	1	0	ROM Enabled. 256 KB at Split Address
0	0	1	ROM Disabled. 384 KB at Split Address
0	1	1	ROM Enabled. 384 KB at Split Address

Table 18. ENSPLIT, SIX40, and ROMEN Memory Configurations

2.1.2.4 Memory Encoding Register 2 00E0H

The bit encodings of this register on the 80-071 and the 80-111 differ, requiring several extra I/O writes to make the 80-111 compatible with the 80-071.

Western Digital implements this 80-111-compatible register on the FE6030. Bits 0 - 3 of this register define the starting address for the Split Memory, and should not be set to zero unless ENSPLIT is one. The Split Address can be used in conjunction with the Split Address Extension Register to map the Split Memory anywhere in the 4 Gigabyte memory space with the following restriction: the split memory should always be remapped at an address that is a multiple of the largest bank size, for example, with 1 M x 1 DRAMs, it should be remapped at a 4 MByte boundary. Table 19 contains the bit assignments for this register.

Bit 0	SPA20 Split Address 20
Bit 1	SPA21 Split Address 21
Bit 2	SPA22 Split Address 22
Bit 3	SPA23 Split Address 23
Bits 4-5	$\overline{EN11}$, $\overline{EN12}$ 00 - 2 MB Enabled in Connector 2 10 - First 1 MB Disabled in Connector 2 01 - 1 MB Enabled in Connector 2 11 - Invalid (Memory Disabled in Connector 2)
Bits 6-7	1 - Reserved

(Power-on Default = 11100010)

Table 19. Memory Encoding Register 2

The Western Digital implementation of the memory encoding registers differs from the IBM implementation. Bits 4 and 5 of these registers ($\overline{EN12}$, $\overline{EN11}$, $\overline{EN01}$, $\overline{EN02}$) are only applicable when all the banks are populated with 256 K x 1 DRAMs, the IBM-compatible power-on default. When other DRAMs are used, the encodings in Table 20 are used. In this table, the "x" in $\overline{ENx2}$ and $\overline{ENx1}$ indicates either a zero or a one.

2.1.2.5 Split Address Extension Register ESF:0183H

This register is another of Western Digital's enhancements and is accessed through the Extended Setup Facility. It is used in combination with the Split Address Register to relocate the Split Address at any 1 MByte boundary in the 4 Gigabyte memory address space of the 80386. Most systems will place the split address above the Channel adapter memory in the memory map. Table 21 contains the bit assignment for this register.

Bit 0	- Split Address Bit 24
Bit 1	- Split Address Bit 25
Bit 2	- Split Address Bit 26
Bit 3	- Split Address Bit 27
Bit 4	- Split Address Bit 28
Bit 5	- Split Address Bit 29
Bit 6	- Split Address Bit 30
Bit 7	- Split Address Bit 31

(Power-on Default = 00000000)

Table 21. Split Address Extension Register

REGISTER	$\overline{ENx2}$	$\overline{ENx1}$	FUNCTION
00E1	0	0	Bank 0 Enabled
	1	1	Bank 0 Disabled
	0	1	Reserved
	1	0	Reserved
00E0	0	0	Bank 1 Enabled
	1	1	Bank 1 Disabled
	0	1	Reserved
	1	0	Reserved

Table 20. DRAM Encodings

2.1.2.6 Bank Enable Register ESF:0182H

This read/write register is a Western Digital enhancement, and does not exist on the Model 80. It disables or enables Memory Banks 2 and 3. Table 22 provides the bit assignment for this register.

Bits 0, 1	$\overline{EN22}$, $\overline{EN21}$ 00 - Enables Bank 2 11 - Disables Bank 2 10 - Reserved 01 - Reserved
Bits 2, 3	$\overline{EN32}$, $\overline{EN31}$ 00 - Enables Bank 3 11 - Disables Bank 3 01 - Reserved 10 - Reserved
Bits 4-7	Reserved

(Power-on Default = 00001111)

Table 22. Bank Enable Register

2.1.2.7 Memory Size Register ESF:0181H (R/W)

This register is another Western Digital enhancement that does not exist on the Model 80. It indicates the type of DRAM chips being used in the memory banks, information that is used internally to implement the memory maps. The software must initialize these bits appropriately, as outlined in Section 2.1.3. Table 23 shows the bit assignment; all the bits are read/write.

Certain points must be kept in mind when using this register.

- When the system integrator uses different-sized DRAMs in the memory banks, the software programming and the hardware must ensure that the larger DRAMs are always placed in the lower banks, and the smaller DRAMs placed in the higher banks.
- To get the best performance from the system, Page Mode DRAMs should be used in Page Mode; this mode requires the system to have DRAMs of the same size in all the banks.

Bits 0, 1	- MSIZ00, MSIZ01 Memory Size in Bank 0 00 - 256 K x 1 DRAMs 10 - 1 M x 1 DRAMs 11 - 4 M x 1 DRAMs 01 - Reserved
Bits 2, 3	- MSIZ00, MSIZ01 Memory Size in Bank 1 00 - 256 K x 1 DRAMs 10 - 1 M x 1 DRAMs 11 - 4 M x 1 DRAMs 01 - Reserved
Bits 4, 5	- MSIZ00, MSIZ01 Memory Size in Bank 2 00 - 256 K x 1 DRAMs 10 - 1 M x 1 DRAMs 11 - 4 M x 1 DRAMs 01 - Reserved
Bits 6, 7	- MSIZ00, MSIZ01 Memory Size in Bank 3 00 - 256 K x 1 DRAMs 10 - 1 M x 1 DRAMs 11 - 4 M x 1 DRAMs 01 - Reserved

(Power-on Default = 00000000)

Table 23. Memory Size Register

2.1.2.8 Memory Window Bank 0 Register ESF:0184H (R/W)

This register is another Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 0 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256 K x 1, 1 M x 1, and 4 M x 1 DRAMs, it relocates Memory Bank 0 at a 1 MByte boundary, a 4 MByte boundary and a 16 MByte boundary respectively, in the processor address space.

To program any of the Memory Window registers correctly, the software must make sure that the address remapping does not cause any address conflicts. This means that it has to account for the size of the DRAMs installed in the banks, and must program the register so that Bank 0 has unique addresses.

Table 24 details the bit assignment for this register. Note that only the combination of bits indicated by the vertical bars in the table needs to be programmed for the different DRAM sizes. This applies to the other memory window registers as well, described in Sections 2.1.2.9 - 2.1.2.11.

Bit 0	- Address Bit 20
Bit 1	- Address Bit 21
Bit 2	- Address Bit 22
Bit 3	- Address Bit 23
Bit 4	- Address Bit 24
Bit 5	- Address Bit 25
Bits 6, 7	- Reserved

Power-on Default = 00000000 (256 K x 1 DRAMs)

Table 24. Memory Window Bank 0 Register

2.1.2.9 Memory Window Bank 1 Register ESF:0185H (R/W)

This register is another Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 1 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256 K x 1, 1 M x 1, and 4 M x 1 DRAMs, it relocates Memory Bank 1 at a 1 MByte boundary, a 4 MByte boundary and a 16 MByte boundary respectively, in the processor address space. Table 25 details the bit assignment for this register.

Bit 0	- Address Bit 20
Bit 1	- Address Bit 21
Bit 2	- Address Bit 22
Bit 3	- Address Bit 23
Bit 4	- Address Bit 24
Bit 5	- Address Bit 25
Bits 6, 7	- Reserved

Power-on Default = 00000001 (256 K x 1 DRAMs)

Table 25. Memory Window Bank 1 Register

2.1.2.10 Memory Window Bank 2 Register ESF:0186H (R/W)

This register is a Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 2 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256 K x 1, 1 M x 1, and 4 M x 1 DRAMs, it relocates Memory Bank 2 at a 1 MByte boundary, a 4 MByte boundary and a 16 MByte boundary respectively, in the processor address space.

Table 26 details the bit assignment for this register.

Bit 0	- Address Bit 20
Bit 1	- Address Bit 21
Bit 2	- Address Bit 22
Bit 3	- Address Bit 23
Bit 4	- Address Bit 24
Bit 5	- Address Bit 25
Bits 6, 7	- Reserved

Power-on Default = 00000010 (256 K x 1 DRAMs)

Table 26. Memory Window Bank 2 Register

2.1.2.11 Memory Window Bank 3 Register ESF:0187H (R/W)

This read/write register is a Western Digital enhancement, accessed through the ESF. It relocates Memory Bank 3 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256 K x 1, 1 M x 1, and 4 M x 1 DRAMs, it relocates Memory Bank 3 at a 1 MByte boundary, a 4 MByte boundary and a 16 MByte boundary respectively, in the processor address space.

While re-mapping banks, the software should ensure that no holes are created in memory, and that the system board memory always starts at Address 00000000H. Further, all system board memory should be placed contiguously in the memory map. The only exception is the split addresses, which are placed contiguously above the Channel RAM. Table 27 details the bit assignment for this register.

Bit 0	- Address Bit 20
Bit 1	- Address Bit 21
Bit 2	- Address Bit 22
Bit 3	- Address Bit 23
Bit 4	- Address Bit 24
Bit 5	- Address Bit 25
Bits 6, 7	Reserved

Power-on Default = 00000011 (256 K x 1 DRAMs)

Table 27. Memory Window Bank 3 Register

2.1.2.12 Memory Configuration Register ESF:0180H

This register is a Western Digital ESF enhancement. It controls the enabling and disabling of the cache and Page Mode for the DRAMs. Table 28 details the bit assignment for this register.

Bit 0	FMISS Cache Forced Miss 0 - Cache Operating in Normal Mode 1 - Cache Operating in Forced Misses Mode
Bits 1-3	Reserved
Bit 4	FRMISS Forced Row Miss 0 - DRAMs Operating in Page Mode 1 - DRAMs Operating in Normal RAS/CAS Mode
Bits 5-6	Reserved
Bit 7	RASTMOUT RAS Time-out 0 - 10 microseconds RAS Time-out Disabled 1 - 10 microseconds RAS Time-out Enabled

Power-on Default = 00010001

Table 28. Memory Configuration Register

At power-on, the software must read the Memory Size Register and ensure that all the banks have DRAMs of the same size before setting Bit 4, FRMISS, to zero. When the cache is set for Forced Misses at power-up to ensure proper cache initialization, read data for the Memory Read cycle comes from the DRAM, and writes go to the DRAM. The TagRAM and cache are updated on each Read Miss. When the DRAMs are set in Forced Row Misses, the DRAMs are not operated in Page Mode, and a RAS/CAS precharge is performed for every DRAM cycle. This mode should be used if there are no Static Column or Page Mode DRAMs being used in the system.

When Bit 7, RASTMOUT, is set, it enables an internal timer, which monitors the length of the NRAS pulse and precharges it every 10 µs. The bit must be set for DRAMs requiring the maximum pulse width on NRAS to be less than or equal to 10 microseconds. Do not however, enable Bit 7 for DRAMs that do not require it, as this will degrade memory performance. The approximate RAS time-out periods at different operating frequencies is tabulated below.

FREQ.	APPROXIMATE RAS TIME-OUT PERIOD
16 MHz	9 µS
20 MHz	8.8 µS
25 MHz	8.96 µS

Western Digital allows memory performance to be fine-tuned to the CPU frequency through a series of Memory Timing Registers which allow the critical DRAM parameters in the memory cycle to be directly programmed. This enables DRAMs with different parameters, including different access times, to be used. The memory wait states obtained are a result of this programming and can not be explicitly programmed. The system's primary (CLK2) and phase clock (CLK) signals provide the time granularity for programming. Refer to Section 2.3, Timing Configuration, for further details on programming.

2.1.2.13 CAS Pulse Width Register ESF:0188H

This read/write register is another Western Digital ESF enhancement; Table 29 describes its format.

Bit 0	- CPW0 CAS Pulse Width from 386/DMA cycles 0 - Pulse Width = 2CLK 1 - Pulse Width = 3CLK
Bit 1	- CPW1 CHRDY Assertion for UCH Master Cycle 0 - CHRDY re-asserted from CAS leading edge 1 -CHRDY re-asserted CLK2 after leading edge
Bits 2-7	- Reserved

(Power-on Default = 00000011)

Table 29. CAS Pulse Width Register

Bit 0 programs the CAS pulse width for DRAM read cycles when the DRAM being used has a CAS access time greater than 35 ns, or when the system is using 100 ns DRAMs and is being run at a frequency higher than 25 MHz. DRAM write cycles can not be programmed. The programming of this bit determines the number of wait states to be provided by the FE6030 wait state generator. In the following, CLK denotes the frequency of the processor clock.

BIT 0	CAS PULSE WIDTH FOR READS	CPU WS WITH PAGE HIT
0	2CLK	1
1	3CLK	2

When a Channel master performs a read to system board memory and a page hit occurs, Bit 1 extends the cycle if the DRAM being used has a CAS access time greater than 35 ns, or when the system is using 100 ns DRAMs and is being run at a frequency higher than 25 MHz. DRAM write cycles can not be programmed. Bit 1 (CPW1) also controls the re-assertion of CHRDY, as shown in this table. Note that CLK2 in this table denotes a frequency twice that of the processor.

BIT 1	CHRDY RE-ASSERTION
0	CHRDY re-asserted at the leading edge of CAS
1	CHRDY re-asserted CLK2 after the leading edge of CAS

2.1.2.14 RAS Precharge Delay Register ESF:0189H (R/W)

This register is another Western Digital ESF enhancement, which permits the RAS precharge time to be programmed in CLK2 (twice the processor frequency) increments to suit the type of DRAM being used. The range extends from a minimum delay of 2CLK2 (62.5 ns at 16 MHz) up to a maximum of 6CLK2 (120 ns at 25 MHz).

Bits 0-2	PREC (2:0) RAS Precharge 000 - 2CLK2 001 - 3CLK2 010 - 4CLK2 011 - 5CLK2 100 - 6CLK2 101 - Reserved 110 - Reserved 111 - Reserved
Bits 3-7	Reserved

(Power-on Default = 00000100)

Table 30. RAS Precharge Delay Register

2.1.2.15 RAS Pulse Width Register ESF:018AH (R/W)

This register is a Western Digital ESF enhancement, which permits the RAS pulse width to be programmed and tailored to the DRAM. The pulse width obtained in actual operation is equal to or greater than the programmed value. It can range from 3CLK2 (93.75 ns at 16 MHz) to 7CLK2 (140 ns at 25 MHz).

Bits 0-2	RPW (2:0) RAS Pulse Width 000 - 3CLK2 001 - 4CLK2 010 - 5CLK2 011 - 6CLK2 100 - 7CLK2 101 - Reserved 110 - Reserved 111 - Reserved
Bits 3-7	Reserved

(Power-on Default = 00000100)

Table 31. RAS Pulse Width Register

2.1.2.16 RAS Access Time Register ESF:018BH (R/W)

This register is a Western Digital ESF enhancement; it programs the RAS pulse width to meet the DRAM RAS access times. The pulse widths can range from 4CLK2 (125 ns at 16 MHz) up to a maximum of 9CLK2 or (180 ns at 25 MHz). Actual pulse widths will be equal to or greater than the value programmed.

Bits 0-2	ACC (2:0) RAS Pulse Width due to access time 000 - 4CLK2 001 - 5CLK2 010 - 6CLK2 011 - 7CLK2 100 - 8CLK2 101 - 9CLK2 110 - Reserved 111 - Reserved
Bits 3-7	Reserved

(Power-on Default = 00000101)

Table 32. RAS Access Time Register

For Memory Configuration Registers ESF:188, ESF:189, ESF:18A, and ESF 18B (Sections 2.1.2.13 - 2.1.2.16), the software must program these registers appropriately before accessing them if the DRAMs being used have parameters that differ from the default values.

2.1.2.17 System Configuration Register ESF:018FH (R/W)

This read/write register is a Western Digital ESF enhancement that provides configuration data for the system. Bit 0 is used to detect the presence/absence of an optional numeric coprocessor device, Intel's 80387. If it is present, the I/O bus cycles with Address Bit 31 (PA31) set are directed towards the 80387, and the 80387 generates a Ready signal. If the coprocessor is absent, the Ready signal for those bus cycles is generated by the FE6030.

Bit 1 enables/disables the optional Weitek 3167 or compatible coprocessor. When Bit 1 is enabled, memory accesses in the range C0000000 - C000FFFFH are directed to the Weitek coprocessor and the coprocessor generates the Ready signal. When it is disabled, the FE6030 generates the Ready signal for those addresses.

Bits 6 and 7 latch the state of the frequency configuration bits. The software uses this information to determine the speed at which the system is operating.

When the system is powered on, the state of the UCHMSTR, A20GTX and SWPDIR signals is latched into F1, F0 and NCOPRES, respectively.

Bit 0	$\overline{\text{COPRES}}$ 80387 Presence/Absence (R/O) 0 - 80387 Present 1 - 80387 Absent
Bit 1	WTKEN Weitek 1167 Enable/Disable (R/W) 0 - Module Disabled 1 - Module Enabled
Bits 2-5	Reserved
Bits 6-7	F1, F0 Frequency bits (R/O) 00 - 16 MHz 01 - 20 MHz 11 - 25 MHz 10 - Reserved

(Power-on Default = xx00000x)

Table 33. System Configuration Register

The value of "x" in the power-on default above depends on the configuration of the system, and may vary.

2.1.3 Operating Modes

The DRAM controller is optimized for Page Mode DRAMs. They allow one wait state operation on a cache miss if the access was to the same DRAM row, thus keeping the cache miss overhead low.

The first cache miss takes two wait states, but subsequent misses only take one wait state, because of the operation of the 80386 and the FE6010 in Pipelined Mode.

Page Mode and ordinary RAS/CAS DRAMs are also supported. Note that the Static Column Mode should be turned off in the DRAM controller when using RAS/CAS DRAMs, or degraded performance could result.

The system requires 100 ns DRAMs. Faster DRAMs can be used, but all accesses to the DRAMs will still take at least one wait state because of the use of the cache.

2.2 MEMORY INITIALIZATION

The system power-on default configuration follows:

- 1 MByte per bank
- Banks 0 and 1 enabled; all other banks disabled
- Split Address at 000100000H
- ROM enabled through Memory Encoding Register 1
- Split Memory enabled through Memory Encoding Register 1
- 640 enabled through Memory Encoding Register 1
- Page Mode disabled
- Cache disabled
- 80386 in Protected Mode at power-on

The following steps describe one possible way to initialize the system board DRAM in a system using a mixture of DRAM sizes.

1. Determine the first bank in the system, which contains Addresses 00000000 - 0007FFFFH.

To determine the bank, enable Bank n (0, 1, 2 or 3) and disable the others. Execute a RAM test on the first 512 K. If the test passes, Bank n is the first bank. If it fails, disable that bank, and identify it as a failed bank. Repeat the test with the next bank, until you find a bank that passes the test. If all the banks fail the test, the system is non-functional.

2. Determine the size of the DRAMs in the first bank that passes the RAM test.

> **NOTE**
> If any portion of a bank is found to be bad, that bank can still be used by setting the memory size bits to the next lower value. For example, if M-Bytes 8-16 are found to be bad with 4 M x 1 DRAMs, set the memory size to 1 M x 1, and use that bank as a 1 M x 1 bank.

Enable Bank n (0, 1, 2, or 3), and disable the others. Set the Memory Window Bank n register to 0000H, and set the memory size bits for the bank to 256 K x 1.

Do a RAM test on the first MByte.
FAIL - Bank is bad; disable it
PASS ↓
Set the memory size bits to 1 M x 1
FAIL - Bank is bad; disable it
PASS ↓
Do a RAM test on Mbytes 0-4
FAIL - DRAMs in this bank are 4 M x 1
PASS ↓
Set the memory size bits to 4 M x 1
Do a RAM test on Mbytes 0 - 16
FAIL - DRAMs are 1 M x 1
PASS -Leave the memory size bits at 4 M x 1

By the end of Step 2, the Memory Size register and the Bank Enable bits should have been correctly programmed.

3. Set ROMEN = 1, read Locations 000E0000-000FFFFFH and write to the same addresses. This copies the ROM to the physical DRAM. Then set ROMEN = 0. This directs all read accesses to the RAM, which now holds the contents of the ROM, and also write-protects these RAM locations. The shadow RAM is now in operation.

4. Perform the RAM tests described in Step 2 on each of the remaining untested banks to determine their availability and memory size. If any bank is bad or is unpopulated, re-assign the addresses through the Memory Window registers.

At the end of this step, the memory size bits for all the populated banks should be known. The software should now re-assign the addresses for the banks using the Memory Window registers, and avoiding address conflicts. All the addresses should be contiguous, starting at 00000000H.

5. If the banks are found to contain DRAMs of different sizes, during address assignment the software must ensure that the larger DRAMs are always mapped to the lower banks. If the DRAMs are of the same size, Page Mode can be turned ON through the Memory Configuration register after initializing the cache as described in Section 3.3. The cache may also be turned ON at this point, using the same register.

2.3 TIMING CONFIGURATION

The FE6030 supports DRAMs with different timing parameters by reprogramming the Memory Timing Registers. To facilitate programming, the critical RAM parameters in the memory cycle can be directly programmed. These parameters include RAS access time (ESF:018B), RAS pulse width (ESF:018A), RAS precharge (ESF:0189) and CAS pulse width (ESF:0188). Thus, the system can be programmed for the best memory performance at different CPU and memory speeds.

At power-up, the FE6030 defaults to the largest value of each parameter so as to accomodate the slowest RAMs. The Memory Timing Registers must then be reprogrammed by the BIOS to extract the best possible performance from the system.

The FE6030 automatically inserts the wait states to satisfy all the programmed parameters. The wait states in the system can not be explicitly programmed.

The minimum time granularity for programming is the primary clock, CLK2: 20 ns with a 50 MHz CLK2 for a system operating at 25 MHz. Note that the system always operates at half the clock speed. The RAS CAS time is always guaranteed to be 2*CLK2.

Table 34 shows the programming for a typical DRAM.

> **NOTE**
> This is intended as an example only; system designers must complete a full timing analysis of the memory cycles for the DRAMs used in their particular systems.

System Operation 25 MHz CLK2: Frequency= 50 MHz CLK2: Period= 20 ns DRAM: 1 M x 1 Fast Page DRAM	
TIMING	DESCRIPTION
tRAC	RAS Access Time = 100 ns RAS Access Time Register 01H. (Programmed for 5CLK2)
tRAS	RAS Pulse Width = 100 ns (min) 100,000 ns (max) RAS Pulse Width Register 02H. (Programmed for 5CLK2)
tRP	RAS Precharge = 80 ns RAS Precharge Delay Register 02H. (Programmed for 4CLK2)
tCAC	Access Time from CAS = 25 ns CAS Pulse Width Register, Bit 0 = 0. (Programmed for CAS pulse width of 4CLK2 = 80 ns, which ensures that a pipelined one-wait state operation to the DRAM can complete. CAS Pulse Width Register, Bit 0 = 1. CHRDY re-asserted from the leading edge of CAS for Master cycles.
tRCD	RAS to CAS Delay Time = 25 ns (min), 75 ns (max) RAS to CAS Delay = 2CLK2 = 40 ns

Table 34. Typical RAM Program Parameters

3.0 CACHE CONTROLLER

The cache is organized in sets. Each set contains one or more lines, a line being the basic unit of data transfer between the cache and the DRAM. The cache controller in the FE6030 implements a direct-mapped, write-through cache for the 80386 with a line-size of four bytes, that executes 80386 bus cycles, DMA, and Channel master bus cycles. Each set in an FE6030-based system contains one line.

The cache subsystem delivers high performance by ensuring zero wait state cache read-hits, and a low, one wait state miss overhead. Zero wait state access is achieved on a cache read-hit, and cache misses are supported by the Page Mode DRAMs which provide fast, one wait state access for a page hit.

3.1 CACHE ORGANIZATION

The FE6030 implements the cache controller on the chip, but the Tag subsystem is implemented externally to ensure more flexibility in design. The cache controller allows the system designer to determine the amount of DRAM to be cached and the size of the cache according to the cost and performance requirements. A typical cache system uses 64 KBytes of cache, caching 16 MB of DRAM.

To build a direct-mapped cache, the processor addresses are organized in the following manner:

$\overline{BE}$(3:0)

They select the bytes in the line for transfer. A write-hit causes only the selected bytes to be replaced, but a cache update operation executed after a cache miss will replace the entire line.

PA (N:2)

They form the index for the cache and determine which line is to be transferred to the device requesting the transfer. "N" depends on the size of the implemented cache.

PA (M:N+1)

They form the tag for the cache. These bits are compared to the ones stored in the TagRAM for that particular index. If they match bit-for-bit, the requested data lies in the cache. "M" depends on the size of the DRAM being cached. The table below shows the values when 16 Mbytes of DRAM are cached.

CACHE SIZE	TAG	INDEX
32 Kbytes	PA (23:15)	PA (14:2)
64 Kbytes	PA (23:16)	PA (15:2)
128 Kbytes	PA (23:17)	PA (16:2)
256 Kbytes	PA (23:18)	PA (17:2)

Table 35. Typical Cache Values

3.2 CACHE POLICY

The cache policy used in an FE6030-based system is described in Table 36. Only the local DRAM, that is, the DRAM set by the Memory Window registers, is cached. All other bus cycles, such as I/O cycles or accesses to the Channel, are treated as non-cachable areas and are not cached.

80386 BUS CYCLES

TYPE	CACHE HIT	OPERATION
Read	Yes No	Read from cache Read from DRAM, Update cache
Write	Yes No	Write to the cache and DRAM Write to the DRAM only

DMA (FE6010) AND CHANNEL MASTER BUS CYCLES

TYPE	CACHE HIT	OPERATION
Read	Yes No	Read from cache Read from DRAM
Write	Yes No	Write to the cache and DRAM Write to the DRAM only

Table 36. Cache Operation in Different Bus Cycles

3.3 CACHE INITIALIZATION AND DIAGNOSTICS

At power-up, invalid tags are stored in the TagRAMs. These tags in the tag directory must be correctly initialized before the cache can be used. To initialize the tags, the power-up default for the cache controller is Forced Misses Mode. The software reads the cache size data (e.g. 64 Kbytes for a 64 K cache) from the DRAM, and this action updates the cache and tags to their correct values. The cache can then be programmed in Normal Mode and is ready for use.

There are several ways to conduct system-level diagnostics and verify the correct operation of the cache and DRAM in a cache-based system. Examples of software DRAM testing and cache testing follow.

To test the DRAMs, a typical write-read-compare operation can be performed on the data. Before doing this, ensure that the data always comes from the DRAMs, by using the Memory Configuration Register to program the cache to Forced Misses Mode; this directs all read and write accesses to the DRAM. The cache is updated on a read operation, but a write operation does not affect the cache. To prevent the code executing this diagnostic routine from being overwritten in the cache, either make the code ROM-based, or ensure that the area being tested does not overlap the area where the code resides. Then execute the write-read-compare operation:

1. Write a pattern of data.

2. Read it back and compare it.

To test the cache, perform another write-read-compare operation, using the following sequence:

1. Disable the cache by setting it in Forced Misses Mode.

Write Pattern 1: DRAM = Pattern 1, Cache = unknown
Read Pattern 1: DRAM = Pattern 1, Cache = Pattern 1
Write Pattern 2: DRAM = Pattern 2, Cache = Pattern 1

2. Enable the cache by setting it to Normal Mode. Read and compare the results. If it is Pattern 1, the cache is functioning properly. If it shows Pattern 2, it indicates that the Hit/Miss circuitry has failed. Any other pattern indicates that the cache is bad.

3.4 CACHE TIMING

The following table shows the typical speeds for the SRAMs required to build the data cache and the TagRAMs required for zero wait state operation.

NOTE
This is intended as an example only; system designers must complete a full timing analysis of the memory cycles for the SRAMs used in their particular systems.

TIMING/FREQUENCY	16 MHz	20 MHz	25 MHz
Processor Address to HIT generation*	57 ns	47 ns	38 ns
Data Cache SRAM Access Time (Address to data)	64 ns	45 ns	35 ns

*The parameters take into account a 6 ns delay to generate A20 externally.

Table 37. Cache Timing

4.0 CHANNEL CONTROLLER

The Channel Controller on the FE6030 controls the 80386 processor and the DMA accesses to the Micro Channel. Accesses by a Channel master to the system board DRAM are controlled by the DRAM controller in the FE6030. The timings generated by the FE6030 are compatible with the Channel specifications. Figure 9 illustrates a typical 80386 access to the Channel.

Control is provided for default and extended memory or I/O Channel cycles. 8-bit, 16-bit and 32-bit data can be transferred to the Channel. The 80386 always treats a port as being at least sixteen bits wide. Therefore, on an access to an 8-bit port, the FE6030 splits a 16-bit cycle into two cycles and performs any necessary byte swaps. Though the byte-swap is implemented by the FE6022 in Data Buffer Mode, the Channel controller provides the controls for it. It also controls the word swaps, which are necessary when a 16-bit master talks to a 32-bit slave. Figure 10 illustrates a typical byte-swap cycle.

The special timings required by the Channel setup cycles are also implemented by the Channel controller. The Channel Controller also functions as a buffer controller, controlling all data transfers to or from the Channel.

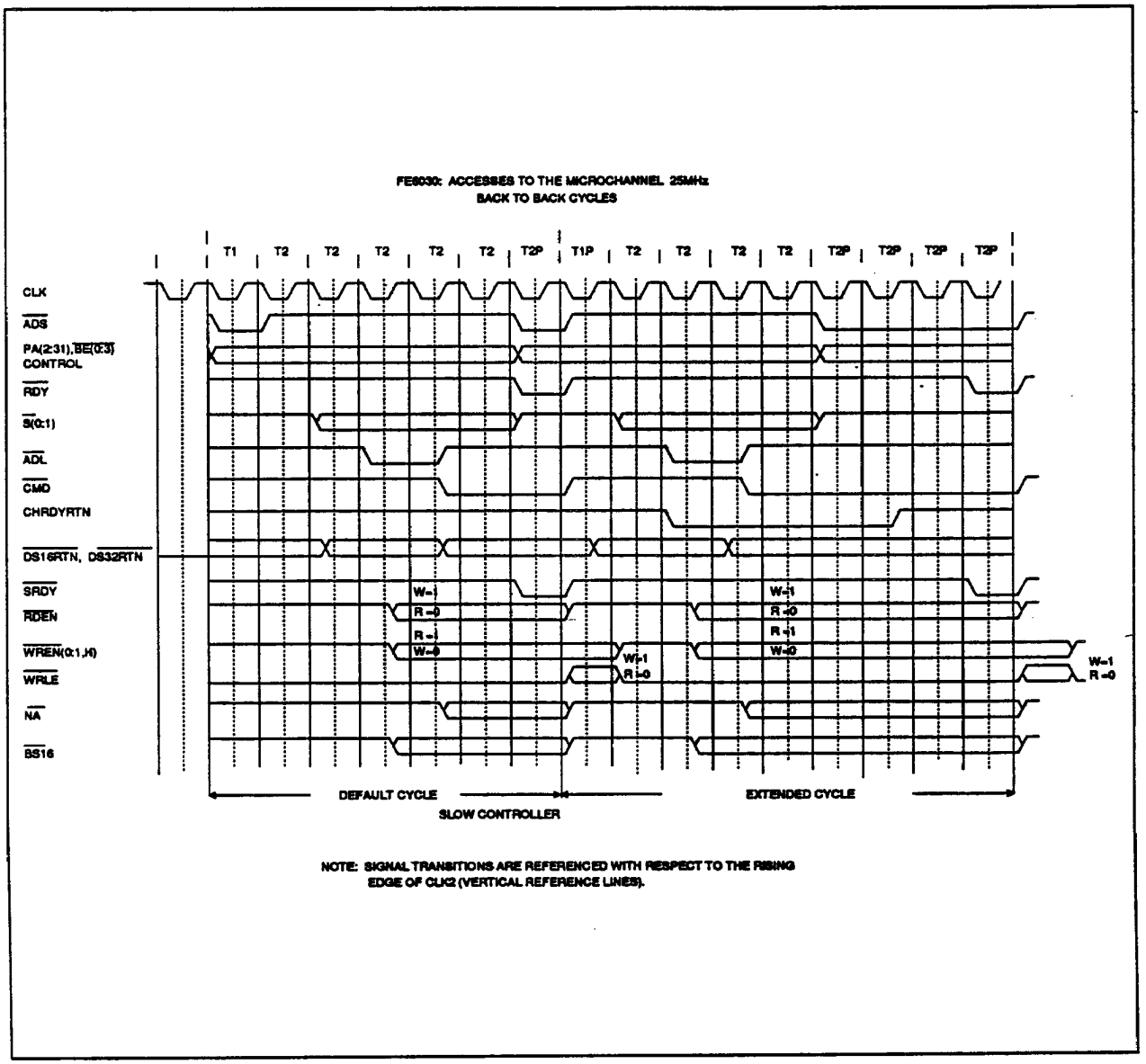

Figure 9. Channel Accesses: 25 MHz Back-to-Back Cycles

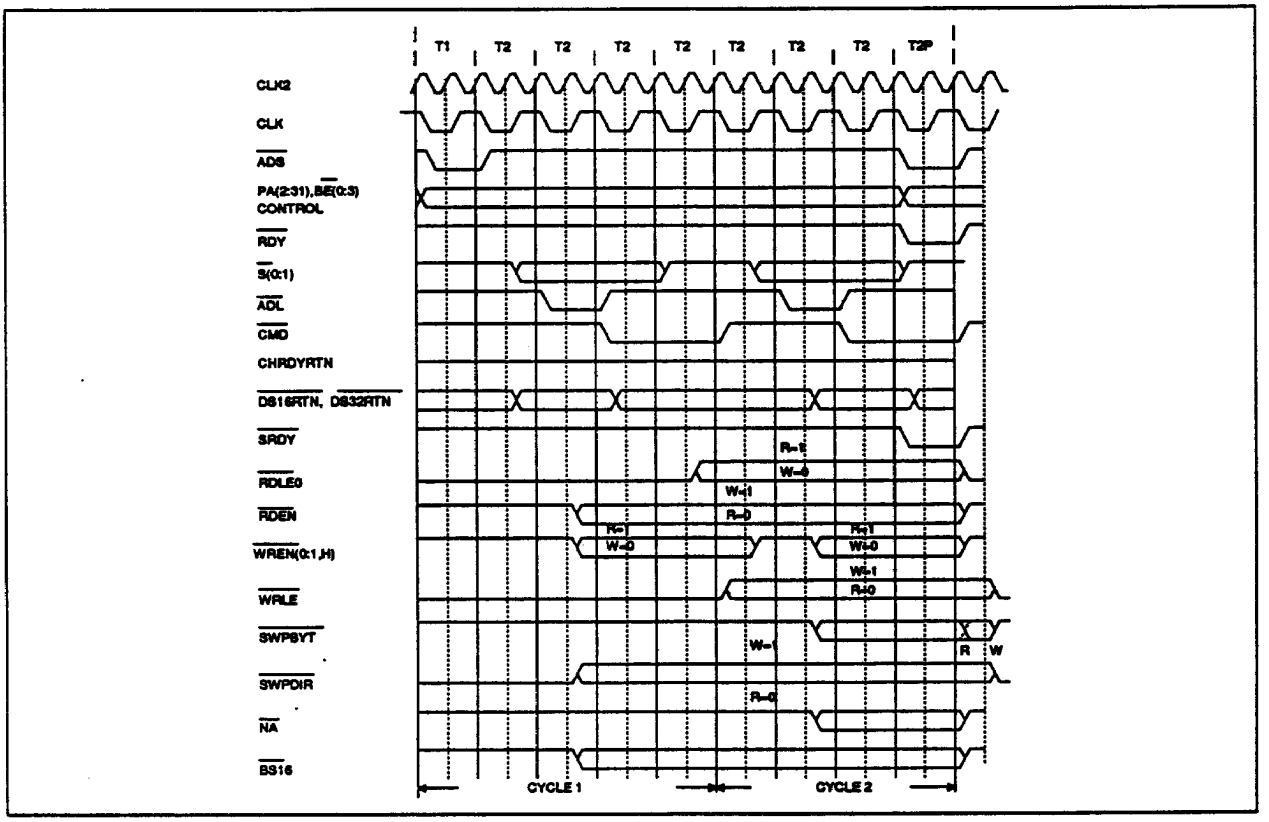

Figure 10. 16-Bit Access to 8-Bit Channel Port: 16 MHz

Since the Channel timings remain constant in a system, the FE6030 determines the speed of the processor and optimizes its Channel bus cycles to match Channel specifications. This allows the controller to support the 80386 processor at different frequencies: 16, 20, and 25 MHz. The speed of the processor is determined by the state of Pins UCHMSTR and A20GTX at power-up. Table 38 supplies a frequency table.

FREQUENCY	UCHMSTR (F1)	A20GTX (F0)
16 MHz	0	0
20 MHz	0	1
25 MHz	1	1

Table 38. Frequency Table

5.0 EXTENDED SETUP FACILITY (ESF)

The Extended Setup Facility (ESF) is a Western Digital enhancement that permits additional functionality to be configured on the board. Based on the concept of "alternate I/O space", it uses memory space that is currently unused on the Model 80 to add more features, or to tailor the board to meet specific needs. The ESF is flexible and can be reprogrammed to other locations if a conflict should arise with future IBM enhancements to the Model 80 design.

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable (NEDRENA) output from the FE6010 to the FE6000. The ESF is designed to extend the configuration architecture established with POS features. Refer to Figures 11 and 12 for an overview of the ESF function. ESF supports:

- System Configuration Registers
- Memory Map Control Registers
- Additional Physical Serial Port (SP2)
- Programmable Port Enables A and B
- EMS Control Registers
- External DRAM Control Configuration
- System Board LAN Configuration
- Customer-specified Enhancements that include:
  System Identification
  System Version

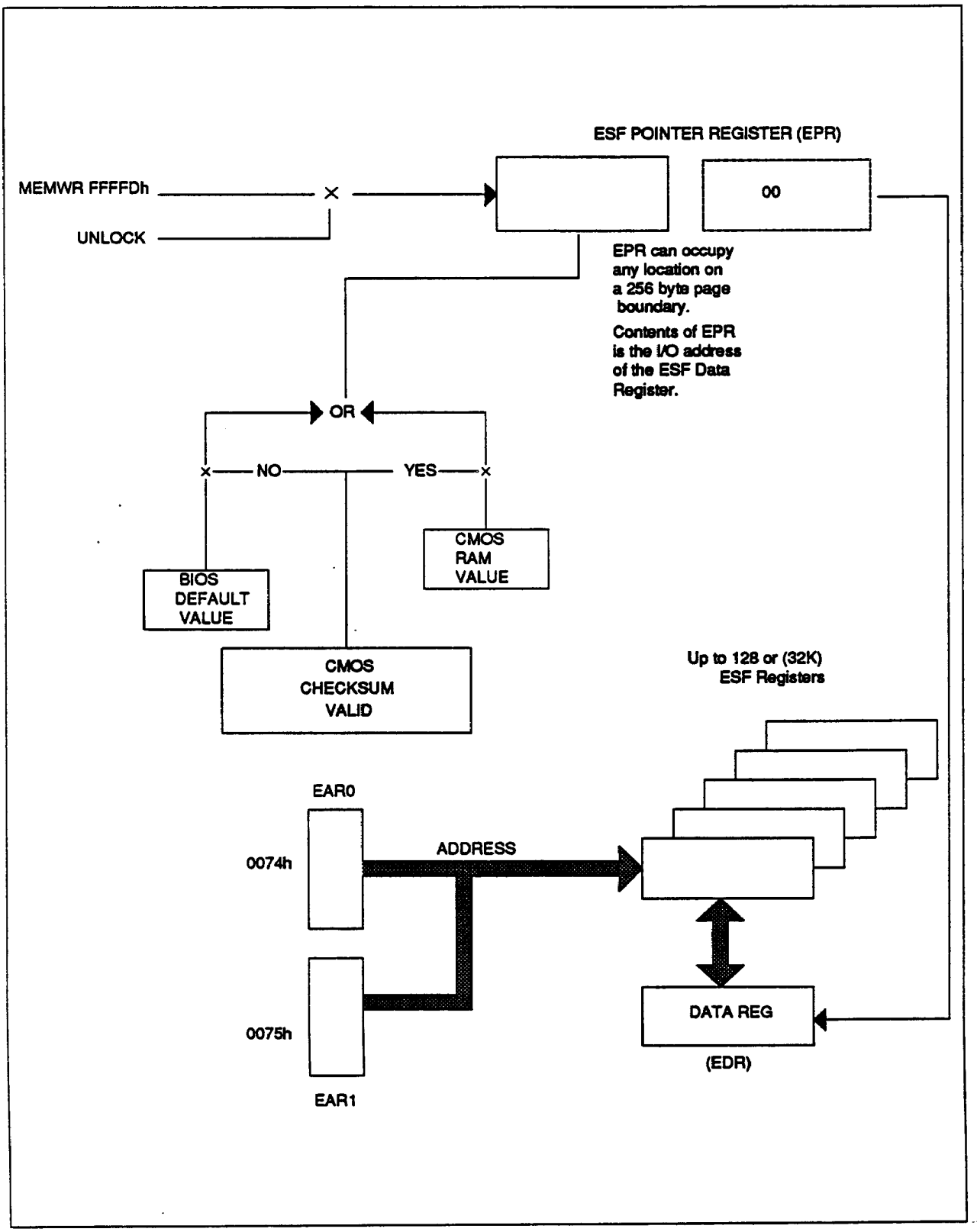

Figure 11. ECR & ESF Block Diagram

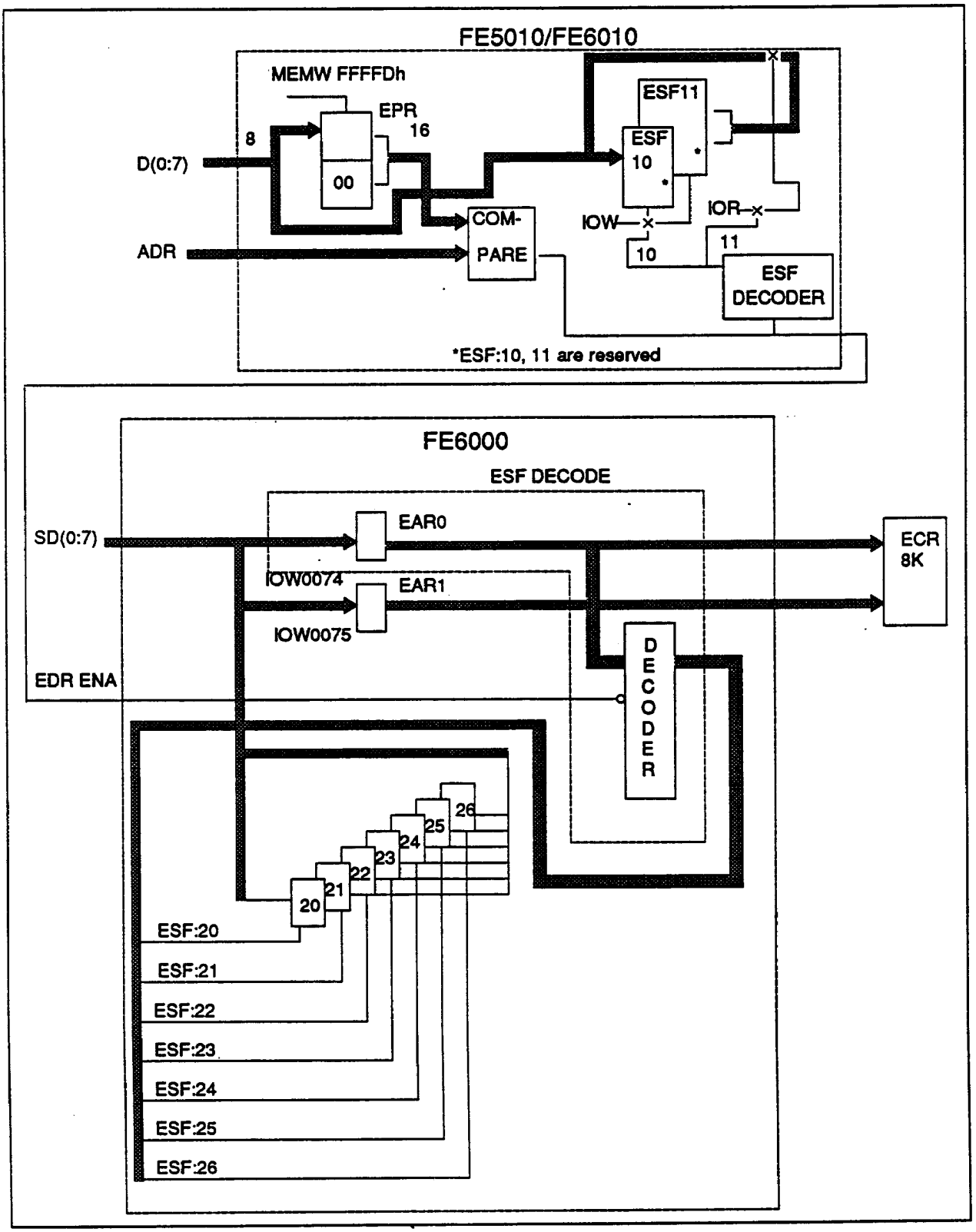

Figure 12. Extended Set-Up Facility Overview

5.1 ESF ADDRESS MAP

The lower sixty-four bytes (EAR0 = 00H - 3FH) of the ESF are reserved for Western Digital functions and features. The upper sixty-four bytes (40H -7FH) can be used by the customer. Refer to Table 39 for details. All functions using ESF must include Bit 7 of EAR0 in the decode. This bit must be zero when addressing only 128 ESF registers. To expand the ESF to Location 32,768, set EAR0 Bit 7 to one and write the second ESF address byte to EAR1.

FUNCTION	ESF ADDRESS	R/W	DEVICE
Reserved	0 - 001FH	-	-
Peripheral Configuration	20H	R/W	FE6000
Port A, B Control	21, 24H	R/W	FE6000
Port A, B Address (LSB)	22, 25H	R/W	FE6000
Port A, B Address (MSB)	23, 26H	R/W	FE6000
Reserved	30 - 3FH	-	-
Customer-specified	40 - 7FH	-	-
Memory Configuration	0180H	R/W	FE6030
Memory Size Register	0181H	R/W	FE6030
Bank Enable Register	0182H	R/W	FE6030
Split Address Extension	0183H	R/W	FE6030
Memory Window Bank 0	0184H	R/W	FE6030
Memory Window Bank 1	0185H	R/W	FE6030
Memory Window Bank 2	0186H	R/W	FE6030
Memory Window Bank 3	0187H	R/W	FE6030
CAS Pulse Width	0188H	R/W	FE6030
RAS PreCharge Delay	0189H	R/W	FE6030
RAS Pulse Width	018AH	R/W	FE6030
RAS Access Time	018BH	R/W	FE6030
Enhanced Addressing	018CH	R/W	FE6010
Reserved	018DH	-	-
Reserved	018EH	-	-
System Control Register	018FH	R/W	FE6030

Table 39. ESF Address Map

5.2 ESF ACCESS

ESF space consists of 128 locations expandable to 32K, and may be implemented as word-wide or byte-wide, at the discretion of the designer. Table 39 provides an address map of the ESF registers, access to which is accomplished through the Extended Data registers EAR0 and EAR1, and a "real I/O space" window, the Extended Data register (EDR). Registers that are not documented in this table are reserved and should not be used. For a discussion of some ESF registers, see Section 2.1.2.

The write-only ESF Pointer Register (EPR), configurable by the software, points to the EDR. It is loaded by writing to memory location FFFFDH or FFFF, FFFDH, a PROM. The power-on default location for the EDR is at I/O Address 0700H. The following procedure is recommended to modify the EPR:

1. Set Port 0700H to 8DH to disable NMI.

2. Read System Control Port B at 0061H, and test for a change in the state of Bit 4, Refresh Toggle, to synchronize it with the refresh circuitry.

3. To unlock the EPR, read EAR0 at 0074H, normally a write-only address.

4. Write the new value into the EPR at FFFFDH. This locks the EPR once again.

5. Enable NMI if required. Note that the EPR is locked when written, or on the next refresh cycle, whichever occurs first. The value in EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K I/O space of the CPU from 0400H to FF00H.

To address the ESF I/O space, follow these steps:

1. Write 8DH to Port 0070H to disable NMI.

2. Write the address value to EAR0 at 0074H. If Expanded ESF is being used, also write the value to EAR1.

3. Issue an I/O Read or Write command to the EDR address.

The selected ESF register is determined by decoding the EAR0 address value.

6.0 PERFORMANCE

6.1 MEMORY PERFORMANCE

The performance of a system using a cache depends on several factors, such as the hit rate, the miss overhead, etc. A 64K direct-mapped cache typically produces an 85 - 90% hit rate, with a 30% improvement in performance over a 2 wait state memory design for memory-intensive applications. In DOS environments, the hit rates can exceed 99%. Table 40 shows the performance that can be obtained from the memory subsystem.

NOTE
The performance figures noted above could vary with the software being run.

6.2 TYPICAL CHANNEL ACCESS PERFORMANCE

Table 41 shows typical performance obtained on 80386 or DMA accesses to the Channel. The numbers refer to the cycle times.

CACHE/PAGE MODE ENABLE	16 MHz	20 MHz	25 MHz
CACHE HIT	125 ns (0)	100 ns (0)	80 ns (0)
CACHE MISS AND PAGE HIT, PIPELINED	187.5 (1)	150 ns (1)	120 ns (1)

Table 40. Typical Performance on a Memory Subsystem

Notes

1. For DRAM accesses, the Page Miss performance may vary, depending on the timing parameters of the DRAMs used and the programming in the registers for the CAS pulse width, RAS precharge delay, RAS pulse width and RAS access time.

2. The CAS access time in Page Mode must be equal to or better than 35 ns to achieve the performance shown in the table.

3. The numbers in parentheses denote the wait states.

As described above, when operating in Pipelined Mode, the default Page Mode results in one wait state on a cache miss.

CHANNEL BUS CYCLE	16 MHz	20 MHz	25 MHz
I/O or Memory without wait*	250 ns	250 ns	240 ns
I/O or Memory with wait*	375+ ns	350+ ns	360+ ns

*The timings shown are for Pipelined Mode. For Non-Pipelined Mode, add an extra wait state.

Table 41. Channel Bus Cycle

6.3 PERFORMANCE FOR OTHER BUS CYCLES

The wait state controller within the FE6030 generates the required number of wait states on an 80386 or DMA bus cycle, by delaying the SRDY signal until the cycle is completed. It does not, however, respond to accesses to the 80387, as the 80387 generates its own signal NRDY0, nor to memory accesses that result in a cache hit.

The wait states generated by the controller obey the following rules:

- Local memory accesses that do not generate cache hits result in wait states as shown in Table 36 (refer to page 35)
- Accesses to the local I/O, including the registers on the FE6010 and the FE6030, and the ESF registers, but excluding Port 00F1H, require an access time of 100 ns, which results in the wait states shown in Table 42.
- Channel cycles, including Interrupt Acknowledge cycles, are determined by the assertion of CHRDYRTN.
- With Halt or Shutdown cycles, a zero wait state operation is completed.
- When a write operation is carried out to Port 00F1H to reset the 80387, 130 wait states are inserted.

I/O CYCLE	16 MHz	20 MHz	25 MHz
Cycle following pipelined cycle	1 WS	1 WS	2 WS
Cycle following non-pipelined cycle	2 WS	2 WS	3 WS

Table 42. Typical Performance for Accesses to Local I/O

7.0 TECHNICAL SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for this device are listed below. Note that permanent device damage could result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}-Vss)	0	7	V
Input Voltage	V_{IABS}	Vss-0.3	V_{DD}+0.3	V
Bias on Output Pin	V_{OABS}	Vss-0.3	V_{DD}+0.3	V
Storage Temperature	T_S	-40	-125	°C

7.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the recommended normal operating conditions for extended periods of time could affect the long-term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.5	10	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Power Dissipation	P_W	-	-	mW
Supply Current	I_{DD}	-	-	mA

7.3 DC CHARACTERISTICS UNDER NORMAL OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance @ fc = 1 MHz	C_I	-	5	pF
I/O Capacitance	C_{IO}	-	10	pF
Logic High Input Voltage	V_{IH}	2.0	-	V
Logic Low Input Voltage	V_{IL}	-	0.8	V
Input Leakage	I_{IL}	-	±10	µA
Tristate Output Leakage	I_{OL}	-	±30	µA
I/O Pin Leakage	I_{IOL}	-	±40	µA
OUTPUT $\overline{CCHCS}$				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	6	mA
OUTPUTS D (7:0), $\overline{S}$ (1:0), $\overline{ADL}$, $\overline{CMD}$, A0, $\overline{SBHE}$				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	24	mA
ALL OTHER OUTPUTS				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	4	mA

Note:
When $\overline{TEST}$ = 0, all outputs and bi-directional lines are tristated.

7.4 AC TEST LOADS

OUTPUTS	SYMBOL	MIN	MAX	UNITS
$\overline{CCHCS}$	C_L	-	75	pF
D (7:0), $\overline{S}$ (1:0), $\overline{ADL}$, $\overline{CMD}$, A0, $\overline{SBHE}$	C_L	-	240	pF
All other outputs	C_L	-	50	pF

8.0 TIMING

PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	NOTES
CLOCKS				
Operating Frequency	4/16	4/20	4/25	MHz
T1C/ CLK2 Period	31.25/125	25/125	20/125	=CLK2
T2AC/CLK2 High Time	9/-	8/-	7/-	@ 2 V
T2BC/CLK2 High Time	5/-	5/-	4/-	@ V_{cc}
T3AC/CLK2 Low Time	9/-	8/-	7/-	@ 2 V
T3BC/CLK2 Low Time	7/-	6/-	4/-	@ 0.8 V
T4C/CLK Period	62.5/250	50/250	40/250	=CLK
T5C/CLK High Time	20/-	14/-	10/-	
T6C/CLK Low Time	15/-	12/-	10/-	
80386 BUS INTERFACE				
RDY T1B/Setup Time T2B/Hold Time	 20/- 3/-	 11/- 3/-	 9/- 3/-	
HLDA T3B/Setup Time T4B/Hold Time	 20/- 3/-	 11/- 3/-	 16/- 3/-	
PA (31:2), $\overline{BE}$ (3:0) T5B/Setup Time T6B/Hold Time	 22/- 2/-	 20/- 2/-	 15/- 2/-	
MIO, DC, WR, $\overline{ADS}$ T7B/Setup Time T8B/Hold Time	 22/- 2/-	 20/- 2/-	 15/- 2/-	
NA, $\overline{BS16}$, SRDY T9B/Valid	 2/15	 2/15	 2/15	
FE6030 Register Read T10B/D (31:0) Valid T11B/D (31:0) Disable	 2/50 2/50	 2/40 2/40	 2/31 2/22	
FE6030 Register Write T12B/D (31:0) Setup T13B/D (31:0) Hold	 30/- 30/-	 30/- 30/-	 30/- 30/-	
CACHE INTERFACE				
HIT T1I/Setup Time T2I/Hold Time	 25/- 5/-	 15/- 5/-	 15/- 5/-	
$\overline{MADS}$, $\overline{HITVALID}$, $\overline{CDIR}$, $\overline{CDEN}$ (3:0), $\overline{TAGWR}$, $\overline{TAGDEN}$, $\overline{CCHCS}$ T3I/Valid	 2/20	 2/20	 2/17	4
$\overline{CCHWR}$ T4I/Assertion T5I/De-assertion T6I/Pulse Width	 2/20 -/20 1.5CLK/-	 2/20 -/20 1.5CLK/-	 2/17 -/17 1.5CLK/-	

PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	NOTES
DATA CACHE TIMINGS REQUIRED (EXTERNAL SRAMS) **				
ADDRESS T1S/Access Time	-/64	-/45	-/35	
OUTPUT HOLD T2S/From Address Change	2/-	2/-	2/-	
CHIP SELECT T3S/Access Time	-/64	-/45	-/35	
WRITE T4S/Pusle Width	-/1.5CLK	-/1.5CLK	-/1.5CLK	
ADDRESS T5S/Hold from WRITE	-/2	-/2	-/2	
CACHE-WRITE T6S/Data Setup T7S/Data Hold	-/CLK-7 -/0	-/CLK-7 -/0	-/CLK-7 -/0	
TAGRAM TIMINGS REQUIRED (EXTERNAL TAGRAM) ***				
HIT T1T/From Address	-/57	-/47	-/38	
WRITE T2T/Pulse Width	-/CLK2	-/CLK2	-/CLK2	
DRAM INTERFACE				
RAS, MUX, CAS (3:0), DRMWR (3:0), MDEN (3:0), MDIR, PARCLK, DRMA (19:18) T1D/Valid	2/20	2/20	2/17	1
DRMWR (3:0) T2D/Hold from NCAS	0/-	0/-	0/-	
CHANNEL CONTROLLER				
CHRDYRTN*, DS16RTN, DS32RTN, MMCR T1E/Setup T2E/Hold	10/- 5/-	10/- 5/-	10/- 5/-	2 2
A0 T3E/Valid from BE (3:0) T4E/Hold from S (1:0)	-/25 0/-	-/25 0/-	-/25 0/-	
ADL, S (1:0), CMD, MMCMD, RDEN, NRDLE0, WREN (1:0, H), WRLE, SWPBYT, SWPWORD, SWPDIR T5E/Valid	2/20	2/20	2/17	
CHANNEL MASTER ACCESSING SYSTEM BOARD DRAM				
PA (31:2), BE (3:0), MIO, SBHE, MADE24, S (1:0), ADL, CMD, TR32 T1M/Setup to CLK2 T2M/Hold from CLK2	15/- 2/-	15/- 2/-	15/- 2/-	2 2
UCHRDY				
T3M/De-assert from address T4M/De-assert from S (1:0) T5M/Valid from CLK2	-/35 0/30 -/15	-/35 -/30 -/15	-/35 -/30 -/15	
MEMDS32 T6M/Assert from Addr, MIO	-/25	-/25	-/25	
RDEN, WREN (1:0, H) T7M/Valid from CMD	-/20	-/20	-/17	
READ DATA T8M/From UCHRDY	-/60	-/60	-/60	3
CENTRAL TRANSLATOR				
SWPWORD from S (1:0), CMD, TR32, DS32RTN, BE (3:0) T1X/Valid	-/25	-/25	-/25	

NOTES

1. These outputs should track each other and the cache control outputs.

2. These inputs can be asynchronous to CLK2.

3. This is a system level specification.

4. These outputs should track each other and the DRAM controller outputs.

* CHRDYRTN can tolerate a 20 ns setup.

** The SRAMs used should have parameters equal to or better than those listed in this table. The numbers shown are only representative numbers for a typical system; designers should do a complete timing analysis for their own systems to select the SRAMs.

*** The TagRAMs used, whether built out of discrete components or not, should have parameters equal to or better than those listed in this table. The numbers shown are only representative numbers for a typical system; designers should do a complete timing analysis for their own systems to select the SRAMs.

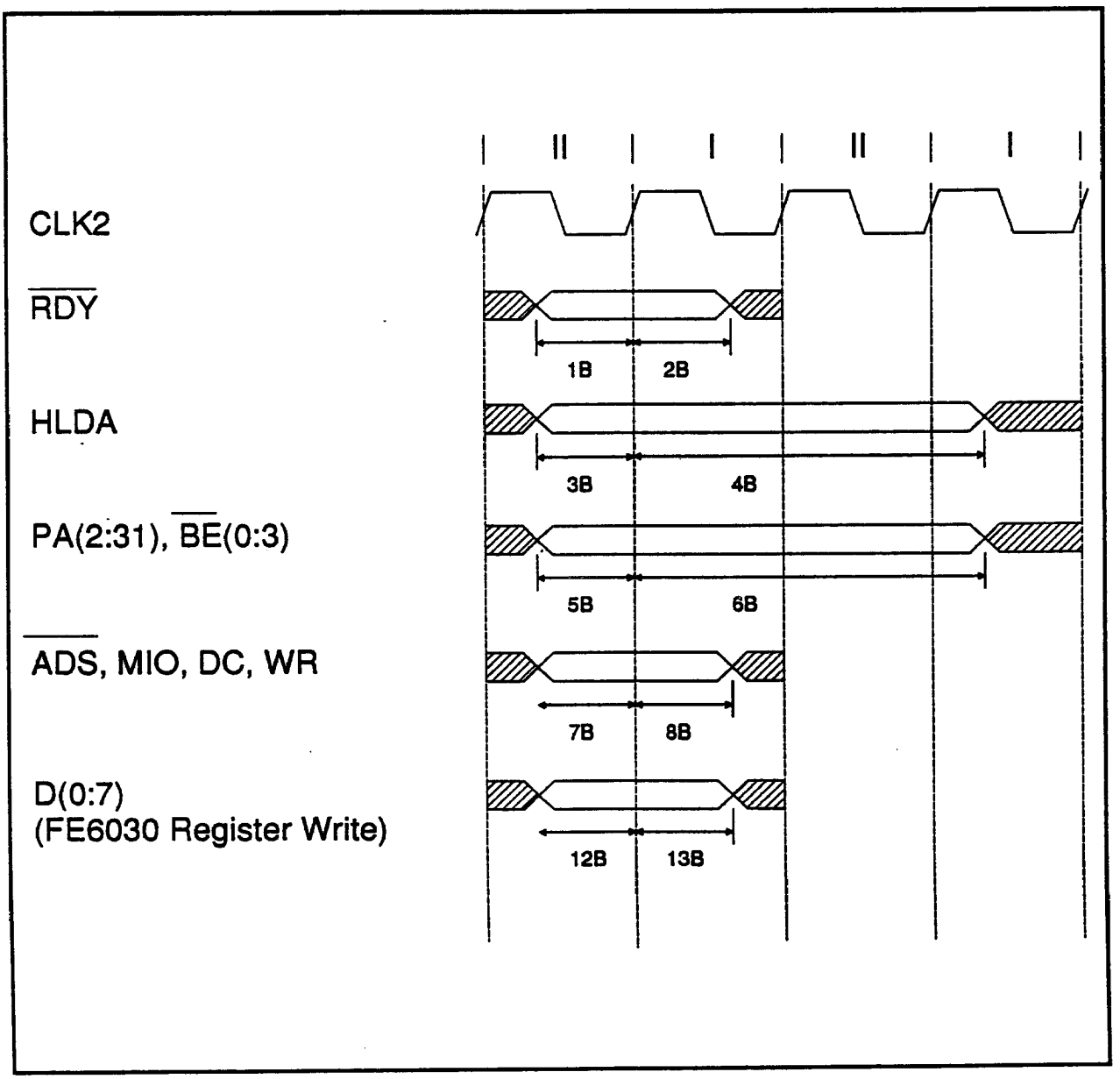

Figure 13. 80386 Bus Interface Input Setup & Hold Timings

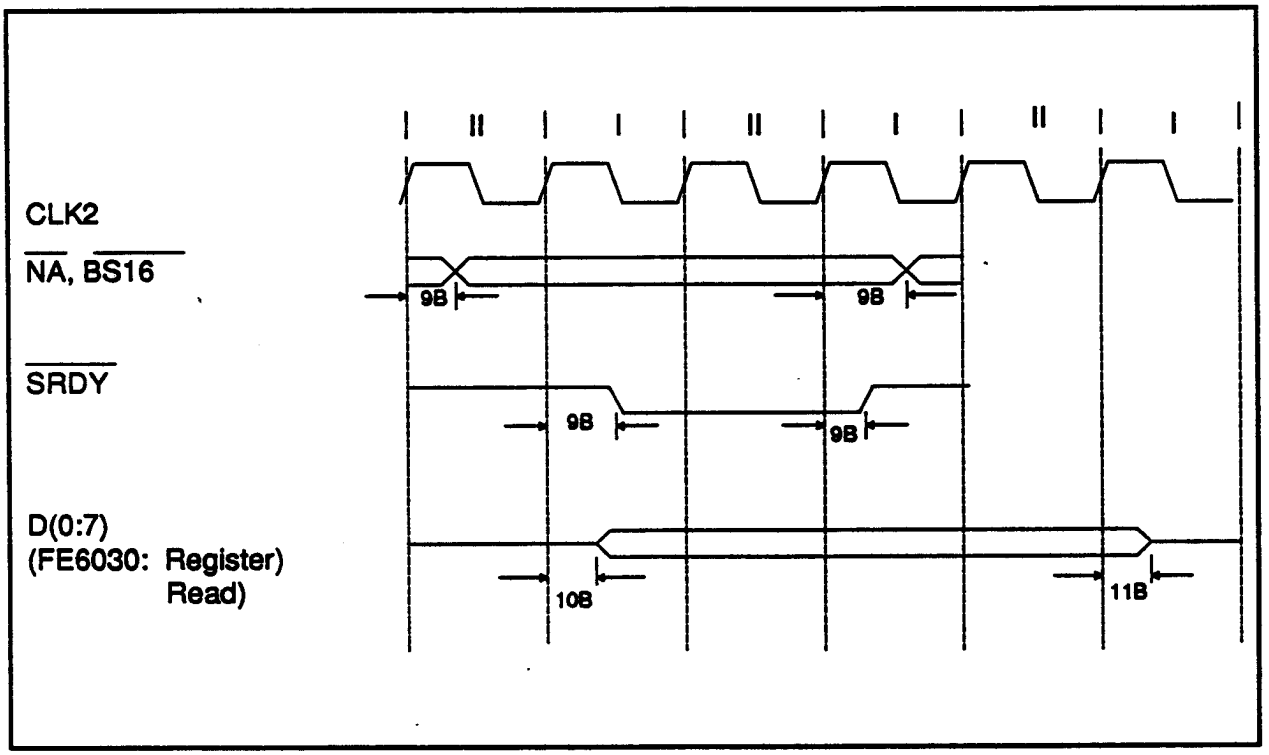

Figure 14. 80386 Bus Interface Output Valid Delay Timing

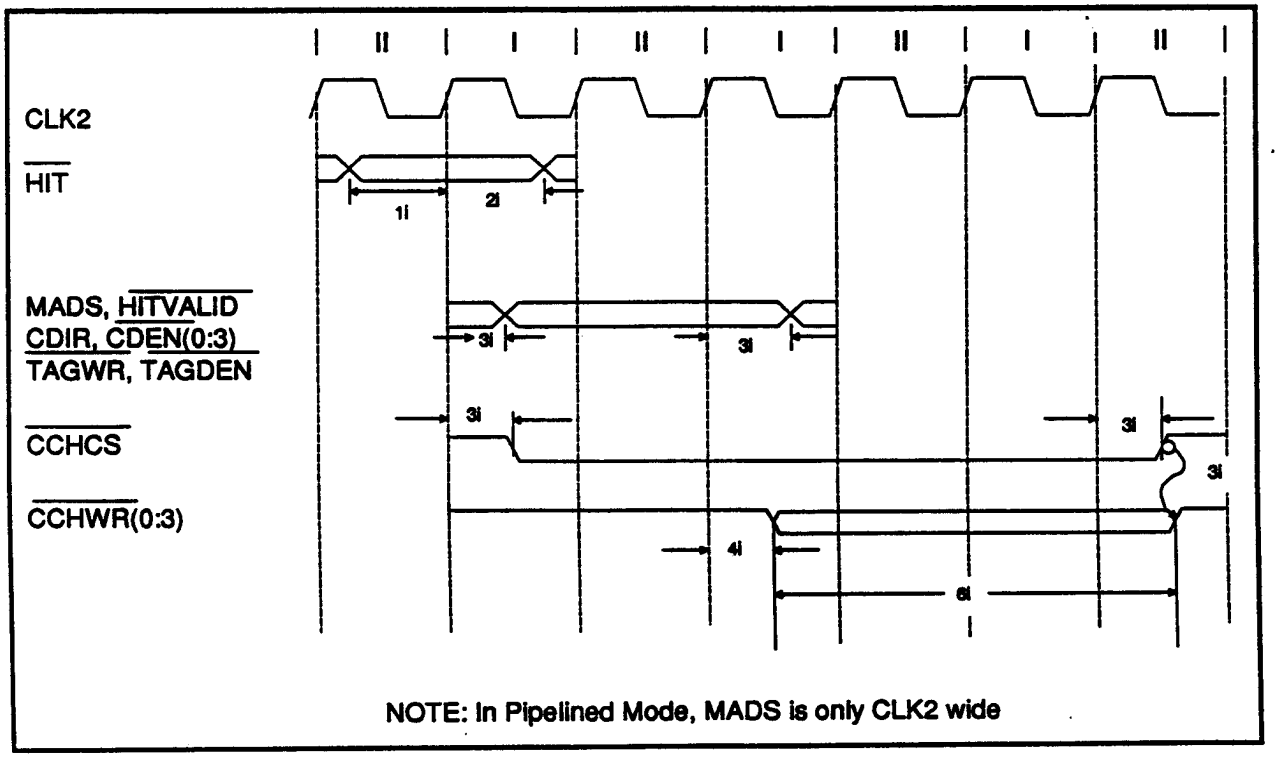

Figure 15. FE6030 Cache Interface Timings

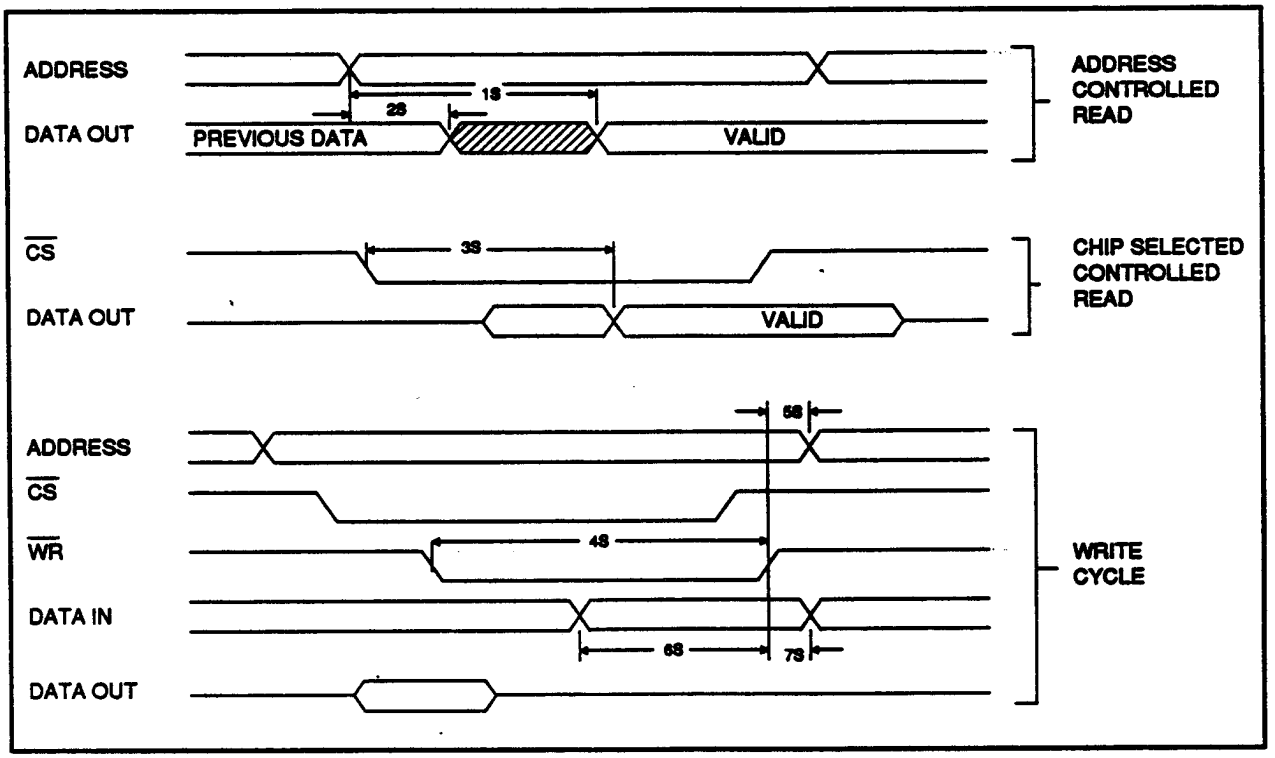

Figure 16. Data Cache SRAM Timings

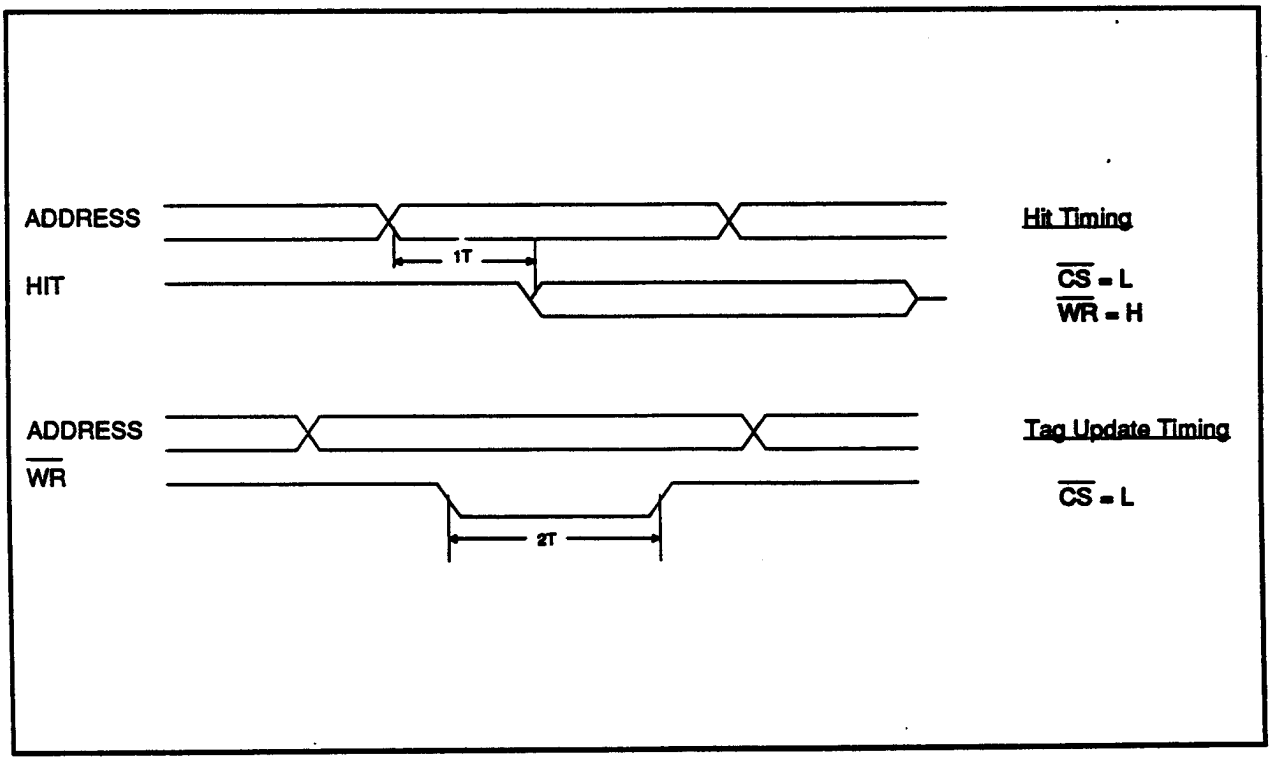

Figure 17. FE6030 TagRAM Timings

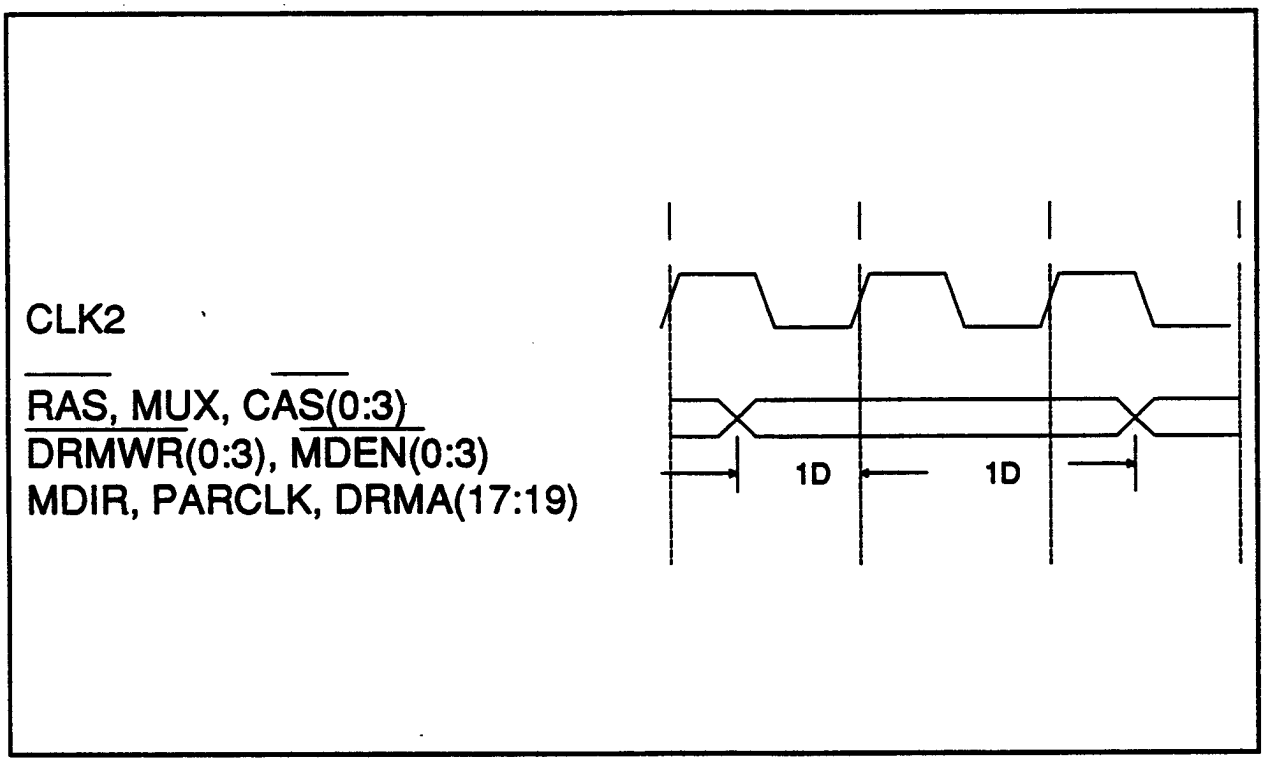

Figure 18. DRAM Interface Output Valid Delay Timing

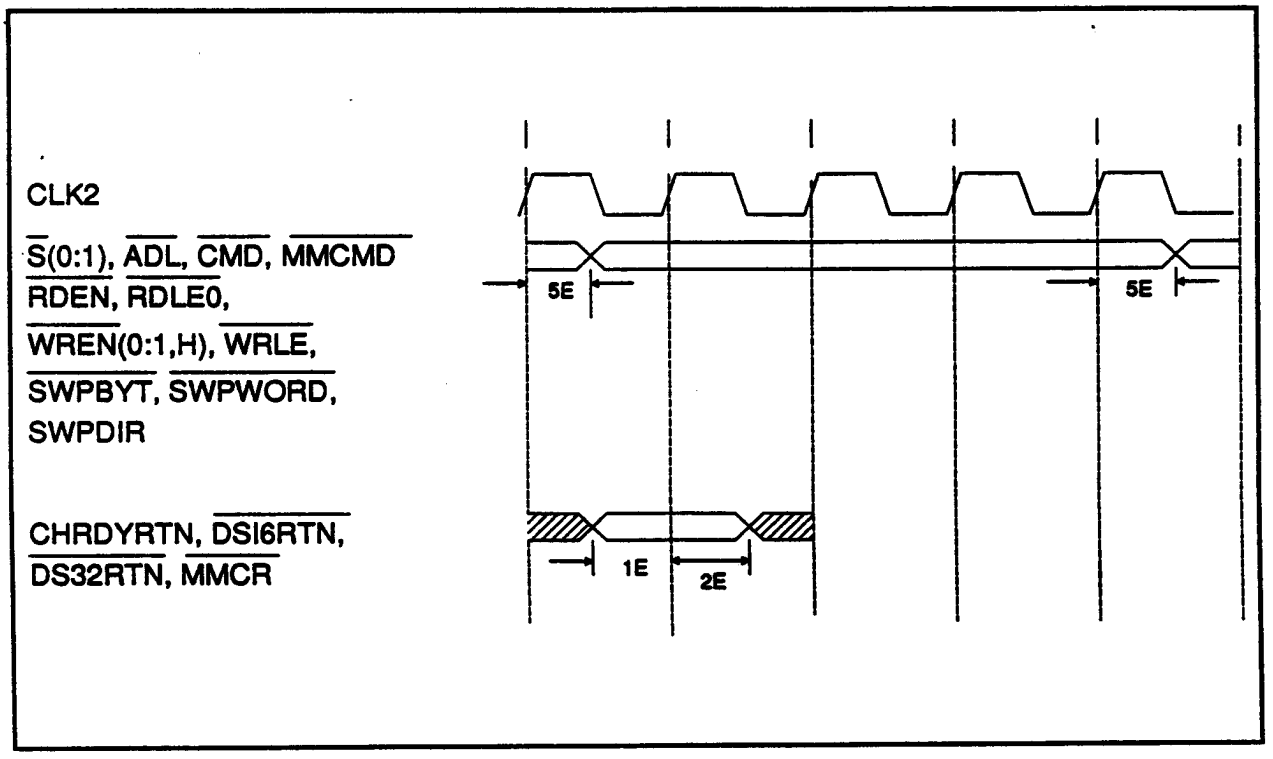

Figure 19. Channel Controller Timing

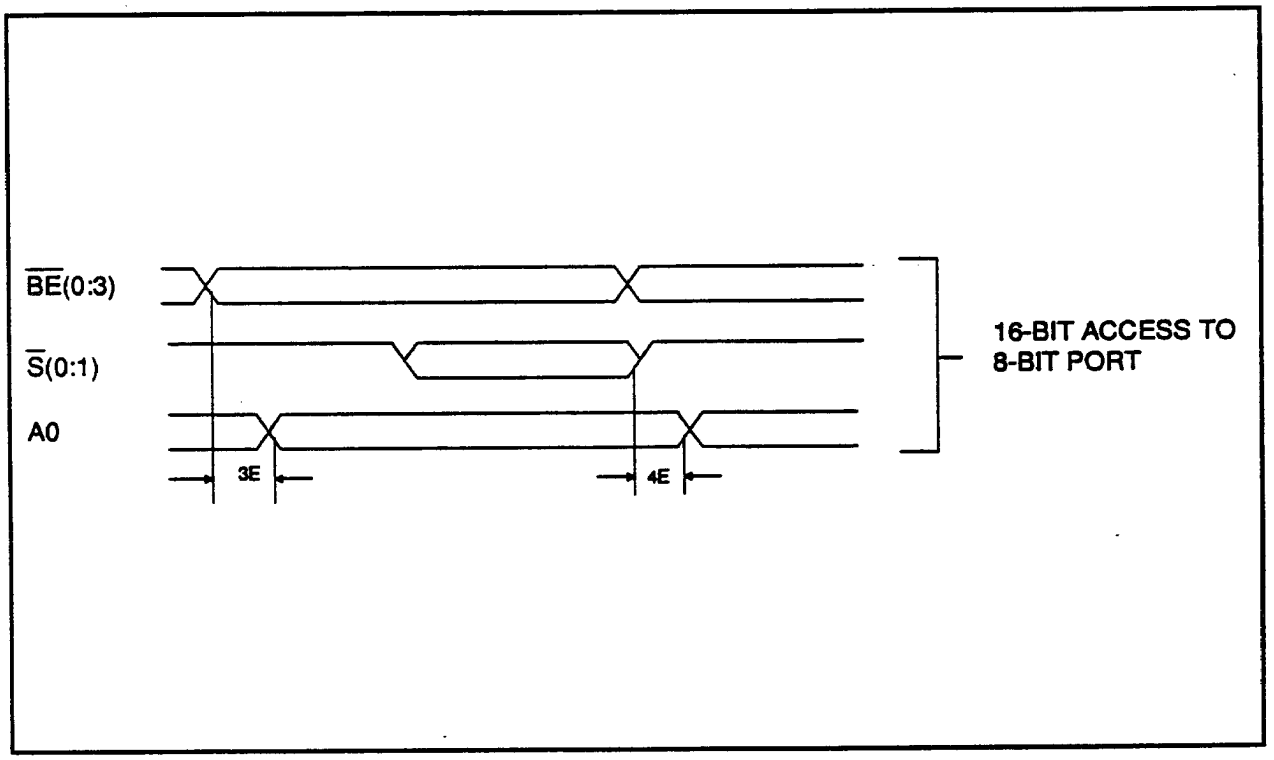

Figure 20. Channel Controller: 16-Bit Access to 8-Bit Port

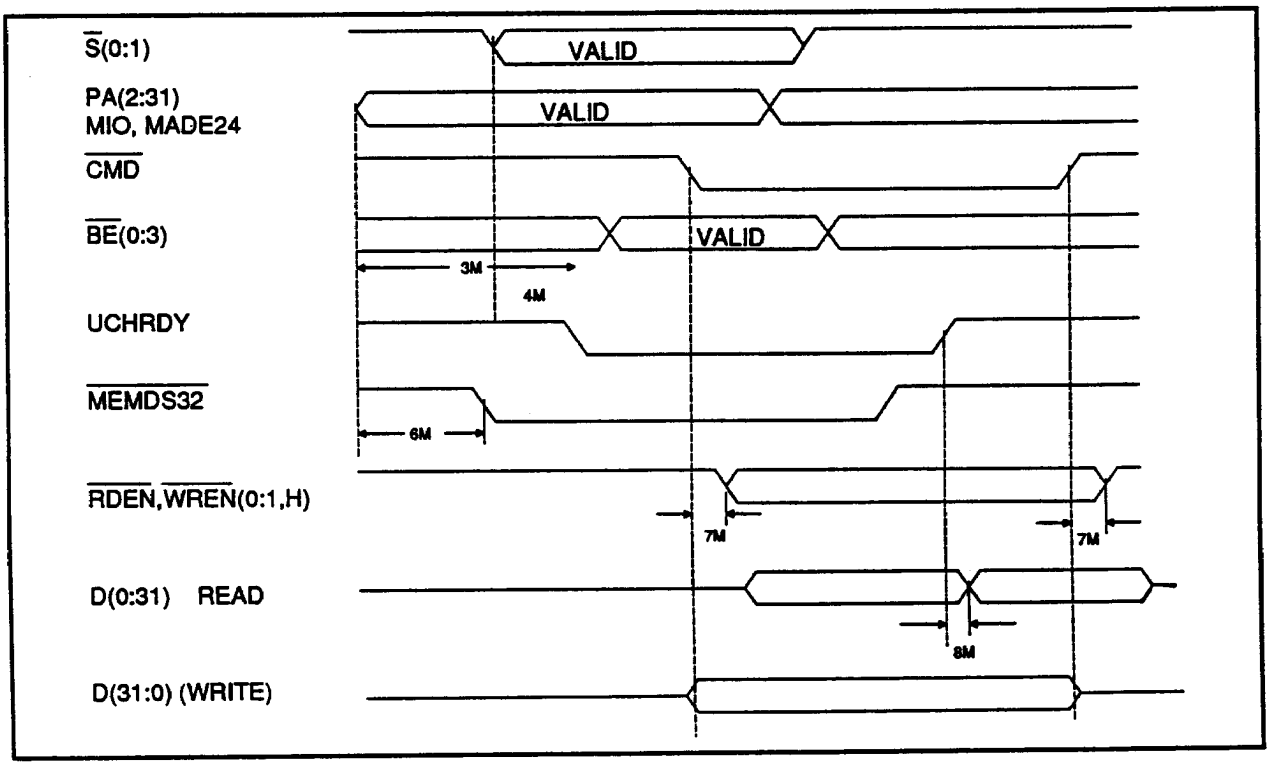

Figure 21. Channel Master Accesses to System Board DRAM-IV

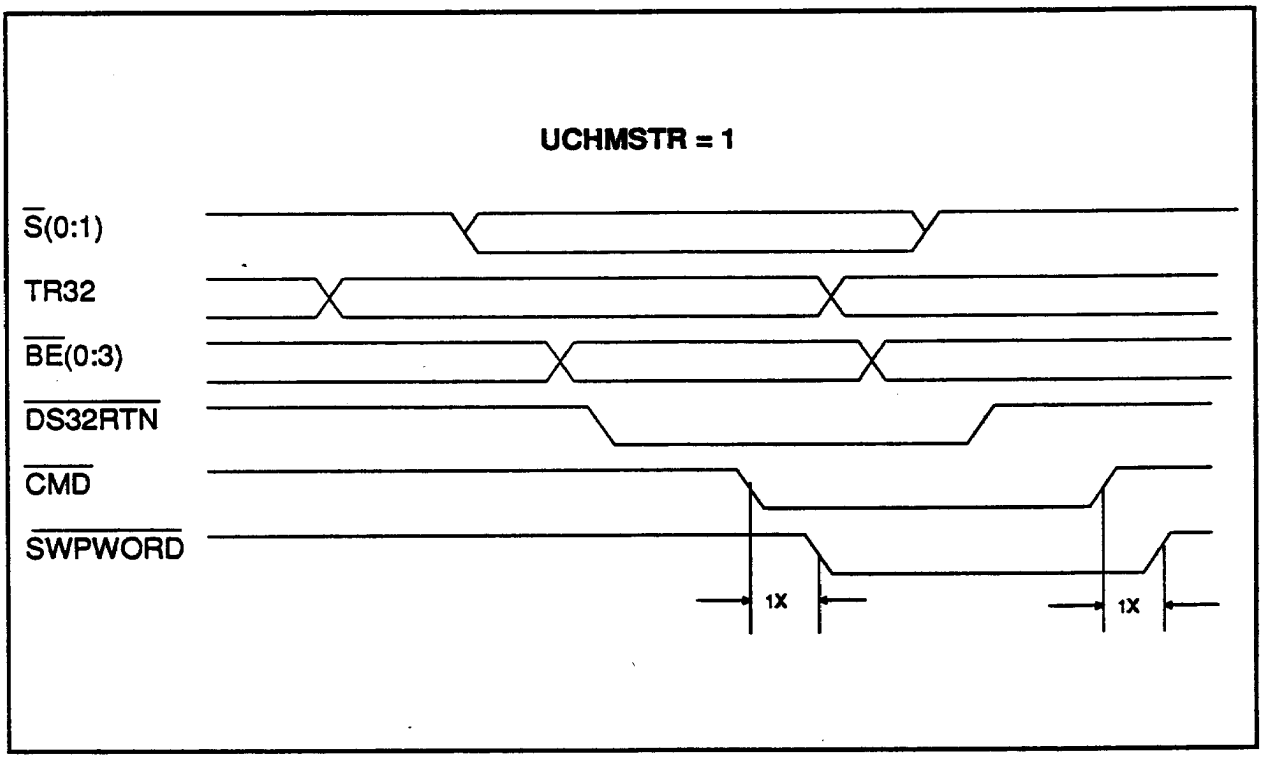

Figure 22. Central Translator Function

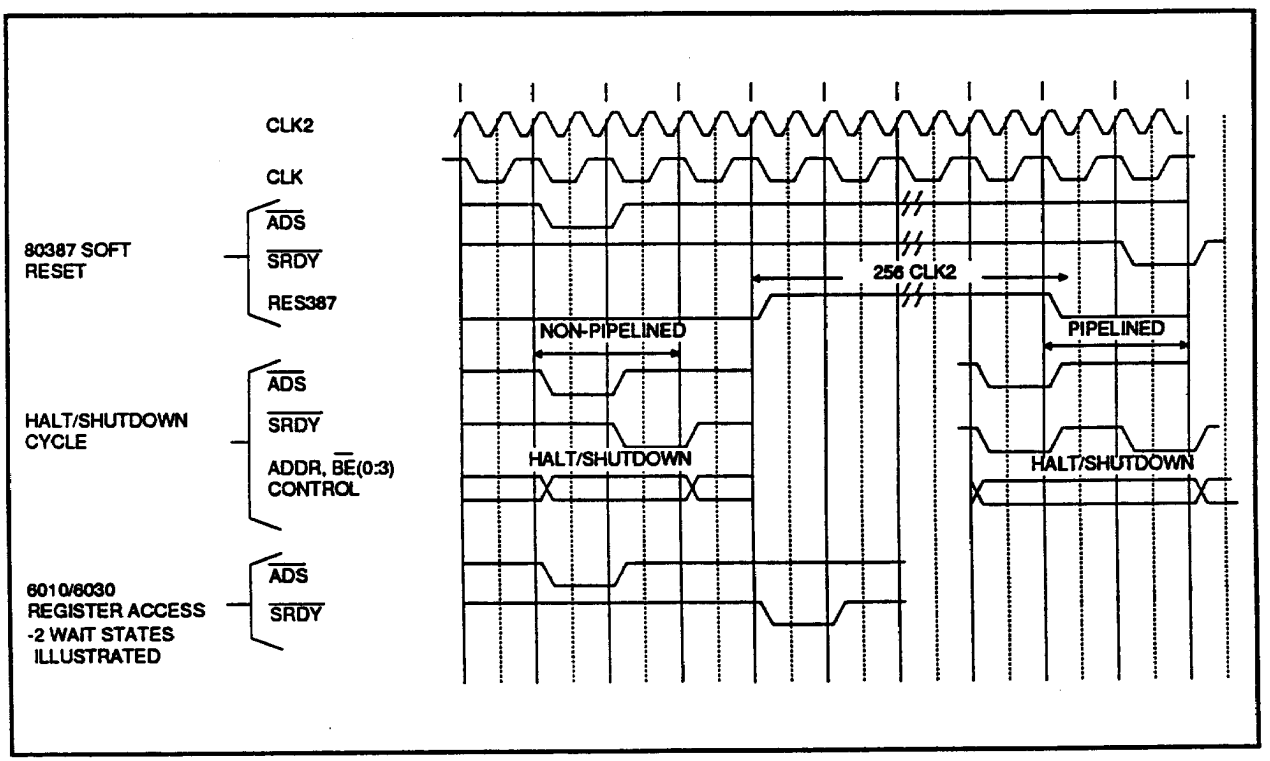

Figure 23. Miscellaneous Cycles

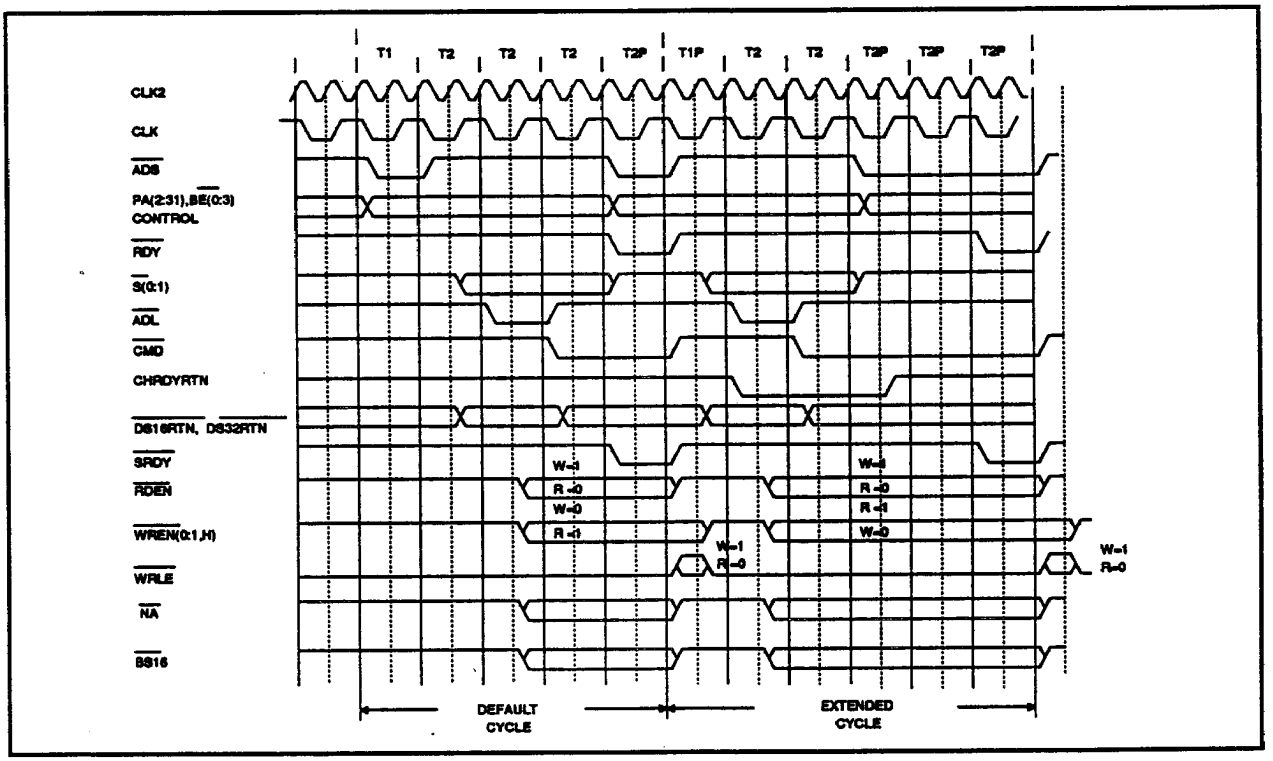

Figure 24. Channel Accesses: 16 MHz Back-to-Back Cycles

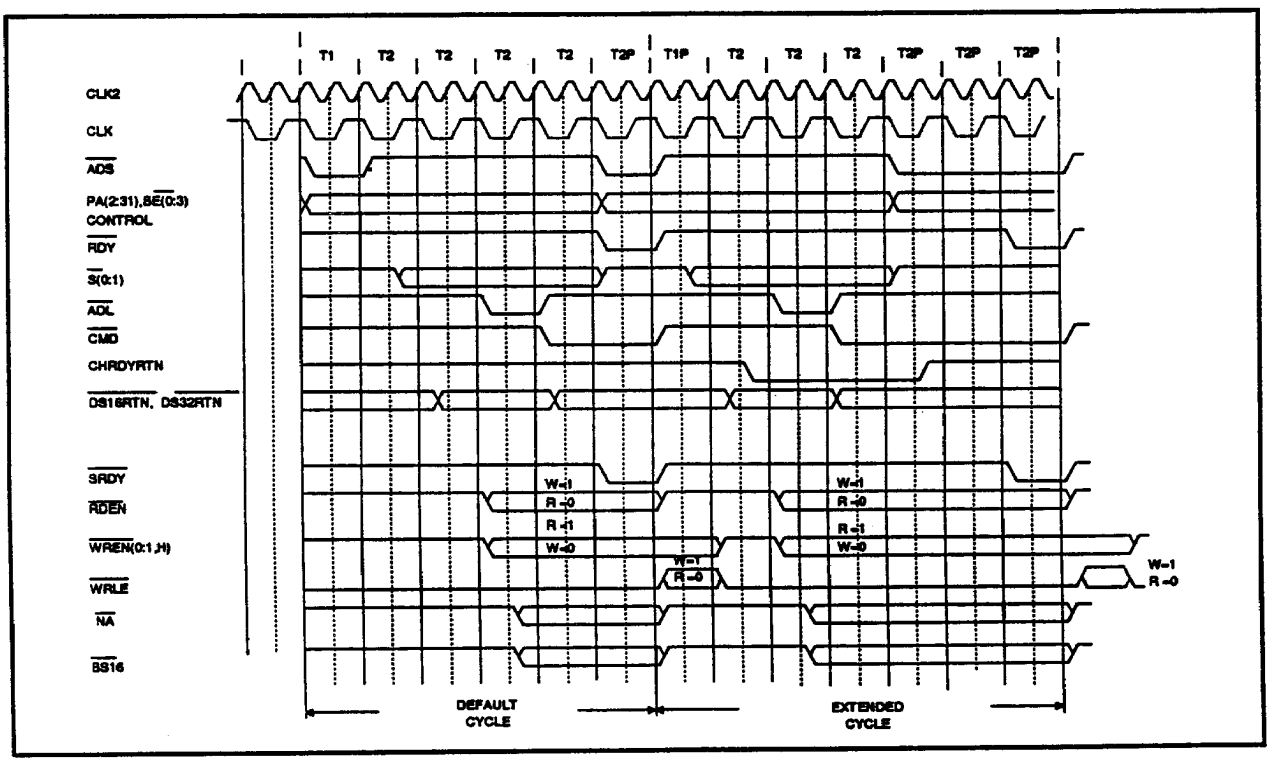

Figure 25. Channel Accesses: 20 MHz Back-to-Back Cycles

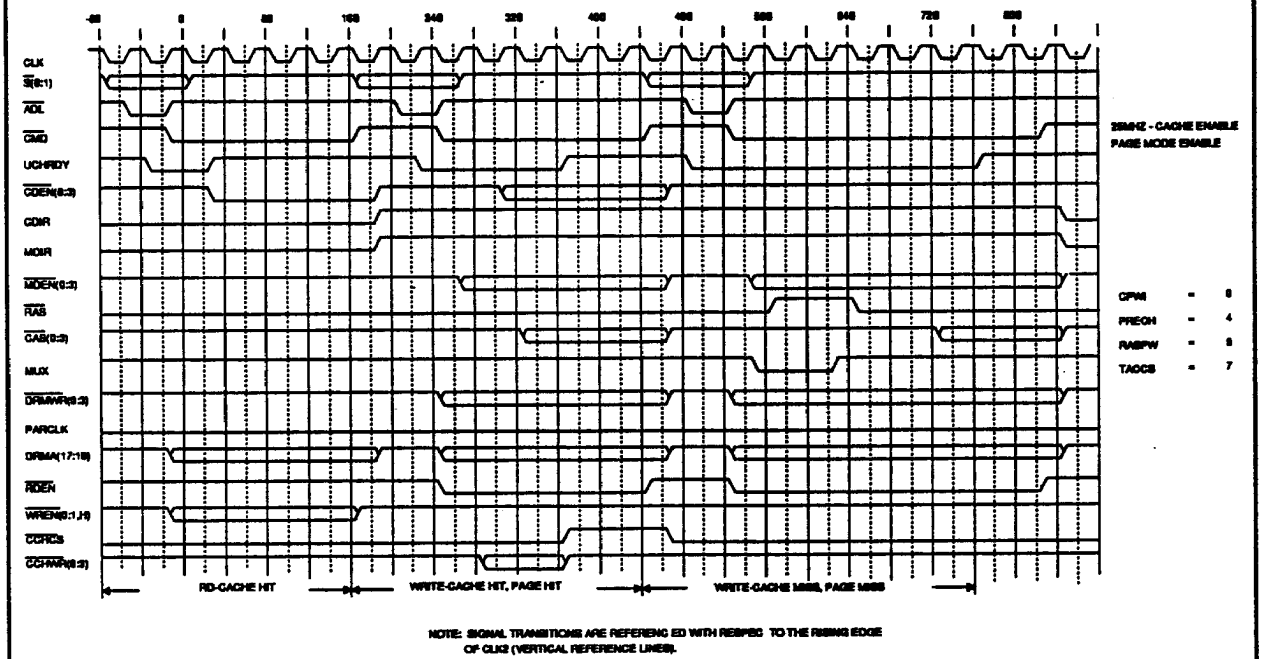

Figure 26. Channel Master Accesses to System Board DRAM-V

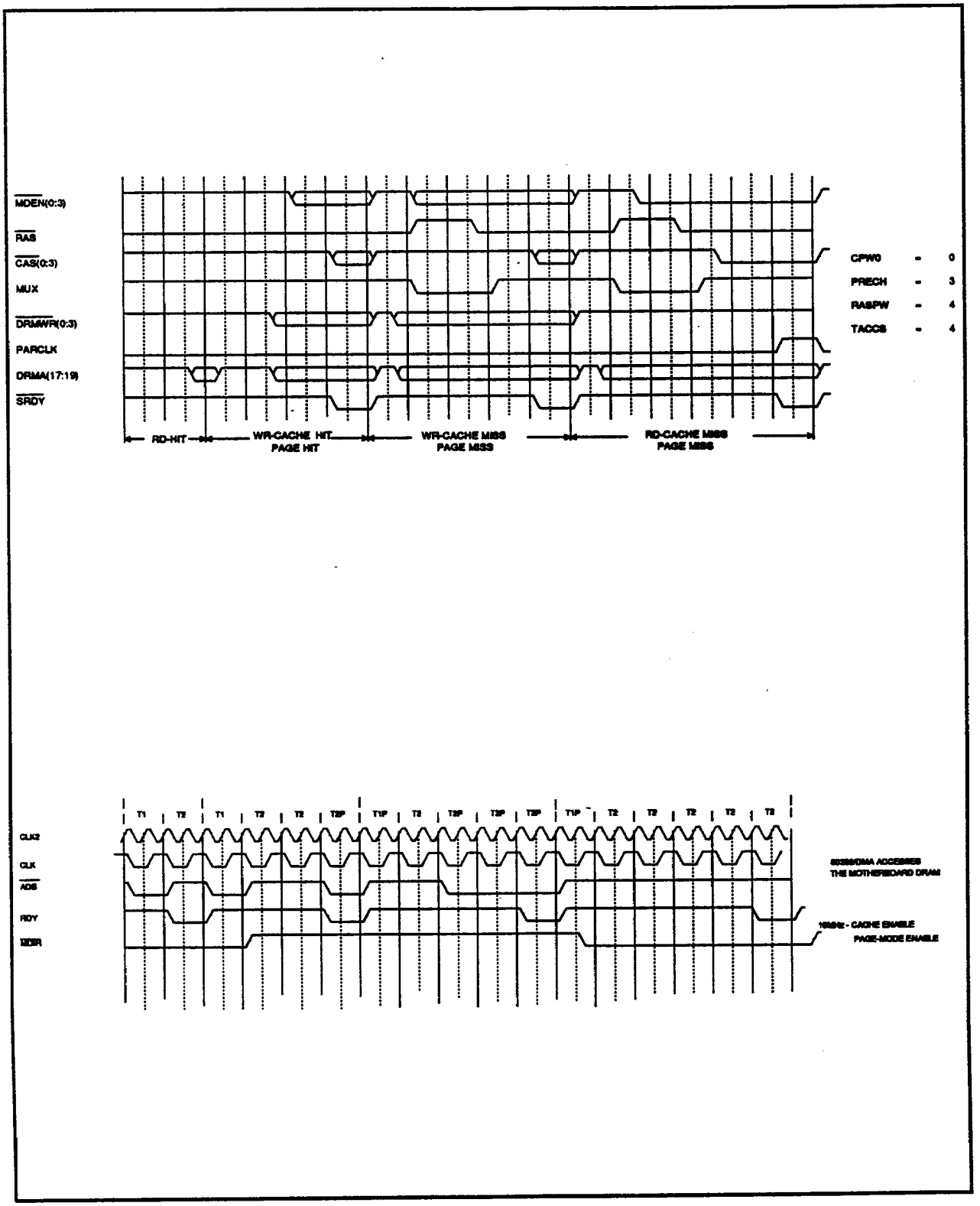

Figure 27. 80386/DMA Access to DRAM-II

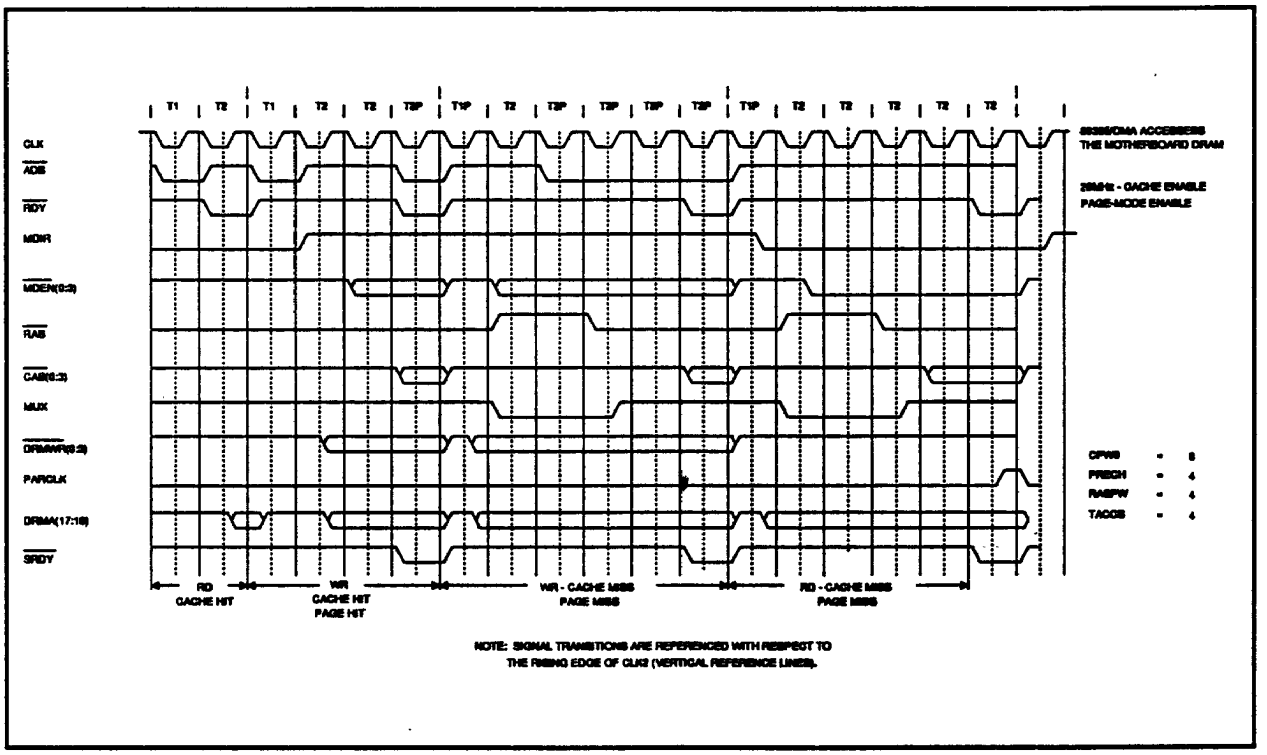

Figure 28. 80386/DMA Access to DRAM-III

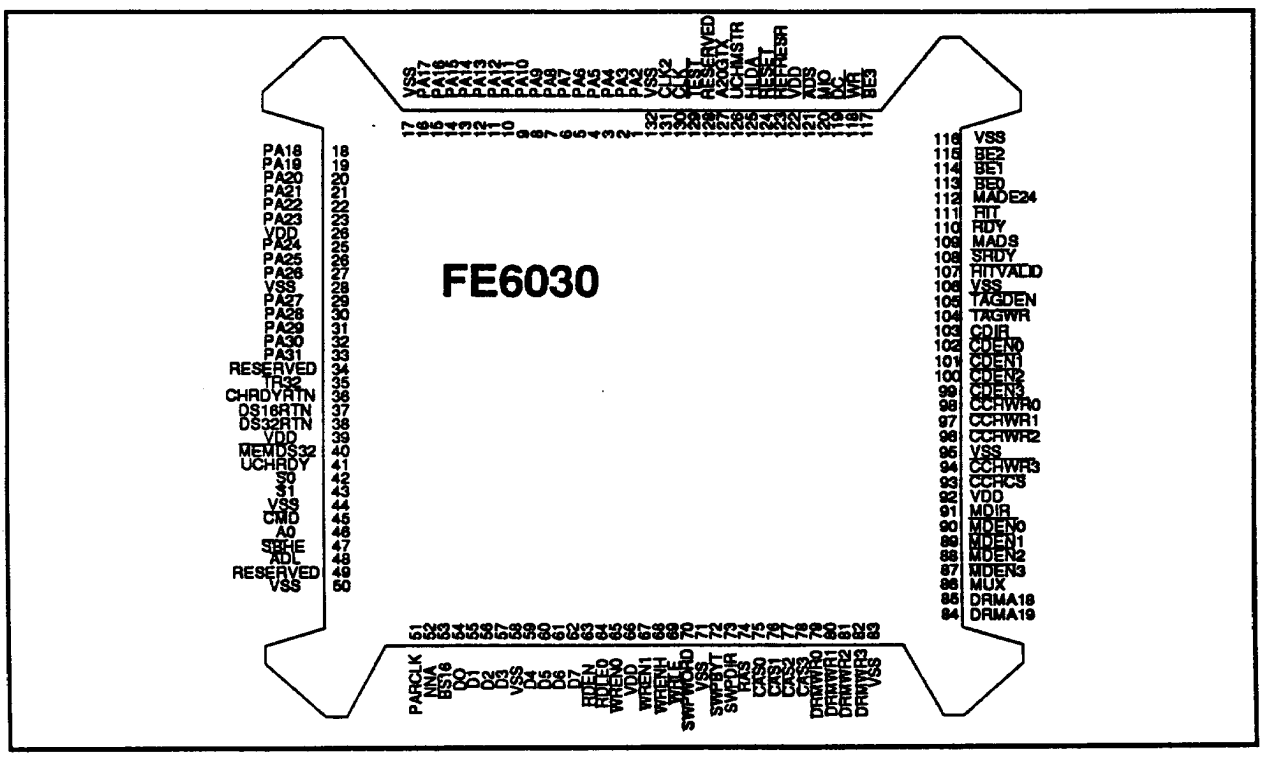

Figure 29. Pin Layout Diagram

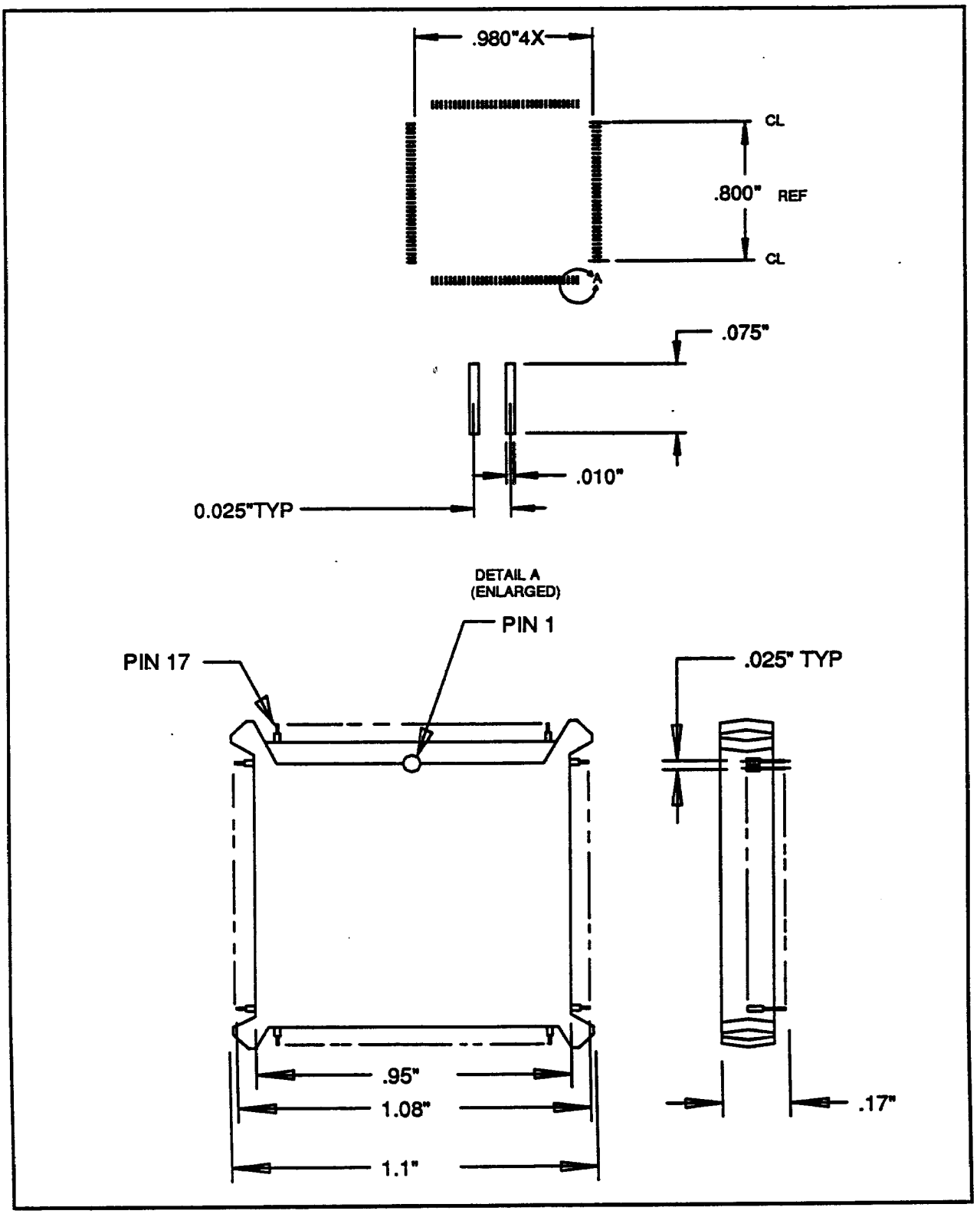

Figure 30. 132-Pin JEDEC Flat Pack Packaging Diagram

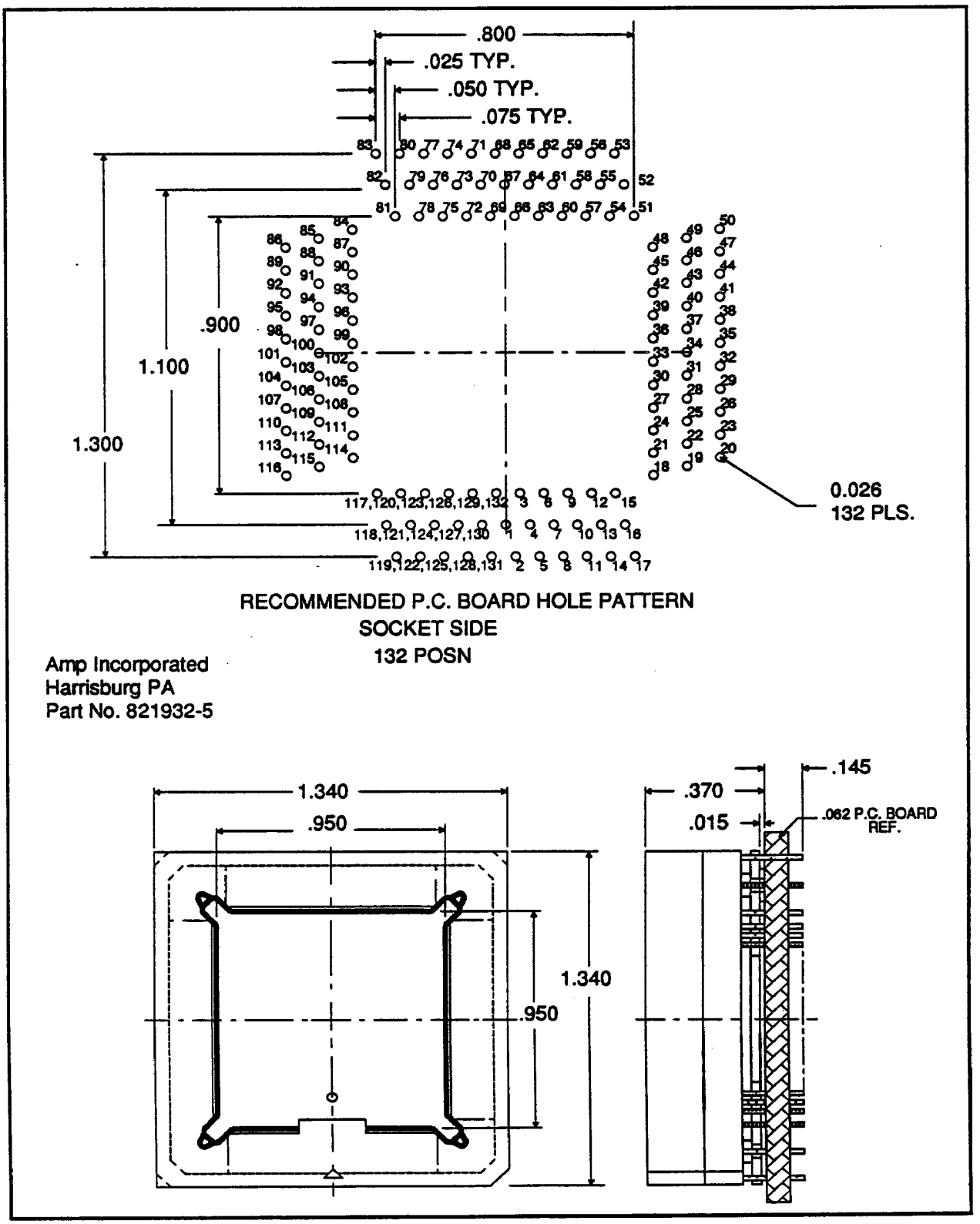

Figure 31. Socket Diagram