Preliminary Data Sheet
May 1992

AT&T Microelectronics

ATT20C458 CMOS RAMDAC

Features

- 200/170/135/110 MHz operation
- Power dissipation = 1.1 W typical at 135 MHz and 1.3 W typical at 200 MHz
- 4:1 or 5:1 multiplexed pixel input
- Internal V_{REF} accuracy better than ±3%
- 256 x 24 dual-port color RAM
- Four-color overlay RAM
- Sync on green DAC
- DAC outputs compatible with RS-343A standard
- Monolithic 0.9 µm CMOS
- Single +5 V power supply
- 84-pin PLCC (plastic package only)

Applications

- Workstation graphics
- *SPARC** clones
- High-resolution PC and *Macintosh*† add-in cards

* *SPARC* is a registered trademark of Sun Microsystems Corporation.
† *Macintosh* is a registered trademark of Apple Computer Corporation.

Description

The ATT20C458 is a high-speed monolithic +5 V CMOS RAMDAC for high-resolution computer graphics. Multiplexed inputs allow the use of TTL signals while maintaining pixel rates up to 200 MHz. High-speed versions (200 MHz) support 1800 x 1350 screen resolutions with 256 displayable colors from a palette of 16 million. The device is pin and function compatible with the Bt458.

A microprocessor port configures the internal registers and writes and reads the color and overlay RAM. The dual-port RAM accepts updates from the MPU without disturbance to the video signal. The device contains a 256 x 24 color look-up table RAM (CLUT) and a 4 x 24 overlay CLUT RAM.

The pixel inputs accept five or four pixels per clock load. A serializer accepts the pixels in parallel and streams them out serially.

Three 8-bit DACs provide red, green, and blue outputs to an RGB monitor. These analog outputs will drive a doubly terminated 75 Ω system.

AT&T fabricates the part in 0.9 µm CMOS for low power dissipation and faster pixel rates. This allows all frequency ranges to be packaged in an 84-pin PLCC. An external or internal voltage reference may be used. Use of the internal voltage reference will reduce power dissipation, part count, and board area.

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Description (continued)

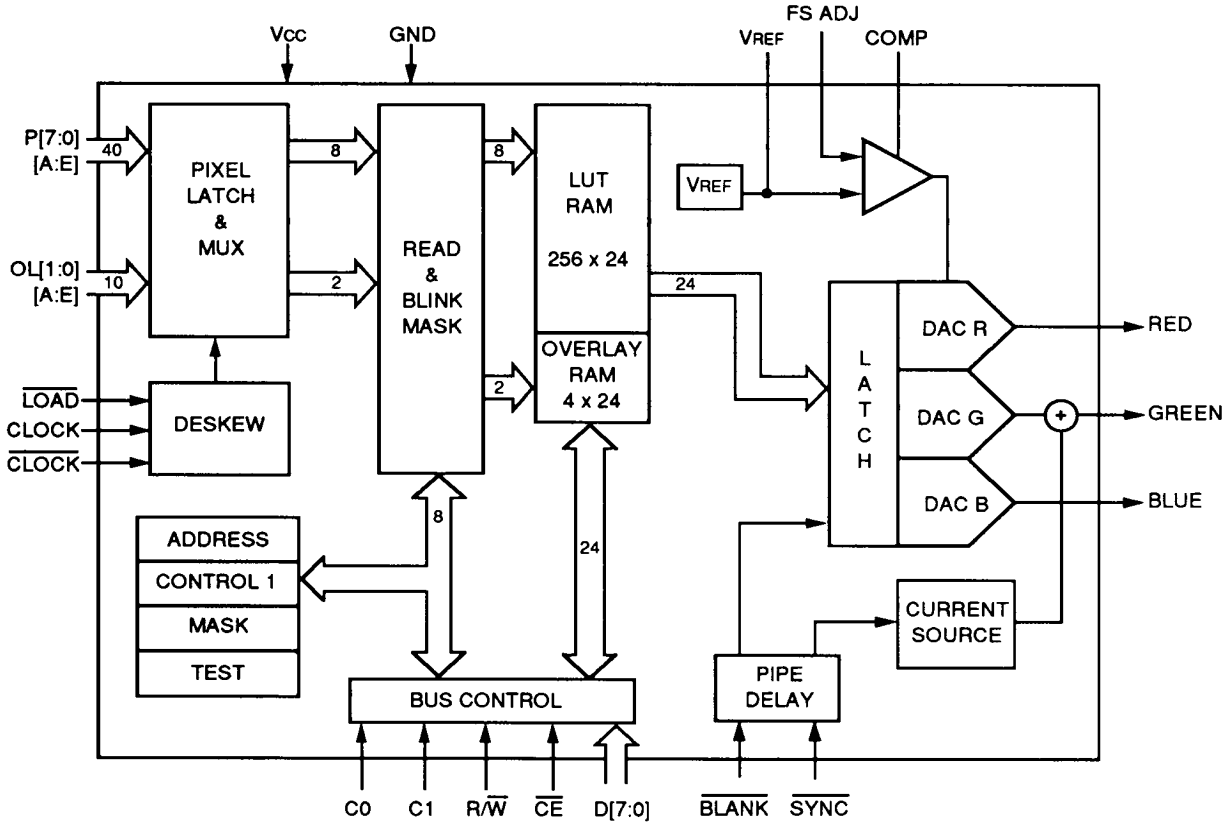


Figure 1. Block Diagram

Pin Information

Top View.

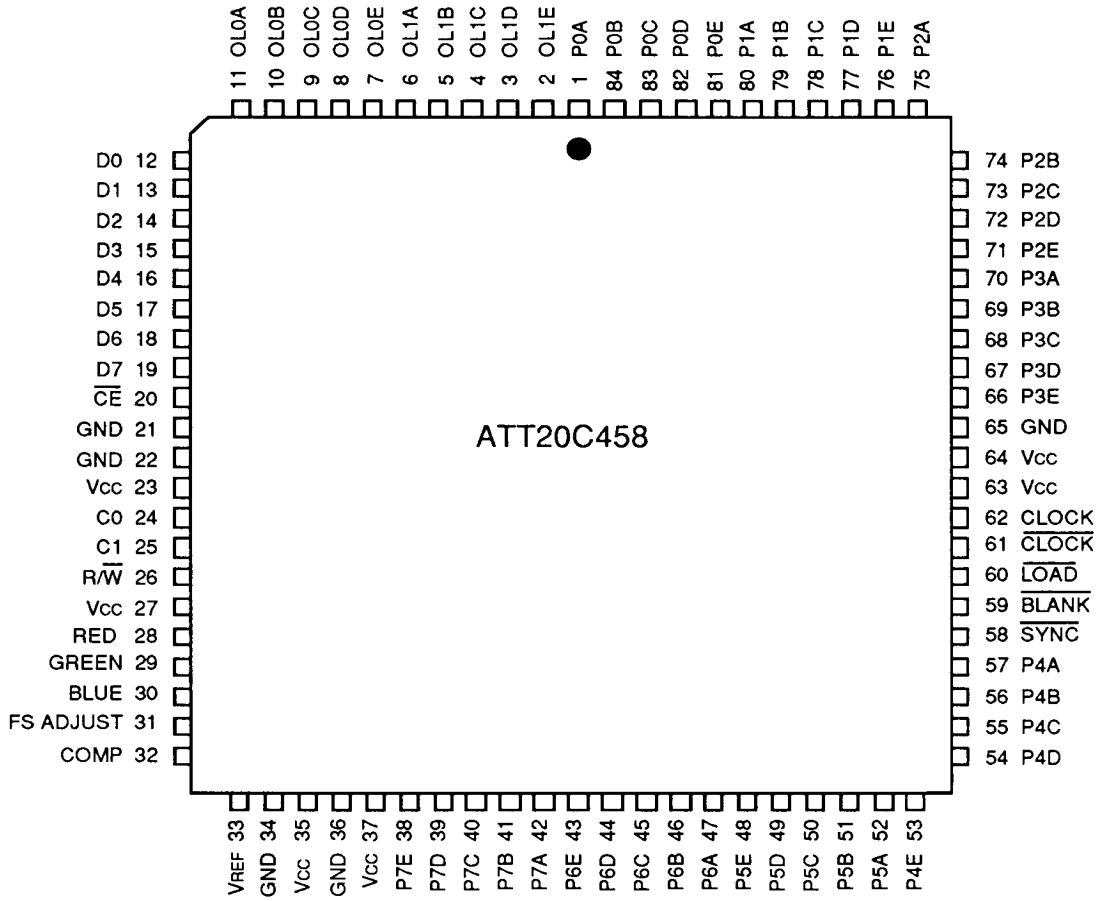


Figure 2. ATT20C458 84-Pin PLCC Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

PLCC Pin #	Symbol	Type	Name/Function
1, 84—81 80—76 75—71 70—66 57—53 52—48 47—43 42—38	P0[A:E] P1[A:E] P2[A:E] P3[A:E] P4[A:E] P5[A:E] P6[A:E] P7[A:E]	I	**Pixel Address.** TTL compatible. The pixel address is used to select one of the 256 entries in the color RAM. Four or five consecutive pixels are input through this port on the rising edge of LOAD . The A pixel is sent through the pipeline first, followed by the B pixel, and so on. Unused inputs should be tied to ground.
11—7 6—2	OL0[A:E] OL1[A:E]	I	**Overlay Address.** TTL compatible. Four or five consecutive overlay addresses are input through this port on the rising edge of LOAD . The overlay address, together with the sixth bit of the command register, determines which RAM (color or overlay) is used. When the overlay RAM is selected, the pixel addresses, P[7:0] [A:E], are ignored. Unused inputs should be tied to ground.
19—12	D[7:0]	I/O	**MPU Data Bus.** TTL compatible. Internal register addresses and data are transferred over this port. D0 corresponds to the least significant bit.
20	$\overline{CE}$	I	**Chip Enable (Active-Low).** TTL compatible. This input must be low to enable reading or writing to the MPU port. During write operations, D[7:0] are latched on the rising edge of CE . Avoid glitches on this edge-triggered input.
24 25	C0 C1	I	**Control.** TTL compatible. These inputs are latched on the falling edge of CE . The C[1:0] inputs, together with the internal address register, control the read/write operations of the color RAM, overlay RAM, and command register.
26	R/ $\overline{W}$	I	**Read/Write Control.** TTL compatible. R/ $\overline{W}$ is latched on the falling edge of CE . A logic zero on R/ W corresponds to a write operation.
28 29 30	RED GREEN BLUE	O	**Red, Green, and Blue Analog Current.** These high-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.
31	FS ADJ	—	**Full-Scale Adjust Control.** A resistor (RSET) should be connected between this pin and ground to control the magnitude of the full-scale video signal.
32	COMP	—	**Compensation Pin.** A 0.1 µF ceramic capacitor should be connected between this pin and Vcc to provide the highest possible power supply noise rejection.
33	VREF	I	**Voltage Reference.** If an external voltage reference circuit is used, it must supply this input with a 1.235 V reference. A 0.1 µF capacitor must be used to decouple this pin to GND. If an external voltage reference is not used, the internal voltage reference generates 1.235 V ± 3%.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

PLCC Pin #	Symbol	Type	Name/Function
58	$\overline{\text{SYNC}}$	I	**$\overline{\text{SYNC}}$ Control (Active-Low).** TTL compatible. $\overline{\text{SYNC}}$ is latched on the rising edge of LOAD and should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ has a four- or five-pixel resolution. A logic 0 on $\overline{\text{SYNC}}$ switches off an internal current source.
59	$\overline{\text{BLANK}}$	I	**Blank Control (Active-Low).** TTL compatible. Latched in on the rising edge of LOAD . When $\overline{\text{BLANK}}$ is asserted, the DAC ignores the color output value from the color RAM and drives the analog outputs to the blanking level. $\overline{\text{BLANK}}$ has a four- or five-pixel resolution.
60	$\overline{\text{LOAD}}$	I	**Load Control.** TTL compatible. The rising edge of $\overline{\text{LOAD}}$ latches the pixel address, overlay address, blank, and sync inputs. LOAD is either 1/4 or 1/5 of the frequency of the pixel clock and may be phase independent.
61, 62	$\overline{\text{CLOCK}}$, CLOCK	I	**Pixel Clock.** +5 V ECL compatible differential clock inputs.
23, 27, 35, 37, 63, 64	Vcc	—	**Power (+5 V).**
21, 22, 34, 36, 65	GND	—	**Ground.**

Functional Description

The ATT20C458 monolithic RAMDAC contains three signal interfaces: a pixel port, MPU port, and analog outputs. The pixel port includes the overlay, SYNC, and BLANK inputs. The MPU port connects to a microprocessor bus or graphics controller. The MPU port includes address, data, and control signals. The red, green, and blue analog outputs connect to the computer graphics CRT.

Pixel Port

To enable the use of lower-cost frame buffer memory, the ATT20C458 accepts four or five pixels in parallel and serializes them at the pixel clock rate. The LOAD clock signal latches the pixel, BLANK, and SYNC information. There are eight color bits and two overlay bits per pixel. The pixel multiplexing requires SYNC and BLANK to be resolved to a four- or five-pixel resolution. The LOAD signal is usually derived from DRAM or VRAM frame buffer timing signals. For 5:1 multiplexing, 50 bits are latched.

The ATT20C458 outputs the A pixel followed by the B pixel, etc. until the ABCDE sequence is complete. It then repeats the sequence with 50 bits of new information latched in with the LOAD signal. In the case of 4:1 multiplexing, the sequence repeats after ABCD.

The overlay inputs operate at pixel speed and can be used for text or graphics overlays or as inputs for external hardware cursor generation logic. Table 2 outlines the truth table of the overlay inputs and control register bit CR6. When CR6 is logic high, the overlay inputs determine whether the color RAM or the overlay RAM is addressed. If OL1 = OL0 = 0, the pixel inputs address the color RAM. If OL1, OL0 ≠ 0, 0, then OL1 and OL0 determine the three overlay colors. If CR6 is logic low, only the overlay colors are displayed. There are four overlay colors in this case.

Table 2. Overlay Location Zero

OL1	OL0	CR6 = 1	CR6 = 0
0	0	Color RAM	Overlay Color 0
0	1	Overlay Color 1	Overlay Color 1
1	0	Overlay Color 2	Overlay Color 2
1	1	Overlay Color 3	Overlay Color 3

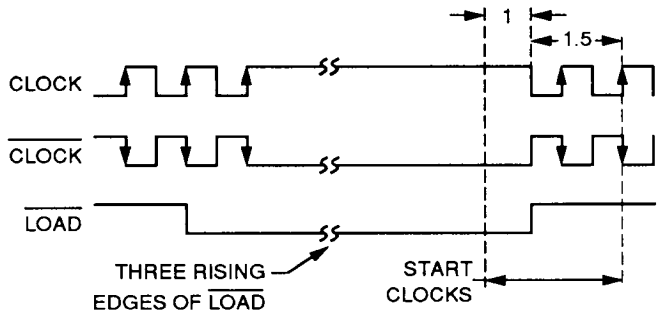


Figure 3. Reset Sequence

Clock and LOAD Signals

The CLOCK and LOAD signal edges do not have to be placed in a fixed-phase relationship. The phase between CLOCK and LOAD can vary up to 360°. This allows LOAD to be derived by dividing the pixel clock. The ATT20C458 eliminates the problem of variation in the propagation delay between LOAD and clock drivers.

During the four or five pixel clocks between LOAD clocks, the ATT20C458 synchronizes the pixel data to an internal LOAD signal. For 4:1 multiplexing, four CLOCK cycles must occur every rising edge of LOAD. For 5:1 multiplexing, five CLOCK cycles must occur every rising edge of LOAD. If this is not the case, the ATT20C458 will assume it is not locked to the LOAD signal and will continuously attempt to resynchronize itself to LOAD.

Internal Pixel Pipeline

To achieve the maximum variable phase relationship between the load and clock signals, the pixel pipeline must be set to eight clocks. Upon powerup, the pipeline delay can be six to ten clock cycles from LOAD. To set the pipeline delay to eight pixel clocks, the chip must be powered up with CLOCK, CLOCK, and LOAD running. Stop the clock with CLOCK high and CLOCK low for at least three rising edges of the LOAD signal. Restart CLOCK and CLOCK as close to the rising edge of LOAD as possible. CLOCK and CLOCK must start switching no more than one clock cycle before LOAD or one and a half clock cycles after LOAD. (See Figure 3.)

Functional Description (continued)

Setting the Pipeline Delay

Care must be taken to avoid glitches and violations of the minimum clock width requirements. Note that if the multiplex select bit, CR7, in the control register is changed, the pipeline delay must be reset. Resetting the pipeline delay resets the blink counter circuitry. Therefore, if multiple devices are used in parallel, the blink rates will be synchronized.

Signal Path Through the ATT20C458

The read mask, blink mask, and control registers operate on an 8-bit pixel and 2-bit overlay every clock cycle. The control registers enable and disable display and blinking for the frame buffer bit planes. There are four blink rates and duty cycles. To prevent a display plane from being partially blinked during a frame, the ATT20C458 updates blink information during the vertical retrace period. Internal logic determines a vertical retrace period by counting the LOAD cycles that occur while BLANK is a logic zero. When BLANK has been a logic zero for more than 256 LOAD cycles, the ATT20C458 recognizes a vertical retrace period.

The RAM information is presented to the triple 8-bit DACs. Sync and blank information are pipelined along with the pixel information. The sync and blank pins control current sources which are summed to the DAC output currents. The sync current source is summed to the green DAC only. This current is converted to voltages by termination resistors producing the voltages shown in Figure 4.

MPU Port

The ATT20C458 supports a standard MPU interface. The MPU accesses all internal registers and memory through the port. The MPU accesses the color RAM through a separate memory port. This allows MPU memory access, while pixels address the CLUT. Although the color and overlay RAM are dual-ported, it is possible for multiple pixels to be disturbed if the pixel port is reading and MPU port is writing the same RAM location. At most, one pixel is disturbed if the D[7:0] data is valid for the entire time of CE .

The value in the address register and the C0 and C1 control pins determines which of the internal registers or color RAM locations are addressed (see Table 3). AD0 (address bit 0) corresponds to D0 and is the LSB.

Table 3. Address Register Operation

C1	C0	AD[7:0]	Selected
0	0	$XX	Address Register
0	1	$00—$FF	Color RAM
1	1	$00	Overlay Color 0
1	1	$01	Overlay Color 1
1	1	$02	Overlay Color 2
1	1	$03	Overlay Color 3
1	0	$04	Read Mask Register
1	0	$05	Blink Mask Register
1	0	$06	Control Register 1
1	0	$07	Test Register

Accessing Color RAM

To write, the MPU loads the address register with the location of the color or overlay RAM to be written. C0 and C1 determine whether the color or overlay RAM is changed when R/ W is low. The MPU performs three successive write cycles by toggling the CE pin. The red value is written first, followed by green, then blue. After the blue write, the 24-bit word is transferred to the color or overlay RAM at the location pointed to by the address register. The address register increments after the blue write cycle. Blocks of information can be written by continuing to write R, G, B sequences.

To read, the MPU loads the address register with the location of color or overlay RAM to be read. C0 and C1 determine whether the color or overlay RAM is changed when R/ W is high. The MPU performs three successive reads by toggling the CE pin.

Functional Description (continued)

Accessing Color RAM (continued)

The red value is read first, followed by green, then blue. After the blue read, the address register increments. Blocks of information may be read by continuing to read R, G, B sequences.

When the MPU continues to read or write the color RAM after location $FF, the address register cycles back to location $00.

The address register increments for the color and overlay RAM only. The MPU port has a modulo three counter to track the red, green, and blue read/write operations.

When the MPU reads or writes to the address register, the modulo counter is reset to zero. The MPU cannot access the modulo 3 counter bits.

Internal Registers

Table 4. Control Register 1

This register can be read or written to at any time and is not initialized. Bit CR0 is the least significant bit.

Bit	Name/Description
CR7	**Multiplex Select.** Logic 0: 4:1 multiplexing. Logic 1: 5:1 multiplexing. This bit controls whether the pixel and overlay inputs are 4:1 multiplexed or 5:1 multiplexed. If 4:1 multiplexing is chosen, only pixel and overlay inputs A—D are used. Pixel E inputs should be connected to ground. For 5:1 multiplexing, all five pixels A—E are used. If this bit is changed, the pipeline delay must be reset.
CR6	**Overlay Color 0 Enable.** Logic 0: Enable overlay color 0. Logic 1: Enable color RAM. A logic 0 causes overlay color 0 to be displayed when the overlay select bits are 00. A logic 1 causes the color RAM to be displayed.
CR5, CR4	**Blink Rate Select.** Logic 00: 16 on, 48 off (25/75). Logic 01: 16 on, 16 off (50/50). Logic 10: 32 on, 32 off (50/50). Logic 11: 64 on, 64 off (50/50). These 2 bits control the overlay blink rate. Selection 00 corresponds to 16 vertical retrace periods on and 48 off. This results in a 25% blink duty cycle. Bit CR4 is the least significant bit.
CR3	**OL1 Blink Enable.** Logic 0: Disable blinking. Logic 1: Enable blinking. A logic 0 in this bit disables the OL1 plane from blinking. A logic 1 allows the OL1 plane to blink. With blinking enabled, any OL1 input [A:E] will toggle between its value and zero. Bit CR1 must be set to enable OL1 blinking.

Functional Description (continued)

Internal Registers (continued)

Table 4. Control Register 1 (continued)

Bit	Name/Description
CR2	**OL0 Blink Enable.** Logic 0: Disable blinking. Logic 1: Enable blinking. A logic 0 in this bit disables the OL0 plane from blinking. A logic 1 allows the OL0 plane to blink. With blinking enabled, any OL0 input [A:E] will toggle between its value and zero. Bit CR0 must be set to enable OL0 blinking.
CR1	**OL1 Display Enable.** Logic 0: Disable. Logic 1: Enable. A logic 0 in this bit forces the OL1 inputs to zero and disables blinking. A logic 1 enables the value of OL1 to address the overlay registers.
CR0	**OL0 Display Enable.** Logic 0: Disable. Logic 1: Enable. A logic 0 in this bit forces the OL0 inputs to zero and disables blinking. A logic 1 enables the value of OL0 to address the overlay registers.

Functional Description (continued)

Read Mask Register

The read mask register logically ANDs each 8-bit pixel with each bit in the read mask register. A value of $FF allows all pixels to pass unchanged. A zero in any bit position returns a zero from the read mask register regardless of the pixel value for that bit. This register can be read or written to any time and is not initialized.

Blink Mask Register

The blink mask register enables the bit planes to blink at the blink rate specified in control register 1. A logic 1 in any bit position enables blinking for that bit plane, and a logic 0 disables blinking. This register can be read or written to at any time and is not initialized.

Test Register

The test register enables the MPU to read the inputs to the D/A converters. The upper 4 bits, D[7:4], contain 4 bits of color information when reading and are ignored when writing to the test register. The lower 4 bits specify which nibble of which DAC is to be read. (See Table 5.) When the MPU is writing or reading the test register, PCLK must be slowed down to the MPU clock speed or the same pixel and overlay data must be presented to the chip during the entire MPU read cycle. The test register can be written to or read by the MPU at any time and is not initialized.

Table 5. Test Register

Bit	Name/Description
TR[7:4]	**DAC Input Data.** Color nibble at the DAC input.
TR3	**High/Low Nibble Select.** Logic 0: High. Logic 1: Low. A logic 0 selects the low nibble of the red, green, or blue DAC. A logic 1 selects the high nibble.
TR2*	**Blue DAC.** A logic 1 enables the blue DAC inputs to be read.
TR1*	**Green DAC.** A logic 1 enables the green DAC inputs to be read.
TR0*	**Red DAC.** A logic 1 enables the red DAC inputs to be read.

* Enable only one DAC at a time.

Functional Description (continued)

Analog Backend

Every clock cycle, the three DACs each receive 8 bits of information from the color or overlay RAM.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are pipelined to provide synchronization with the pixel data. $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ provide offset currents to the analog outputs to produce the required video levels shown in Figure 4. Only the green DAC contains sync information. Table 6 details how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

The DACs source current in varying amounts. When converted to a voltage through a termination resistance, these signals drive a color CRT monitor. The varying voltage levels from each termination resistance determine the intensity of the primary red, green, and blue colors on the monitor.

The DACs steer current between the output or ground. This eliminates transients caused by turning currents on and off. An on-chip feedback amplifier stabilizes the full-scale current level against supply and temperature variations.

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below:

Green (mA) = [11,294 * V_{REF}(V)] / RSET(Ω)

Red, Blue (mA) = [8,067 * V_{REF}(V)] / RSET(Ω)

V_{REF} is the voltage reference in volts, and RSET is the resistor connected between the full-scale adjust (FS ADJ) pin and ground. The recommended RSET is 523 Ω for RS-343A signals. If an external voltage reference is used, it should be 1.235 V.

For example, the green output current is 26.67 mA and the red and blue outputs are 19.05 mA for the conditions above with RSET = 523 Ω and V_{REF} = 1.235 V. For RS-343A output voltage levels, convert this current to voltage with a doubly terminated 75 Ω system.

Functional Description (continued)

DAC Gain (continued)

RED, BLUE		GREEN	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

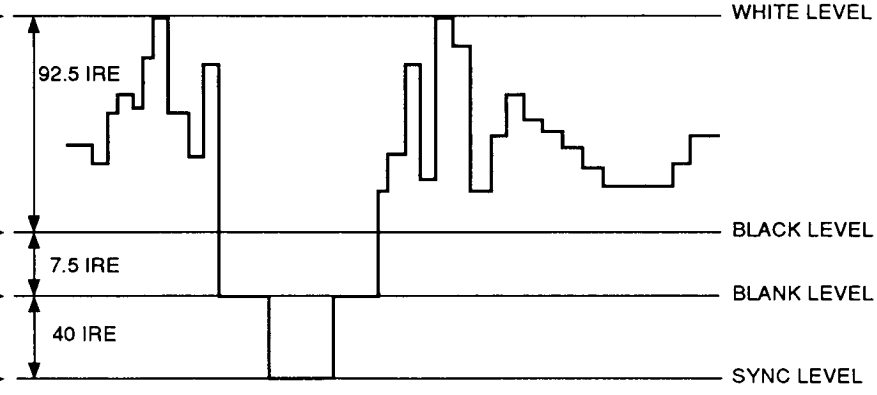


Figure 4. RS-343A Composite Video Output Waveform

Table 6. RS-343A Video Output Truth Table (blank offset current equal to 7.5 IRE)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA) Red or Blue	I_{OUT} (mA) Green
$FF	1	1	WHITE	19.05	26.67
data	1	1	DATA	data + 1.44	data + 9.05
data	0	1	DATA- $\overline{\text{SYNC}}$	data + 1.44	data + 1.44
$00	1	1	BLACK	1.44	9.05
$00	0	1	BLACK- $\overline{\text{SYNC}}$	1.44	1.44
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Notes:
Figure 4 corresponds to RS-343A ratios using an RSET resistor of 523 Ω, a voltage reference of 1.235 V, and 37.5 Ω on the DAC output.
The current values in Table 6 match those of Figure 4 under the same conditions.

Application Information

Initializing the ATT20C458

The following information represents a possible initialization routine following a power-on sequence. Note that the control register bit, CR7, must be written before performing a pipeline reset. If bit CR7 is written after resetting the pipeline delay, the eight pipeline delay is not guaranteed. The following program steps initialize the device for 4:1 multiplexing, no overlays, and no blinking. Write the following values to the control register:

Value (Hex)	Location (Register)	Control Bits C1, C0
04	Address	00
FF	Read Mask	10
05	Address	00
00	Blink Mask	10
06	Address	00
40	Control 1	10
07	Address	00
00	Test	10

Write the following values to the color RAM:

Data Value (Hex)	Location (Register)	Control Bits C1, C0
00	Address	00
Red	Color RAM 0	01
Green	Color RAM 0	01
Blue	Color RAM 0	01
Red	Color RAM 1	01
Green	Color RAM 1	01
Blue	Color RAM 1	01
•	•	•
•	•	•
•	•	•
Red	Color RAM 255	01
Green	Color RAM 255	01
Blue	Color RAM 255	01

Write the following values to the overlay RAM:

Data Value (Hex)	Location (Register)	Control Bits C1, C0
00	Address	00
Red	Overlay RAM 0	11
Green	Overlay RAM 0	11
Blue	Overlay RAM 0	11
Red	Overlay RAM 1	11
Green	Overlay RAM 1	11
Blue	Overlay RAM 1	11
•	•	•
•	•	•
•	•	•
Red	Overlay RAM 3	11
Green	Overlay RAM 3	11
Blue	Overlay RAM 3	11

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

The ATT20C458 should be placed close to the video output connector and the edge card connector. This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

Power Distribution

If individual layers for digital and analog power planes are not possible, separate the power plane into digital and analog areas. Place all digital components over the digital plane and all analog components over the analog plane. The analog components will include the RAMDAC, reference circuitry, comparators, all mixed signal chips (such as a clock synthesizer), and any passive support components for analog circuits.

Application Information (continued)

Power Distribution (continued)

The analog and digital power planes should be connected with at least one ferrite bead across the separation as illustrated in Figure 5. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance higher than the maximum signal frequency on the board but lower than the second harmonic (2X) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz, Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001. If using multiple RAMDACs, each should have its own isolated power tub with a ferrite for each tub. Each RAMDAC will have its own circuitry as shown in Figure 5.

Ground Distribution

For low-frequency designs (<100 MHz), a single solid ground plane can be used. For high-speed designs, the optimal solution is separate digital and analog ground layers. If separate layers are not possible, separate the ground plane into three areas. Create ground areas for digital, analog, and analog RGB termination and return currents. Place all digital components over the digital plane and all analog components over the analog plane. The high-speed digital pixel traces leading up to the RAMDAC should be placed over the digital plane to reduce capacitive coupling into the analog ground layer. The video termination and return circuitry should connect into a separate ground return plane leading to the card edge connector. This isolates the video return currents from the analog and digital circuitry. All three ground planes should be connected together at the card edge connector or at the lowest-impedance point in the ground path.

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Place chip capacitors directly under the RAMDAC on double-sided surface-mount boards.

For axial and radial capacitors, keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT20C458, decouple the Vcc pin pairs (23/27, 35/37, 63/64) to ground with 0.1 µF and 0.01 µF capacitors in parallel (see Figure 5). Power supply noise should be less than 200 mV for a good design. Supply noise greater than 400 mV should be avoided. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figure 5, the COMP pin should be decoupled with a 0.1 µF capacitor to Vcc. For designs showing ghosting or smearing, try adding a parallel COMP capacitance of up to 2.2 µF.

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P[7:0], [A:E] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges because they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Wherever possible, use slower edge rate (3 ns—5 ns) logic such as 74LS or 74ALS devices. If this is not possible, edges can be slowed down using series termination (75 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in. The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled impedance striplines and parallel termination.

Application Information (continued)

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector. Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace may be added to the ground plane or signal layer. This trace connects directly to the ground of the edge card connector.

High-Speed Clock

The ATT20C458 requires a high-speed clock usually consisting of an ECL oscillator operating on a +5 V supply. The clock should be connected as shown in Figure 6. The ECL oscillator connects to a divider circuit. A simple divide-by-four circuit consists of an ECL counter such as the MC10H136. The divider feeds an ECL to TTL converter such as an MC10H350. Reset circuitry stops the ECL clock and $\overline{\text{LOAD}}$ clock to reset the pipeline delay of the RAMDAC. Alternately, the Bt438 clock chip may be used between the oscillator and the RAMDAC. The high-speed differential ECL clocks must be terminated with 220 Ω/330 Ω pull-up/down resistors before connection to the CLOCK and $\overline{\text{CLOCK}}$ inputs.

DAC Outputs

The ATT20C458 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figure 5 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

ESD and Latch-up

Proper power sequencing will help ensure resistance to latch-up. All signal pins should be held low until the Vcc pins rise in voltage. All Vcc pins should be at the same potential. Any signal pin rising 0.5 V above the Vcc level endangers the device to latch-up. This includes signal spikes and overshoot.

Proper ESD handling procedures will help guarantee no electrostatic damage to device inputs either resulting in nonoperating devices or leaky inputs. Leaky inputs can result in erratic behavior. Injured parts may reduce reliability.

System Connection

Figure 6 shows a typical block diagram for the connection of the ATT20C458 in a system. The ECL clock circuitry consists of a high-speed (up to 200 MHz) clock oscillator, divide, ECL to TTL translation circuitry, and reset circuitry.

The pixel and overlay pins connect to banks A through E of DRAM frame buffer memory. Optionally, the overlay inputs may be connected to hardware cursor generation logic. The red, green, and blue analog outputs connect to the system monitor for display. These connections should be coax cable (usually 75 Ω) for maximum fidelity of the pixel waveform and minimum radiated frequencies and reflections.

The MPU port connects to a host processor, which may be a local graphics CPU on the graphics card or subsystem or a remote CPU on an ISA bus. The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ signals may come from a local controller or graphics CPU. The V_{REF}, COMP, and FS ADJ pins are not shown in Figure 6, but are connected as shown in Figure 5.

Application Information (continued)

System Connection (continued)

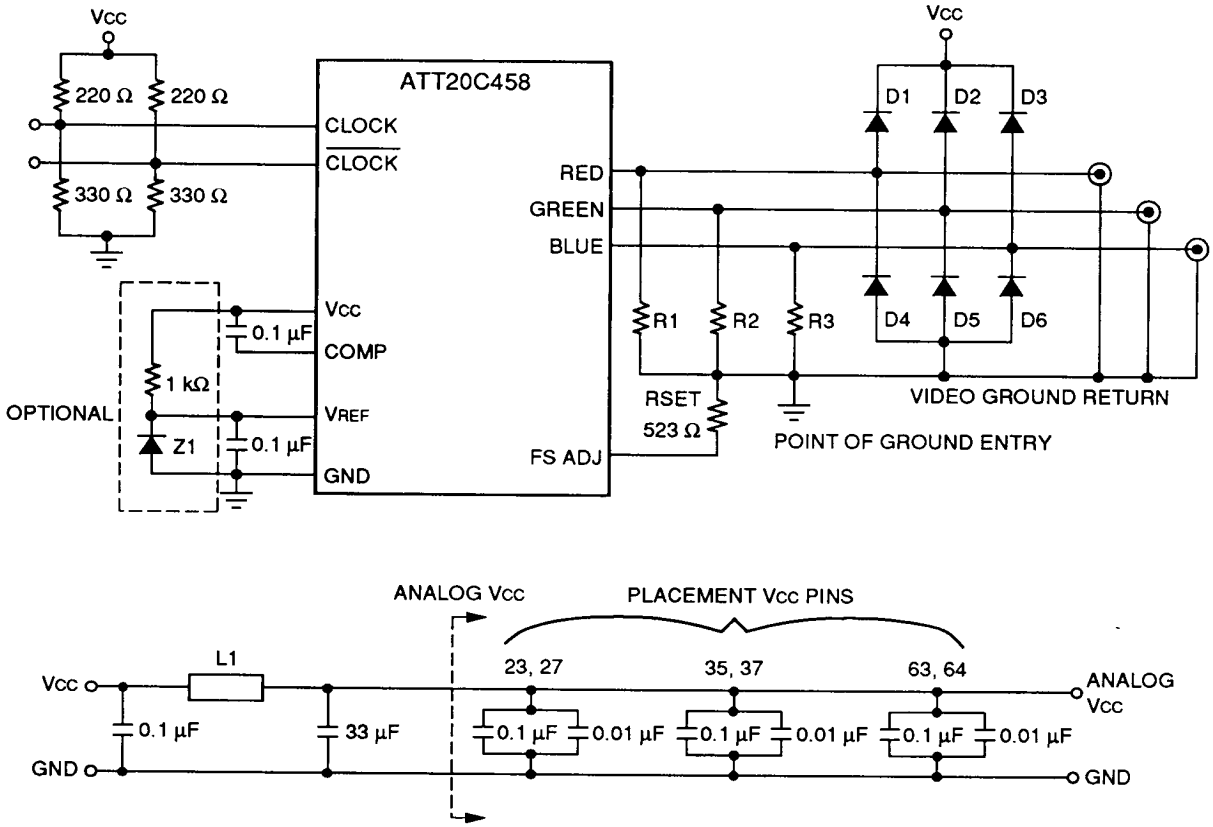


Figure 5. Typical Connection Diagram

Table 7. External Voltage Reference Parts List

Location	Description	Vendor Part Number
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C458.

Application Information (continued)

System Connection (continued)

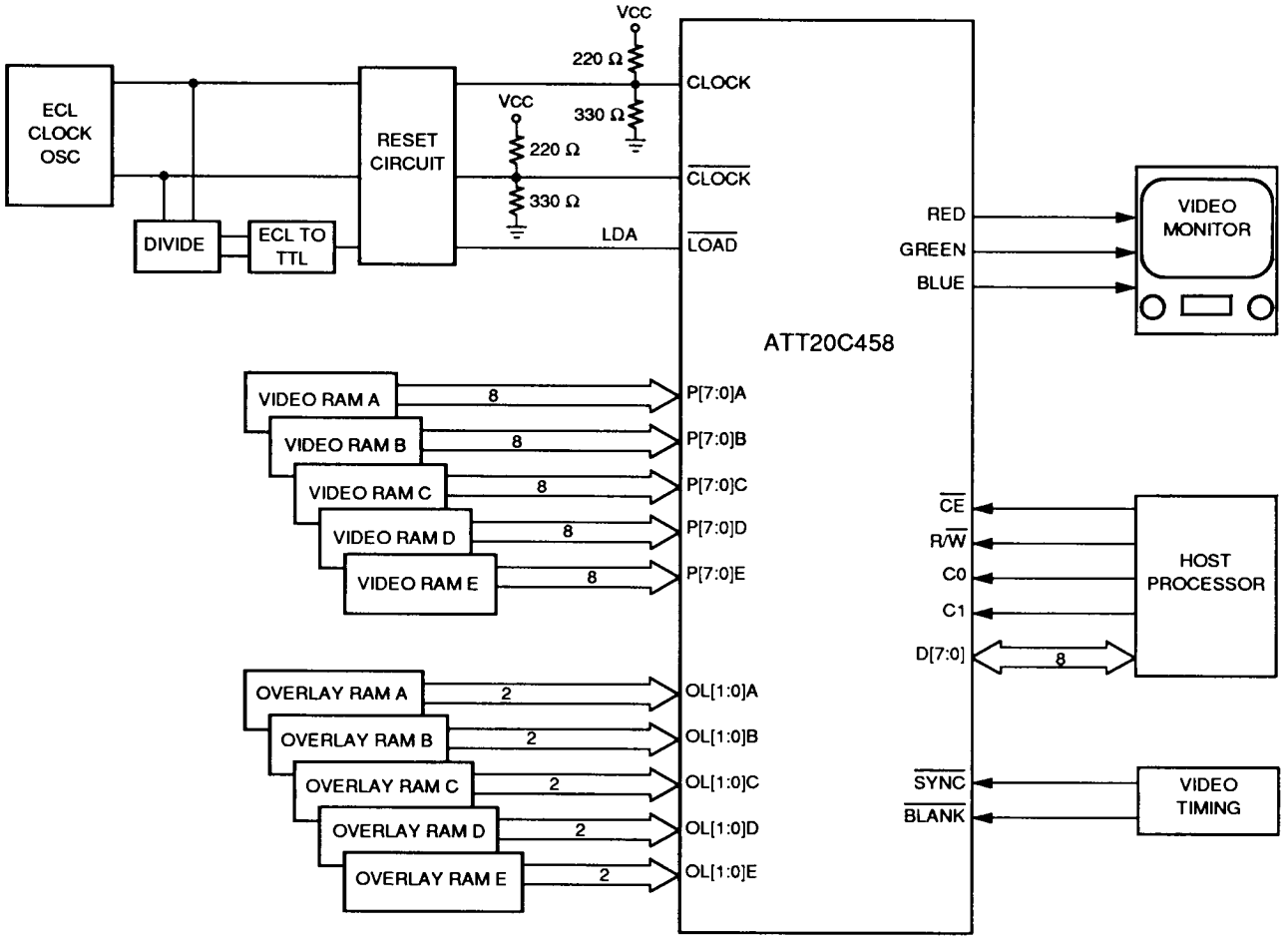


Figure 6. Typical System Block Diagram

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} (measured to GND)	—	—	—	7.0	V
Voltage on Any Signal Pin	—	GND – 0.5	—	V_{CC} + 0.5	V
Analog Output Short Circuit: Duration to Any Power Supply or Common	ISC	—	indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	T_{stg}	–65	—	150	°C
Junction Temperature	T_J	—	—	—	—
Plastic Package	—	—	—	150	°C
Soldering Temperature (5 s, 1/4 in. from pin)	T_{SOL}	—	—	260	°C
Vapor Phase Soldering (60 s)	TV_{SOL}	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.75	5.00	5.25	V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	R_L	—	37.5	—	Ω
External Voltage Reference	V_{REF}	1.2	1.235	1.26	V
FS ADJUST Resistor	RSET	—	523	—	Ω

Electrical Characteristics

Table 8. dc Characteristics

Test conditions (unless otherwise specified): recommended operating conditions with RSET = 523 Ω, V_{REF} = 1.235 V. Since the parameters below are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Parameter	Symbol	Min	Typ	Max	Unit
Digital Outputs D[7:0]:					
Output Voltage:					
Low (I_{OL} = 8 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –8 mA)	V_{OH}	2.4	—	—	V
3-State Current	I_{OZ}	—	—	10	µA
Capacitance	C_{DOUT}	—	10	—	pF
Digital Inputs:*					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}	—	4	10	pF
Clock Inputs:					
Differential Input Voltage	ΔV_{CLK}	0.6	—	6	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{ILC}	—	—	–1	µA
High (V_{IN} = 4.0 V)	I_{IHC}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 4.0 V)	C_{IN}	—	4	10	pF

* Except CLOCK and $\overline{\text{CLOCK}}$.

Electrical Characteristics (continued)

Table 8. dc Characteristics (continued)

Test conditions (unless otherwise specified): recommended operating conditions with RSET = 523 Ω, V_{REF} = 1.235 V. Since the parameters below are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Parameter	Symbol	Min	Typ	Max	Unit
Analog Outputs:					
Resolution (each DAC)	—	8	8	8	bits
Accuracy (each DAC):					
Integral Linearity Error	IL	—	—	±1	LSB
Differential Linearity Error	DL	—	—	±1	LSB
Gain Error	—	—	—	±5	% Gray Scale
Monotonicity	—	—	guaranteed	—	—
Coding	—	—	—	—	Binary
Output Current:					
White Level Relative to Blank	—	17.69	19.05	20.40	mA
White Level Relative to Black	—	16.74	17.62	18.50	mA
Black Level Relative to Blank	—	0.95	1.44	1.90	mA
Blank Level on IOR, IOB	—	0	5	50	µA
Blank Level on IOG or I_{OUT}	—	6.29	7.62	8.96	mA
Sync Level on IOG or I_{OUT}	—	0	5	50	µA
LSB Size	—	—	69.1	—	µA
DAC to DAC Matching	—	—	2	5	%
Output Compliance	V_{OC}	–0.5	—	1.2	V
Output Impedance	RA_{OUT}	—	50	—	kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}	—	13	20	pF
Internal Reference Output (±3%)	V_{REF}	1.2	1.235	1.27	V
Power Supply Rejection Ratio	PSRR	—	0.5	—	%/%Vcc
(COMP = 0.1 µF, f = 1 kHz)	—	—	—	–6	dB

Electrical Characteristics (continued)

Table 9. ac Characteristics

Timing measurements made from the 50% point for rising or falling edges. TTL edges are 0 V to 3 V at 3 ns or less from the 10% to 90% points. ECL edges are Vcc – 0.8 V to Vcc – 1.8 V at 2 ns or less from the 20% to 80% points. The loading of the DACs is 10 pF or less; the loading of D[7:0] is 75 pF or less. Specifications are over full temperature of 0 °C to 70 °C and Vcc = 5.25 V to 4.75 V. Tested under the recommended operating conditions with RSET = 523 Ω, VREF = 1.235.

		200 MHz Devices			170 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Inputs:								
Clock Rate	fmax	—	—	200	—	—	170	MHz
Clock Cycle Time	1	5	—	—	5.88	—	—	ns
Clock Pulse Width High Time	2	2	—	—	2.6	—	—	ns
Clock Pulse Width Low Time	3	2	—	—	2.6	—	—	ns
$\overline{\text{LOAD}}$ Rate	LDmax	—	—		—	—		
4:1		—	—	50	—	—	42.5	MHz
5:1		—	—	40	—	—	34	MHz
$\overline{\text{LOAD}}$ Cycle Time	4							
4:1		20	—	—	23.52	—	—	ns
5:1		25	—	—	29.5	—	—	ns
$\overline{\text{LOAD}}$ Pulse Width High or Low Time	5, 6							
4:1		8	—	—	10	—	—	ns
5:1		10	—	—	12	—	—	ns
Pixel Port:								
Pixel and Control Setup Time	7	3	—	—	3	—	—	ns
Pixel and Control Hold Time	8	2	—	—	2	—	—	ns
DAC Measurements:								
Analog Output Delay	9	—	12	—	—	12	—	ns
Analog Output Rise/Fall Time	10	—	2	—	—	2	—	ns
Analog Output Settling Time	—	—	—	8	—	—	8	ns
Clock and Data Feedthrough	—	—	35	—	—	35	—	pV-s
Glitch Impulse	—	—	50	—	—	50	—	pV-s
Analog Output Skew	—	—	0	2	—	0	2	ns
MPU Port:								
R/$\overline{\text{W}}$, C0, C1 Setup Time	11	0	—	—	0	—	—	ns
R/$\overline{\text{W}}$, C0, C1 Hold Time	12	15	—	—	15	—	—	ns
$\overline{\text{CE}}$ Low Time	13	50	—	—	50	—	—	ns
$\overline{\text{CE}}$ High Time	14	25	—	—	25	—	—	ns
$\overline{\text{CE}}$ Asserted to Data Bus Driven	15	7	—	—	7	—	—	ns
$\overline{\text{CE}}$ Asserted to Data Valid	16	—	—	75	—	—	75	ns
$\overline{\text{CE}}$ Negated to Data Bus 3-Stated	17	—	—	15	—	—	15	ns
Write Data Setup Time	18	35	—	—	35	—	—	ns
Write Data Hold Time	19	3	—	—	3	—	—	ns
Pipeline Delay	—	6	—	10	6	—	10	Clocks
Vcc Supply Current	Icc	—	240	290	—	225	270	mA

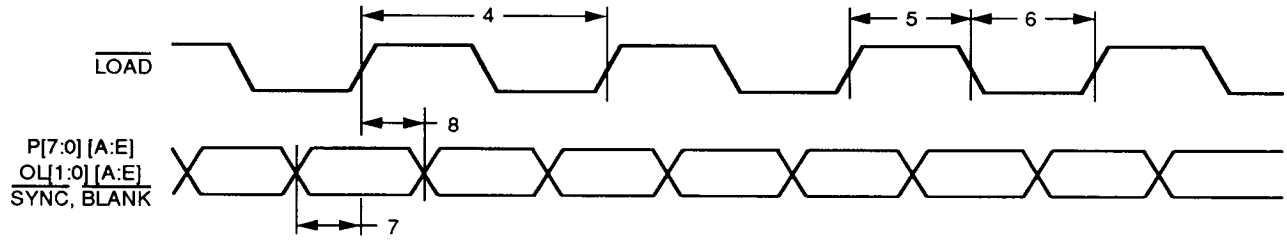
Electrical Characteristics (continued)

Table 9. ac Characteristics (continued)

Timing measurements made from the 50% point for rising or falling edges. TTL edges are 0 V to 3 V at 3 ns or less from the 10% to 90% points. ECL edges are Vcc – 0.8 V to Vcc – 1.8 V at 2 ns or less from the 20% to 80% points. The loading of the DACs is 10 pF or less; the loading of D[7:0] is 75 pF or less. Specifications are over full temperature of 0 °C to 70 °C and Vcc = 5.25 V to 4.75 V. Tested under the recommended operating conditions with RSET = 523 Ω, VREF = 1.235.

		135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Inputs:								
Clock Rate	fmax	—	—	125	—	—	110	MHz
Clock Cycle Time	1	7.4	—	—	9.09	—	—	ns
Clock Pulse Width High Time	2	3	—	—	4	—	—	ns
Clock Pulse Width Low Time	3	3	—	—	4	—	—	ns
$\overline{\text{LOAD}}$ Rate	LDmax							
4:1		—	—	31.25	—	—	27.5	MHz
5:1		—	—	25	—	—	22	MHz
$\overline{\text{LOAD}}$ Cycle Time	4							
4:1		29.6	—	—	36.36	—	—	ns
5:1		37	—	—	45.45	—	—	ns
$\overline{\text{LOAD}}$ Pulse Width High or Low Time	5, 6							
4:1		12	—	—	15	—	—	ns
5:1		15	—	—	18	—	—	ns
Pixel Port:								
Pixel and Control Setup Time	7	3	—	—	3	—	—	ns
Pixel and Control Hold Time	8	2	—	—	2	—	—	ns
DAC Measurements:								
Analog Output Delay	9	—	12	—	—	12	—	ns
Analog Output Rise/Fall Time	10	—	2	—	—	2	—	ns
Analog Output Settling Time	—	—	—	8	—	—	8	ns
Clock and Data Feedthrough	—	—	35	—	—	35	—	pV-s
Glitch Impulse	—	—	50	—	—	50	—	pV-s
Analog Output Skew†	—	—	0	2	—	0	2	ns
MPU Port:								
R/$\overline{\text{W}}$, C0, C1 Setup Time	11	0	—	—	0	—	—	ns
R/$\overline{\text{W}}$, C0, C1 Hold Time	12	15	—	—	15	—	—	ns
$\overline{\text{CE}}$ Low Time	13	50	—	—	50	—	—	ns
$\overline{\text{CE}}$ High Time	14	25	—	—	25	—	—	ns
$\overline{\text{CE}}$ Asserted to Data Bus Driven	15	7	—	—	7	—	—	ns
$\overline{\text{CE}}$ Asserted to Data Valid	16	—	—	75	—	—	75	ns
$\overline{\text{CE}}$ Negated to Data Bus 3-Stated	17	—	—	15	—	—	15	ns
Write Data Setup Time	18	35	—	—	35	—	—	ns
Write Data Hold Time	19	3	—	—	3	—	—	ns
Pipeline Delay	—	6	—	10	6	—	10	Clocks
Vcc Supply Current	Icc	—	205	250	—	195	240	mA

Timing Characteristics

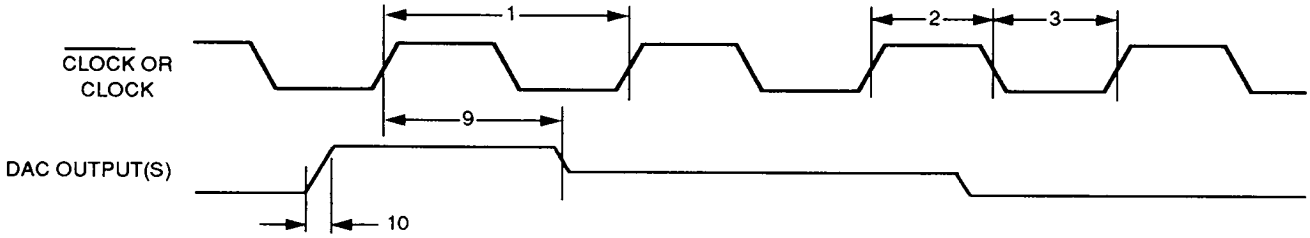


Notes:
Rise/fall measurements made from 10% to 90% points.

Settling time measured from midpoint of full-scale transition to the point where the waveform is inside a ±1 LSB error band.

All timing delays are measured from the 50% points.

Figure 7. Video Input Timing



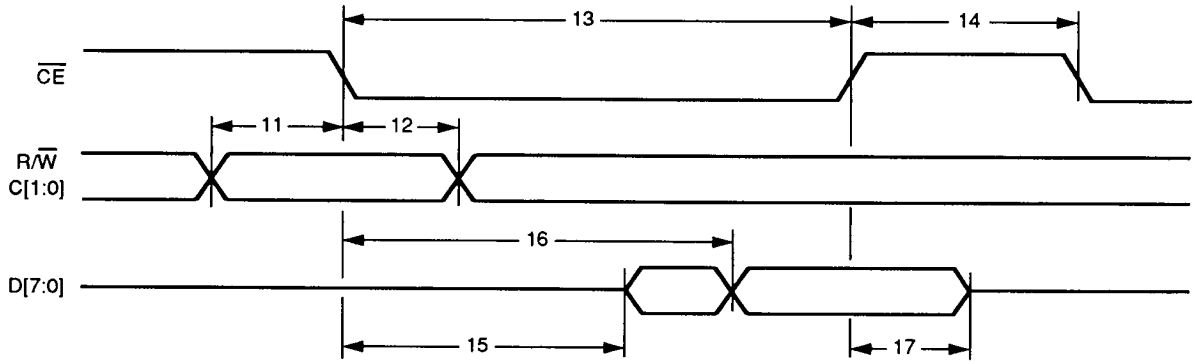
Notes:
Rise/fall measurements made from 10% to 90% points.

Settling time measured from midpoint of full-scale transition to the point where the waveform is inside a ±1 LSB error band.

All timing delays are measured from the 50% points.

Figure 8. Video Output Timing

Timing Characteristics (continued)

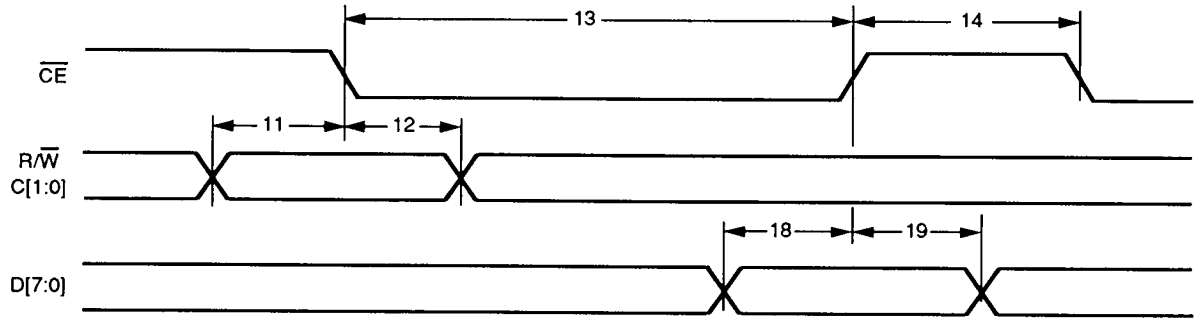


Notes:
Rise/fall measurements made from 10% to 90% points.

Settling time measured from midpoint of full-scale transition to the point where the waveform is inside a ±1 LSB error band.

All timing delays are measured from the 50% points.

Figure 9. MPU Read Cycle



Notes:
Rise/fall measurements made from 10% to 90% points.

Settling time measured from midpoint of full-scale transition to the point where the waveform is inside a ±1 LSB error band.

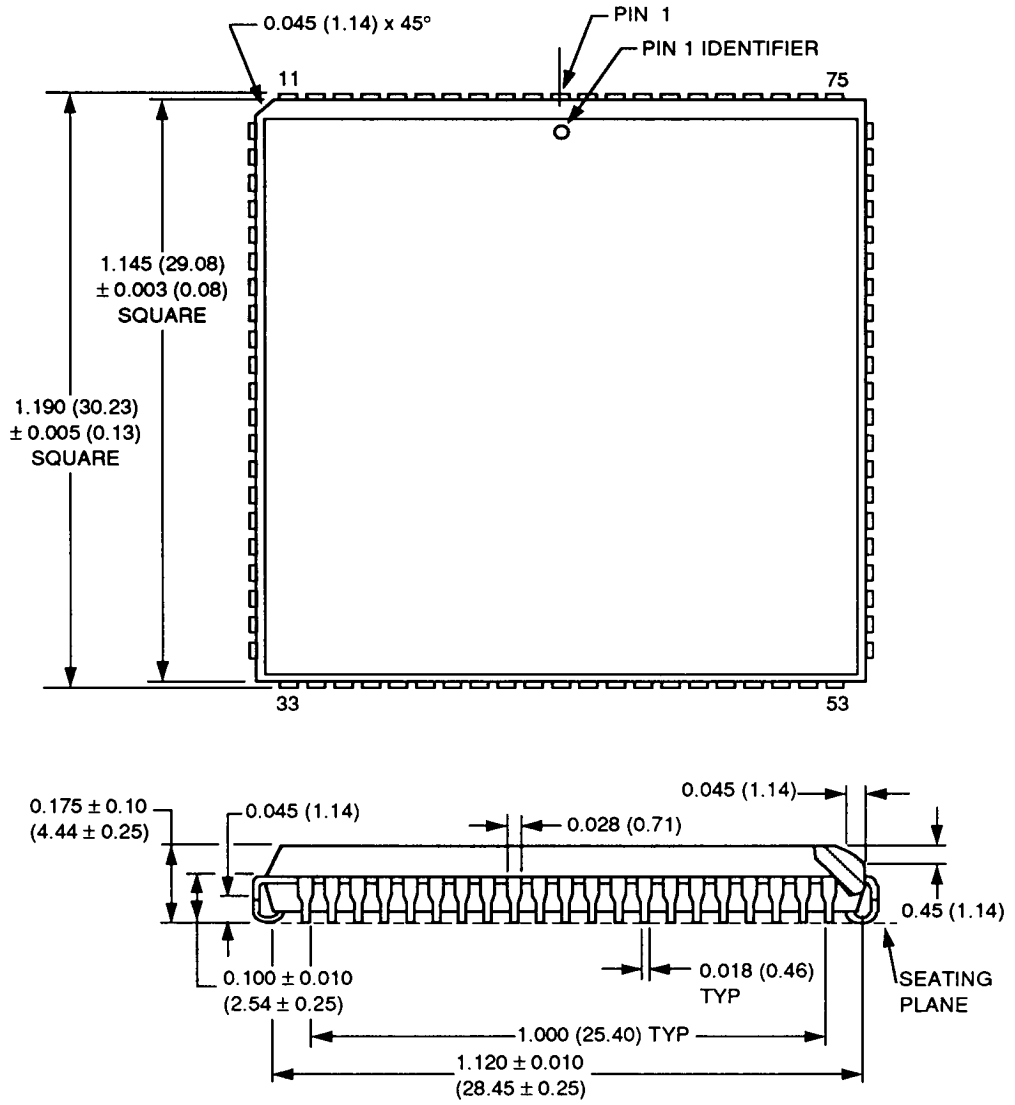
All timing delays are measured from the 50% points.

Figure 10. MPU Write Cycle

Outline Diagram

84-Pin PLCC

Dimensions are in inches and (millimeters).



Ordering Information

Device*	Speed	Package Types
ATT20C458-XXM84	200/170/135/110 MHz	84-Pin PLCC

* XX refers to speed grade:
20 = 200 MHz
17 = 170 MHz
13 = 135 MHz
11 = 110 MHz

For additional information, contact your AT&T Account Manager or the following:
U.S.A.: AT&T Microelectronics, Dept. AL-520404200, 555 Union Boulevard, Allentown, PA 18103
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