

PRODUCT OVERVIEW

The Vadem VG-469 is a compact, highly integrated PC Card controller chip implementing the PC Card Standard along with ExCA™ extensions. It is register-compatible to the Intel® 82365SL. Supporting two PC Card sockets, it is uniquely designed for space-limited, cost-sensitive applications where battery life is an important factor. For systems requiring more than two sockets, the VG-469 can be cascaded to support up to four sockets without external logic. With external decoder logic, unlimited cascading is possible. Typical VG-469 applications include small notebook computers, palmtops and other personal information devices.

The VG-469 supports the system bus timing of standard ISA and EISA architectures. A programmable configuration mechanism allows the system manufacturer to control many PC Card setup parameters in software or firmware.

The VG-469 supports mixed voltage operation. The internal logic, the ISA bus interface and each of the two PC Card sockets can be independently operated at either 3.3V or 5V.

Power management based on activity monitoring and the VG-469's very low current-draw minimize the demand for battery power.

Jumperless add-in card installation is supported by the VG-469 with the on-chip implementation of the Plug and Play ISA version 1.0a, which lets the software relocate the VG-469 registers from the default at 3E0h/3E1h or 3E2h/3E3h.

PRODUCT FEATURES

- 208-pin chip provides full ExCA implementation of two PC Card sockets.
 - ⇒ Complies with PC Card Standard, and backward compatible to PCMCIA 2.1/JEIDA 4.1.
 - ⇒ Supports both memory cards and I/O cards.
 - ⇒ Supports PCMCIA-ATA specification.
 - ⇒ Memory-saving execute-in-place standard (XIP).
 - ⇒ Supports overlapping I/O windows across sockets and duplicate I/O cards via *INPACK signal.
 - ⇒ Cascadable up to four sockets without “glue,” unlimited cascading with external logic.
- Register-compatible with Intel 82365SL.
- Five mappable memory windows and two I/O windows for each socket.
- Internal buffering supports ‘hot’ insertion and removal of cards.
- Integrated timer supports power management based on activity monitoring.

Preface

- Socket activity LED support.
- Plug and Play ISA version 1.0a with EEPROM support.
 - ⇒ Allows dynamic relocation of VG-469 in the address space to avoid conflict with system resources.
 - ⇒ Allows use of as many PCMCIA controllers as needed.
 - ⇒ Simplifies interface to and design of docking stations.
- Mixed voltage operation.
 - ⇒ Supports 3.3V or 5V ISA bus interface.
 - ⇒ Supports 3.3V or 5V PCMCIA socket interface.
 - ⇒ Internal logic operates at either 3.3V or 5V.
- Built-in over-voltage protection logic.
 - ⇒ Prevents damage to low-voltage cards (3.3V and future X.XV).
- Optional buffer directional/enable control for buffered cable driving.
- Support for PC Card DMA operation.
- Includes two GPIO pins.

This chapter provides the pin assignment, signal description, and pin descriptions for the VG-469 PC Card Socket Controller.

DEFAULT PIN ASSIGNMENT



Signal Description

Pin #	Signal Names	Typ	Characteristics	# Pins
204	AEN	I	TTL Compatible	1
205	BALE	I	TTL Compatible	1
54, 125	BVD1 (*STSCHG/*RI)	I	Schmitt Trigger w/pull-up	2
52, 123	BVD2 (*SPKR)	I	Schmitt Trigger w/pull-up	2
15, 19, 21, 23-26, 28, 29, 31, 33- 41, 43, 44, 46, 48, 50, 51, 53, 86, 90, 92, 94- 99, 102, 104-107, 109-115, 117, 119, 121, 122, 124	CA[25:0]	O	2mA Tri-State	52
63, 1, 134, 141	*CD[2:1]	I	Schmitt Trigger w/pull-up	4
18, 11, 89, 83	*CE[2:1]	O	2mA Tri-State	4
187	CLK	I	TTL Compatible	1
2, 4-10, 12, 13, 55-58, 60, 62, 73, 76-82, 84, 85, 101, 126-130	D[15:0]	I/O	I = TTL Compatible O = 2 mA Tri-state	32
14, 42, 75, 131, 156, 166, 188	GND			7
67	A_GPIO	I/O	I = TTL Compatible O = 12 mA Tri-state	1
68	B_GPIO	I/O	I = TTL Compatible O = 12 mA Tri-state	1
49, 120	*INPACK	I	TTL Compatible w/pull-up	2

Pin #	Signal Names	Typ	Characteristics	# Pins
152	*INTR (E2SK)	I/O	I = TTL Compatible O = 2 mA Tri-state	1
150	IOCHRDY	O	16 mA Tri-State	1
148	*IOCS16	O	16 mA Tri-State	1
20, 91	*IORD	O	2 mA Tri-State	2
22, 93	*IOWR	O	2 mA Tri-State	2
138	IRQ12(LED)	O	12 mA Tri-State	1
136-137, 139,140,146 144-142	IRQ[15, 14, 11:9, 5:3]	O	2 mA Tri-State	8
145	IRQ7(*HDACK)	I/O	I = TTL Compatible O = 2mA Tri-State	1
181-175	LA[23:17]	I	TTL Compatible	7
149	*MEMCS16	O	16 mA Tri-State	1
174	*MEMR	I	TTL Compatible	1
173	*MEMW	I	TTL Compatible	1
16, 87	*OE	O	2mA Tri-State	2
32, 103	RDY/*BSY (*IREQ)	I	Schmitt Trigger w/pull-up	2
3, 74	*REG	O	2mA Tri-State	2
45, 116	RESET	O	2mA Tri-State	2
189	RESETDRV	I	Schmitt Trigger	1
202-192, 190, 186- 183	SA[16:0]	I	TTL Compatible	17
182	*SBHE	I	TTL Compatible	1
206	*SIOR	I	Schmitt Trigger	1
207	*SIOW	I	Schmitt Trigger	1

Chapter 1
Introduction

VADEM VG-469
PC Card Socket Controller

Pin #	Signal Names	Typ	Characteristics	# Pins
155, 154, 157-162, 172-170, 168, 167, 165-163	SD[15:0]	I/O	I = TTL Compatible O = 12 mA Tri-state	16
153	*SPKROUT (E2DIO)	I/O	I = TTL Compatible O = 2 mA Tri-state	1
66, 64, 69, 71	VCCEN[1:0]	I/O	I = TTL Compatible O = 2 mA Tri-state	4
17, 59	A_VCC			2
88, 108	B_VCC			2
27	CORE_VCC			1
72, 169, 191	ISA_VCC			3
65, 70	VPPEN1	O	2 mA Output	2
151, 135	*VS2(VPPEN0)	I/O	I = TTL Compatible O = 12 mA Tri-state	2
208	A_*VS1(*VSENBL)	I/O	I = TTL Compatible O = 2 mA Tri-state	1
133	B_*VS1 (E2CS/*HDACK)	I/O	I = TTL Compatible O = 2 mA Tri-state	1
47, 118	*WAIT	I	TTL Compatible w/pull-up	2
30, 100	*WE/*PRGM	O	2 mA Tri-State	2
61, 132	WP (*IOIS16)	I	TTL Compatible w/pull-up	2
147	*ZWS	O	16 mA 5V Tri-State	1

Pin Descriptions

Symbol	Type	Pin No.	Description
AEN	I	204	System Address Enable. High during DMA cycles, low otherwise.
BALE	I	205	Bus Address Latch Enable. An active high input used to latch LA[23:17] at the beginning of a bus cycle.
BVD1 (*STSCHG/*RI)	I	54,125	<p>If BVD1 is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost.</p> <p>For I/O PC Cards, this signal is held high when either or both the Signal on Change bit and Changed bit in the Card Status Register on the PC Card are set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP, and CBSYRDY in the Pin Replacement Register on the PC Card. Or this pin is connected to Ring Indicate, which is qualified by Ring Indicate Enable to become *RIO. *RIO can be routed to one of the following output pins: A_GPIO, B_GPIO or *INTR.</p>
BVD2 (*SPKR)	I	52,123	<p>BVD1 and BVD2 are generated by memory PC Cards with onboard batteries. These signals indicate the health of the battery. Both are asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery should be replaced, although data integrity on the memory PC Card is still assured.</p> <p>When the I/O interface is selected, BVD2 may be used to provide a single amplitude Digital Audio waveform intended to be passed through to the system's speaker without signal conditioning. If the PC Card is the DMA device, this pin can be redefined as *DREQ input from the card.</p>

Symbol	Type	Pin No.	Description
CA[25:0]	O	15, 19, 21, 23-26, 28, 31, 33-41, 43, 44, 46, 48, 50, 51, 53, 86, 90, 92, 94-99, 102, 104-107, 109-115, 117, 119, 121, 122, 124	Card Address
*CD[2:1]	I	63, 1, 134, 141	Detects proper card insertion. The signals are connected to ground internally on the PC Card and will be forced low whenever a card is placed in a host socket. Status is available to software through the Interface Status Register.
*CE[2:1]	O	18, 11, 89, 83	Active low card enable signals. *CE1 is used to enable even bytes. *CE2 for odd bytes. A multiplexing scheme based on A0, *CE1, *CE2 allows 8-bit hosts to access all data on Card Data [7:0] if desired.
CLK	I	187	System Clock
D[15:0]	I/O	2, 4-10, 12, 13, 55-58, 60, 62, 73, 76-82, 84, 85, 101, 126-130	Card Data
A_GPIO	I/O	67	General purpose input/output. May also be used for one of several purposes. <ul style="list-style-type: none"> - An active low input indicates that Vpp power line has reached the user specified range. - An input indication a card eject or card insertion pending. - An input source for generating a card status change interrupt. - Power down control input. - Programmable chip select output. - Option A_VPPEN0. - *LED output. - *RIO output. - Host TC (Terminal Count) input in a DMA operation. - Zoom Video Buffer Control.

Symbol	Type	Pin No.	Description
B_GPIO	I/O	68	General purpose output. May also be used for one of several purposes. <ul style="list-style-type: none"> - Programmable chip select output. - Optional B_VPPEN0. - *LED output. - *RIO output. - HDRQ output in a DMA operation. - Resistor strapping input during RESETDRV to indicate the voltage of the ISA bus; high for 3.3 volt and low for 5 volt.
*INPACK	I	49,120	Input Acknowledge. Asserted by some PC Cards during I/O read cycles. This signal is used by the VG-469 to control the enable of its input data buffer between the card and CPU. If the PC Card is the DMA device, this pin can be redefined as *DREQ input from the card.
*INTR (E2SK)	I/O	152	Interrupt Request output: Active low output requesting a nonmaskable interrupt to the CPU. Ring Indicator from PC Card can be steered to this pin. If B_*VS1 is strapped low in the extended configuration, this pin becomes the clock output to the external serial EEPROM for supporting Plug and Play ISA. Also, a resistor strapping input during RESETDRV to select the internal register address.
IOCHRDY	O	150	I/O Channel Ready. This active high signal indicates that the current I/O bus cycle has completed. When a PC Card needs to extend a Read or Write cycle, the VG-469 pulls IOCHRDY low. IOCHRDY can be deasserted by either *WAIT, or by programming to add wait states for 16-bit memory and I/O cycles.
*IOCS16	O	148	This active low I/O 16-bit chip select signal indicates to the host system the current I/O cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.

Symbol	Type	Pin No.	Description
*IORD	O	20, 91	I/O Read signal is driven active to read data from the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
*IOWR	O	22, 93	I/O Write signal is driven active to write data to the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
IRQ[14, 9, 5:3]	O	137, 146, 144-142	Interrupt Request signals to the ISA bus.
IRQ7	I/O	145	By default this is IRQ7 to the ISA bus. In external mode when Plug and Play is enabled, this pin can become *HDACK from the DMA controller if bit 7 of the Extended Mode Register-A is written with a 1.
IRQ[11:10]	O	139, 140	By default these are the Interrupt Request signals to the ISA bus. Alternately, these become the VPPEN0 outputs if bit[1:0] of the Extended Mode Register-A are so programmed.
IRQ12	O	138	By default this is the Interrupt Request to the ISA bus. It becomes *LED if LED function is enabled and no GPIO is programmed as RIO.
IRQ15	O	136	By default this is the Interrupt Request to the ISA bus. It becomes *RIO if RIO function is enabled and no GPIO is programmed as RIO.
LA[23:17]	I	181-175	Local Address bus used to address memory devices on the ISA bus. Together with the system address signals, they address up to 16MB on the ISA bus.
*MEMCS16	O	149	This active low 16-bit memory chip select signal indicates to the host system that the current memory cycle is a 16-bit access.
*MEMR	I	174	Active low command signal indicates a memory read cycle on the ISA bus.
*MEMW	I	173	Active low command signal indicates a memory write cycle on the ISA bus.

Symbol	Type	Pin No.	Description
*OE	O	16, 87	Active low signal used to gate memory reads from memory cards.
RDY/*BSY (*IREQ)	I	32,103	Memory PC Cards drive Ready / *Busy low to indicate that the memory card circuits are busy processing a previous write command. It is set high when they are ready to accept a new data transfer command. For I/O PC Cards, this pin is used as an interrupt request and driven low to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested.
*REG	O	3, 74	Select attribute memory. This signal is set inactive (high) for all accesses to common memory of a PC Card. When it is active, access is limited to Attribute Memory when *WE or *OE are active, and to I/O ports when *IORD or *IOWR are active. I/O PC Cards will not respond to *IORD or *IOWR when the *REG signal is inactive. During ISA DMA operations the *REG signal is inactive. If the PC Card is the DMA device, this pin is redefined as DACK output to the socket.
RESET	O	45,116	Provides a hard reset to a PC Card and clears the Card Configuration Option Register, thus placing card in an unconfigured (memory interface) state.
RESETDRV	I	189	Active high indicates a main system reset.
SA[16:0]	I	203-192, 190, 186-183	System Address bus used to address memory and I/O devices on the ISA bus. These signals are latched and are valid throughout the bus cycle.
*SBHE	I	182	System Byte High Enable. When asserted, this active low signal indicates that a data transfer is occurring on the upper byte of the system data bus.

Symbol	Type	Pin No.	Description
SD[15:0]	I/O	155, 154, 157-162, 172-170, 168, 167, 165-163	System Data Bus.
*SIOR	I	206	Active low command signal indicates an I/O read cycle on the ISA bus.
*SIOW	I	207	Active low command signal indicates an I/O write cycle on the ISA bus.
*SPKROUT (E2DIO)	I/O	153	Digital audio signal which provides a single amplitude (digital) audio waveform to drive the system's speaker. Passes through *SPKR from an I/O PC Card. This signal must be held high when no audio signal is present. Also, a resistor strapping input during RESETDRV to determine if the chip is operated in extended configuration for cable driving. While in extended configuration, if B_*VS1 is strapped low, this pin becomes the data port to and from the external serial EEPROM for supporting Plug and Play ISA.
VCCEN[1:0]	I/O	66, 64, 69, 71	Power Control signals for card Vcc. These are resistor strapped to the level which turns off the Vcc Switch and are input during RESETDRV to determine the polarity of the Vcc Enable functions.
VPPEN1	O	65, 70	Power Control signal for card Vpp.

Symbol	Type	Pin No.	Description
*VS2	I/O	151, 135	Voltage Sense 2 inputs, which are connected to pin 57 of the PCMCIA sockets. Together with *VS1, these pins determine the operating voltage of the card. In a 5-volt only system where the voltage sensing is not needed, or in a system which provides limited voltage sensing capability (5 volt versus 3.3 volt, but not X.X volt) these pins can be redefined as VPPEN0 outputs if bit [1:0] of the Extended Mode Register are so programmed. In the extended configuration where capable driving is required, these pins become ISA buffer direction controls (HBUFDIR and LBUFDIR) if B_*VS2 is strapped low; or become socket B buffer enable (*BSIGEN) and direction control (DIR) if B_*VS2 is strapped high.
A_*VS1	I/O	208	Voltage Sense 1 input, which is connected to pin 43 of the A socket. It determines the operating voltage of the card along with *VS2. If external voltage sense logic is implemented and bit 2 of the Extended Mode Register is set, this pin becomes *VSENBL output for external buffer enable.

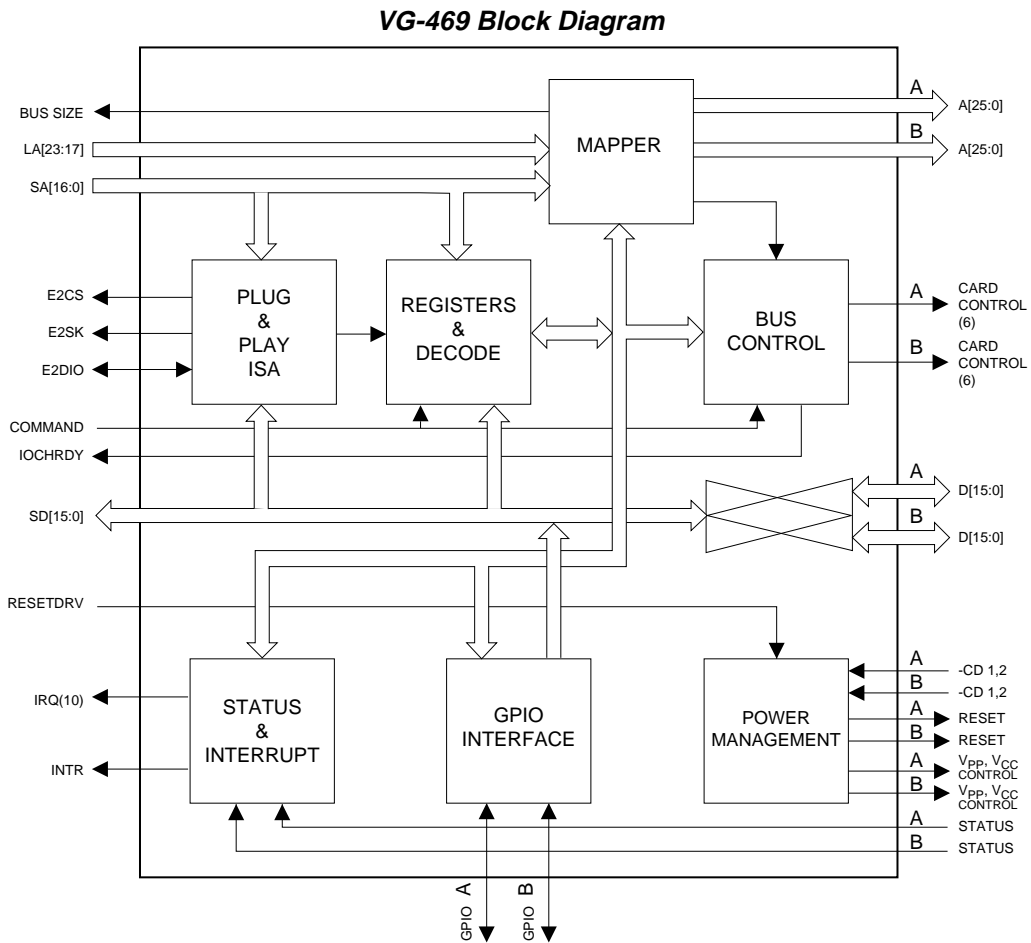
Symbol	Type	Pin No.	Description
B_*VS1 (E2CS/*HDACK)	I	133	<p>Voltage Sense 1 input, which is connected to pin 43 of the B socket. It determines the operating voltage of the card along with *VS2. If the card is a DMA device, and the DMA function is activated this pin becomes *HDACK which is passed through to *REG (redefined as *DACK) in one of three cases:</p> <p>(1) 5 volt only system.</p> <p>(2) The chip is in the basic configuration (*SPKROUT strapped high) and external voltage sense is used.</p> <p>(3) The chip is in the extended configuration (*SPKROUT strapped low) and this pin is strapped high.</p> <p>If this pin is strapped low in the extended configuration this pin becomes the chip select for the external serial EEPROM to support the Plug and Play ISA.</p>
*WAIT	I	47, 118	<p>This signal is driven by the PC Card to delay completion of the memory or I/O cycle in progress.</p>
*WE/*PRGM	O	30, 100	<p>The host uses *WE for gating memory write data, and for memory PC Cards that employ programmable memory.</p>

Symbol	Type	Pin No.	Description
WP (*IOIS16)	I	61, 132	<p>Reflects the status of the Write Protect switch on some memory PC Cards. If the memory PC Card has no write protect switch, the card will connect this line to ground (the card can always be written) or to Vcc (permanently write protected).</p> <p>When the I/O interface is selected, this pin is used for the "I/O is 16-bit Port" function: asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16-bit access. If this signal is not asserted during a 16-bit I/O access, the system will generate 8-bit references to the even and odd byte of the 16-bit port being accessed. If the 8-bit window size is selected, *IOIS16 is ignored. If the PC Card is the DMA device, this pin can be redefined as *DREQ input from the card.</p>
*ZWS	O	147	<p>Zero Wait State. An active low output indicates that the PC Card wishes to terminate the present bus cycle without inserting additional wait states. This cycle will not be driven during a 16-bit I/O access.</p>

Chapter 2 Functional Description

VADEM VG-469 PC Card Socket Controller

This chapter provides a description of the functional blocks that comprise the VG-469 PC Card Socket Controller. Major functional blocks of the VG-469 include the ISA bus interface, Plug and Play ISA, PC Card socket interface, memory and I/O window mapping, power management support, interrupt handling, configuration, status and control registers and GPIO.



ISA INTERFACE

The VG-469 has built in a standard ISA interface, including 10 IRQs. If DMA capability is needed in the system design, the chip can be configured to provide one set of DMA handshake signals plus Terminal Count. The VG-469 also provides special signals such as *SPKROUT, *INTR, *RIO, and *LED, the latter two can be brought out through several options.

The ISA interface is selectable to work with either 5V or 3.3V ISA bus. This will be discussed further in section titled 'Mixed Voltage Operation'.

PCMCIA/JEIDA PC CARD SOCKET INTERFACE

The 68-pin PCMCIA/JEIDA PC Card socket interface consists of 60 signals and 8 power connections. A single VG-469 supports two PC Card sockets directly. Up to four PC Card sockets may be supported by cascading VG-469's. If an external decoder is used, any number of sockets can be supported. Each VG-469 is uniquely selected using pull-up/pull-down resistors

Control/Status Signal Multiplexers

The VG-469 supports two PC Card types (either memory or I/O) interchangeably. A number of the PC Card signals have different uses based on the PC Card type. The VG-469 incorporates multiplexers to redirect the appropriate signals that are defined differently for memory and I/O PC Cards. These signals are configured correctly based upon the setting of the PC Card type bit in the Interrupt and General Control Register.

PC Card Status

The status of the PC Card including detection of card insertion or removal, memory write protect status, battery voltage warnings, PC Card power status, and Ready/Busy is accessible through the interface status register. A change in status can cause a card status change interrupt (such as when a PC Card is inserted or removed). The various sources of the interrupt may be enabled separately.

Mixed Voltage Operation

The VG-469 has four power planes: ISA bus interface, socket A interface, socket B interface, and the internal core, each can be independently connected to 3.3V or 5.0V. The voltage levels for the ISA interface and internal core are fixed at the board level, while those for the socket interface are set after a PC Card is inserted. Two card voltage sense pins: *VS1 and *VS2, determine the voltage to be applied according to the following table:

	5.0 Volt Only	3.3V Capable	X.XV Only	X.X/3.3 Volt Capable
*VS1	H	L	H	L
*VS2	H	H	L	L

X.X volt is a future Vcc level yet to be defined.

In a mixed voltage implementation, the socket is not powered without a card in the socket. After a card is inserted, the system reads the state of the two voltage sense pins and possibly CIS to determine the voltage to be applied to the card. Then it writes to the Power and RESETDRV Control Register, bit 4, which enables the outputs to the voltage switch. To provide the flexibility of interfacing different polarity voltage switches, the voltage enable pins must be resistor-strapped to the level that turns off the switch. The voltage switch supplies power to the socket as well as the VG-469 socket interface.

Since X.X volt is undefined and is not supported by the current generation of voltage switch devices, VG-469 uses the X.X volt combination of VCCEN[1:0] pins to turn off the socket voltage.

The ISA bus voltage level is indicated by a resistor strapping on B_GPIO. The value of this pin is latched at the falling edge of RESETDRV, and is readable at bit D7 of Card Voltage Select Register.

Strapping Table for ISA Bus Voltage Indication

B_GPIO Resistor	ISA Bus Voltage
Pull-up	3.3 volt
Pulldown	5 volt

MEMORY AND I/O MAPPING

Multiple PC Cards in a system can conflict if they try to utilize the same system memory and I/O range. The VG-469 allows the operating system to map PC Card memory into up to five separate memory ranges, and PC Card I/O into two separate I/O ranges, thus avoiding system configuration conflicts.

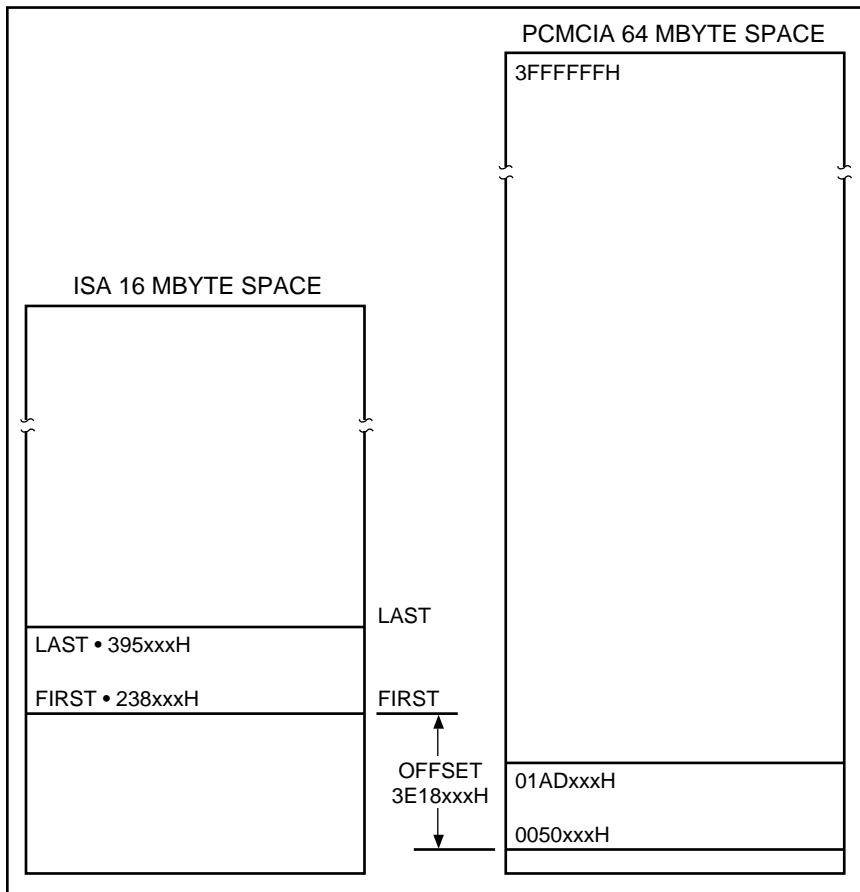
The VG-469 provides memory paging and memory address mapping for both PC Card attribute and common memory and I/O address mapping. The VG-469 includes registers which provide access to the card information structure and card configuration registers within PC Card's attribute memory described by the PCMCIA/JEIDA PC Card Standard.

PC Card Memory Addressing

The VG-469 provides logic to map portions of the 64MB common memory and/or 64MB attribute memory spaces found on PC Cards into the smaller 16MB system (ISA) address space. These mapping functions allow expansion of the system address space up to the full 64MB PC Card capability.

The VG-469 supports 5 independently enabled and controlled system memory address mapping windows. Each system memory window may map into either the common or attribute memory space of the PC Card and may independently control memory data bus width, system bus wait states, software write protect, and card enable.

Mapping of each system memory window starts and stops on any 4K byte boundary of ISA system memory above 64K. The VG-469 does not allow mapping of a system memory window between 0 and 64K in the system address space. Only I/O address windows are allowed to be mapped into that range. This limitation allows the VG-469 to resolve conflicts when accessing I/O PC Cards that contain memory.



Opening a Window

To open a window, software sets the system memory start address (Start), system memory stop address (Stop), and PC Card memory offset appropriately. If Start = Stop, the minimum size of

4K bytes is realized. The offset address is set by the software to be equal to the 2's complement of the difference between Start and the start address of the PC Card, and is added to the system address to generate the address for the PC Card.

PC Card memory is accessed only when all of the following conditions are satisfied:

1. The system memory address mapping window is enabled.
2. The system memory address is greater than or equal to the system memory address mapping start register A[23:12].
3. The system memory address is less than or equal to the system memory address mapping stop register A[23:12].

All the system memory address mapping windows can be configured by software to be independently used, or can be used together for special memory mapping requirements, like LIM/EMS or XIP.

Multiple ROM executable images on a single PC Card may be organized by the system memory address mapping windows. These images must be aligned to start on a 4 K byte boundary of the memory PC Card. Software can access these ROM executable images by setting the size of a system memory address mapping window to the size of the executable image (minimum 4 K block), and setting the PC Card memory offset from the system memory start address (Start) to generate the address of the first byte of the executable image on the PC Card.

The PC Card memory offset can be either a positive or negative value. Furthermore, the VG-469 does not check for a window whose size and offset allow it to wrap from the last PC Card address to the first PC Card address. Software must check to prevent address wrapping.

Memory Address Mapping

Common/Attribute memory on the PC Card can be accessed through any of the system memory address mapping windows. This is accomplished by selectively setting the "REG Active Bit" in the Card Memory Offset Address Register. When this bit is set to zero, common memory can be accessed; when this bit is set to one, attribute memory can be accessed. The system memory window to common/attribute memory can be mapped from any ISA address above 64K to any PC Card address.

Multiple system memory address mapping windows to separate common/attribute memory address spaces can be opened simultaneously. Each of these windows can be configured to use a different number of wait states, software write protect, and data width.

Memory Paging

System memory paging is supported in the VG-469 through the use of multiple system memory address mapping windows. When using LIM or XIP, software should assign a window to each page required to support the LIM/XIP function. The software has the responsibility to set up the system memory address mapping windows to be in one contiguous system address space with

each window controlling a single page in the PC Card memory. When changing the page pointer only the PC Card memory offset address value needs to be altered to change the mapping.

PC Card I/O Addressing

The ISA system bus is limited to 768 bytes of common I/O address space between I/O addresses 100H and 3FFH. The VG-469 supports system I/O address decode from 0 to 64K. A PC Card can request specific common I/O address locations or it can request a block of I/O space by the size required. When I/O space is requested by size, the system is free to locate the PC Card anywhere in the 64K system I/O address space. The PC Card decodes the *CE[2:1], *IORD, and *IOWR signals to respond to an I/O access.

The VG-469 provides two independently enabled and controlled I/O address windows which are defined by 16-bit addresses to achieve a 1 byte resolution. Each window has independent control of I/O data bus width, zero wait state system bus access, and generation of *IOCS16.

A PC Card I/O address is accessed only when all of the following conditions are satisfied:

1. The I/O address window is enabled.
2. The system address is greater than or equal to the I/O address start register A[15:0].
3. The system address is less than or equal to the I/O address stop register A[15:0].
4. The access is not a DMA transfer. AEN = 0 to access the I/O PC Card.

It is the responsibility of the system software to account for each I/O address range assigned to a particular PC Card. The reservation of a particular I/O address range for each PC Card can reduce card power consumption since only one PC Card is enabled during each I/O access.

The VG-469 can directly map the system I/O address space to the PC Card I/O ports with single byte granularity. Each PC Card is guaranteed a reserved system I/O address space, and an I/O cycle will be generated to the PC Card only within the assigned space.

PC CARD DMA OPERATION

The VG-469 supports using the socket as an interface to a DMA device. PC Cards that take advantage of this new DMA extension in PC Card Standard are sound card, network card, and floppy drive card.

DMA mode can be used in a 5V-only socket, or a mixed voltage socket where voltage sensing is done using an external buffer. Only one socket at a time should be enabled for DMA transfer because the ISA bus DMA handshake signals are shared between both socket interfaces.

DMA transfers to and from the DMA-capable PC Card may be 8-bit or 16-bit, as specified by bit D4 of the DMA register (index 3Eh/7Eh). External steering logic is needed to direct the DMA signals to the desired channel.

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To use the DMA mode, the socket interface must be set to I/O card type (bit D5 of the Interrupt and General Control Register). Setting D0 of the DMA and Programmable Chip Select Configuration Register enables the DMA mode, and other bits in this register define the card *DREQ steering, DMA data size, and terminal count steering. Once DMA mode is enabled and DMA operation is taking place, several PCMCIA signals are re-defined as DMA interface signals, according to the following table:

Standard I/O Card Signals	DMA Card Signals	Condition
*IOIS16	*DREQ	DMA register D[6:5] = 00
*SPKR	*DREQ	DMA register D[6:5] = 01
*INPACK	*DREQ	DMA register D[6:5] = 10
*REG	DACK	During actual DMA cycles
*OE	*TC	During DMA write cycles if DMA register D[2:1] = 00
*WE	*TC	During DMA read cycles if DMA register D[2:1] = 00

The VG-469 multiplexes the ISA bus DMA handshake signals onto the pins also used for other purposes. The table below specifies these signals:

VG-469 Signals	ISA Bus DMA Signals	Condition
B_GPIO	HDRQ	DMA register D0 = 1
A_GPIO	HTC	DMA register D0 = 1
B_*VS1	*HDACK	DMA register D0 = 1 and Plug-and-Play is not enabled
IRQ7	*HDACK	DMA register D0 = 1, Plug-and-Play is enabled, and D7 of Extended Mode Register A is set.

When a PC Card and socket are configured for DMA operations, the DACK (*REG) signal is used to distinguish between a DMA cycle and a normal I/O cycle. The *REG is negated (high) during the entire DMA bus cycle, as opposed to being active (low) for a normal I/O cycle. It should be noted that DMA acknowledgment is indicated when DACK (*REG) is high and either *IORD or *IOWR is active. DACK (*REG) may be high before DMA request is issued, therefore a high DACK without an active I/O command does not mean DMA is acknowledged by the system.

Address lines to the PC Card are ignored during DMA operations.

A PC Card requests a DMA transfer by asserting *DREQ, VG-469 then asserts HDRQ to the core logic. Once receiving an active *HDACK from the core logic, VG-469 drives DACK high and sets up the internal logic for DMA transfer. An I/O command is then asserted (*IOWR for DMA read and *IORD for DMA write). When the DMA transfer is complete and the core logic

asserts terminal count (HTC), VG-469 by default steers *TC to *WE for DMA read, or *OE for DMA write. It is recommended to use the default conditions (bits D[2:1] of the DMA register) in order to be compliant with the PC Card Standard, although other options for terminal count steering are provided. *TC is asserted for one ISA Bus clock (TCKLK). It will not be asserted beyond the trailing edge of an ISA bus I/O command to avoid being misinterpreted by the PC Card as a common memory access.

INTERRUPT HANDLING

Since multiple PC Cards in a system can conflict if they try to utilize the same interrupt, the VG-469 can be programmed to eliminate this conflict by routing each PC Card interrupt request to a different system interrupt. Based upon four bits in the Interrupt and General Control Register, the interrupt request signal (*IREQ) from an I/O PC Card will be directed to one of ten interrupt request lines on the system bus.

The VG-469 provides a card status change interrupt which can notify the system of a change in the battery voltage levels, card insertion/removal detection, Ready/*Busy condition, and status change. It can be directed to one of the ten interrupt request lines on the system bus based upon four bits in the Card Status Change Interrupt Configuration Register. When used with a CPU that supports SMI, it should be configured as the *INTR signal and connected to the *EXTSMI input of the CPU.

The ten interrupt request lines can all be configured as edge-triggered to support the standard interrupt from I/O cards and card status change interrupts, or as level mode interrupts to support I/O cards with pulse-mode interrupt requests.

POWER MANAGEMENT

The VG-469 implements power management for each PC Card socket. Programming the Power and RESETDRV control register controls socket power management.

The VG-469 will automatically enter into lower power consumption state when memory windows and I/O windows are disabled, and when sockets become empty. Further, the lowest power consumption level can be achieved by putting the VG-469 into power down mode. This mode is entered by disabling all the I/O, memory windows, output buffers, configuring one of the GPIO as power down control input enabling the power down mode, and driving the GPIO pin to high.

During the power down mode, VG-469's Vcc will still be powered up, and the internal register contents will be maintained. The interrupt (IRQs) can still be generated to the host system from either card status change, or PC Card interrupt requests. *RIO can still be armed to route either *RI or Card detect change. *INTR can still be armed for card status change interrupts but will not be generated until power down mode is exited.

CONFIGURATION, STATUS AND CONTROL REGISTERS

The VG-469 provides complete control of a PC Card through its registers. Among the functions provided are bit programmable memory write protect for the attribute and common memory, Vcc, and Vpp power control, and interrupt steering. Control of the signal multiplexers for directing the appropriate memory or I/O signals to the socket is also provided, as well as control bits to set memory and I/O data path size. Other registers set the boundaries of the memory and I/O mapping windows. Finally, a number of registers reflect the status of the PC Card.

Register Addressing

All VG-469 control registers are byte wide and accessed using an indirect indexing scheme. Two I/O addresses are required to access the control registers. The first address is the index register. The second address, which equals to index register address plus 1, points to the data register. Each socket contains a block of 64 indirectly addressed registers. In order to support up to two VG-469's in a system, two sets of selectable I/O addresses are available. These values are selected by pull-up/pulldown strapping resistor on the *INTR pin, according to the table. While RESETDRV is true this pin becomes an input, the falling edge of RESETDRV latches the pulled up or down state of the pin, and thereafter the pin resumes its normal function.

The index register and the data register are read/write registers. The VG-469 will not respond to a data register read or write operation or to an index register read operation unless the index register has first been written to with a valid index.

Strapping Option Table for Selecting the I/O Address

*INTR Resistor	I/O Address
Pull-up	3E0h/3E1h
Pulldown	3E2h/3E3h

External Decoding

The VG-469 can be configured to respond to an external chip select input, allowing an unlimited number of VG-469's to exist in a system. One VG-469 using internal decoding can coexist with an unlimited number using external decoding. The devices which use external decoding may have the same or different strapping resistor configurations, which must be different from the configurations of the device which uses internal decoding.

With external decoding, index register is accessed if ISA address A0 = 0, and data register is accessed if A0 = 1.

OPERATING MODES

VG-469 is very flexible in that it can be configured to provide different functions to meet system's requirement. During power on reset, a number of resistor strapping options determine the operating modes. The two primary configuration strappings are to decide: (1) if the socket is operated at 5 volt only, or it is designed to be switchable between 5 volt and 3.3 volt. (2) if the VG-469 is to be used in a small computer environment, in which it is connected directly to ISA bus and PC Card sockets (Basic Mode); or expandability is the design goal such that Plug-and-Play or cable driving is required (Extended Mode).

For a 5 volt only socket, one VCCEN pin (VCCEN1) is sufficient to select between power on and off. The extra pin from each socket is then strapped in opposite sense: A_VCCEN0 to VCC, and B_VCCEN0 to ground, for example. For a mixed voltage socket, both VCCEN1 and VCCEN0 are required to select among 5 volt, 3.3 volt and power off. Since all VCCENs are strapped to the level that would turn off the switch, A_VCCEN0 and B_VCCEN0 are strapped to the same level.

A_VCCEN0 and B_VCCEN0 Resistors	Socket Voltage Support
Strapped to opposite levels	5 volt only
Strapped to the same level	mixed voltage

A mixed voltage socket can have two ways of accessing the voltage sense pins. The first method is to have all the voltage sense pins connected to the VG-469, and are readable through an internal Voltage Sense Register (index 1Fh/5Fh). The other method is to use an external buffer chip as the voltage sense register. When the same indexed register is accessed, A_*VS1 becomes Voltage Sense Read Enable which is connected to Output Enable of the external buffer.

A second resistor strapping, which is on the *SPKROUT pin, is used to differentiate the Basic Mode and Extended Mode:

*SPKROUT Resistor	Operating Mode
Pull-up	Basic Mode
Pulldown	Extended Mode

Basic Mode

In Basic Mode, VG-469 is connected directly to ISA bus and PC Card sockets. DMA is available for a 5 volt only socket and a mixed voltage socket with external voltage sense, but not available if internal voltage sense is implemented.

Extended Mode

The VG-469 can be configured to enable the Extended Mode to support buffered cable driving applications. In this configuration two options are available: VG-469 can be located at the drive

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bay and is connected through cable to the buffers that drive the ISA bus, or it can be near the ISA bus and drives the socket_B through cable. When enabled, the definitions of several pins are changed to provide buffer direction controls.

Pin Definition in Basic Mode	Pin Definition for ISA Buffer with B_*VS2 pulled low	Pin Definition for Socket_B Buffer with B_*VS2 pulled high
A_*VS2	HBUFDIR ¹	*BSIGEN
B_*VS2	LBUFDIR ¹	DIR ²
B_GPIO	D7BUFDIR ¹	B_GPIO
<i>Notes:</i> 1. Normally low, from ISA bus to VG-469. 2. Normally high, from VG-469 to socket_B.		

In the case of ISA buffer support, if a floppy or hard disk is installed in the socket, the VG-469 can be programmed to avoid contention with a motherboard drive. In this situation VG-469 either tri-states SD7 (with hard disk in the socket) or SD[6:0] (with floppy disk in the socket) when reading the drive address register. If this feature is used in a cable driving configuration, LBUFDIR will control the SD[6:0] and D7BUFDIR will control the SD7 buffer.

In the extended mode, VG-469 can also support both Plug and Play ISA and DMA. Plug and Play ISA requires an external serial EEPROM for configuration storage. The interface signals to the EEPROM are provided by strapping B_*VS1 low. The alternate definitions for these pins are shown in the next table:

Pin Definition in Basic Mode or in Extended Mode with B_*VS1 pulled high	Pin Definition for Plug and Play ISA Support with B_*VS1 pulled low
B_*VS1 (*HDACK)	E2CS (serial EEPROM chip select)
*INTR	E2SK (serial EEPROM clock input)
*SPKROUT	E2DIO (Serial EEPROM data port)

When Plug and Play is enabled, DMA can still be used if IRQ7 is configured to be *HDACK. This can be accomplished by setting bit D7 of the Extended Mode Register-A.

PLUG AND PLAY

VG-469 supports the Plug and Play ISA Specification Version 1.0a to provide automatic configuration capability. This plug and play implementation lets the software relocate the VG-469 registers from the default at 3E0h/3E1h or 3E2h/3E3h. Plug and Play is only available in extended mode.

The major steps of the auto-configuration process are as follows:

1. Put all Plug-and-Play devices in configuration mode.
2. Isolate one Plug-and-Play device at a time.
3. Assign a handle and read the card's resource data structure.
4. After the resource requirements and capabilities are determined for all cards, use the handle to assign conflict free resources to each device.

Auto-configuration Ports

The Plug-and-Play software identifies and configures devices with a set of commands that are executed using three 8-bit I/O ports. These ports are listed below:

Port Name	Location	Type
Address	0279H	Write-only
Write_Data	0A79H	Write-only
Read_Data	Relocatable in range 0200H to 03FFH	Read-only

Note: All three ports use a 12-bit ISA address decode.

The Plug-and-Play Registers are accessed by first writing the address of the desired register to the Address port, followed by a read of data from the Read_Data port or a write of data to the Write_Data port. A write to the Address port may be followed by any number of Write_Data or Read_Data accesses to the same register location without the need to write to the Address port before each access.

The Write_Data port is used to write information to the Plug-and-Play registers. The destination of the data is determined by the last setting of the Address port.

The Read_Data port is used to read information from the Plug-and-Play registers. The source of the data is determined by the last setting of the Address port. The address of the Read_Data port is set by writing the proper value to a Plug-and-Play control register. The isolation protocol verifies that the location selected for the Read_Data port is free of conflict.

Initiation Key

The initiation key places the Plug-and-Play logic into configuration mode. The VG-469 implements a Plug-and-Play compliant linear feedback shift register (LFSR) to generate data patterns needed to provide an initiation key protocol and to provide a checksum verification during serial data read in the isolation protocol. The software should perform two write operations of value 00h to the Address port to insure that the LFSR is in the initial state (LFSR value = 6Ah) before sending the initiation key. The initiation key is a series of 32 writes to the Address port with the data in the following sequence:

6A,B5,DA,ED,F6,FB,7D,BE,
DF,6F,37,1B,0D,86,C3,61,
B0,58,2C,16,8B,45,A2,D1,
E8,74,3A,9D,CE,E7,73,39

Isolation Protocol

Once the initiation key is sent, all devices with the matching key are in the configuration mode. The software can then isolate each device one by one by matching each device's serial identifier. The serial identifier is a 72-bit unique, non-zero, number composed of two, 32-bit fields and an 8-bit checksum. The first 32-bit field is a vendor identifier. The other 32 bits can be put in by the vendor. The VG-469 system design requires a serial EEPROM to store this information. VG-469 generates signals, defined earlier in 'Extended Mode' section, to read from serial EEPROM. For detailed isolation protocol, refer to Plug and Play ISA Specification, Version 1.0a.

Card Select Number

Once the VG-469 has been isolated by the software, it will be assigned a unique number: Card Select Number (CSN). This number enables the Plug-and-Play software to select VG-469 at later points in the configuration process, without going through the isolation protocol again.

Resource Relocation

After CSN is assigned to VG-469, the software can read and program the VG-469's resource selections. The VG-469 configuration register I/O port can be relocated from the default 3E0h or 3E2h to avoid conflict with other devices.

DIGITAL AUDIO SUPPORT

The VG-469 supports special signals such as digital audio. These signals are passed through to the system bus without signal conditioning. The digital audio signal (*SPKR) from the socket is passed through to the speaker output pin (*SPKROUT) of the VG-469.

SOCKET CONTROL REGISTERS

VG-469 has two groups of registers: Socket Control Registers and Plug and Play Registers. All Socket Control Registers are accessed through address ports 3E0h/3E1h or 3E2h/3E3h unless these ports are relocated by Plug and Play. Plug and Play are accessed through address port 279h.

The General Setup Registers (except Power and RESETDRV Control Register, Card Voltage Sense Register and Card Voltage Select Register), Interrupt Registers, I/O Registers and Memory Registers are all fully compatible with the Intel 82365SL B stepping at power up. By writing a 1 to bit 4 of the Extended Mode Register-A, those registers are compatible with 82365SL DF silicon. All other registers are unique to the VG-469. All reserved bits must be set to zero to avoid unpredictable problems.

The Unique Registers are locked after reset and cannot be read or written. To unlock, do two consecutive writes to the index register, first with 0Eh then followed by 37h. Any index or data register access between these two writes will abort the unlock sequence.

General Setup Registers

Name	Socket A Index	Socket B Index	Access
Identification and Revision	00H	40H	RO
Interface Status	01H	41H	RO
Power and RESETDRV Control	02H	42H	R/W
Card Status Change	04H	44H	R/W
Address Window Enable	06H	46H	R/W
Card Detect and General Control Register	16H	56H	R/W
Global Control Register	1EH	5EH	R/W
Card Voltage Sense Register	1FH	5FH	R/O
Card Voltage Select Register	2FH	6FH	R/W

Interrupt Registers

Name	Socket A Index	Socket B Index	Access
Interrupt and General Control	03H	43H	R/W
Card Status Change Interrupt Configuration	05H	45H	R/W

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Register Summary

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I/O Registers

Name	Socket A Index	Socket B Index	Access
I/O Control	07H	47H	R/W
I/O Address 0 Start Low Byte	08H	48H	R/W
I/O Address 0 Start High Byte	09H	49H	R/W
I/O Address 0 Stop Low Byte	0AH	4AH	R/W
I/O Address 0 Stop High Byte	0BH	4BH	R/W
I/O Address 1 Start Low Byte	0CH	4CH	R/W
I/O Address 1 Start High Byte	0DH	4DH	R/W
I/O Address 1 Stop Low Byte	0EH	4EH	R/W
I/O Address 1 Stop High Byte	0FH	4FH	R/W

Memory Registers

Name	Socket A Index	Socket B Index	Access
System Memory Address 0 Mapping Start Low Byte	10H	50H	R/W
System Memory Address 0 Mapping Start High Byte	11H	51H	R/W
System Memory Address 0 Mapping Stop Low Byte	12H	52H	R/W
System Memory Address 0 Mapping Stop High Byte	13H	53H	R/W
Card Memory Offset Address 0 Low Byte	14H	54H	R/W
Card Memory Offset Address 0 High Byte	15H	55H	R/W
System Memory Address 1 Mapping Start Low Byte	18H	58H	R/W
System Memory Address 1 Mapping Start High Byte	19H	59H	R/W
System Memory Address 1 Mapping Stop Low Byte	1AH	5AH	R/W

System Memory Address 1 Mapping Stop High Byte	1BH	5BH	R/W
Card Memory Offset Address 1 Low Byte	1CH	5CH	R/W
Card Memory Offset Address 1 High Byte	1DH	5DH	R/W
System Memory Address 2 Mapping Start Low Byte	20H	60H	R/W
System Memory Address 2 Mapping Start High Byte	21H	61H	R/W
System Memory Address 2 Mapping Stop Low Byte	22H	62H	R/W
System Memory Address 2 Mapping Stop High Byte	23H	63H	R/W
Card Memory Offset Address 2 Low Byte	24H	64H	R/W
Card Memory Offset Address 2 High Byte	25H	65H	R/W
System Memory Address 3 Mapping Start Low Byte	28H	68H	R/W
System Memory Address 3 Mapping Start High Byte	29H	69H	R/W
System Memory Address 3 Mapping Stop Low Byte	2AH	6AH	R/W
System Memory Address 3 Mapping Stop High Byte	2BH	6BH	R/W
Card Memory Offset Address 3 Low Byte	2CH	6CH	R/W
Card Memory Offset Address 3 High Byte	2DH	6DH	R/W
System Memory Address 4 Mapping Start Low Byte	30H	70H	R/W
System Memory Address 4 Mapping Start High Byte	31H	71H	R/W
System Memory Address 4 Mapping Stop Low Byte	32H	72H	R/W
System Memory Address 4 Mapping Stop High Byte	33H	73H	R/W
Card Memory Offset Address 4 Low Byte	34H	74H	R/W
Card Memory Offset Address 4 High Byte	35H	75H	R/W

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Register Summary

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Unique Registers

Name	Socket A Index	Socket B Index	Access
Control	38H	78H	R/W
Activity Timer	39H	79H	R/W
Miscellaneous	3AH	7AH	R/W
GPIO Configuration	3BH	7BH	R/W
Extended Mode	3CH	7CH	R/W
Programmable Chip Select	3DH	7DH	R/W
DMA and Programmable Chip Select Configuration	3EH	7EH	R/W
ATA	3FH	7FH	R/W

PLUG AND PLAY REGISTERS

Card Control Registers

Name	Index	Access
Set RD_DATA Port	00H	W/O
Serial Isolation	01H	R/O
Config Control	02H	W/O
WAKE[CSN]	03H	W/O
Resource Data	04H	R/O
Status	05H	R/O
Card Select Number	06H	R/W

Logical Device Control Registers

Name	Index	Access
Activate	30H	R/W
I/O Range Check	31H	R/W

I/O Configuration Registers

Name	Index	Access
I/O Port Base Address High Byte	60H	R/W
I/O Port Base Address Low Byte	61H	R/W

This chapter describes all PCMCIA socket control registers and Plug and Play registers. All read/write registers are cleared by RESETDRV.

SOCKET CONTROL REGISTERS

Identification and Revision Register

Type: Read Only

Address: Socket A Index 00H
Socket B Index 40H

Bit	Function			
D[7:6]	PCSC Interface Type. Read 10, signifying that both memory and I/O cards are supported by the socket			
D[5:4]	Reserved			
D[3:0]	The function of these bits changes under control of the UNLOCK and VADEMREV bits in the DMA register, according to the table:			
	UNLOCK	VADEMREV	D3	Revision
	0	X	RO	0YYY (Intel)
	1	0	RW	XYYY (D3 is R/W to identify Vadem chip)
	1	1	RO	1101 (Vadem)
<i>Note: YYY is 011 in B step mode, 100 in C step mode, when UNLOCK = 0.</i>				

Chapter 4
Register Bit Declarations

VADEM VG-469
PC Card Socket Controller

Interface Status Register

Type: Read Only
Address: Socket A Index 01H
 Socket B Index 41H

Bit	Function
D7	GPI. This bit is only meaningful for register index 01H. When GPSEL[2:0] = 000 in the GPIO Configuration Register (index 3BH), the logic value of this bit is the complement to the A_GPIO pin. Otherwise, it reads 1.
D6	PC Card Power Active. 0: Power to the socket is off (Vcc, Vpp1 and Vpp2 are all no connects) 1: Power to the socket is on, (Vpp1 and Vpp2 are set according to bits D[1:0] of the power and RESETDRV Control Register).
D5	Ready / *Busy. 0: PC Card is busy. 1: PC Card is ready.
D4	Memory Write Protect. Bit value is the logic level of the WP signal on the memory PC Card interface. 0: PC Card is not write protected. 1: PC Card is write protected.
D[3:2]	Card Detect. Complement of the values of *CD[2:1] on the PC Card interface. Bit is set to 1 if the corresponding *CD is active, set to 0 if inactive.
D[1:0]	Battery voltage detect. Following are the values of BVD[2:1] signals for memory PC Cards. 00: battery dead. 01: battery warning. 10: battery dead. 11: battery good. For I/O PC Cards, bit 0 indicates the current status of the *STSCHG/*RI signal from the PC Card.
<i>Note:</i> This register provides the current status of the PC Card socket interface signals.	

Power and RESETDRV Control Register

Type: Read/Write
 Address: Socket A Index 02H
 Socket B Index 42H

Bit	Function																				
D7	Output Enable. If this bit is set to zero CA[25:12], *CE[2:1], *IORD, *IOWR, *OE, *REG, RESET, and *WE are tri-stated. <i>Note: This bit should not be set until after this register has been written to set PC Card Power Enable.</i>																				
D6	Reserved																				
D5	Auto Power Switch Enable. 0: automatic socket power switching based on card detects is disabled. Power to the socket is solely determined by bit D4 of this register. 1: automatic socket power switching based on card detects is enabled. If bit D4 is set, power to the socket is turned on when the card is inserted, off when removed.																				
D4	PC Card Power Enable. 0: Vcc off 1: Vcc is on for the following conditions: <ul style="list-style-type: none"> • D5 = 0, or D5 = 1 and card is in the socket; and • reg 2Fh/6Fh, D[1:0] ≠ 10 																				
D3	Reserved																				
D2	GPO. If the GPIO pin for this socket is selected to be GPO (GPSEL[2:0] = 3), and the VPPEN0 pins are not steered to GPIO (VPPST[1:0] not equal 3), this bit causes the GPIO pin to go high when set, and low when cleared.																				
D[1:0]	PC Card Vpp Power Control. VG-469 generates two power control outputs for Vpp (VPPEN[1:0]). VPPENx will be 0 if PC Card Power Enable bit is 0. VPPEN1 is always available but VPPEN0 is only available when a multi-function pin is programmed to be VPPEN0. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>D[1:0]</th> <th>VPPEN0 not available</th> <th>VPPEN available</th> <th>VPPEN[1:0]</th> </tr> </thead> <tbody> <tr> <td>00:</td> <td>Vpp gets Vcc</td> <td>Vpp gets no connect</td> <td>00</td> </tr> <tr> <td>01:</td> <td>Vpp gets Vcc</td> <td>Vpp gets Vcc</td> <td>01</td> </tr> <tr> <td>10:</td> <td>Vpp gets Vpp</td> <td>Vpp gets Vpp</td> <td>10</td> </tr> <tr> <td>11:</td> <td>Reserved (Vcc)</td> <td>Reserved (no connect)</td> <td>00</td> </tr> </tbody> </table>	D[1:0]	VPPEN0 not available	VPPEN available	VPPEN[1:0]	00:	Vpp gets Vcc	Vpp gets no connect	00	01:	Vpp gets Vcc	Vpp gets Vcc	01	10:	Vpp gets Vpp	Vpp gets Vpp	10	11:	Reserved (Vcc)	Reserved (no connect)	00
D[1:0]	VPPEN0 not available	VPPEN available	VPPEN[1:0]																		
00:	Vpp gets Vcc	Vpp gets no connect	00																		
01:	Vpp gets Vcc	Vpp gets Vcc	01																		
10:	Vpp gets Vpp	Vpp gets Vpp	10																		
11:	Reserved (Vcc)	Reserved (no connect)	00																		

Chapter 4
Register Bit Declarations

VADEM VG-469
PC Card Socket Controller

Card Status Change Register

Type: Read/Write
Address: Socket A Index 04H
 Socket B Index 44H

Bit	Function
D7	Activity Timeout Bit is set to one when activity timer times out (if compatibility bit in the Control register is set).
D[6:5]	Reserved, always 0.
D4	GPI Change. This bit will contain the status of the GPI card status change interrupt. This bit will be set to 0 as long as the GPI Enable bit in the Card Detect and General Control Register is set to 0. When the GPI Enable bit is set to 1 and the GPI input has transition (the edge that generates an interrupt will depend on the setting of the GPI Transition control bit in the Card Detect and General Control Register), then this bit will be set to 1 indicating that a card status change interrupt has occurred. Acknowledgment of this card status change interrupt will be done in the same way that the other sources of the card status change interrupt are acknowledged.
D3	Card Detect Change. This bit will stay at 0 as long as the Card Detect Enable bit is set to 0. When the Card Detect Enable bit is set to 1, this bit will be set to one when a debounced change has been detected on *CD[2:1].
D2	Ready Change. This bit will stay at 0 as long as the Ready Enable bit is set to 0. When the Ready Enable bit is set to 1, this bit will be set to one when a low to high has been detected on the Ready/*Busy signal indicating that the memory PC Card is ready to accept a new data transfer. Bit reads zero for I/O PC Cards.
D1	Battery Warning. This bit will stay at 0 as long as the Battery Warning Enable bit is set to 0. When the Battery Warning Enable bit is set to 1, this bit will be set to one when a battery warning condition has been detected. Bit reads zero for I/O PC Cards.

Bit	Function
D0 (cont.)	<p>Battery Dead/*STSCHG. For memory PC Cards, bit is set to one when a battery dead condition has been detected. This bit reads zero if Battery Dead Enable bit is set to 0. For I/O PC Cards, bit is set to one if ring indicate enable bit in the interrupt and general control register is set to zero and the *STSCHG/*RI signal from the I/O PC Card has been pulled low. The system software then has to read the status change register in the PC Card to determine the cause of *STSCHG. This bit reads zero if the ring indicate enable bit in the interrupt and general control register is set to one.</p>
<p><i>Notes:</i> 1. This register contains the status for sources of the card status change interrupt. These sources can be enabled to generate a card status change interrupt by setting the corresponding Enable bit in the Card Status Change Interrupt Configuration Register or the Card Detect and General Control Register (except for the activity timer and GPI which are enabled by other registers). The bits in this register will be read as 0 if the corresponding Enable bits are set to 0.</p> <p>2. If the Explicit Write Back bit is set in the Global Control Register, the acknowledgment of sources for the card status change interrupt will be done by writing back 1 to the appropriate bit in the Card Status Change Register that was read as a 1. Once acknowledged, that particular bit in the Card Status Change Register will be read back as 0. The interrupt signal caused by card status change, if enabled on a system IRQ line, will be active until all of the bits in the register are zero.</p> <p>3. If the Explicit Write Back bit is not set, the card status change interrupt when enabled on a system IRQ line, will remain active until this register is read. Reading this register causes the register bits that were read as set to be reset to zero.</p>	

Address Window Enable Register

Type: Read/Write
Address: Socket A Index 06H
 Socket B Index 46H

Bit	Function
D[7:6]	<p>I/O Window Enable [1:0].</p> <p>0: Inhibit the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window.</p> <p>1: Generate the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window. I/O accesses pass addresses from the system bus directly through to the PC Card.</p> <p>The start and stop register pairs must all be set to the desired window values before setting this bit to one.</p>
D5	<p>MEMCS16 Decode A[23:12].</p> <p>0: *MEMCS16 is generated from a decode of the ISA address A[23:17] only. This means that at a minimum, a 128K block of memory address space is set aside as 16-bit memory.</p> <p>1: *MEMCS16 is generated from decode of the address lines A[23:12].</p>
D[4:0]	<p>Memory Window Enable [4:0].</p> <p>0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window.</p> <p>1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.</p> <p>The start, stop, and offset registers pairs must all be set to the desired window values before setting bit to one.</p>
<p>Note: This register controls the enabling of the memory and I/O mapping windows to the PC Card memory or I/O space.</p>	

Card Detect and General Control Register

Type: Read/Write
Address: Socket A Index 16H
Socket B Index 56H

Bit	Function
D[7:6]	These bits reserved.
D5	<p>Software Card Detect Interrupt. If the Card Detect Enable bit is set to 1 in the Card Status Change Interrupt Configuration Register, then writing a 1 to this bit will cause a card detect card status change interrupt for the associated slot. The functionality and acknowledgment of this software interrupt will work the same way as the hardware generated interrupt. This bit will always read back as 0.</p> <p>The functionality of the hardware card detect card status change interrupt will not be affected. If a card status change occurs on the *CD1 and *CD2 inputs, a H/W card detect card status change interrupt will be generated. If the Card Detect Enable bit is set to 0 in the Card Status Change Interrupt Configuration Register, then writing a 1 to the S/W Card Detect Interrupt bit has no effect.</p>
D4	<p>Card Detect Resume Enable. The default state of this bit is 0. If this bit is set to 1, then once a card detect change has been detected on the *CD1 and *CD2 inputs, the *RIO output will go from high to low and the Card Detect Change bit in the Card Status Change Register will be set to 1. The *RIO output will remain low until either a read or a write of 1 to the Card Detect Change bit in the Card Status Change register, (acknowledge cycle) which will cause the Card Detect Change bit to be cleared and the *RIO output to go from low to high. The Card Detect Enable bit must be set in the Card Status Change Interrupt Configuration Register in order to generate the *RIO.</p> <p>If the card status change is routed to either the *INTR signal of any of the IRQ signals, the setting of Card Detect Resume Enable bit to one will prevent *INTR and IRQ signal from going active as a result of H/W card detect status change. Once the resume software has detected a card detect change interrupt from *RIO (by reading the Card Status Change Register), the software should indicate a software card detect change so the card detect change conditions will generate active interrupt on the IRQ or *INTR signals (depending on the active configuration).</p>

Bit	Function
D4 (cont.)	<p>If this bit is set to zero, then the card detect resume functionality is disabled. This means that the *RIO output will not go low due to a card detect change.</p> <p>The *RIO output will be the logical AND of all the active low sources for ring indicate output including the *RI inputs from slot A and slot B and the card detect changes on *CD1, *CD2 from both slots.</p>
D3	<p>GPI Transition Control.</p> <p>The default state of this bit is 0. Setting the General Purpose Input (GPI) Enable bit to 1 enables a card status change interrupt once the *GPI input goes high to low of the GPI Transition Control bit is set to 0. If the GPI Enable bit is set to one and the GPI Transition Control bit is set to 1, then once the *GPI input has gone from low to high, a card status change interrupt will be generated.</p>
D2	<p>GPI Enable.</p> <p>The default state of this bit is 0. Setting it to 0 disables the generation of a card status change interrupt based on the *GPI input transitioning.</p> <p>Setting it to 1 enables a card status change interrupt based on the *GPI input transition. The GPI Transition Control bit sets the triggering edge of the *GPI.</p> <p>The GPI card status change interrupt functions independent of the setting of the PC Card Type bit in the Interrupt and General Control register.</p>
D1	<p>Configuration Reset Enable.</p> <p>The default state of this bit is 0. If it is set to 0, the configuration register reset function based on card detects is disabled. When it is set to 1, when both the *CD1 and *CD2 inputs for a particular slot go high, a reset pulse will be generated to reset the configuration registers for that particular slot to their default state (zeros). The registers involved are all I/O registers, all Memory registers, Interrupt and General Control register (except INTR ENABLE bit) and Address Window Enable Register (except MEMCS16 Decode A[23:12]).</p>

Bit	Function
D0 (cont.)	16-Bit Memory Delay Inhibit. The default state of this bit is 0. If it is set to 0 and a system memory window is set up to be 16-bit by setting the Data Size bit in the System Memory Address Mapping Start High Byte Register to 1, the falling edge of the control strobes *WE and *OE for the corresponding slot will be delayed synchronously by CLK. The falling edge of the control strobes will be generated from the first falling edge of CLK after the falling edge of *MEMW or *MEMR. If it is set to 1, the control strobe falling edge will not be synchronously delayed.

Global Control Register

Type: Read/Write
Address: Socket A Index 1EH
Socket B Index 5EH

Bit	B Step Mode Function
D[7:4]	These bits reserved.
D3	IRQ14 Pulse Mode Enable. When this bit is set to 1 and bit 1 (level mode interrupt enable) is 0, and PC Card Type bit is set to 1 (I/O Card), and the Card *IREQ is steered to IRQ14, IRQ14 will operate in level mode and all other IRQs will operate in edge triggered mode. This is intended to support a PC Card which generates a PCMCIA pulse mode *IREQ, while other IRQs operate in ISA/EISA edge-triggered mode.
D2	Explicit Write Back Card Status Change Acknowledge. Setting this bit to a one will require an explicit write of a one to the Card Status Change Register bit which indicates an interrupting condition to acknowledge the interrupt. When this bit is set to zero (default state), the card status change interrupt is acknowledged by reading the Card Status Change Register, and the register bits are cleared upon a read.

D1 (cont.)	<p>Level Mode Interrupt Enable. Level mode refers to EISA level mode operation, not necessarily PCMCIA level mode.</p> <p>If this bit is low (default), all IRQ outputs operate as ISA rising edge-triggered interrupts. All IRQs will normally be tristated. An IRQ will go low when an interrupt is steered to it, and will go high when the interrupt becomes active. In the case of the card *IREQ, the IRQ will go low when *IREQ goes inactive (high). If caused by a card status change, IRQ will go low when the status is cleared.</p> <p>If this bit is high, all IRQ outputs operate as EISA active low level-triggered interrupts. An IRQ will go from tristate to low when the interrupt steered to it becomes active.</p> <p>Level mode can also be used to enable interrupt sharing an ISA system (which uses edge-triggered interrupts) when all interrupt sources on the shared level operate in pulse mode. If the shared IRQ is used for status change interrupts, the Vadem proprietary STATIRQSHARE bit must also be set. If the shared IRQ is used for PCMCIA card *IREQ interrupt, the cards must operate in PCMCIA pulse mode. The IRQ pulse will go low for the duration of the *IREQ pulse or for the same duration as *INTR would, and the host will respond to the rising edge of the IRQ.</p>
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Bit	B Step Mode Function
D0 (cont.)	<p>When set to 1, and all windows are disabled, the VG-469 enters power down. All internal registers cannot be read, outputs remain inactive, and the chip is at minimum power consumption level.</p> <p>IRQs and RIO will still be active to monitor the card status change and *RI status for resume indication. If a status change occurs during power down and INTR is enabled, the INTR will occur upon exit from power down mode. If a GPIO is programmed as external chip select or Power Down Control, that pin must also be high to enter power down mode, and the internal registers will not be writeable.</p>
<p><i>Note: 1. This register is not duplicated per slot. Thus, this register can be accessed from either the slot A or the slot B index.</i></p> <p><i>2. If the *CS pin is not available and the GPIO pin is not programmed to be either *CS or Power Down Control, then Power Down mode can still be entered if the other Power Down conditions are satisfied, but internal registers will remain writeable.</i></p>	
Bit	C Step Mode Function
D[7:4]	Reserved
D3	<p>Socket B and Socket A IREQ Level Mode.</p> <p>0: I/O Card IREQ operates in ISA edge triggered mode. For use with PCMCIA level-mode cards.</p> <p>1: I/O Card IREQ operates in EISA level triggered mode. For use with PCMCIA pulse-mode cards in ISA systems.</p>
D2	Explicit Writeback Card Status Change Acknowledge.
D1	<p>Card Status Change Level Mode.</p> <p>0: Status IRQ operates in ISA edge triggered mode.</p> <p>1: Status IRQ operates in EISA level triggered mode. Also can be used for interrupt sharing in ISA systems if STATIRQSHARE is set.</p>
D0	Power down.

Card Voltage Sense Register

Type: Read Only

Address: Socket A Index 1FH
Socket B Index 5FH

Bit	Function
D[7:4]	Reserved, always read 0, if the chip is configured as internal voltage sense.
D3	B_*VS2
D2	B_*VS1
D1	A_*VS2
D0	A_*VS1
<p>Notes: 1. There is only one register. It is mirrored so that it can be accessed from either socket.</p> <p>2. If external voltage sense is configured and a '244 is used as the voltage sense register, *VS[2:1] of the sockets are connected to '244 instead of VG-469. VG-469 will not drive the SD bus if the register is read. Instead, it will generate a Read Enable signal (*VSENBL) to '244 for the voltage sense information.</p>	

Card Voltage Select Register

Type: Read/Write (except bits 4 to 7, which are read-only)
Address: Socket A Index 2FH
 Socket B Index 6FH

Bit	Function
D7	ISA Bus Interface Voltage. 0: 5 volt. 1: 3.3 volt.
D6	Mixed Voltage. This bit is read-only. 0: 5 volt only socket. 1: Mixed voltage socket.
D5	Extended Configuration Bus Select. Valid only when bit D4 is true. This bit is read-only. 0: External buffers on socket B. 1: External buffers on ISA bus.
D4	Extended Configuration. This bit is read-only. 0: Basic configuration. 1: Extended configuration.
D[3:2]	Voltage Limits. These bits are set by software to limit card Vcc to a specified value, so that errant software cannot damage a card. Once either of these bits is set to 1, neither can be changed by software. Reset or removing the card clears both bits. 00: Maximum Vcc is 5 volt. 01: Maximum Vcc is 3.3 volt. 10: Maximum Vcc is X.X volt. (off if X.X volt is not available) 11: Maximum Vcc is 3.3 volt.
D[1:0]	Voltage Select. These bits control the Vcc that will be applied to the card when the PC Card Power Enable bit in register 02/42H is set. 00: 5 volt.. 01: 3.3 volt. 10: X.X volt. (off if X.X volt is not available) 11: 3.3 volt.

Interrupt and General Control Register

Type: Read/Write
Address: Socket A Index 03H
 Socket B Index 43H

Bit	Function
D7	<p>Ring Indicate Enable.</p> <p>0: For I/O PC Cards, (PC Card type bit is set to one), the change signal *STSCHG/*RI signal from the I/O PC Card is used as the status change signal *STSCHG. The current status of the signal is then available to be read from the Interface Status Register and this signal can be configured as a source for the card status change interrupt.</p> <p>1: For I/O PC Cards (PC Card type bit is set to one), the *STSCHG/*RI signal from the I/O PC Card is used as a ring indicator signal and is passed through to a pin that is register selectable among IRQ15, A_GPIO, and B_GPIO. For memory PC Cards, bit has no function.</p>
D6	<p>PC Card Reset.</p> <p>This is a software reset to the PC Card.</p> <p>0: Activates the RESET signal to the PC Card. The RESET signal will be active until bit is set to one.</p> <p>1: Deactivates the RESET signal to the PC Card.</p>
D5	<p>PC Card Type.</p> <p>0: Memory PC Card</p> <p>1: I/O PC Card.</p>
D4	<p>INTR Enable.</p> <p>0: The *INTR signal does not indicate a card status change interrupt and the card status change interrupt is steered to one of the IRQ lines according to bits [7:4] in the Card Status Change Interrupt Configuration Register.</p> <p>1: Enables the card status change interrupt on the *INTR signal, except in *CS power down mode.</p>

Bit	Function			
D[3:0] (cont.)	IRQ Level Selection (I/O Cards only). These bits select the redirection of the PC Card interrupt:			
	0000:	IRQ not selected.	1000:	Reserved.
	0001:	Reserved.	1001:	IRQ9 Enabled.
	0010:	Reserved.	1010:	IRQ10 Enabled.
	0011:	IRQ3 Enabled.	1011:	IRQ11 Enabled.
	0100:	IRQ4 Enabled.	1100:	IRQ12 Enabled.
	0101:	IRQ5 Enabled.	1101:	Reserved.
	0110:	Reserved.	1110:	IRQ14 Enabled.
	0111:	IRQ7 Enabled.	1111:	IRQ15 Enabled.
<p><i>Notes: This register controls the interrupt steering for the I/O PC Card interrupt as well as general control.</i></p>				

Chapter 4
Register Bit Declarations

VADEM VG-469
PC Card Socket Controller

Card Status Change Interrupt Configuration Register

Type: Read/Write

Address: Socket A Index 05H
Socket B Index 45H

Bit	Function																																
D[7:4]	<p>Interrupt Steering for the Card Status Change Interrupt. These bits select the redirection of the card status change interrupt if the interrupt is not selected to the output on the *INTR pin. With INTR Enable bit inactive:</p> <table border="1"> <tr> <td>0000:</td> <td>IRQ not selected.</td> <td>1000:</td> <td>Reserved.</td> </tr> <tr> <td>0001:</td> <td>Reserved.</td> <td>1001:</td> <td>IRQ9 Enabled</td> </tr> <tr> <td>0010:</td> <td>Reserved.</td> <td>1010:</td> <td>IRQ10 Enabled</td> </tr> <tr> <td>0011:</td> <td>IRQ3 Enabled</td> <td>1011:</td> <td>IRQ11 Enabled</td> </tr> <tr> <td>0100:</td> <td>IRQ4 Enabled</td> <td>1100:</td> <td>IRQ12 Enabled</td> </tr> <tr> <td>0101:</td> <td>IRQ5 Enabled</td> <td>1101:</td> <td>Reserved.</td> </tr> <tr> <td>0110:</td> <td>Reserved.</td> <td>1110:</td> <td>IRQ14 Enabled</td> </tr> <tr> <td>0111:</td> <td>IRQ7 Enabled</td> <td>1111:</td> <td>IRQ15 Enabled</td> </tr> </table>	0000:	IRQ not selected.	1000:	Reserved.	0001:	Reserved.	1001:	IRQ9 Enabled	0010:	Reserved.	1010:	IRQ10 Enabled	0011:	IRQ3 Enabled	1011:	IRQ11 Enabled	0100:	IRQ4 Enabled	1100:	IRQ12 Enabled	0101:	IRQ5 Enabled	1101:	Reserved.	0110:	Reserved.	1110:	IRQ14 Enabled	0111:	IRQ7 Enabled	1111:	IRQ15 Enabled
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0101:	IRQ5 Enabled	1101:	Reserved.																														
0110:	Reserved.	1110:	IRQ14 Enabled																														
0111:	IRQ7 Enabled	1111:	IRQ15 Enabled																														
D3	<p>Card Detect Enable. 0: Disables the generation of a card status change interrupt when the card detect signals change state. 1: Enables a card status change interrupt when a change has been detected on the *CD1 or *CD2 signals.</p>																																
D2	<p>Ready Enable (memory PC Cards only). 0: Disables the generation of a card status change interrupt when a low to high transition has been detected on the Ready/*Busy signal. 1: Enables a card status change interrupt when a low to high transition has been detected on the Ready/*Busy signal.</p>																																
D1	<p>Battery Warning Enable (memory PC Cards only). 0: Disables the generation of a card status change interrupt when a battery warning condition has been detected. 1: Enables a card status change interrupt when a battery warning condition has been detected.</p>																																

D0 (cont.)	<p>Battery Dead Enable / *STSCHG.</p> <p>0: Disables the generation of a card status change interrupt when either a battery dead condition (memory card) or an active *STSCHG (I/O card) is detected.</p> <p>1: For memory PC Cards, enables a card status change interrupt when a battery dead condition has been detected. For I/O PC Cards, enables a card status change interrupt if the *STSCHG/*RI signal has been pulled low by the I/O PC Card, assuming that the Ring Indicate Enable bit in the Interrupt and General Control Register is set to zero.</p>
<p><i>Note:</i> 1. This register controls interrupt routing of the card status change interrupt and enables the sources for card status change interrupt.</p>	

I/O Control Register

Type: Read/Write

Address: Socket A Index 07H
 Socket B Index 47H

Bit	Function
D7	<p>I/O Window 1 Wait State.</p> <p>0: 16-bit system accesses occur without additional wait states.</p> <p>1: 16-bit system accesses occur with 1 additional wait state.</p>
D6	<p>I/O Window 1 Zero Wait State for 8-bit I/O Access.</p> <p>0: System I/O access will occur with additional wait states.</p> <p>1: System I/O access will occur with no additional wait states and the *ZWS signal will be returned to the system bus.</p>
D5	<p>I/O Window 1 *IOCS16 Source.</p> <p>0: *IOCS16 is generated based on the value of the data size bit.</p> <p>1: *IOCS16 is generated based on the *IOIS16 signal from the PC Card.</p>
D4	<p>I/O Window 1 Data Size.</p> <p>0: 8-bit I/O data path</p> <p>1: 16-bit I/O data path</p>
D3	<p>I/O Window 0 Wait State.</p> <p>0: 16-bit system accesses occur without additional wait states.</p> <p>1: 16-bit system accesses occur with 1 additional wait state.</p>
D2	<p>I/O Window 0 Zero Wait State, for 8-bit I/O access.</p> <p>0: System I/O access will occur with additional wait states.</p> <p>1: System I/O access will occur with no additional wait states and the *ZWS signal will be returned to the system bus.</p>

D1 (cont.)	I/O Window 0 *IOCS16 Source. 0: *IOCS16 is generated based on the value of the data size bit. 1: *IOCS16 is generated based on the *IOIS16 signal from the PC Card.
D0	I/O Window 0 Data Size. 0: 8-bit I/O data path. 1: 16-bit I/O data path.
<p>Notes:</p> <ol style="list-style-type: none"> <i>1. This register indicates the configuration for both I/O mapping windows. This register is set based on information read from the PC Card's Card Information Structure. Dynamic bus sizing on a cycle by cycle basis is implemented to the PC Card interface if the source of the *IOCS16 signal is the PC Card as determined by the window's *IOCS16 source bit. In order to be compatible with some software and hardware implementations such as an IDE interface, the PC Card must decode two consecutive I/O addresses to determine the cycle data width. In order to meet the system bus timing, this type of PC Card must decode the address lines A[9:0] prior to the card enable signal becoming active at the interface. The card decodes the address and responds to a 16-bit cycle by enabling *IOIS16. The PCSC qualifies *IOIS16 with the card enable signals to generate *IOCS16 to the system bus.</i> <i>2. These bits set the data path size and select zero wait states for the appropriate bus access, and are used to determine system bus signal *IOCS16.</i> <i>3. *IOWR is delayed so that data will be valid at the falling edge of *IOWR, as required by the PCMCIA specification. This does not lengthen normal 8-bit cycles but adds one wait state to 16-bit write cycles. Setting bit D2 or D6 will inhibit this delay in the corresponding window.</i> 	

I/O Address Start Register Low Byte

Type: Read/Write
Address: Socket A Index 08H, 0CH for windows 0-1
Socket B Index 48H, 4CH for windows 0-1

Bit	Function
D[7:0]	I/O Window Start Address A[7:0]. Low order address bits used to determine the start address of the corresponding I/O address window. This provides a minimum 1 byte window for the I/O address window.

I/O Address Start Register High Byte

Type: Read/Write
Address: Socket A Index 09H, 0DH for windows 0-1
Socket B Index 49H, 4DH for windows 0-1

Bit	Function
D[7:0]	I/O Window Start Address A[15:8]. High order address bits used to determine the start address of the corresponding I/O address Window.

I/O Address Stop Register Low Byte

Type: Read/Write
Address: Socket A Index 0AH, 0EH for windows 0-1
Socket B Index 4AH, 4EH for windows 0-1

Bit	Function
D[7:0]	I/O Window Stop Address A[7:0]. Low order address bits used to determine the stop address of the corresponding I/O address window. This provides a minimum 1 byte window for the I/O address window.

Chapter 4 Register Bit Declarations

VADEM VG-469 PC Card Socket Controller

I/O Address Stop Register High Byte

Type: Read/Write

Address: Socket A Index 0BH, 0FH for windows 0-1
Socket B Index 4BH, 4FH for windows 0-1

Bit	Function
D[7:0]	I/O Window Stop Address A[15:8]. High order address bits used to determine the stop address of the corresponding I/O address window.

System Memory Address Mapping Start Register Low Byte

Type: Read/Write

Address: Socket A Index 10H, 18H, 20H, 28H, 30H for windows 0-4
Socket B Index 50H, 58H, 60H, 68H, 70H for windows 0-4

Bit	Function
D[7:0]	System Memory Window Start Address A[19:12]. Low order address bits used to determine the start address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4K bytes.
<i>Note: A memory window cannot be set up below the first 64K of address space.</i>	

System Memory Address Mapping Start Register High Byte

Type: Read/Write

Address: Socket A Index 11H, 19H, 21H, 29H, 31H for windows 0-4
Socket B Index 51H, 59H, 61H, 69H, 71H for windows 0-4

Bit	Function
D7	Data Size. 0: 8-bit memory data path. 1: 16-bit memory data path.
D6	Zero Wait State. 0: System memory access will complete in 3 CLKs (16-bit) or 6 CLKs (8-bit) with IOCHRDY high. 1: System memory access completes in 2 CLKs (16-bit) or 3 CLKs (8-bit) with *ZWS signal driven low. The *WAIT signal will override this bit. If the Compatibility bit is low, *ZWS will not be asserted for access to an 8-bit memory window when both A0 and *SBHE are low. If the Compatibility bit is low, *ZWS will not be qualified with *MEMR or *MEMW during accesses to a 16-bit memory window.
D[5:4]	Scratch bits. These bits can be used for general purpose register storage and retrieval.
D[3:0]	System Memory Window Start Address A[23:20]. High order address bits used to determine the start address of the corresponding system memory address mapping window.
<i>Note: Bits in this register control the data path and additional wait states associated with each system memory window.</i>	

System Memory Address Mapping Stop Register Low Byte

Type: Read/Write

Address: Socket A Index 12H, 1AH, 22H, 2AH, 32H for windows 0-4
Socket B Index 52H, 5AH, 62H, 6AH, 72H for windows 0-4

Bit	Function
D[7:0]	System Memory Window Stop Address A[19:12]. Low order address bits used to determine the stop address of the corresponding system memory address mapping window. This provides a minimum memory mapping window of 4K bytes.

System Memory Address Mapping Stop Register High Byte

Type: Read/Write

Address: Socket A Index 13H, 1BH, 23H, 2BH, 33H for windows 0-4
Socket B Index 53H, 5BH, 63H, 6BH, 73H for windows 0-4

Bit	Function
D[7:6]	Wait States Select for 16-bit Memory Access. These bits determine the number of additional wait states for a 16-bit access to the system memory window. If the PC Card supports the *WAIT signal, wait states will be generated by the PC Card asserting the *WAIT signal. 00: standard 16-bit cycle (3CLKs per access). 01: 1 additional wait state (4 CLKs per access). 10: 2 additional wait states (5 CLKs per access). 11: 3 additional wait states (6 CLKs per access).
D[5:4]	Reserved
D[3:0]	System Memory Window Stop Address A[23:20]. High order address bits used to determine the start address of the corresponding system memory address mapping window.
<i>Note: Two bits in this register select the number of wait states for a 16-bit access to the corresponding system memory window.</i>	

Card Memory Offset Address Register Low Byte

Type: Read/Write

Address: Socket A Index 14H, 1CH, 24H, 2CH, 34H for windows 0-4
Socket B Index 54H, 5CH, 64H, 6CH, 74H for windows 0-4

Bit	Function
D[7:0]	Card Memory Offset Address A[19:12]. Low order address bits which are added to the system address bits A[19:12] to generate the memory address for the PC Card.

Card Memory Offset Address Register High Byte

Type: Read/Write

Address: Socket A Index 15H, 1DH, 25H, 2DH, 35H for windows 0-4
 Socket B Index 55H, 5DH, 65H, 6DH, 75H for windows 0-4

Bit	Function
D7	Write Protect. 0: write operations to the PC Cards through the corresponding system memory window are allowed. 1: write operations to the PC Card through the corresponding system memory window are inhibited.
D6	REG Active. 0: access to the system memory will result in common memory on the PC Card being accessed. 1: access to the system memory will result in attribute memory on the PC Card being accessed.
D[5:0]	Card Memory Offset Address A[25:20]. High order address bits which are added to the system address bits A[23:20] to generate the memory address for the PC Card.
<i>Note: For each corresponding system memory window, this register controls the software write protect of PC Card memory and whether the window is mapped to attribute or common memory on the PC Card.</i>	

UNIQUE REGISTERS

After reset, the Unique Registers are locked and cannot be read or written. To unlock, first write 0Eh to the index register and then write 37h to the index register. Any index or data register access between these two writes will abort the unlock sequence.

Control Register

Type: Read/Write

Address: Socket A Index 38H
Socket B Index 78H

Bit	Function
D7	Compatibility. This bit controls several compatibility functions. When set, it allows the activity timer status to be read on bit 7 of the Card Status Change register. See System Memory Address Mapping Start Register High Byte for more information.
D6	Slow Attribute Memory. If the card is operated at 3.3 volts, setting this bit will force the chip to access the attribute memory in 600ns memory cycle timing.
D5	INPACKEN: INPACK Enable. 0: VG-469 ignores *INPACK and always drives the SD bus. 1: VG-469 drives the SD bus during card I/O read cycles only when the card asserts *INPACK.
D4	LEDSTRETCH. 0: LED pulse width is directly controlled by read or write strobe width. Led brightness is proportional to access rate. 1: LED pulse is stretched to 50ms minimum width by internal digital oneshot.
D3	TSSI: Tri-states *SPKROUT and *INTR to save power in pull-up/pulldown resistors. 0: *SPKROUT, *INTR outputs are enabled. 1: *SPKROUT, *INTR are tri-stated.
D2	Wait State Compatibility. 0: IOCHRDY timing and operation are 82365 compatible. 1: *IOWR to card delayed in 16-bit I/O cycles and one wait state is added to meet PCMCIA write data setup time. In memory cycles where wait states are specified, IOCHRDY is driven active high for one clock at the end of the cycle.
D1	ASYNC. Set when CLK is asynchronous to ISA bus read/write strobes. Setting this bit will cause a wait state in certain cycles.

D0 (cont.)	<p>SLOW.</p> <p>0: Normal PCMCIA memory timing.</p> <p>1: Enable 600ns PCMCIA memory cycle timing. This delays the *OE or *WE command strobe to the PC Card and generates automatic wait states, for both 8 and 16-bit CPU and DMA cycles. If wait states have been programmed in the memory map registers, those will be in addition to the automatic wait states, and will be generated for 8 and 16-bit CPU and DMA cycles. One additional wait state should be programmed if CLK is 8 MHz. Read cycles will have two more automatic wait states than write cycles.</p>
------------	--

Timer Register

Type **Read/Write (except bits 5 and 6)**
Address: **Socket A Index 39H**
 Socket B Index 79H

Bit	Function
D7	<p>TMRES: Timer resolution.</p> <p>0: 15 seconds.</p> <p>1: 1 minute</p>
D6	TMRSTAT: Activity timer status, a read-only bit. Timed out when set.
D5	<p>SIGEN: This bit is read-only.</p> <p>When set, it indicates to software that the card is powered up, the PCMCIA interface outputs are enabled, and all power-up delays have been satisfied.</p>
D4	<p>ZEROPWR: Zero power.</p> <p>0: CDATA[15:0] are controlled as described in the Power and RESETDRV Register description.</p> <p>1: CDATA[15:0] are controlled as described in the Power and RESETDRV Register description, except that when both card detects are high and card Vcc is off, CDATA[15:0] becomes low instead of tristate. This reduces power dissipation in the chip.</p>
D[3:0] (cont.)	Activity Timer Timeout.
<p>Note: 1. This register controls the activity timer. The activity timer is programmable from 1 to 15 steps of 15 seconds, or 1 minute. The timer is disabled when set to 0. The timer is retriggered by an access to the card, or a card interrupt, or status change interrupt (except for card detect interrupts) when the card is present, powered up and the card interface is enabled. It is also retriggered when this register is written. A status change interrupt will be generated when the timer times out. The timer status is readable on bit D6, and if the Computability bit in the Control Register is set, it is also readable with the other interrupt status bits in the Card Status Change register.</p> <p>2. In order for the timer status to be properly latched into bit D6, following a card status change interrupt, the Card Status Change register must be read first.</p>	

Chapter 4
Register Bit Declarations

VADEM VG-469
PC Card Socket Controller

Miscellaneous Register

Type: Read/Write
Address: Socket A Index 3AH
 Socket B Index 7AH

Bit	Function
D7	UNLOCK: reads back as a 1 when Unique indexed registers are unlocked and accessible, undefined when registers are locked. Registers can be locked by writing a 0 to this bit. This bit is shared between two sockets.
D6	VADEMREV: When VADEMREV and UNLOCK are set, Identification and Revision Register reads Vadem PCSC revision. Otherwise, it reads revision of similar Intel part.
D5	Reserved.
D4	Activity LED Enable. When set, non-DMA accesses to this slot cause the LED output to go low. If no GPIO pin is programmed to be the LED output, IRQ12 will be used.
D3	DMAWSB. 0: Enables wait states as specified in the System Memory Address Mapping Stop Register High Byte to be generated for DMA cycles. For use with 8 MHz DMA cycles. 1: Wait states specified in the System Memory Address Mapping Stop Register High Byte are not generated for DMA cycles. For use with standard ISA DMA cycles.
D2	Reserved.
D1	TSBIT60. 0: Host bus SD[6:0] functions normally. 1: When the host reads the ATA drive address register at port 3F7H or 377H, bits SD[6:0] will remain tristated to avoid contention with a hard disk interface on the host bus.
D0	Reserved. This bit should not be set to 1.

A_GPIO Configuration Register

Type: Read/Write (except bits 0 to 3, which are read-only)

Address: Index 3BH

Bit	Function
D7	EXTDECODE: Enables external chip select. This bit disables internal address decoding for the VG-469 index and data registers, and enables the A_GPIO pin to become the active low external chip select input.
D[6:4]	GPSEL[2:0]. These bits decode the function of A_GPIO if external chip select is disabled (EXTDECODE=0). 000: A_GPIO = *GPI input. 001: A_GPIO = *RIO output. 010: Not used. 011: A_GPIO = GP output. Choose this setting if A_VPPEN0 is directed to A_GPIO, or when defining Zoom Video. 100: A_GPIO = *PCS output. 101: A_GPIO = *LED output. 110: A_GPIO = Power Down Control input. The VG-469 will enter Power Down mode when the Power Down bit in the Global Control register is set, and the A_GPIO pin is high. 111: GPIO = DMA function. A_GPIO becomes the HTC (host TC) input from the ISA bus. When EXTDECODE = 1, A_GPIO = *CS input.
D[3:1]	These bits are reserved, always read 0.
D0	Plug-and-Play Availability. 0: Plug-and-Play not available. 1: Plug-and-Play available.
Note: This register controls the A_GPIO pin. All bits in this register are 0 after reset. Since A_GPIO defaults to an input, a 1 Megohm pull-up resistor is required if this pin will be used as *PCS. If *GPI is not assigned to the A_GPIO pin, bit 7 of the Interface Status Register will always read 1.	

Chapter 4
Register Bit Declarations

VADEM VG-469
PC Card Socket Controller

B_GPIO Configuration Register

Type: Read/Write (except bits 0 to 3, which are read-only)

Address: Index 7BH

Bit	Function
D7	Reserved. This bit should be left at 0.
D[6:4]	GPSEL[2:0]. These 3 bits decode the function of B_GPIO if external chip select is disabled (EXTDECODE=0). 000: Not used. 001: B_GPIO = *RIO output. 010: Not used. 011: B_GPIO = GP output. Choose this setting if B_VPPEN0 is directed to B_GPIO. 100: B_GPIO = *PCS output. 101: B_GPIO = *LED output. 110: Not used. 111: B_GPIO = DMA function. B_GPIO becomes the HDRQ (host DRQ) output to the ISA bus or steering logic.
D[3:1]	These bits are reserved, always read 0.
D0	Plug-and-Play Availability 0: Plug-and-Play not available. 1: Plug-and-Play available.

Extended Mode Register-A

Type: Read/Write

Address: Index 3CH

Bit	Function
D7	IRQ7 Pin Functionality. This bit should not be set unless the chip is configured to enable Plug-and-Play. 0: IRQ7 pin functions as Interrupt Request output. 1: IRQ7 pin is redefined to be *HDACK input for DMA function.
D6	RIO Steered to INTR. If set, RIO is directed to the INTR pin.
D5	Test Mode Enable.
D4	C Step Computability. 0: VG-469 is Intel 82365 B step compatible. 1: VG-469 is Intel 82365 C step compatible, except for Power and RESERTDRV Control Register.
D3	CABLEMODE. Controls IOCHRDY, *MEMCS16, *IOCS16, *ZWS. 0: These signals operate normally (open drain outputs). 1: These signals become totem pole outputs, for driving a cable with open drain receiver buffers at the far end.
D2	Internal Voltage Sense. 0: Voltage sense register is external. If this bit is low and the VG-469 is not connected for DMA operation, *B_VS1 must be pulled up to ISA Vcc. 1: Voltage sense register is internal. Bit cannot be set in extended configuration.
D[1:0]	VPPST[1:0]. These bits steer A_VPPEN0 and B_VPPEN0. 00: A_VPPEN0 and B_VPPEN0 not available. 01: A_VPPEN0 and B_VPPEN0 steered to IRQ10 and IRQ11 respectively. 10: A_VPPEN0 and B_VPPEN0 steered to *A_VS2 and *B_VS2. 11: A_VPPEN0 and B_VPPEN0 steered to A_GPIO and B_GPIO. GPSEL[2:0] must be set to 3 for both sockets.

Chapter 4
Register Bit Declarations

VADEM VG-469
PC Card Socket Controller

Extended Mode Register-B

Type: Read/Write
 Address: Index 7CH

Bit	Function
D[7:1]	Reserved.
D0	Select 3.3 volt for socket B. In extended mode buffered socket B configuration, controls threshold for socket B power plane. 0: 5 volt. 1: 3.3 volt.

Programmable Chip Select Register

Type: Read/Write
 Address: Socket A Index 3DH
 Socket B Index 7DH

Bit	Function
D[7:0]	A[9:2] for I/O; A[23:16] for memory.
<i>Note: This register is for Programmable Chip Select in the VG-469.</i>	

DMA and Programmable Chip Select Configuration Register

Type: Read/Write
 Address: Socket A Index 3EH
 Socket B Index 7EH

Bit	Programmable Chip Select Configuration Function
D7	Reserved.
D[6:5]	PCSSIZE[1:0]: select the size of the decoded block. 00: 64 Kbyte (Memory), 4 byte (I/O). 01: 128 Kbyte (Memory), 8 byte (I/O). 10: 256 Kbyte (Memory), 16 byte (I/O). 11: 512 Kbyte (Memory), 32 byte (I/O).

D4	PCSIO. 0: Memory mode. 1: I/O mode.
D3	STATIRQSHARE. Enables sharing of status interrupts in an ISA system if status interrupt is steered to an IRQ pin. When a status change occurs, the IRQ will pulse low for at least 4 clock periods. 0: Status IRQ is active high level. 1: Status IRQ is active low, open drain pulse.
D[2:0]	Reserved.
Bit	DMA Function
D7	Reserved.
D[6:5]	*DREQ steering. 00: *DREQ assigned to *IOIS16. 01: *DREQ assigned to *SPKR. 10: *DREQ assigned to *INPACK. 11: Reserved.
D4	DMA data size. 0: 8-bit DMA 1: 16-bit DMA.
D3	STATIRQSHARE. Enables sharing of status interrupts in an ISA system if status interrupt is steered to an IRQ pin. When a status change occurs, the IRQ will pulse low for at least 4 clock periods. 0: Status IRQ is active high level. 1: Status IRQ is active low, open drain pulse.
D[2:1]	Terminal count steering. 00: Automatic steering, to *WE if DMA read, to *OE if DMA write. 01: Steered to *WE. 10: Steered to *OE. 11: TC disabled.
D0	DMA Mode. If the card is the DMA device, setting this bit enables the DMA function.
<i>Note: In default mode, where D0 is low this register is for programmable chip select configuration in the VG-469. Once D0 is programmed to 1, the card DMA function is enabled.</i>	

Chapter 4 Register Bit Declarations

VADEM VG-469 PC Card Socket Controller

ATA Register

Type: Read/Write

Address: Socket A Index 3FH
Socket B Index 7FH

Bit	Function
D[7:3]	General Purpose Outputs for ATA drive. When ATA bit is true, these bits drive CA[25:21].
D2	TSBIT7. 0: host bus bit SD7 functions normally. 1: When the host reads the ATA Drive Address register at port 3F7h or 377h, bit SD7 of the host bus will remain tristated to avoid contention with a floppy disk interface on the host bus.
D1	BVD2LED: defines the definition of BVD2 in I/O mode. 0: *SPKR input. 1: LED input to be used with ATA drive.
D0	ATA. 0: normal operation for CA[25:21]. 1: CA[25:21] become GP outputs controlled by D[7:3].

PLUG AND PLAY REGISTERS

Set RD_DATA Port

Type: Write Only
Address: Index 00h

Bit	Function
D[7:0]	Writing to this location modifies the address of the port used for reading from VG-469. D[7:0] become I/O read port address bits [9:2].

Serial Isolation

Type: Read Only
Address: Index 01h

Bit	Function
D[7:0]	A read to this register causes VG-469's Plug and Play logic in the isolation state to compare one bit of the boards ID.

Configuration Control

Type: Write Only
Address: Index 02h

Bit	Function
D[7:3]	Reserved.
D2	A write to this bit causes CSN to be reset to 0.
D1	A write to this bit causes VG-469 to enter the Wait for Key state but CSN is preserved and the logical device is not affected.
D0	A write to this bit performs a reset function on the logical device. This resets the contents of configuration register to their default state. VG-469's logical device enters the default state and the CSN is preserved.

The values are not sticky, that is, VG-469 will automatically clear them and there is no need for software to clear this bit.

Chapter 4 Register Bit Declarations

VADEM VG-469 PC Card Socket Controller

Wake[CSN]

Type: Write Only

Address: Index 03h

Bit	Function
D[7:0]	A write to this address will cause VG-469 with its CSN matching the write data [7:0] to go from the Sleep state to either the Isolation state if the write data for this command is zero or the Config state if the write data is not zero.

Resource Data

Type: Read Only

Address: Index 04h

Bit	Function
D[7:0]	A read from this address reads the next byte of resource information. The Status register (index 05h) must be polled until bit D0 is set before this register may be read.

Status

Type: Read Only

Address: Index 05h

Bit	Function
D[7:6]	Reserved
D0	When set indicates it is okay to read the next data byte from the Resource Data register.

Card Select Number

Type: Read/Write

Address: Index 06h

Bit	Function
D[7:0]	A write to this port sets CSN for VG-469. The CSN is a value uniquely assigned after the serial identification process so that VG-469 may be individually selected during a Wake[CSN] command.

Activate

Type: Read/Write

Address: Index 30h

Bit	Function
D[7:6]	Reserved, must be zero.
D0	This bit controls if the logical device is active on the ISA bus. If set, activates the logical device. I/O range check must be disabled before setting this bit.

I/O Range Check

Type: Read/Write

Address: Index 31h

Bit	Function
D[7:2]	Reserved.
D1	Enable I/O Range Check, if set then I/O Range Check is enabled. I/O Range Check is only valid when the logical device is inactive.
D0	If set, forces the logical device to respond to I/O reads of the logical device's assigned I/O range with a 55h when I/O range check is in operation. If clear, the logical device drives AAh.

This register is used to perform a conflict check on the I/O port range programmed for use by a logical device.

I/O Port Base Address High Byte

Type: Read/Write

Address: Index 60h

Bit	Function
D[7:0]	I/O port address [15:8] for accessing the VG-469 index register, defaults to 03h.

Chapter 4
Register Bit Declarations

VADEM VG-469
PC Card Socket Controller

I/O Port Base Address Low Byte

Type: Read/Write

Address: Index 61h

Bit	Function
D[7:0]	I/O port address [7:0] for accessing the VG-469 index register, defaults to E0h or E2h, depending on resistor strapping on *INTR.

DC Characteristics

DC Characteristics for $V_{CC} = 5.0V \pm 0.5V$

Symbol	Parameter	Min	Max	Units
V_{CC}	Power Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage, $V_{CC} = 5.5V$		0.4	V
V_{OH}	Output High Voltage, $V_{CC} = 4.5V$	2.4		V
I_{IL}	Input Leakage Current		± 10	μA
I_{OL}	Output Leakage Current		± 10	μA

DC Characteristics for $V_{CC} = 3.3V \pm 0.3V$

Symbol	Parameter	Min	Max	Units
V_{CC}	Power Supply Voltage	3.0	3.6	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage, $V_{CC} = 3.6V$		0.4	V
V_{OH}	Output High Voltage, $V_{CC} = 3.0V$	2.4		V
I_{IL}	Input Leakage Current		± 10	μA
I_{OL}	Output Leakage Current		± 10	μA

Capacitance

Symbol	Parameter	0° to +70°C	Units
C_{IN}	Maximum Input Capacitance	10	pF
C_{OUT}	Maximum Output Capacitance	10	pF
C_{IO}	Maximum I/O Capacitance	10	pF

Chapter 5
DC Specs and Maximum Ratings

VADEM VG-469
PC Card Socket Controller

Absolute Maximum Ratings*

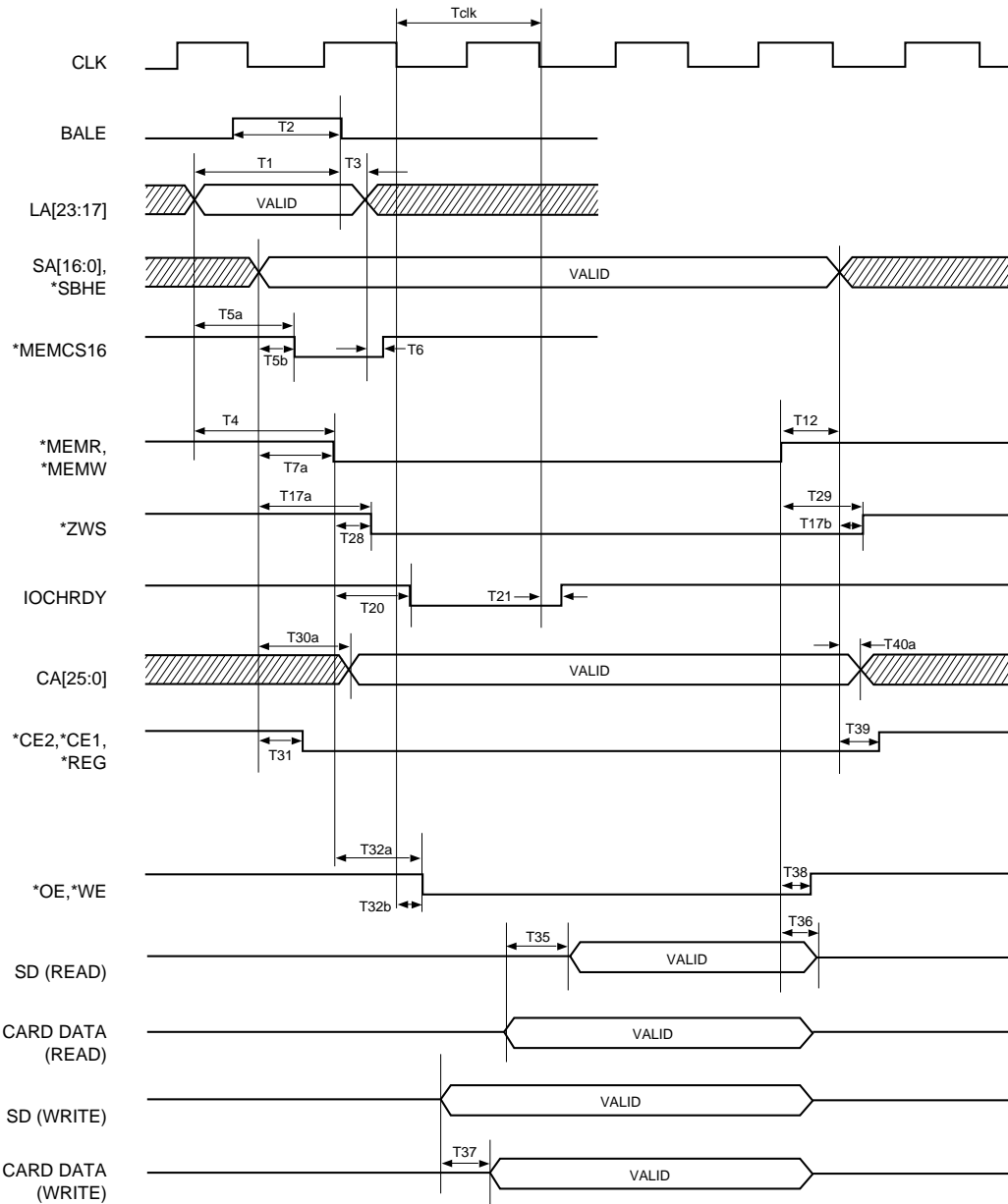
Symbol	Parameter	Value	Units
V _{CC}	DC Power Supply Voltage	-0.5 to + 7.0	V
V _{IN} , V _{OUT}	DC Input, Output Voltage	-0.5 to V _{DD} + 0.5	V
I	DC Current Drain V _{DD} and V _{SS} Pins	100	mA
T _{STG}	Storage Temperature	-55 to + 150	°C
T _L	Lead Temperature	250	°C
T _{OPER}	Operating Temperature	0 to + 70	°C

**Note: Stress beyond ranges listed in this table may cause physical damage to a device and should be avoided. This table does not imply that operations at conditions above those listed in AC Timings is possible. This is a stress rating and operation of a device at or above this rating for an extended period of time may cause failure or affect reliability.*

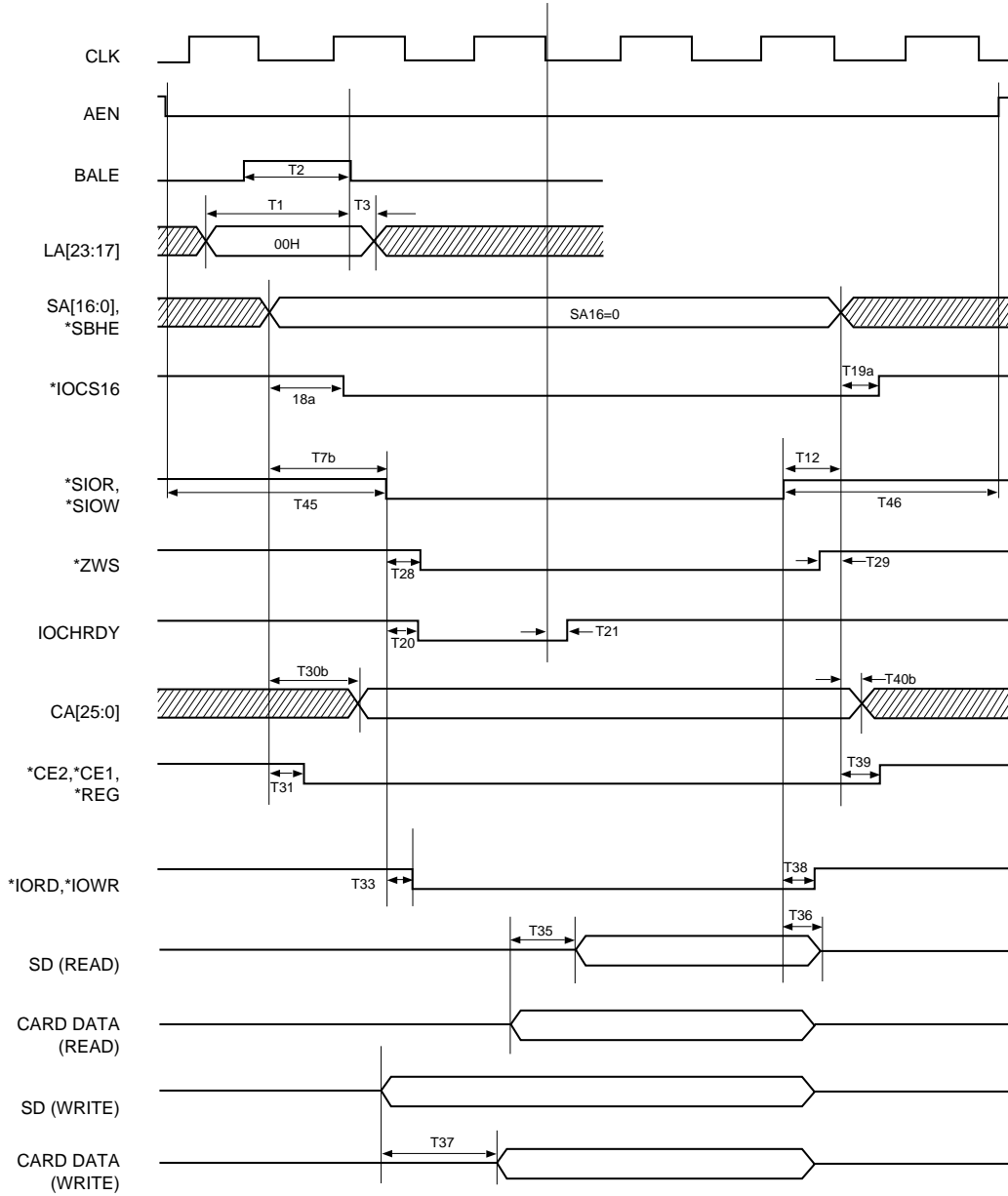
Icc Specifications

Symbol	Parameter	Typical	Max	Units
I _{CC}	Supply Current	12	-	mA
I _{CC1}	Supply Current / Suspend Mode Outputs Tri-stated / No Clock / Inputs Not Toggling	10	-	μA

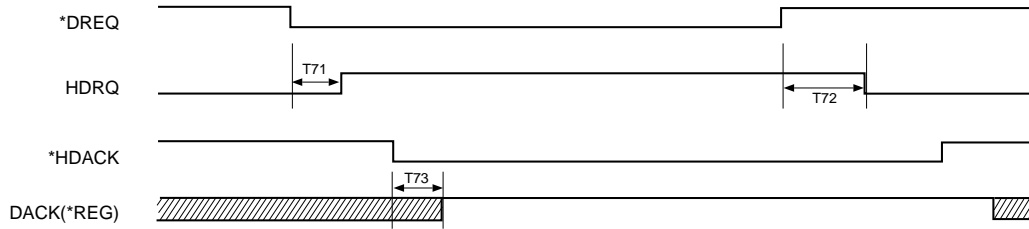
Memory Cycle



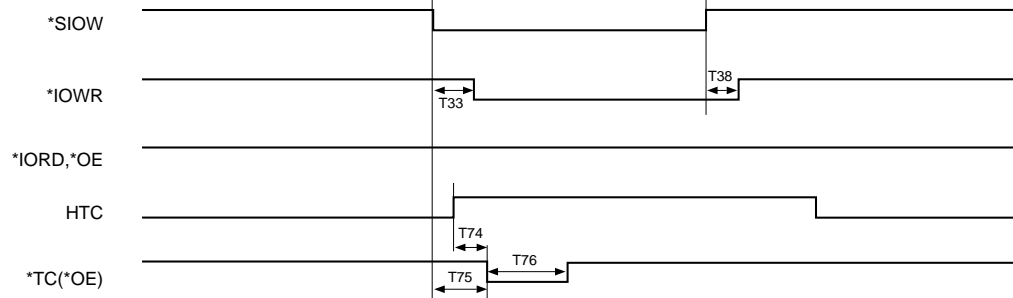
I/O Cycle



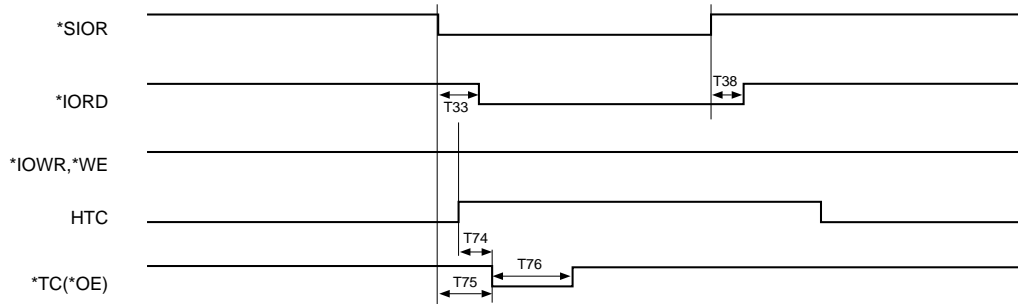
DMA Cycle



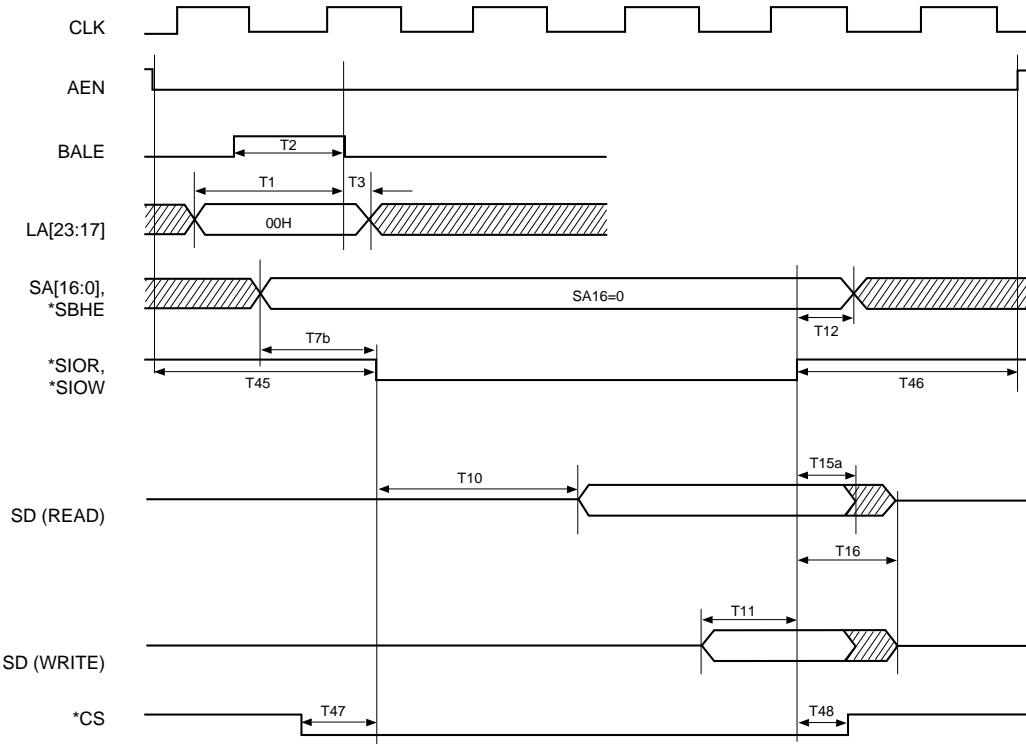
DMA READ



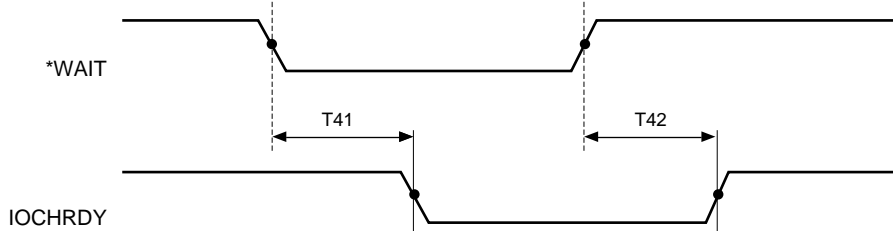
DMA WRITE



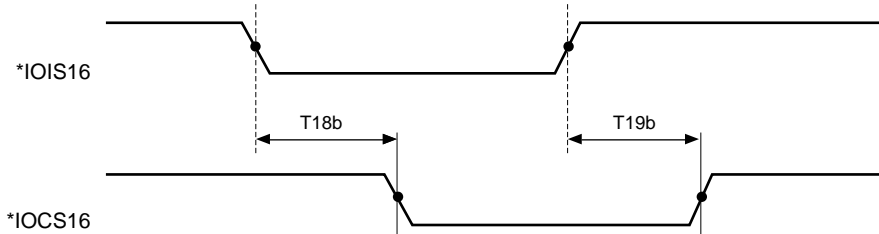
Register Access



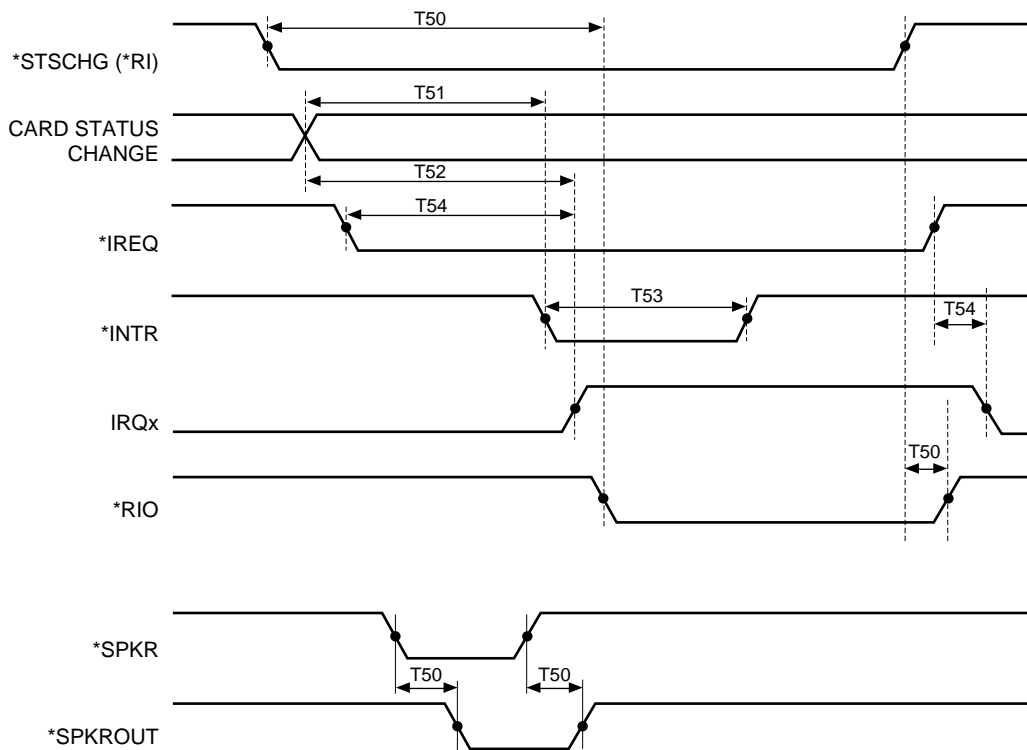
Wait



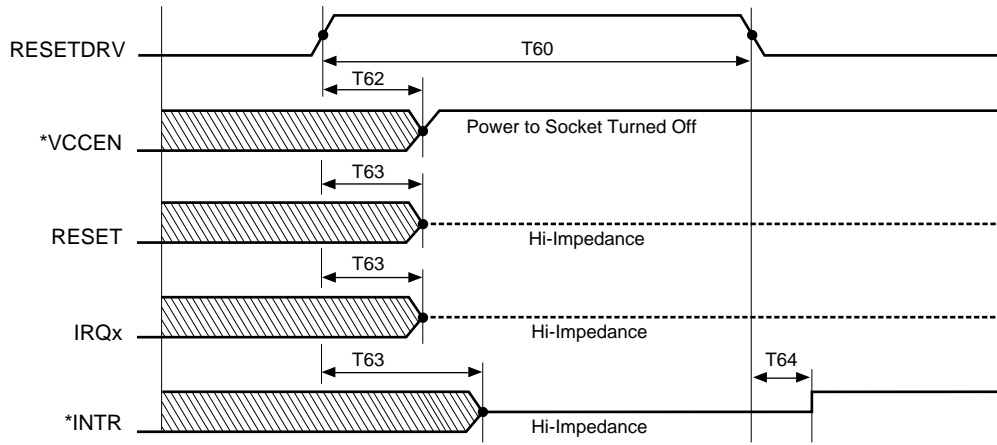
IOIS16



Interrupt, Ring Indicate, Speaker Timings



RESET



AC Characteristics

T = 0C to 70C, Vcc = 5.0V +/- 0.5V, all units in nanosecond.

Symbol	Parameter	Min	Max	Notes
Tclk	ISA Bus Clock Period	120	210	
T1	LA[23:17] Setup to BALE Falling	45	-	1
T2	BALE Pulse Width	50	-	1
T3	LA[23:17] Hold from BALE Falling	15	-	1
T4	LA[23:17] Setup to Memory Command Active	23	-	
T5a	*MEMCS16 Valid from LA[23:17]	-	40	2
T5b	*MEMCS16 Valid from SA[16:12]	-	30	3
T6	*MEMCS16 Hold from LA[23:17]	-	40	2
T7a	SA[16:12] and *SBHE Setup to Memory Command Active	23	-	
T7b	SA[15:0] and *SBHE Setup to I/O Command Active	45	-	
T10	Internal Register Read Data Access	-	60	
T11	Internal Register Write Data Setup	40	-	
T12	SA[16:0] and *SBHE Hold from Command Inactive	25	-	
T15a	Internal Register Read Data Hold	0	-	
T15b	Internal Register Write Data Hold	15	-	
T16	Internal Register Access Command Inactive to SD[7:0] Tri-state	-	30	
T17a	*ZWS Active from LA[23:17], SA[16:12] Valid (16-bit Memory Only)	-	60	
T17b	*ZWS Tristate from SA[16:12] Invalid (16-bit Memory Only)	-	55	
T18a	*IOCS16 Valid Delay from SA[15:0] Internally Generated		40	4
T18b	*IOIS16 Active to *IOCS16 Active	-	25	
T19a	*IOCS16 Hold from SA[15:0] Internally Generated	0	40	
T19b	*IOIS16 Inactive to *IOCS16 Inactive	0	25	
T20	IOCHRDY Low from Memory or I/O Command	-	32	5
T21	IOCHRDY Active from Falling Edge of CLK	-	24	5
T28	*ZWS Active from 8-bit Command (Memory or I/O)	-	25	
T29	*ZWS Hold from Command (Memory or I/O)	0	35	
T30a	CA[25:12] Valid Delay from SA[16:12] (Memory Cycle)	-	60	
T30b	CA[15:0] Valid Delay from SA[15:0] (I/O Cycle)	-	30	
T31	*CE2, *CE1, *REG Valid from LA[23:17], SA[16:0]	-	50	
T32a	*OE, *WE Valid from Memory Command (except for 16-bit with Memory Delay)	-	35	
T32b	*OE, *WE Valid from Falling Edge of CLK (16-bit with Memory Delay)	-	35	

Chapter 7
Timing Tables

Vadem VG-469
PC Card Socket Controller

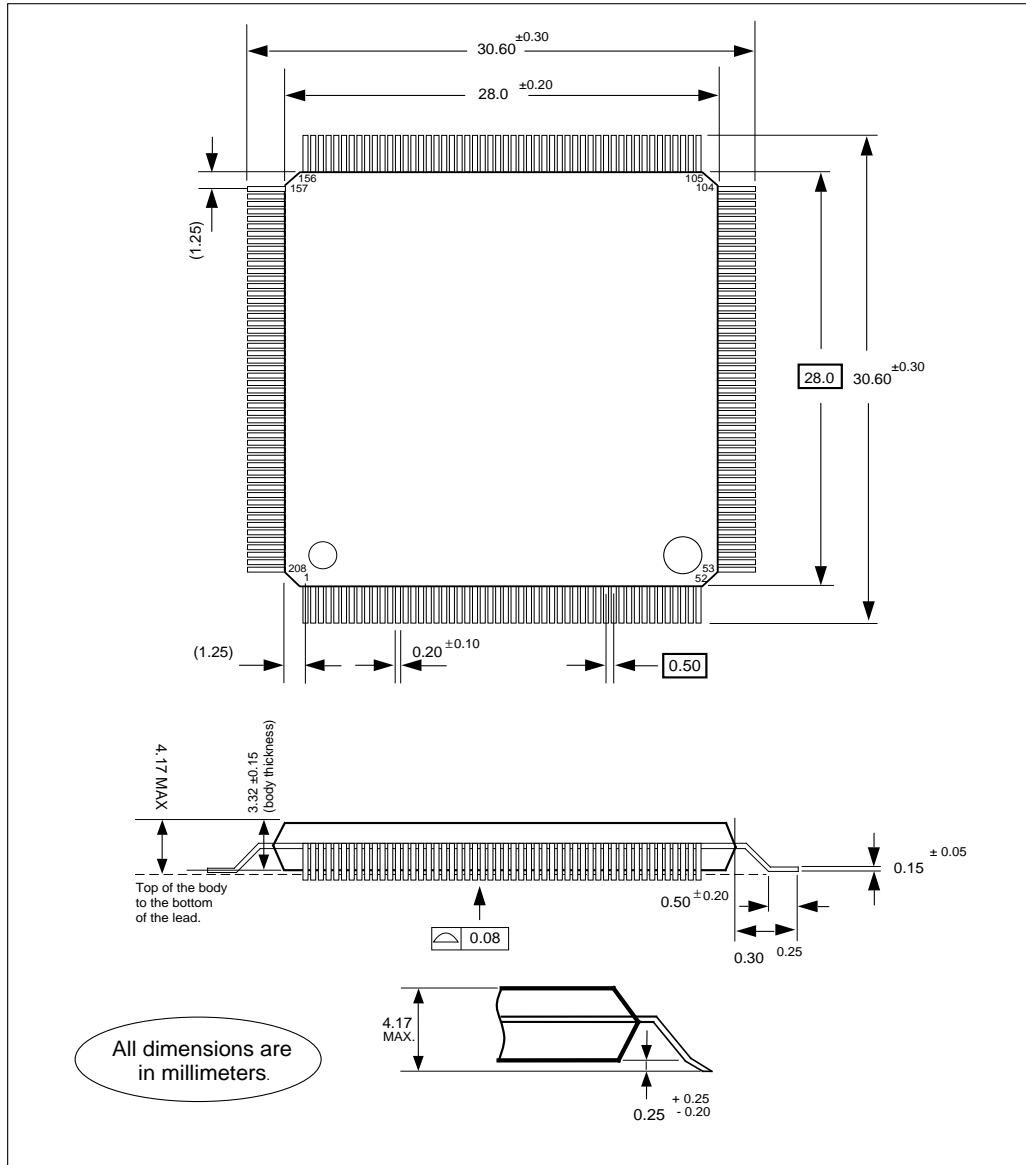
Symbol	Parameter	Min	Max	Notes
T33	*IORD, *IOWR Valid from I/O Command	-	25	
T35	SD[15:0] Valid Delay from Card Data[15:0] when Read	-	30	
T36	SD[15:0] Hold from Memory or I/O Read Command Inactive	10	-	
T37	Card Data[15:0] Valid Delay from SD[15:0] when Write	-	30	
T38	Socket Command Invalid from ISA Command Inactive	0	25	
T39	*CE2, *CE1, *REG Invalid from SA[16:0] Invalid	-	45	
T40a	CA[25:12] Hold from SA[16:12] (Memory Cycle)	0	-	
T40b	CA[15:0] Hold from SA[15:0] (I/O Cycle)	0	-	
T41	*WAIT Active to IOCHRDY Inactive	-	20	
T42	*WAIT Inactive to IOCHRDY Active	0	20	
T45	AEN Low to Command Active Setup	45	-	
T46	Command Inactive to AEN High	25	-	
T47	*CS Active to Internal Register Access Command Active	100	-	
T48	*CS Hold from Internal Register Access Command Inactive	0	-	
T50	*RI to *RIO Delay, *SPKR to *SPKROUT Delay	-	30	
T51	Card Status Change to *INTR Valid Delay	-	2 Tclk + 50	
T52	Card Status Change to IRQn Valid Delay	-	50	
T53	*INTR Pulse Width	4 Tclk	-	
T54	*IREQ to IRQn Valid Delay	-	50	
T60	RESETDRV Pulse Width	1000	-	
T62	Signal Inactive from RESETDRV Rising	-	200	
T63	Signal Tri-state from RESETDRV Rising	-	200	
T64	*INTR Inactive from RESETDRV Falling	10	50	
T71	*DREQ Active to HDRQ Active	-	30	
T72	*DREQ Inactive to HDRQ Inactive	-	40	
T73	*HDACK Active to DACK (*REG) High	-	40	
T74	HTC Active to *TC (*WE or *OE) Active	Tclk + 10	2 Tclk + 30	6
T75	ISA I/O Command to *TC (*WE or *OE) Active	Tclk + 10	2 Tclk + 30	7
T76	*TC (*WE or *OE) Pulse Width	Tclk - 10	Tclk	

Notes:

1. BALE may be pulled high for applications which do not have LA[23:17] transition during the cycle.
2. MEMCS16 Decode A[23:12] (bit D5) must be set to zero in the Address Window Enable Register.
3. MEMCS16 Decode A[23:12] (bit D5) is set to zero in the Address Window Enable Register.
4. I/O Window *IOCS16 Source is based on the value of the data size bit. I/O Control Register bit D1 or D5 set to zero.
5. Internal Wait State Generator.
6. Maximum Delay is applicable if HTC becomes active after ISA I/O command is asserted.
7. Maximum Delay is applicable if ISA I/O command is asserted after HTC becomes active.

QFP Diagram

208 LEAD QUAD FLAT PACK



Vadem VG-469
PC Card Socket Controller



V A D E M

1960 Zanker Rd. San Jose, CA 95112
Tel 408 467 2100 Fax 408 467 2100

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V A D E M

VADEM VG-469
PC CARD SOCKET CONTROLLER

DATA MANUAL

July 1995

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V A D E M

1960 Zanker Road San Jose, CA 95112 Tel: 408.467.2100 Fax: 408.467.2199

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