NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6355G

16 Bit D/A CONVERTER

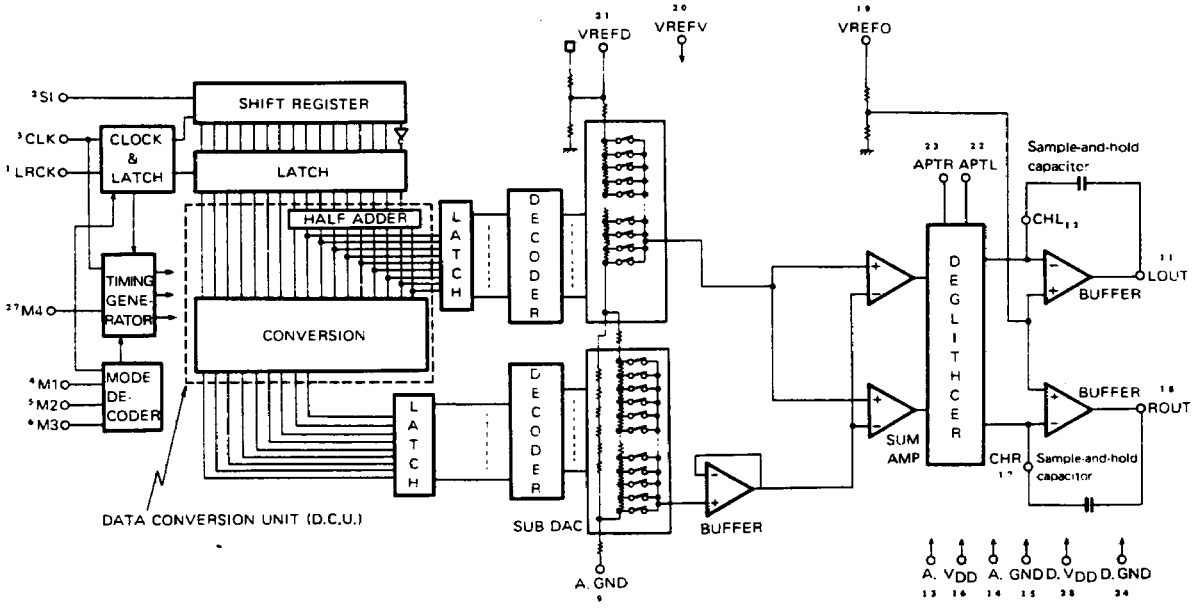
The μPD6355G is a 16-bit D/A converter for digital audio equipment. To facilitate application as an audio D/A converter, this LSI incorporates built-in sample-and-hold circuit, output operational amplfier, and zero-point offset circuit.

This COMS LSI operates on +5 V single power supply at low current consumption.

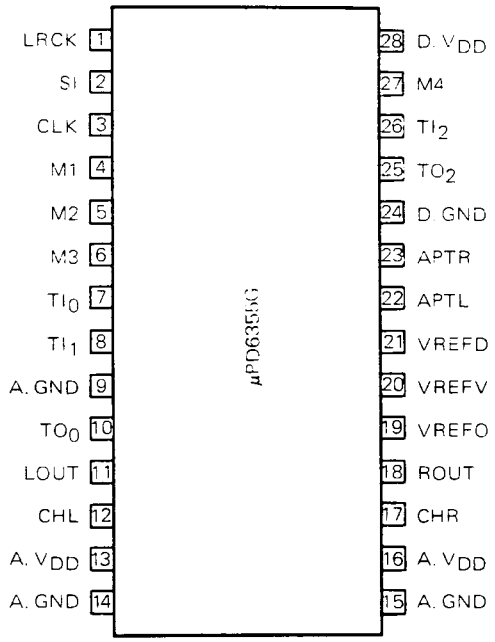
FEATURES

- +5 V single power supply
- CMOS configuration
- Built-in sample-and-hold circuit
- Built-in output operational amplifier
- Built-in 0-point offset circuit
- Resistance strings system
- 2 f_S (2 channels X 88.2 kHz sampling) capability
- 28-pin MF package

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Output Voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V
Input Voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (T_a=−20 to +75 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
High-level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V
Low-level Input Voltage	V_{IL}	0		0.3 V_{DD}	V

ELECTRICAL CHARACTERISTICS (T_a=25 °C, V_{DD}=+5 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Resolution	RES		16		Bit	
Total Harmonic Distortion 1	THD1		.007	.01	%	f_{IN}=1 kHz, 0 dB
Total Harmonic Distortion 2	THD2		.07		%	f_{IN}=1 kHz, −20 dB
Full Scale Output Voltage	V_{FS}	1.50	1.65	1.80	V	
Cross Talk	C·T	77	83		dB	f_{IN}=1 kHz
S/N Ratio	S/N	84	90		dB	
Load Resistance	R_L	5			kΩ	R_{OUT}, L_{OUT} terminal.
Sampling Time	T_{SP}	2			μs	Sample & hold capacitor is 47 pF.
Hold Time	T_{HLD}			32	μs	
Settling Time	T_S	2			μs	
Clock Frequency	f_{CLK}			5	MHz	M4 is low level.
				3	MHz	M4 is high level.
Clock Pulse Width	t_{SCK}	100			ns	
SCK, LRCK Setup Time	t_{DC}	100			ns	
SCK, LRCK Hold Time	t_{CD}	100			ns	
Supply Current	I_{DD}		13	20	mA	

TERMINAL FUNCTION

Terminal No.	Symbol	Terminal Name	Description	Input Output
1	LRCK	Left/Right Clock	Input terminal for left/right identification signal	Input
2	SI	Series Input	Input terminal for serial data	Input
3	CLK	Clock	Input terminal for serial input data read clock	Input
4	M_1	Mode 1.	Input data mode switching terminal	Input
5	M_2	Mode 2.		
6	M_3	Mode 3.		
7	TI_0	Test Input	Testing terminal. Normally connected to A. GND.	Input
8	TI_1	Test Input		
9	A. GND	Analog Ground	Ground terminal for the analog circuit.	
10	TO_0	Test Out	Testing terminal. Normally kept open.	Output
11	LOUT	L-ch Output	Left analog signal output terminal.	Output
12	CHL	Hold Capacitance L-channel	Terminal for left analog signal sample-and-hold capacitor connection.	Output
13	A. V_{DD}	Analog Power Supply	Power supply terminal for the analog circuit.	
14	A. GND	Analog Ground	Ground terminal for the analog circuit.	
15	A. GND	Analog Ground		
16	A. V_{DD}	Analog Power Supply	Power supply terminal for the analog circuit.	
17	CHR	Hold Capacitance R-channel	Terminal for right analog signal sample-and-hold capacitor connection.	Output
18	R_{OUT}	R-channel Output	Right analog signal output terminal.	Output
19	VREFO	Voltage Reference	Operational amplifier reference bias terminal. Normally connected to A. GND via a capacitor.	
20	VREFV	Voltage Reference	Normally connected to A. GND via a capacitor.	
21	VREFD	Voltage Reference	Resistance strings bias terminal. Normally connected to A. GND via a capacitor.	
22	APTL	Aperture L-channel	Terminal for sample and hold of the left analog output.	Input
23	APTR	Aperture R-channel	Terminal for sample and hold of the right analog output.	Input
24	D. GND	Digital Ground	Ground terminal for the logic circuit.	
25	TO_2	Test Out	Test terminal. Normally kept open.	Output
26	TI_2	Test	Test terminal. Normally connected to D. V_{DD}	Input

Terminal No.	Symbol	Terminal Name	Description	Input/ Output
27	M4	Mode 4.	Selects the clock for the internal logic circuit. This terminal selects whether to divide the signal input from the CLK terminal. The signal is not divided at high level, or is divided in half at low level.	Input
28	D. V_{DD}	Digital Power Supply	Power supply terminal for the logic circuit.	

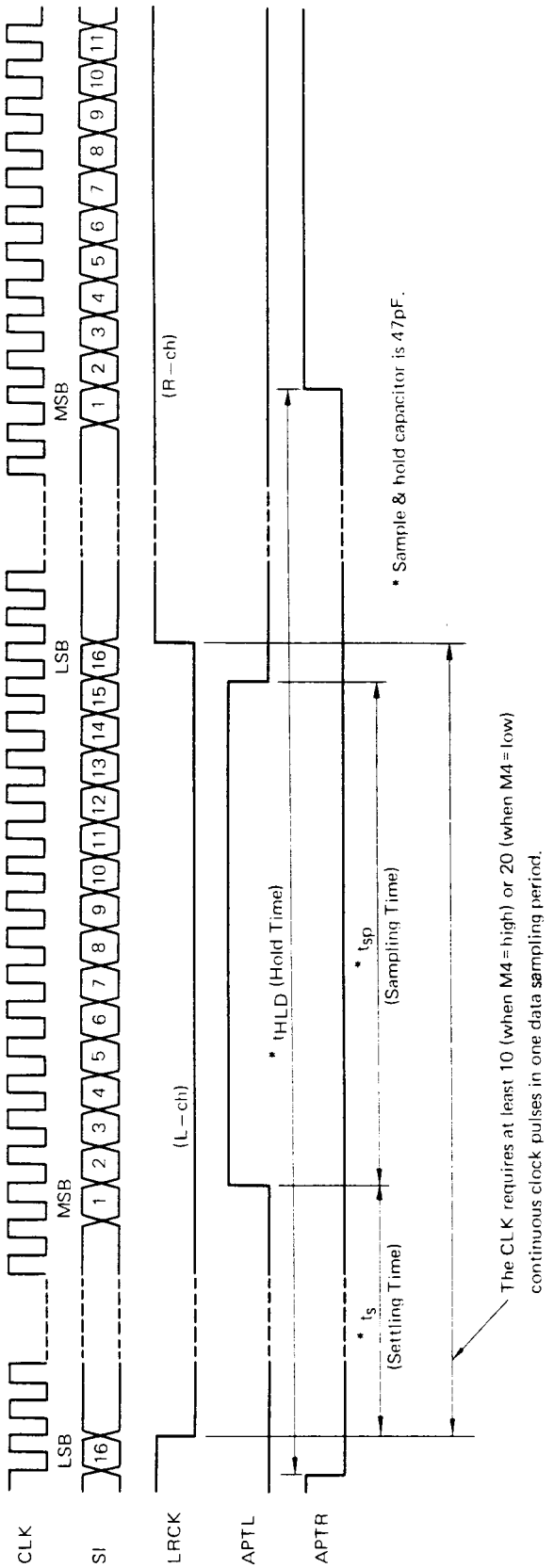
SERIAL DATA INPUT TIMING

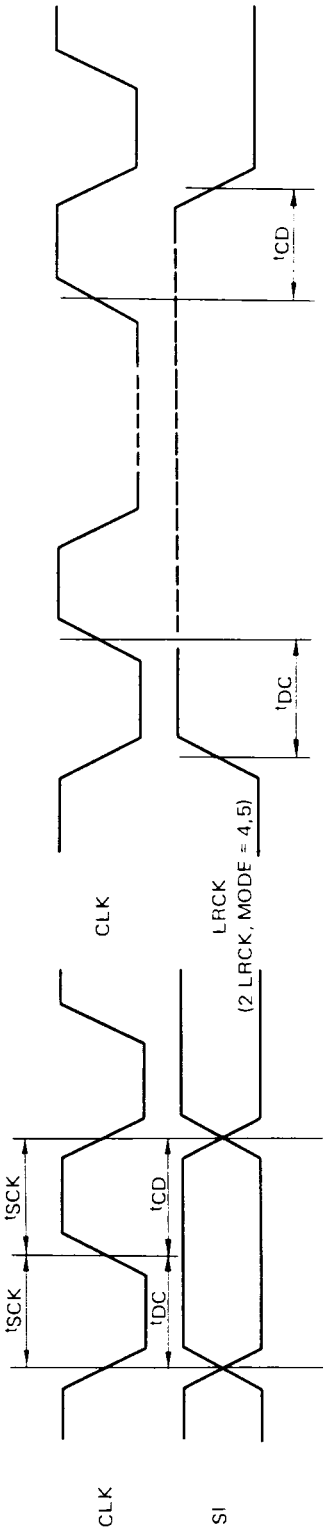
The μPD6355G conforms to multiple interface system with its mode switching terminals (M0, M1, M2).

Mode List

Mode	M_3	M_1	M_2	APTL, APTR	Phase Relationship between LRCK and Serial Data (LSB)	2's/BIN
0	0	0	0	Input from external terminals APTL and APTR	Phase of LRCK and LSB are synchronous	2's
2	0	0	1			BIN
1	0	1	0		LRCK shifts 1CLK in advance of LSB	2's
3	0	1	1			BIN
4	1	0	0	Generated in the LSI by 2LRCK (APTL terminal) and LRCK.	Phases of LRCK and LSB are synchronous	2's
5	1	1	0			BIN
6	1	0	1	Inhibit		
7	1	1	1			

INPUT TIMING CHART





TYPICAL CHARACTERISTICS (T_a=25 °C)

Note: 20 kHz Low Pass Filter is Toko (APQ-25).

Fig. 1 Total Harmonic Distortion (THD) VS Frequency

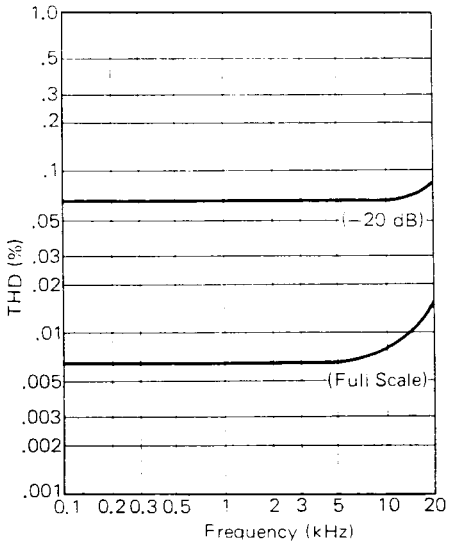


Fig. 2 Total Harmonic Distortion (THD) VS V_{DD}

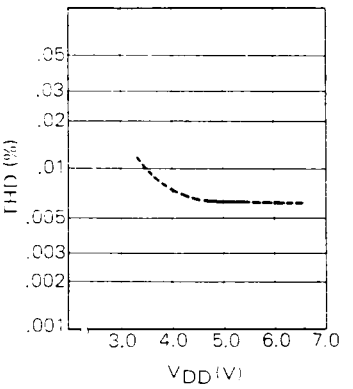


Fig. 3 Voltage Gain VS Frequency

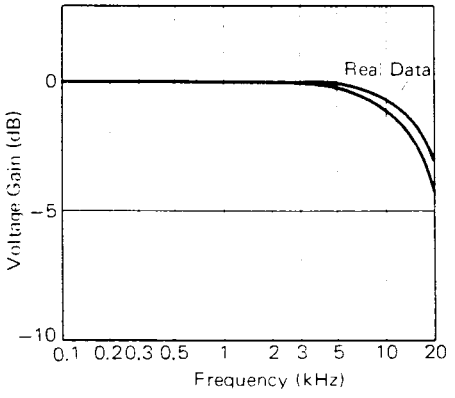


Fig. 4 Total Harmonic Distortion (THD) VS V_{OUT}

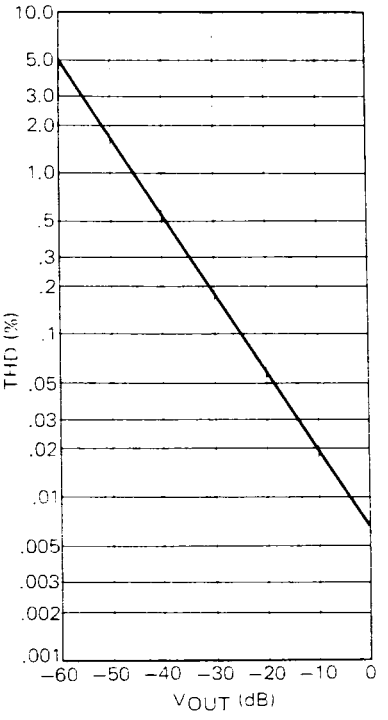
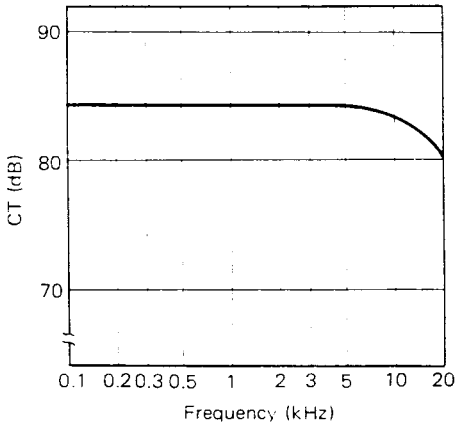
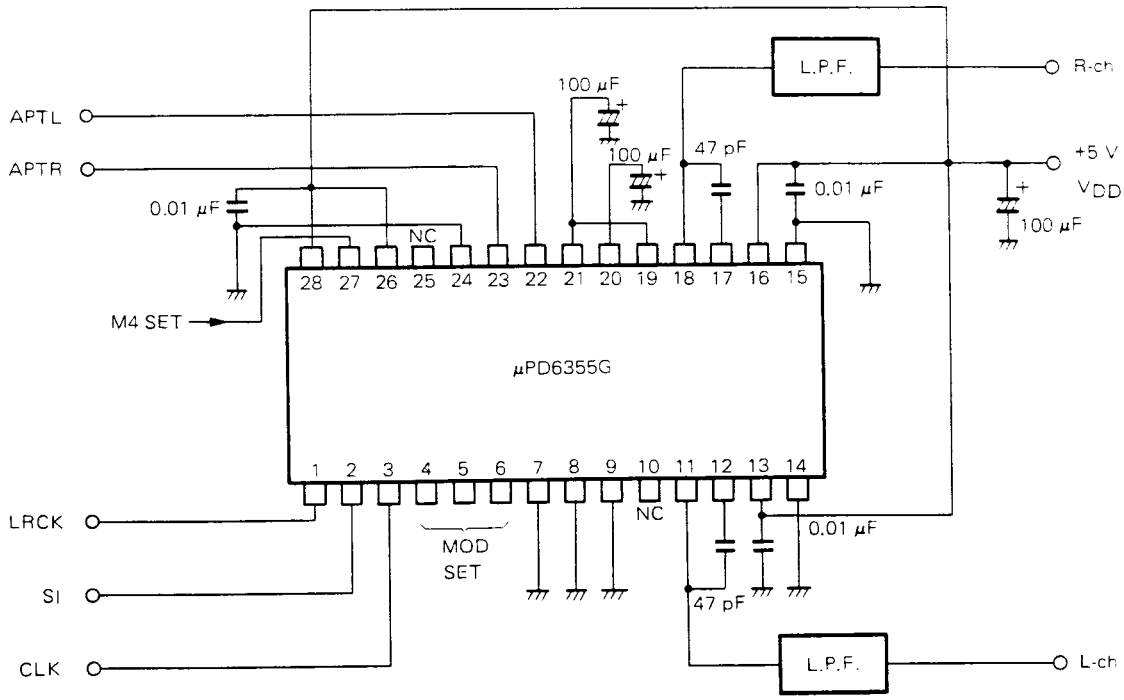


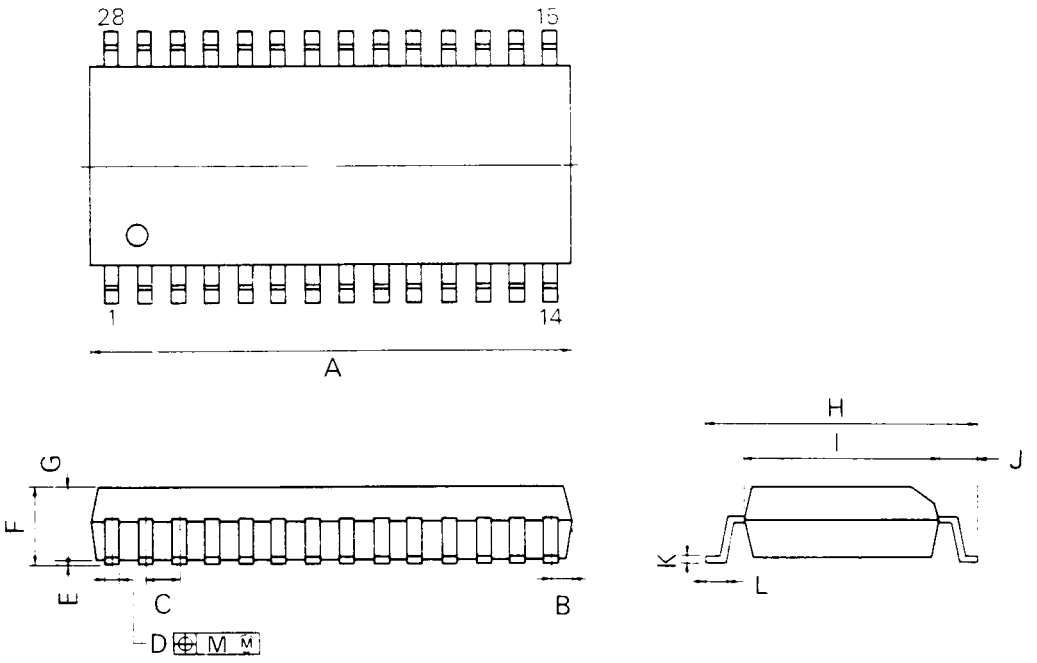
Fig. 5 Cross Talk (CT) VS Frequency



EXAMPLE OF THE APPLICATION CIRCUIT



28PIN PLASTIC MINI FLAT (375 mil)



P28GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005