Bt101

50 MHz

Monolithic CMOS

Triple 8-bit

VIDEODAC™

Distinguishing Features

- 50, 30 MHz Operation
- Triple 8-bit D/A Converters
- ± 1 LSB Differential Linearity Error
- ± 1 LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Outputs
- TTL Compatible Inputs
- +5v CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

Product Description

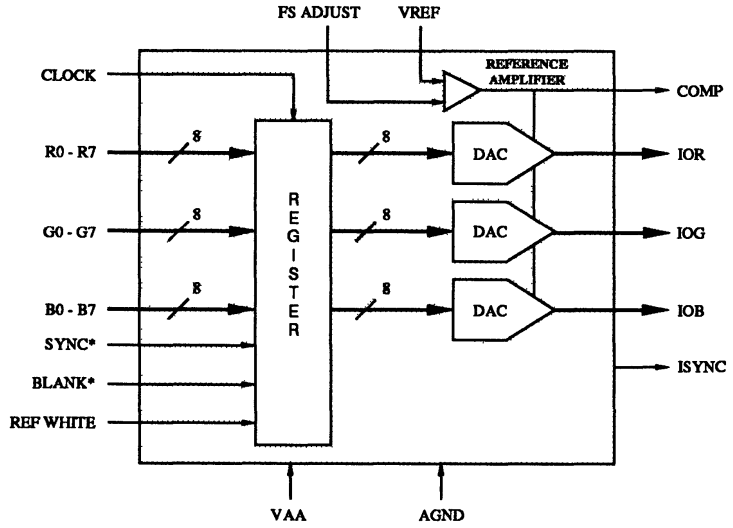
The Bt101 is a triple 8-bit VIDEODAC, designed specifically for high performance, high resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog outputs to the reference white level, regardless of the data inputs.

An external 1.2v voltage reference and a single resistor control the full scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt101 generates RS-343A compatible video signals into a doubly-terminated 75-ohm load, and RS-170 compatible video signals into a singly-terminated 75-ohm load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

Functional Block Diagram



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Circuit Description

As illustrated in the functional block diagram, the Bt101 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, 24 bits of color information (R0 - R7, G0 - G7, and B0 - B7) are latched into the device and presented to the three 8-bit D/A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, forces the inputs of each D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output levels.

The ISYNC current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If ISYNC is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG, and IOB outputs will have the same full scale output current.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 ohms for generation of RS-343A video into a 37.5-ohm load. The VREF input requires an external 1.2v (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converters on the Bt101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt101 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

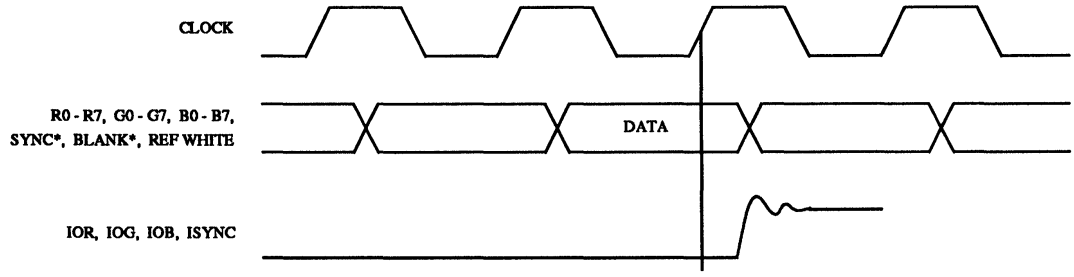
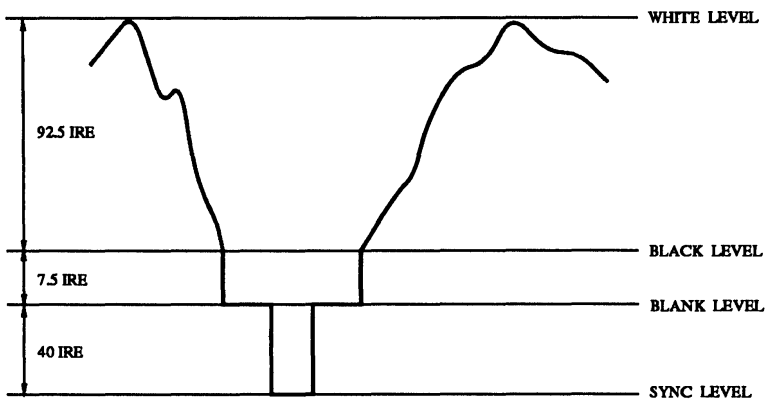


Figure 1. Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, RSET = 542 ohms, VREF = 1.2v. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	1	$xx
WHITE	26.67	19.05	0	1	1	$FF
DATA	data + 9.05	data + 1.44	0	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	0	1	data
BLACK	9.05	1.44	0	1	1	$00
BLACK - SYNC	1.44	1.44	0	0	1	$00
BLANK	7.62	0	x	1	0	$xx
SYNC	0	0	x	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA. RSET = 542 ohms, VREF = 1.2v. ISYNC connected to IOG.

Table 1. Video Output Truth Table.

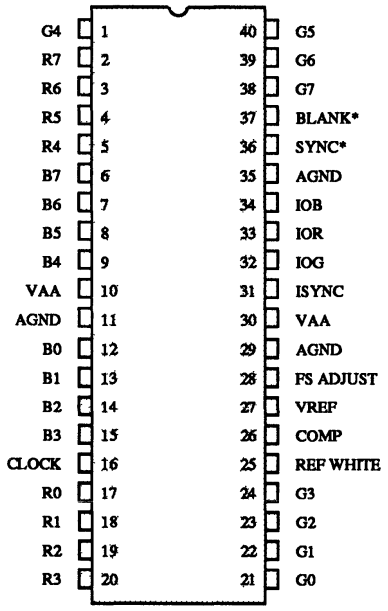
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0 - R7, G0 - G7, B0 - B7, and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the R0 - R7, G0 - G7, and B0 - B7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
R0 - R7, G0 - G7, B0 - B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0 - R7, G0 - G7, B0 - B7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. Typically, this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logical zero on the SYNC* input results in no current being output onto this pin, while a logical one results in the following current being output: ISYNC (mA) = 3,442 * VREF (v) / RSET (ohms) If sync information is not required on the green channel, this output should be connected to AGND.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG (assuming ISYNC is connected to IOG) is: RSET (ohms) = 12,046 * VREF (v) / IOG (mA) The full scale output current on IOR and IOB for a given RSET is defined as: IOR, IOB (mA) = 8,604 * VREF (v) / RSET (ohms)

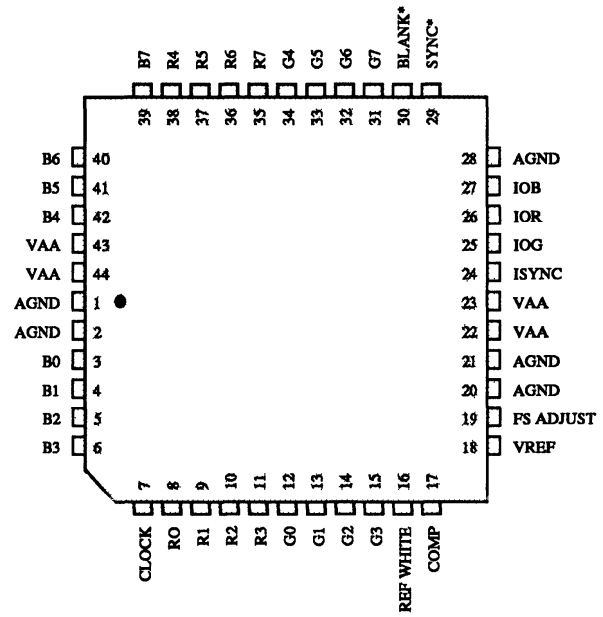
Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the nearest VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2v (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.

40-pin DIP Package



44-pin Plastic J-Lead (PLCC) Package



PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt101 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The Bt101 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt101.

The analog ground plane area should encompass all Bt101 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt101, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt101.

Power Planes

The Bt101 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within three inches of the Bt101.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt101 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 μF ceramic capacitor should be used to decouple each of the two groups of VAA pins to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt101 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt101 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt101 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

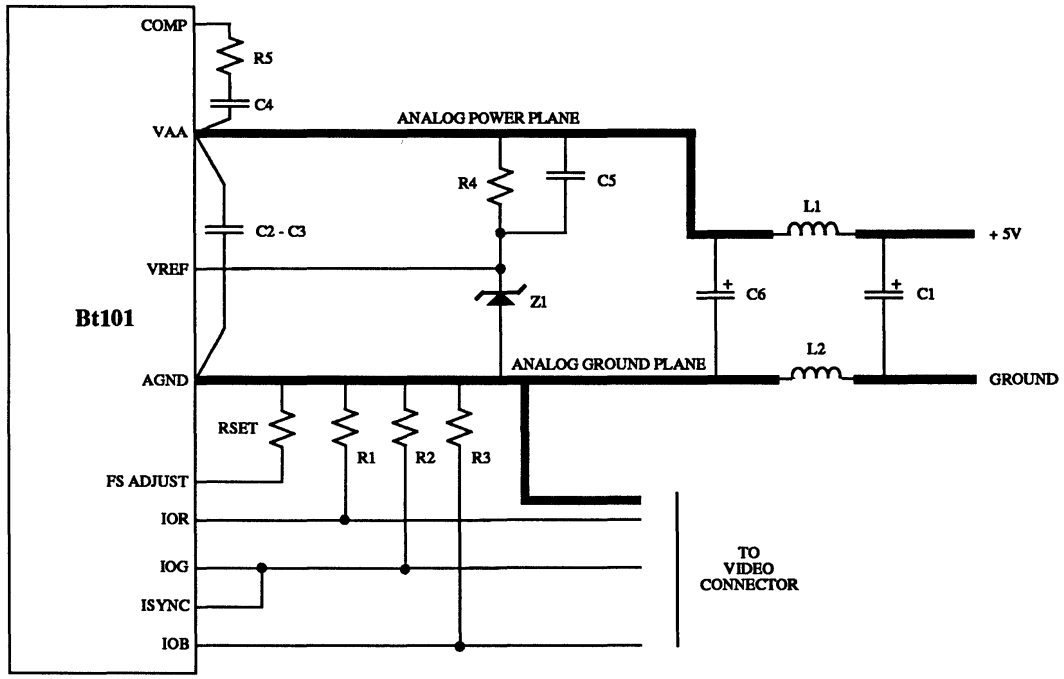
Analog Signal Interconnect

The Bt101 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt101 to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm 1% metal film resistor	Dale CMF-55C
R4	1000-ohm 1% metal film resistor	Dale CMF-55C
R5	15-ohm 1% metal film resistor	Dale CMF-55C
RSET	549-ohm 1% metal film resistor	Dale CMF-55C
Z1	1.2v voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt101.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly-terminated 75-ohm load be used with an RSET value of about 774 ohms. If the Bt101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly-terminated 75-ohm and singly-terminated 75-ohm loads.

If driving a large capacitive load (load RC > 1/ (20Fcπ)), it is recommended that an output buffer be used to drive a doubly-terminated 75-ohm load.

COMP Resistor

To optimize the settling time of the Bt101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 ohms, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Non-Video Applications

The Bt101 may be used in non-video applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be a logical zero and BLANK* should be a logical one. ISYNC should be connected to AGND. All three outputs will have the same full scale output current.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (ohms) = 7,958 * VREF (v) / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 650 * VREF (v) / RSET (ohms)

Therefore, the total full scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a "force to full scale" control.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA				
Bt101KC30, Bt101KPJ		0		+ 70	°C.
Bt101BC		- 25		+ 85	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.20	1.26	Volts
FS ADJUST Resistor	RSET		542		Ohms

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Digital Pin		AGND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ				
Ceramic Package				+ 175	°C.
Plastic Package				+ 150	°C.
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL		± 0.3	± 1	LSB
Differential Linearity Error	DL		± 0.3	± 1	LSB
Gray Scale Error			± 1	± 5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	µA
Input Low Current (Vin = 0.4v)	IIL			- 1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		10		pF
Analog Outputs					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching			2		%
Output Compliance	VOC	- 1.0		+ 1.4	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Voltage Reference Input Current	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 ohms, VREF = 1.200v, ISYNC connected to IOG. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

A.C. Characteristics

		50 MHz Devices			30 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time	TSU	6			8			ns
Data and Control Hold Time	TH	2			2			ns
Clock Cycle Time	TCYC	20			33.3			ns
Clock Pulse Width High Time	TCLKH	8			10			ns
Clock Pulse Width Low Time	TCLKL	8			10			ns
Analog Output Delay	TDLY		25			25		ns
Analog Output Rise/Fall Time	TVRF			8			9	ns
Analog Output Settling Time	TS		12			15		ns
Clock and Data Feedthrough*			- 28			- 28		dB
Glitch Impulse*			100			100		pV - sec
DAC to DAC Crosstalk			- 23			- 23		dB
Analog Output Skew			0	3		0	3	ns
Differential Gain Error	DG		1.8			1.8		% Gray Scale
Differential Phase Error	DP		1.2			1.2		Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current**	IAA		120	175		100	140	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 ohms, VREF = 1.200v, ISYNC connected to IOG. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 15 ohms. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

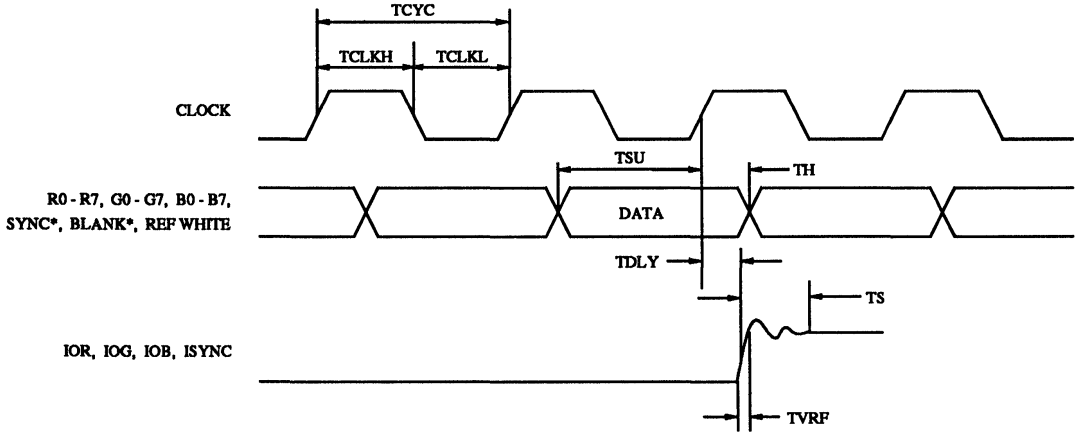
*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0v. IAA (max) at VAA = 5.25v.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt101BC	50 MHz	40-pin 0.6" CERDIP	-25° to +85° C.
Bt101KC30	30 MHz	40-pin 0.6" CERDIP	0° to +70° C.
Bt101KPJ	30 MHz	44-pin Plastic J-Lead	0° to +70° C.
Bt101EVM	Evaluation Board for the Bt101		

Timing Waveforms



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 4. Input/Output Timing.

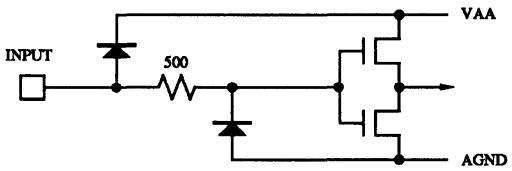


Figure 5. Equivalent Circuit of the Digital Inputs.

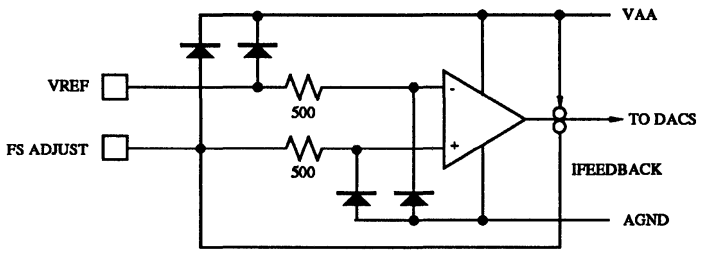


Figure 6. Equivalent Circuit of the Reference Amplifier.

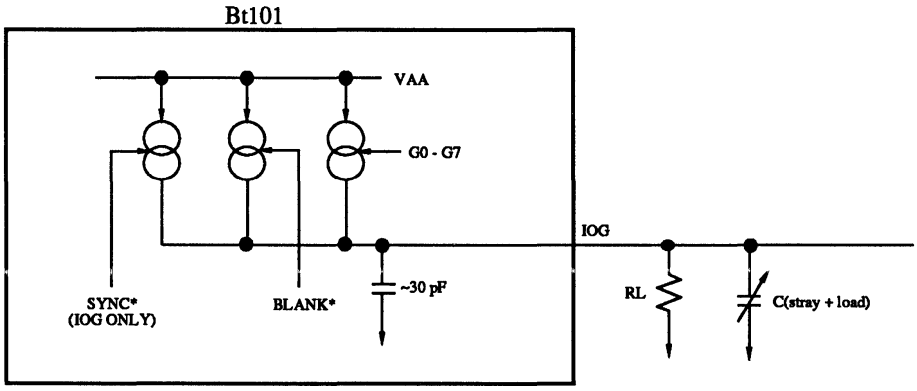


Figure 7. Equivalent Circuit of the Current Output (IOG).