

A 1-MICRON CMOS 128 MHZ VIDEO SERIALISER, PALETTE,
AND DIGITAL-TO-ANALOGUE (DAC) CHIP

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Introduction

This paper describes a fully integrated 1-micron CMOS Video Serialiser, Colour Palette and Digital-to-Analogue Converter (DAC) chip, which is being designed as a key component for a Personal Computer graphics system. One application for this chip is in the IBM Image Adapter/A which has been described by Bowater (BOWATER89). The chip drives high resolution monitors up to 1600 by 1200 pixels at 128 MHz video frequency with 8 bits per pixel. It offers a colour palette of 256 colours selectable from a possible 16 million colours. The design represents the state of the art in mixed analogue and digital CMOS design. The design tools and methodology were chosen to minimise the design time and provide right-first-time hardware.

Key Features

The key features are a high performance 256x24 palette RAM, three 8-bit DACs, a reconfigurable video serialiser, and approximately 6K (equivalent) gates of standard cell logic to manage the control and interfacing of the chip.

Data Flow

The data flow path through the chip is from parallel video word input up to 32 bits wide, serialised to a maximum of an 8-bit wide word to form the palette address at the pixel clock rate. The address accesses a 24-bit word which forms the 3x8 bit input to the DACs. Analogue Red, Green, and Blue information is presented at the outputs of the DACs as a differential current drive into external 37.5 ohm loads to meet the RS343A specification. The data flow is pipelined throughout to achieve a 128 MHz pixel rate, taking five clock cycles to pass through the system.

Other features of the chip include:

- A direct colour that by-passes the palette, and presents 16 bits directly to the DACs giving a possible 65,536 colours.
- Masking facilities on the video word for diagnostics and compatibility with existing graphics formats.
- Self-test capability at the palette output using a linear feedback shift register for signature analysis.

Simulation Tools

The circuit design of this chip used a mixture of computer-aided design tools. The analogue portions of the chip (which include the DACs, and some of the high performance logic) were designed and analysed as

macro elements at the device level. Circuit simulation was carried out using circuit analysis program on an IBM 3084 mainframe system. The logic was designed as several functional macros from a high level logic description language and synthesised to a standard cell book set which was already available in IBM 1-micron CMOS technology. The logic was simulated using an IBM rules-driven logic simulator running on the same IBM 3084 system. The technology rules for the standard cell book set were already available as a part of an integrated IBM VLSI design system. However, for the design of this particular VLSI chip, the rules were used to drive a specialised custom chip design system.

Physical Design Tools

The chip physical design was carried out hierarchically using a mix of autoplacement/autowire tools for the standard cell macros; and manual placement and wire for the analogue macros and global interconnections. Electrical performance and physical to logical integrity of the analogue macros was guaranteed using a device recognition program which automatically regenerates the logical circuit topology from a physical layout and presents an ASTAP model to the user. Simulation of the model and comparison with the pre-physical design model allows a comprehensive check of the effects of stray capacitance and of overall connectivity. Global logical simulation of the chip was carried out from a compilation of the individual macros using a top level net list of global interconnections. The same net list was used to check the physical interconnection of the individual macros using a comprehensive system of attributing net names to physical layout data.

Package

The large rate of change of current in the power supply due to switching transients in the RAM and logic are a cause for concern in any inductive package system. The package chosen for this design is a ceramic Pin Grid Array (PGA) with ceramic chip capacitors mounted on the same substrate to decouple both the RAM and logic power supplies adjacent to the chip.

Summary

Prototypes of this design are currently working in engineering test of the system as of the date of this abstract. No problems have been found so far with any aspect of the design.

References

- [1] BOWATER89 - The IBM Image Adapter/A