# TECHNICAL NOTE

# BANK INTERLEAVING WITH EXTENDED DATA-OUT VRAMs

## INTRODUCTION

The extended data-out (EDO) functionality introduced on 2 Meg VRAMs provides faster PAGE-MODE cycle times by allowing data to remain or appear on the outputs beyond the deactivation of the related $\overline{CAS}$ signal (please refer to Technical Note TN-04-21, Reduce DRAM Cycle Times with Extended Data-Out). The tradeoff for this improved performance is that $\overline{CAS}$ alone can no longer be used to disable the data outputs. In situations where this behavior is required, such as bank-interleaved systems, the $\overline{OE}$ signal must be used to disable the data outputs.

## BANK INTERLEAVED SYSTEMS

In bank-interleaved systems, the data outputs of non-selected banks must be disabled while data is being read from the selected bank. When using non-EDO parts, this can be achieved by deactivating the $\overline{CAS}$ signals of the non-selected banks. However EDO parts require that $\overline{OE}$ signals be used. For example, an interleaved design using two banks of MT42C8256 2 Meg VRAMs requires an $\overline{OE}$ signal for each bank. This configuration and related general timing are shown in Figure 1.

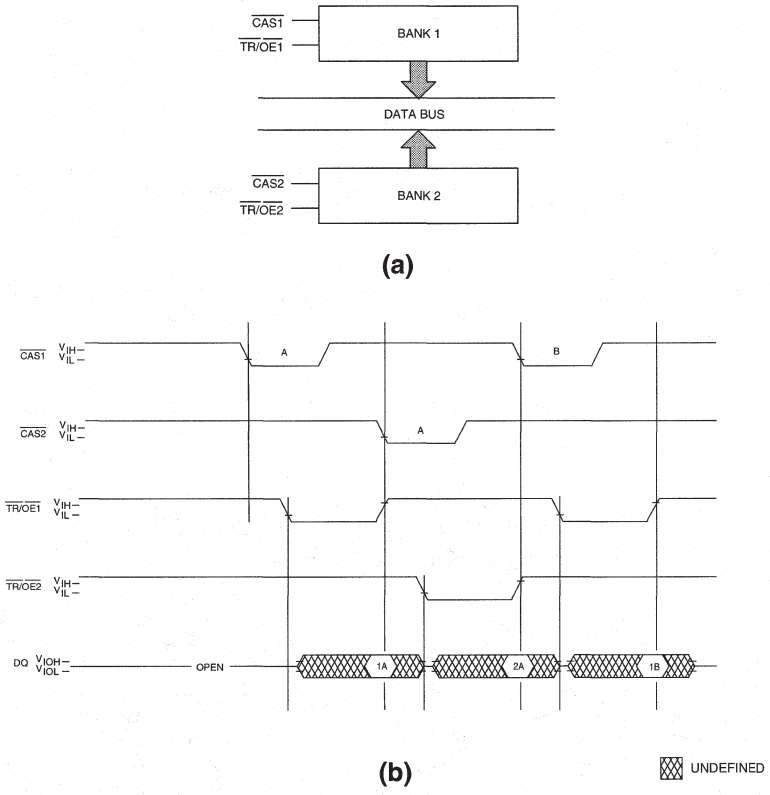
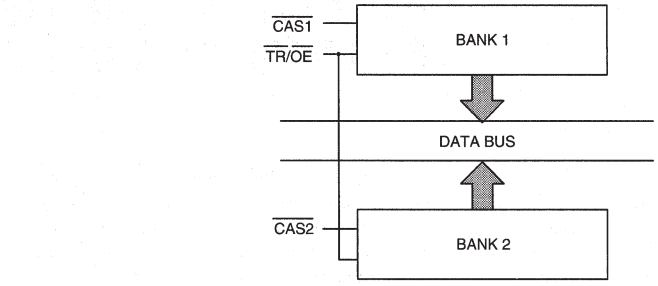
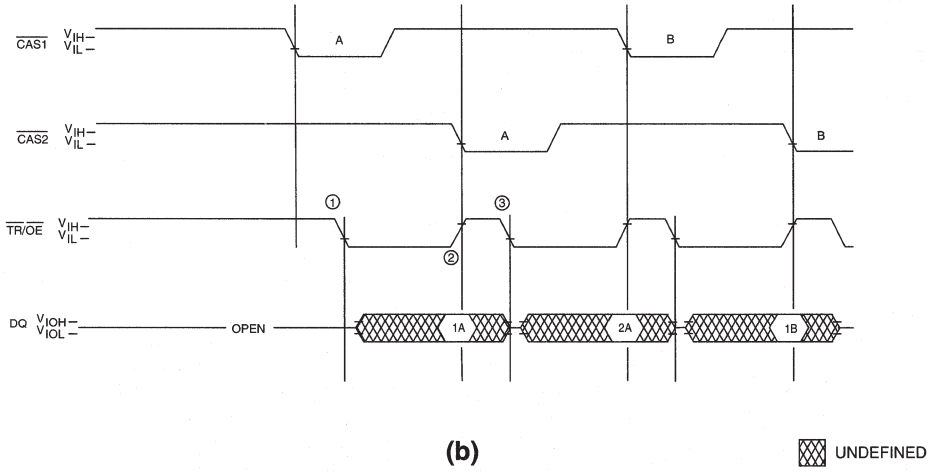



**Figure 1**
**(a) TWO BANKS, WITH SEPARATE $\overline{OE}$s (b) RELATED GENERAL READ TIMING**

NEW APPLICATION/TECHNICAL NOTE




(a)




(b)

**Figure 2**
**(a) TWO BANKS, WITH A COMMON $\overline{OE}$**
**(b) RELATED GENERAL READ TIMING**

For some designs, providing an $\overline{OE}$ signal for each bank may be considered undesired overhead. For this reason, the EDO operation of the Micron MT42C256K16A1 4 Meg VRAM was modified to allow bank interleaving with a single $\overline{OE}$ line common to all banks. System timing for common $\overline{OE}$ operation is shown in Figure 2. Note that edge ③ of $\overline{OE}$ causes the devices in bank 2 to drive the bus, but the outputs of the devices in bank 1 remain disabled. This reflects the modified EDO functionality provided by the MT42C256K16A1; this operation is shown in more detail in Figure 3. Initial EDO devices cannot be used as shown in Figure 2 because both banks would drive data as a result of $\overline{OE}$ edge ③. The data from bank 1 that was disabled at edge ② would simply be re-enabled at edge ③.

The "latched output-disable" functionality of modified EDO parts, such as the MT42C256K16A1, takes into account that $\overline{CAS1}$ is HIGH when $\overline{OE}$ goes HIGH at edge ②. When this occurs, the data outputs of bank 1 are disabled, and will remain disabled until $\overline{CAS1}$ goes LOW again.

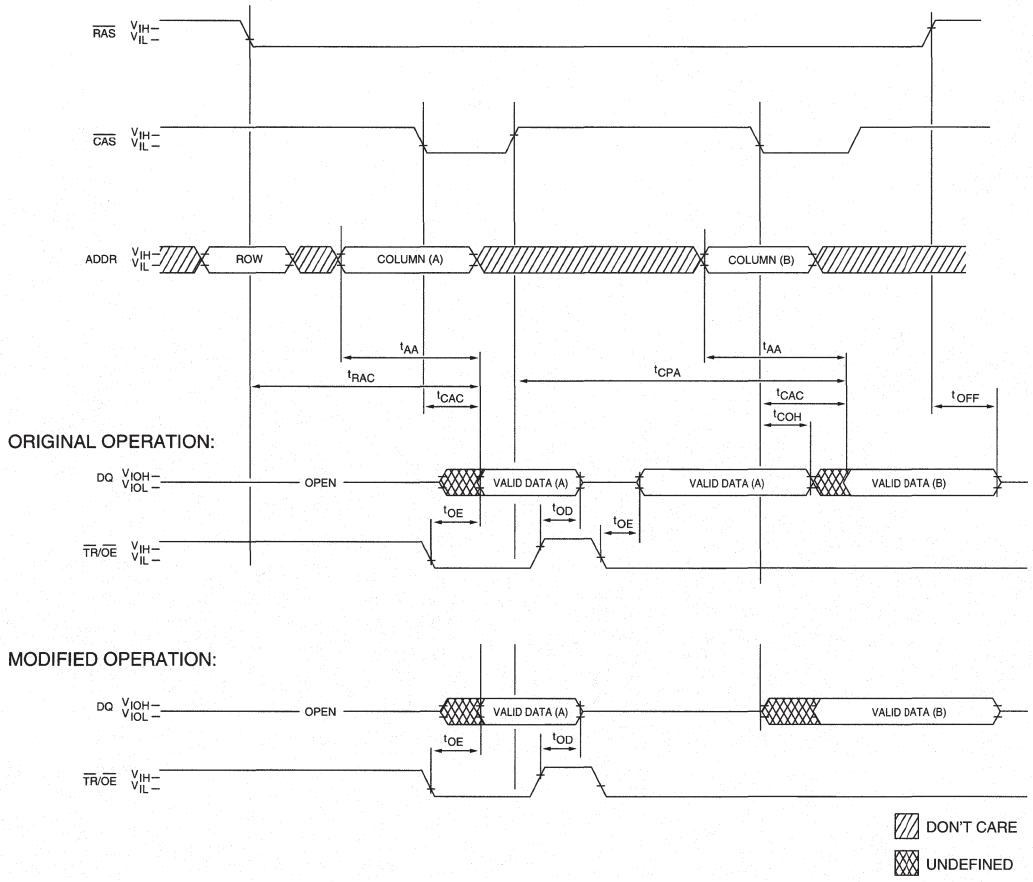



**Figure 3**
**FAST-PAGE-MODE EDO READ CYCLE SHOWING ORIGINAL AND MODIFIED OPERATION**

## SUMMARY

When interleaving banks of EDO VRAMs, it is necessary to use $\overline{OE}$ signals to select the appropriate bank to drive the bus, and to deselect the other banks. The original parts that include EDO functionality require a separate $\overline{OE}$ signal for each bank. The MT42C256K16A1 4 Meg VRAM provides modified EDO operation which allows for the use of a common $\overline{OE}$ signal for all banks. The MT42C256K16A1 functions identically to previous EDO devices in all other cases.