TECHNICAL NOTE

FOUR-COLUMN VS EIGHT-COLUMN BLOCK WRITE

INTRODUCTION

The BLOCK WRITE feature on VRAMs allows for a single value to be written to several locations in the DRAM array in one WRITE cycle. Prior to the introduction of 4 Meg VRAMs, the BLOCK WRITE feature had been defined to apply to four column locations. This definition has been expanded to eight column locations for 4 Meg VRAMs; this expansion doubles the achievable bandwidth of BLOCK WRITEs.

This note discusses four- and eight-column BLOCK WRITEs in the context of graphics systems, where the data stored in memory represents pixels to be displayed on a screen.

BLOCK WRITE OPERATION

A BLOCK WRITE cycle affects a block of memory cells in the DRAM array. This is shown in Figures 1 and 2 for a four-bit-wide VRAM (four memory planes or DQ pins) with four-column BLOCK WRITE capability. The data to be written to the cells is stored, in advance, in an internal data register known as the COLOR REGISTER. The row-address n is provided on the address inputs at $\overline{RAS}$ time, and the column-address m, at $\overline{CAS}$ time. The two least significant column-address bits are ignored, and the four columns corresponding to the four possible combinations of those bits are all selected.

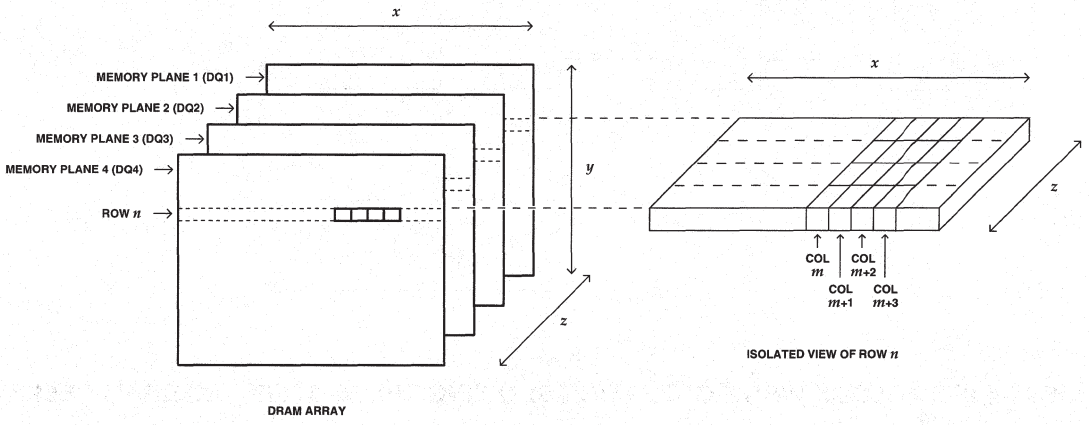

Figure 1
MEMORY CELLS AFFECTED BY BLOCK WRITE IN 4-BIT-WIDE, FOUR-COLUMN BLOCK WRITE VRAMs

NEW ■ APPLICATION/TECHNICAL NOTE

The two-dimensional (x-z) representation of the 16 affected cells shown in Figure 2 illustrates the masking capabilities within a BLOCK WRITE cycle. The write-per-bit (WPB) mask is used to prevent the BLOCK WRITE cycle from affecting the cells associated with a particular DQ line (or lines). The WPB mask is either stored in advance in an internal mask register, or it is presented at $\overline{RAS}$ time on the DQ lines. The column mask, which is presented on the DQ lines at $\overline{CAS}$ time, is used to mask the cells in a particular column (or columns).

FOUR-COLUMN BLOCK WRITES

FOUR-BIT-WIDE VRAMs

As mentioned, when a four column BLOCK WRITE is performed in VRAMs with four-bit-wide data paths (such as the MT42C4256 1 Meg VRAM), the four-bit column mask is presented on the DQ pins at $\overline{CAS}$ time. If a 32-bit-wide array is constructed with four-bit-wide VRAMs, the total number of memory cells affected by a BLOCK WRITE cycle

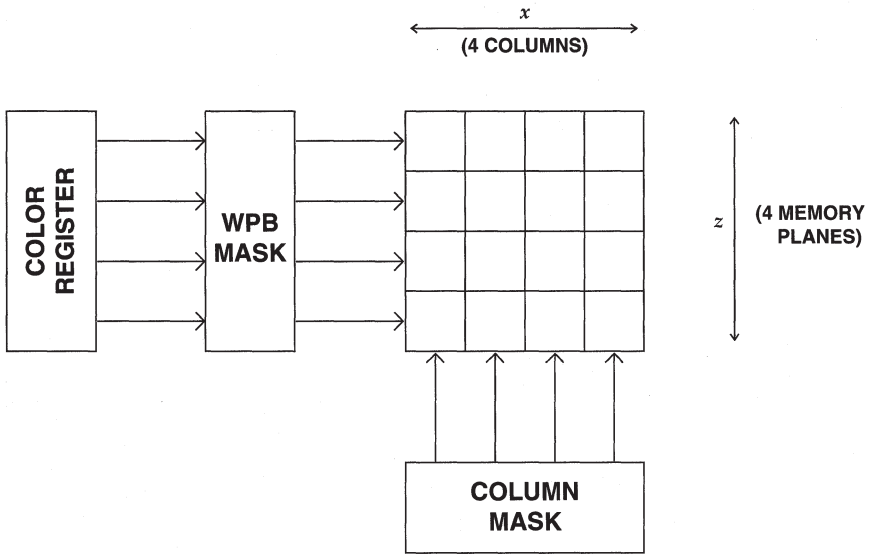

Figure 2
SIMPLIFIED BLOCK WRITE OPERATION SHOWING THE 16 AFFECTED DRAM CELLS

is 128 (32 memory planes multiplied by 4 columns). This is shown in Figure 3.

Assuming four-bit pixels in a packed-pixel implementation, each column in Figure 3 contains 8 pixels. These 4-bit pixels are shown numbered (1-32) in Figure 4(a). In this 32-bit-wide implementation, a column mask is presented on each nibble of the bus (see Figure 4[b]). This allows for single pixel granularity during area fills or color expansion operations when using four-bit pixels.

Consider an area fill operation, where a rectangle on the screen is to be filled with a single color. Assume that the left boundary of the rectangle falls on pixel 2 (i.e. pixel 1 should remain unaltered, pixels 2 through 32 should be "colored"). This would be accomplished by performing a BLOCK

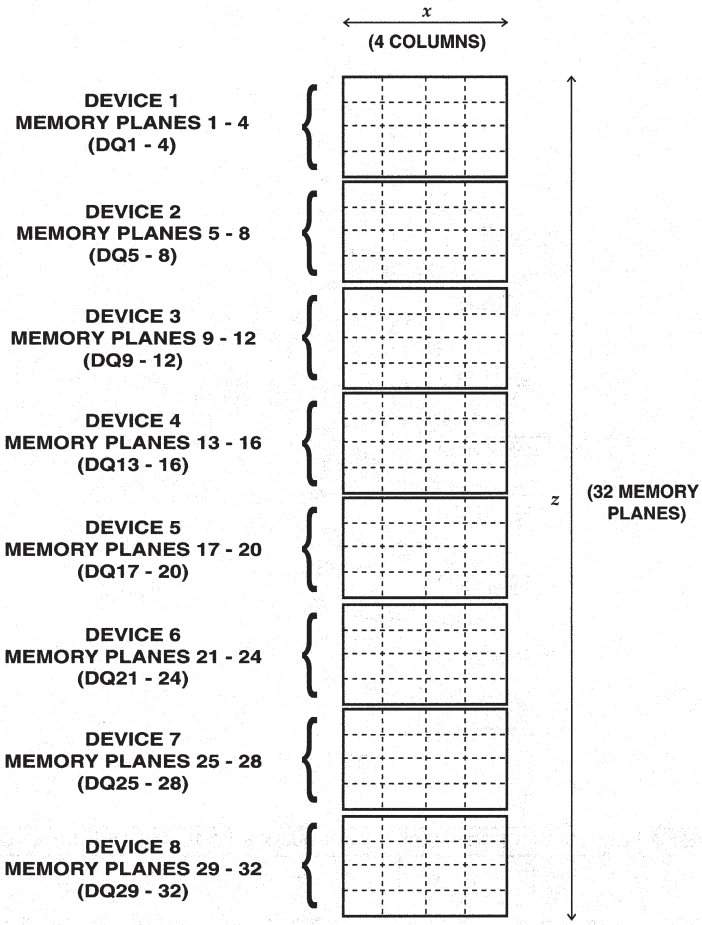

Figure 3
DRAM CELLS AFFECTED BY A BLOCK WRITE CYCLE IN A 32-BIT-WIDE ARRAY CONSISTING OF EIGHT MT42C4256 VRAMS

WRITE with column mask 1 = 0111 and column masks 2 through 8 all = 1111 (i.e at $\overline{CAS}$ time, DQ1 = 0, DQ2-32 = 1).

Assume that the above BLOCK WRITE cycle was repeated for the number of rows in the rectangle, and then BLOCK WRITEs were performed on additional columns as needed until the rectangle was completely "colored." Further, assume that this rectangle was to act as a background for text or other objects that consist of a foreground color. The text or other objects are represented by a monochrome bit map, and require color expansion. Returning to the 32 pixels represented in Figure 4, the corresponding section of the monochrome bit map contains a 1 for each of the 32 pixels that is to appear in the foreground color and a 0 for each of the pixels that is to remain as the background color. To "color" the foreground pixels, a BLOCK WRITE is performed with the foreground color value present in the color register, and with the monochrome bit-map presented as the column mask.

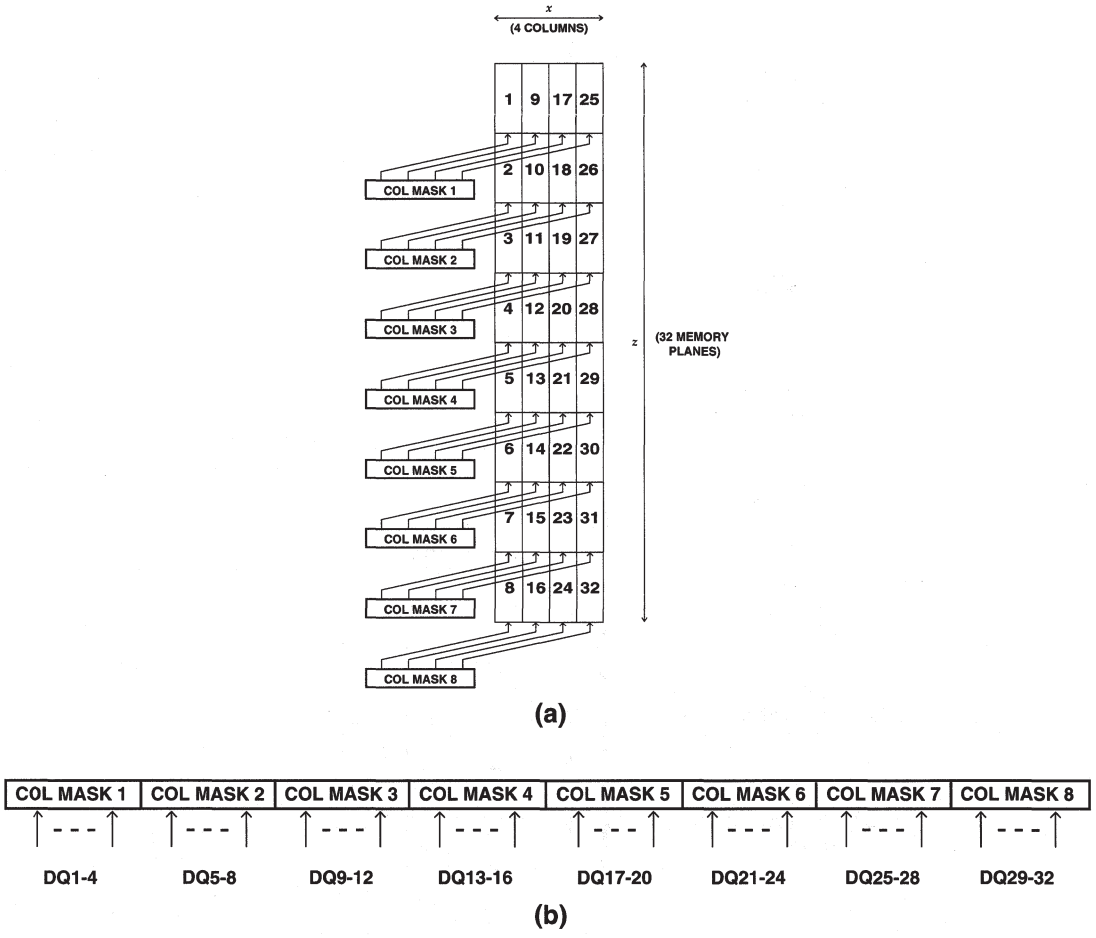

FIGURE 4
(a) 4-BIT PIXELS (1-32) STORED IN THE DRAM CELLS SHOWN IN FIGURE 3 AND THE RELATED COLUMN MASKS (b) ASSIGNMENT OF DQ PINS TO COLUMN MASKS

EIGHT-BIT-WIDE VRAMs

When four-column BLOCK WRITEs are performed in 8-bit-wide VRAMs, such as the MT42C8128 1 Meg or the MT42C8254/5/6/7 2 Meg VRAMs, the 4-bit column mask is presented on the lower nibble of the DQ pins (DQ1-DQ4). This 4-bit mask is then internally provided to both nibbles within the VRAM. Again, looking at a 32-bit array, a column mask is presented on every other nibble on the bus (see Figure 5). The result is that single-pixel resolution can be achieved on 8-, 16-, 24- or 32-bit pixels, but not for four-bit pixels.

In order to achieve the same single-pixel granularity as described previously for four-bit-wide VRAMs, it is necessary to make two passes with the BLOCK WRITE cycles, while using the WPB mask to mask alternating nibbles.

EIGHT-COLUMN BLOCK WRITES

Eight-column BLOCK WRITE is introduced on 4 Meg VRAMs such as the MT42C256K16A1, which is configured as 256K x 16. In conjunction with the expansion to eight columns, these devices also allow for two 8-bit column

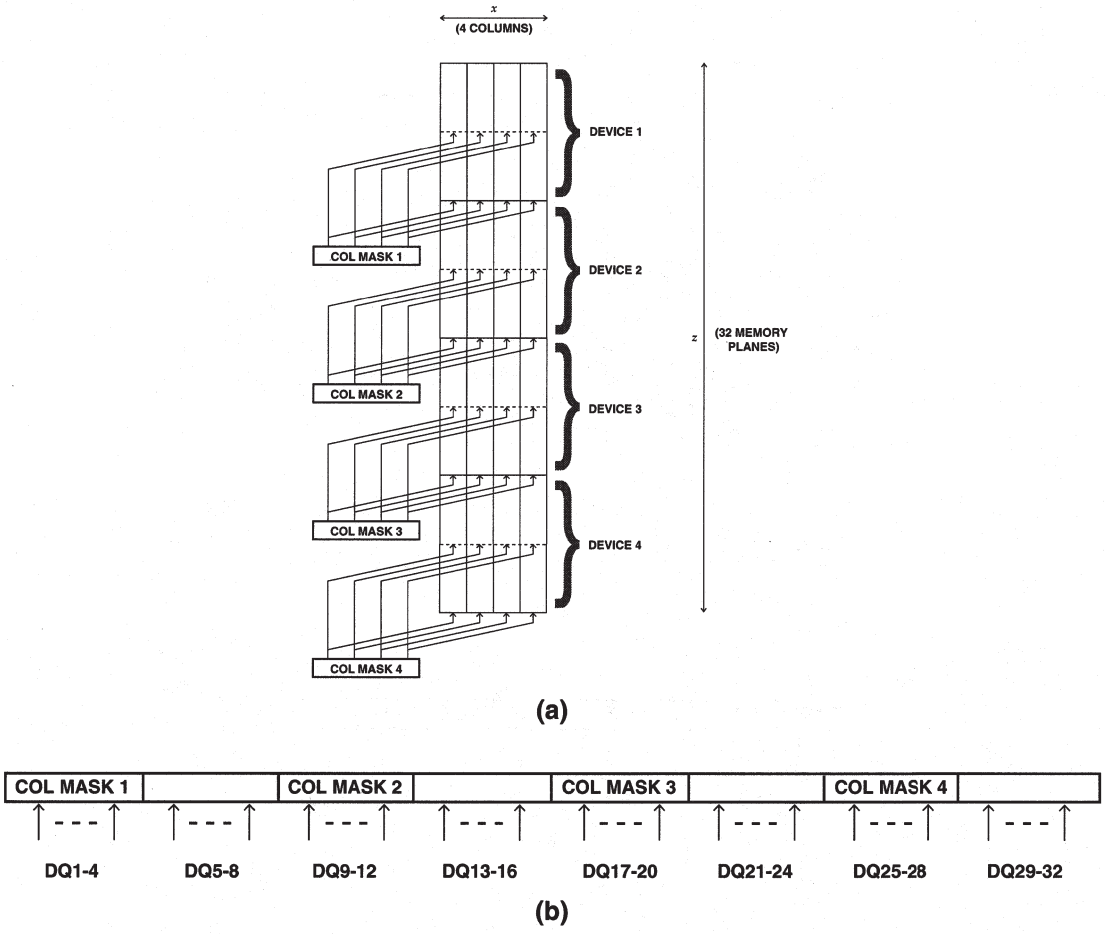

Figure 5
(a) A 32-BIT-WIDE ARRAY BASED ON 8-BIT-WIDE, 4-COLUMN BLOCK WRITE VRAMs
(b) ASSIGNMENT OF DQ PINS TO COLUMN MASKS

masks to be presented on the DQs. The 8-bit column mask for the lower byte is presented on DQ1-DQ8 and the column mask for the upper byte, on DQ9-DQ16. Again, considering a 32-bit array (see Figure 6), a column mask is provided on each byte of the bus. This preserves the single-pixel granularity that was available on 8-bit-wide devices when using 8- , 16- , 24- and 32-bit pixels. In addition, the 2x improvement in bandwidth due to eight columns being included in the BLOCK WRITE cycle negates the penalty of using two passes with four-bit pixels. Therefore, eight-column BLOCK WRITE with two eight-bit column masks is the optimal implementation overall.

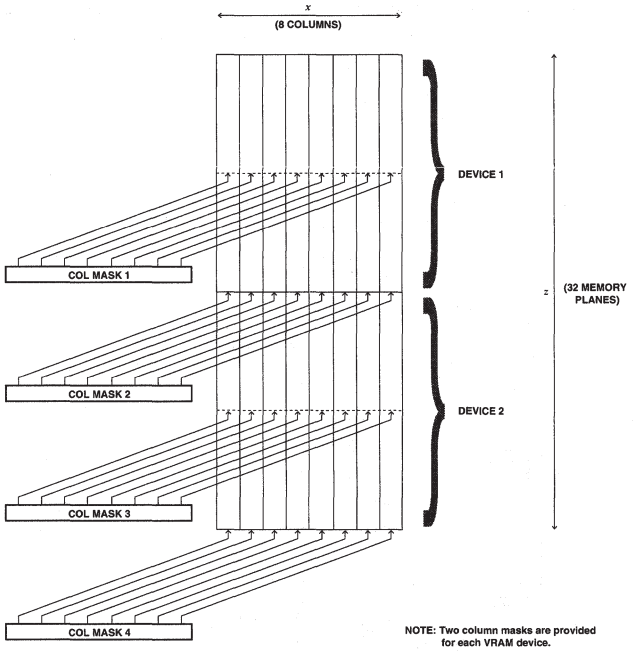

Figure 6
(a) A 32-BIT-WIDE ARRAY BASED ON 16-BIT-WIDE, 8-COLUMN BLOCK WRITE VRAMS
(b) ASSIGNMENT OF DQ PINS TO COLUMN MASKS

Table 1
COMPARISON OF BLOCK WRITE IMPLEMENTATIONS

NUMBER OF COLUMNS	VRAM WIDTH	MINIMUM PIXEL SIZE FOR SINGLE PIXEL GRANULARITY	NORMALIZED PERFORMANCE	
			4-BIT PIXELS	8-, 16-, 24-, AND 32-BIT PIXELS
4	4 BITS	4 BITS	1.0	1.0
	8 BITS	8 BITS	0.5	1.0
8	16 BITS	8 BITS	1.0	2.0

SUMMARY

BLOCK WRITE cycles allow for several locations of the DRAM array within VRAMs to be modified simultaneously. In graphics systems, this operation can improve system performance when executing area fills and/or color expansion functions.

There are several implementations of BLOCK WRITE, depending on the density and width of the VRAM. Relative to the others, the eight-column BLOCK WRITE, two-mask implementation provided by the MT42C256K16A1, 4 Meg VRAM delivers equivalent performance for four-bit pixels and twice the performance for 8-, 16-, 24- and 32-bit pixels, making it the optimal overall BLOCK WRITE implementation.