RF6609ANC-015
CMOS Low-pass Filter

Description

The Reticon RF6609ANC-015 is a CMOS, seven-pole, six-zero, elliptic low-pass switched-capacitor filter. It is pin- and function-compatible with the Reticon RF5609A with the exception of supply voltages (RF6609ANC-015 requires ±5V ±10%; the RF5609A accepts supply voltages from ±5V to ±10V) and features significantly reduced power consumption, noise, clock feedthrough, and output DC offset.

Key Features

- Low power
- Easy to use – no external components required
- Compact 8-pin DIP
- Excellent dynamic range
- Wide cutoff frequency range
- Low output noise
- Low distortion
- Excellent out-of-band rejection
- Low passband ripple
- Latchup-free

Typical Applications

- Antialiasing filters
- Portable instrumentation
- Biomedical/geophysical instruments
- Speech processing
- Audio analysis
- Telecommunications
- Data communications
- Reconstruction filters
- Tracking filters

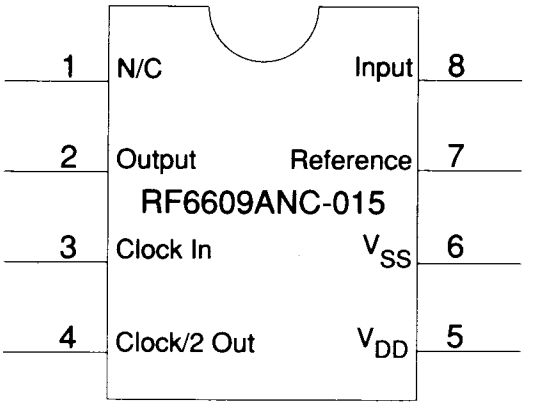


Figure 1. Pinout Configuration

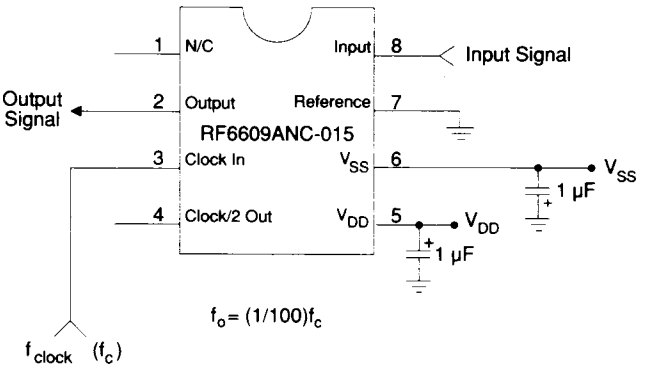


Figure 2. Basic Configuration

Device Operation

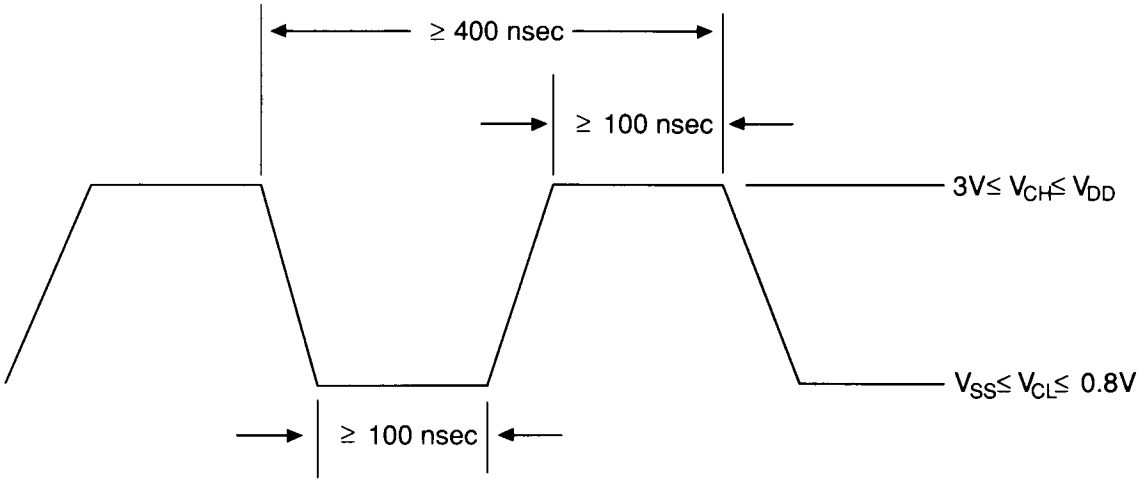
The operation is straightforward. Only power supplies and an external clock are needed. The filter's pinout configuration is shown in Figure 1 and a basic circuit is shown in Figure 2. The signal to be filtered is input at pin 8; the filtered result is output at pin 2. The magnitude and group delay characteristics of the filter are shown in Figures 4 and 5.

The power supplies (V_{DD}, V_{SS}) should be bypassed with capacitors to Reference (pin 7), which is usually grounded for split-supply operation. The voltage at the Reference pin can be adjusted to minimize the output DC offset of the filter (see Figure 7 and the paragraph addressing DC offset).

The clock is normally run at TTL levels (0V to 5V), but can extend from V_{SS} to V_{DD}. The main requirement is that the clock high and low levels be within the limits shown in Figure 3. The high and low clock states should each be at least 100 nsec long; there are no explicit duty cycle requirements. However, the maximum clocking frequency limit of 2.5 MHz requires that one clock period be at least 400 nsec long. The chip's internal state changes on the rising edge of the clock.

The cutoff frequency, f_o (also called the "corner frequency"), is 1/100 of the clock frequency, f_c. The sampling frequency for the input, f_s, is generated on-chip and is 1/2 the clock frequency ($f_s = f_c/2$). This sampling frequency is available as a square wave (levels V_{SS} to V_{DD}) at pin 4.

Filter caracteristics and operating range limits are given in Table II. Guaranteed performance standards are provided in Table III. RF6609ANC-015 temperature characteristics are shown in Figures 12 through 23.



$V_{C\,H}$ = Clock High Level, Referenced to Pin 7
$V_{C\,L}$ = Clock Low Level, Referenced to Pin 7

Figure 3. Clocking Requirements

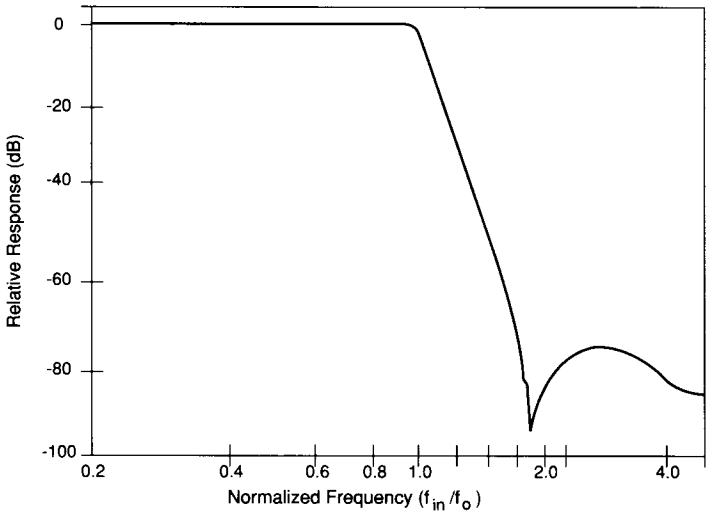


Figure 4. Magnitude Response

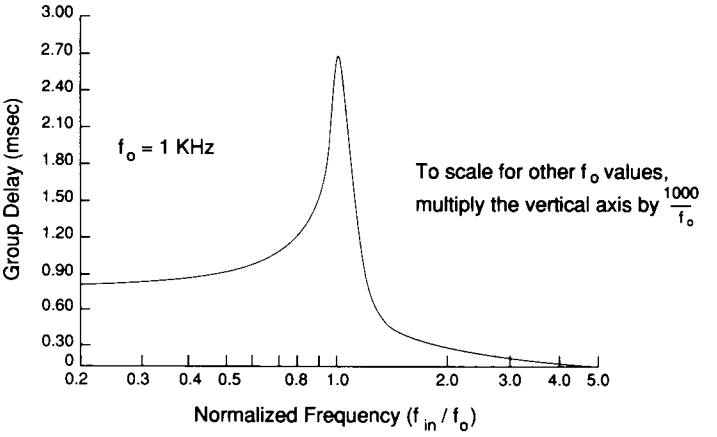


Figure 5. Group Delay

Sampling and Second-Order Effects

The RF6609ANC-015 is a switched-capacitor filter. Such a filter operates by sampling the input signal periodically (such as every millisecond) instead of continuously. This requires the user to accommodate for sampling errors at the input (aliasing) and sampling residue at the output.

Aliasing will occur if the input signal contains frequencies above 1/2 the sampling frequency (1/4 the clock frequency). Many aliased frequencies will "fold back" into the stopband and may not be of concern to the designer. Frequencies near integer multiples of the sampling frequency will alias into the passband and should be filtered out. A two-pole, antialiasing filter with cutoff frequency at 1/20 the clock frequency should give ample protection.

The output is in sampled-and-held form. If closely examined, it appears that a stairstep is superimposed on the output waveform (Figure 6). This stairstep is called "sampling residue". It occurs at the sampling frequency, so all of its signal energy is near integer multiples of f_s.

If sampling residue is a problem, it can be removed with a simple RC filter at the output, as shown in Figure 7 and discussed in the next section. Setting the RC cutoff at $f_c/20$ will have little effect on the desired passband. The RC values should be chosen so as not to overload the drive capability of the RF6609ANC-015 output stage; more information on loading is given below.

Loading, DC Offset

The current load on the output is limited to 0.2 mA. Overloading the filter's output stage can attenuate and distort the output signal. Any RC network connected to the output pin (for filtering, etc.) should have large resistances and small capacitances to reduce the amount of current the device must source or sink. If more drive is needed, a buffer can be used (Figure 7).

There is up to ±200 mV DC offset at the output. This offset can be nulled out by adjusting the voltage at pin 7 (Reference). Such an adjustment will shift the clock threshold level (V_{th}), possibly requiring a change in the clock input voltage levels. The Reference pin voltage must always be stable; noise or power supply ripple will affect the accuracy of the filter. A capacitor of at least 1 µF will usually give sufficient filtering.

Example Correction Circuit

Figure 7 shows a circuit to correct for aliasing, output DC offset, sampling residue, and output drive limitations.

The input 2-pole filter is used to prevent aliasing; its cutoff frequency is $1/2\pi R_1C_1$. A good choice for its cutoff frequency is $5f_o$ (that is, $f_c/20$). For example, if f_o = 3 KHz, then $R_1C_1 = 1/2\pi(5f_o) = 1.06 \times 10^{-5}$. If C_1 = .001µF, then R_1 = 10KΩ.

The resistor divider, composed of two 10KΩ resistors and a 10KΩ potentiometer, is used to remove output DC offset by adjusting the Reference pin voltage.

The simple RC circuit on the output pin filters out sampling residue. A suggested cutoff is $5f_o$, the same as the antialiasing filter. If the same R and C values are used, though, these would load down the output stage. Letting C_2 = .0001 µF, then $R_2 \approx$ 100KΩ, reducing the load substantially. A filter should be used whenever the next stages in the circuit could malfunction from the sampling residue or clock feedthrough (internal switching transients present on the output).

Finally, the op amp voltage follower presents virtually no load but increases drive capability. This should be used whenever total loading requires an output current greater than 0.2 mA.

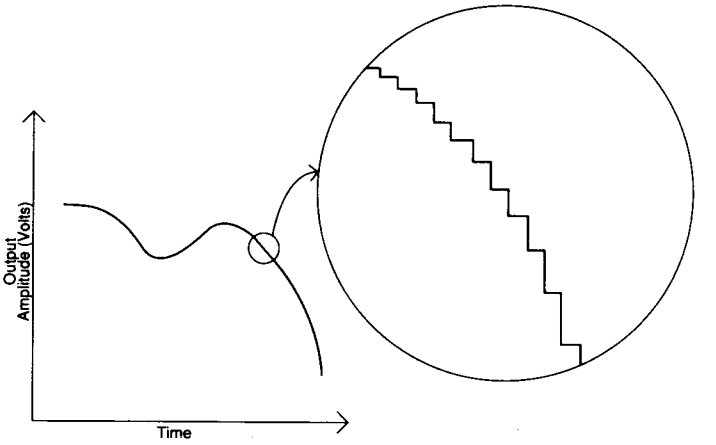


Figure 6. Sampling Residue

Other Effects

Attempts to AC couple to the input or output should be checked for distortion. External capacitors connected to the chip may interact with internal capacitances and change the filter response. The source impedance seen by the input pin should be as small as possible; the load impedance seen by the output pin as large as possible.

Total harmonic distortion is specified at a maximum of 0.2% under the listed conditions, but can be improved by reducing the amplitude of the input signal. Lower input amplitude minimizes the effect of nonlinearities in the circuit, with a trade off of reduced dynamic range.

Single-Supply Operation

It is easy to use this device with a single supply by shifting the DC levels of all inputs up by $(V_{DD}-V_{SS})/2$. The outputs will be likewise shifted. As shown in Figure 8, the only significant change in the circuit is that the bypass capacitors to the power supply pins must go from ground (V_{SS}) to the Reference pin and from ground to the positive supply, V_{DD}. The capacitor from V_{SS} to V_{DD} should be several µF to ensure proper filtering and to protect the chip from being destroyed by transient conditions at turn-on.

The input signal is referenced to V_{REF} (the voltage at the reference pin, $V_{DD}/2$) with AC coupling as shown in Figure 8. The output will be referenced to V_{REF} plus any DC offset in the device. AC coupling can be used to change the output reference level, subject to restrictions already discussed in the section on loading and DC offset.

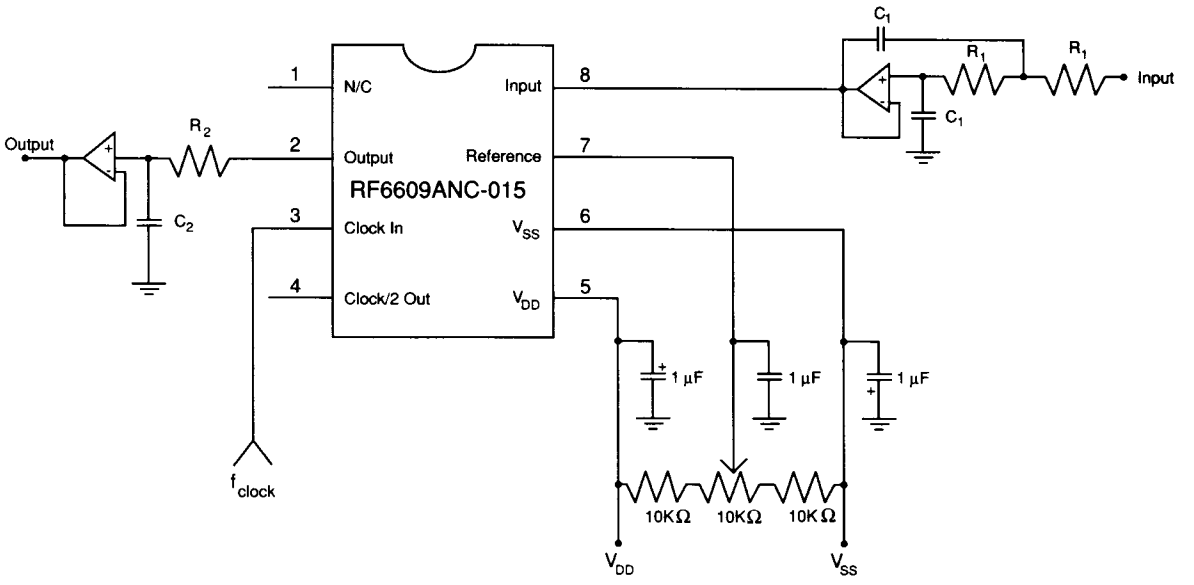
The input clock also needs to be shifted up in voltage because the clock threshold level is between 0.8V and 3V above the Reference pin voltage. A 5KΩ resistor in series with the Clock pin will reduce transients at the pin. The output of the Clock/2 pin is a squarewave signal at $f_c/2$ with voltage levels from V_{SS} (ground) to V_{DD}.

V_{REF} is set with a resistor voltage divider, similar to the DC offset correction circuit shown in Figure 7. The Reference pin takes very little current, but the divider tap point should be low-impedance (i.e., resistors on the order of 10KΩ) to minimize noise pickup at the pin. A capacitor (approx. 1 μF) is needed from the tap point to ground. A 5KΩ resistor in series with this pin helps protect the chip from large transient current at turn-on and turn-off. If the resistor is too large, crosstalk from the external circuit to filter input increases.

1-Decade Bandpass Filter Application

A 1-decade bandpass filter can be easily realized with cascading and the use of the RF6609 Clock/2 output (pin 4). This is demonstrated in Figure 9. The Reticon RF5611 is a high-pass switched-capacitor filter with a pinout identical to the RF6609, except that the RF5611 must have pin 1 (V_{SUB}) connected to V_{SS}. Cutoff frequency is 1/500 of its clock frequency.

By using the RF6609 Clock/2 signal for the RF5611 clock, a high pass cutoff frequency of $f_c/1000$ is generated. Then connecting the RF5611 output directly to the RF6609 input, we get a 1-decade bandpass filter (BPF) is achieved with cutoff frequencies close to $f_c/100$ and $f_c/1000$ (Figure 10). Setting f_c = 300 KHz realizes a BPF with a passband from 300 Hz to 3 KHz—a useful range for many audio applications.



$R_1C_1 = R_2C_2 = 1/10\pi f_o = 10/\pi f_c$

Bypass the op amp supply pins with capacitors.

Figure 7. Circuit to Correct Aliasing, Output DC Offset, Sampling Residue, Drive Limitations

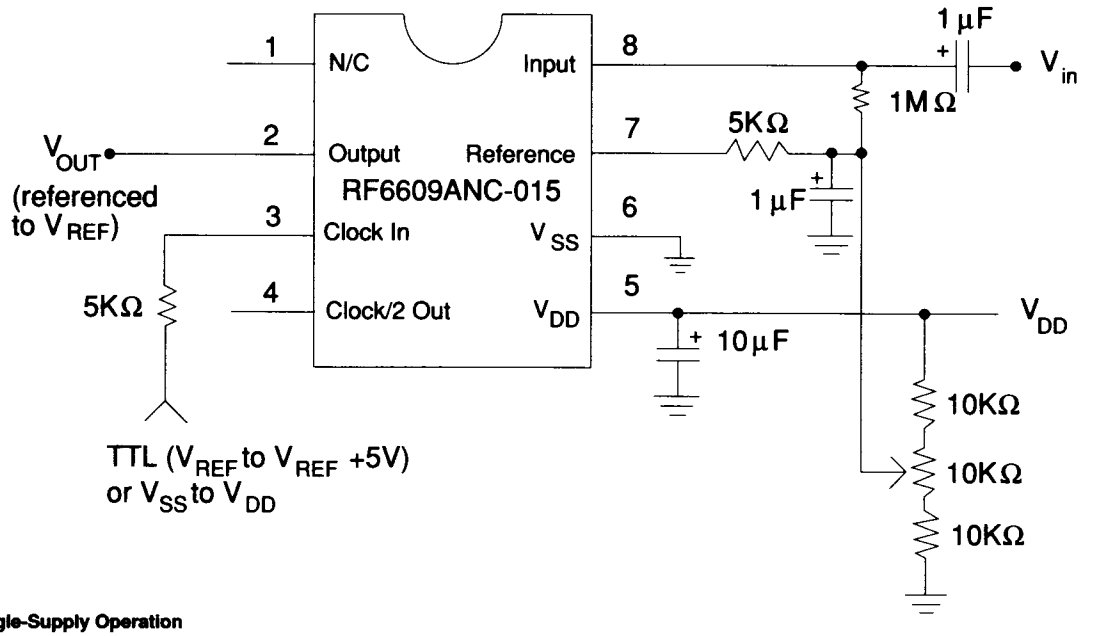


Figure 8. Single-Supply Operation

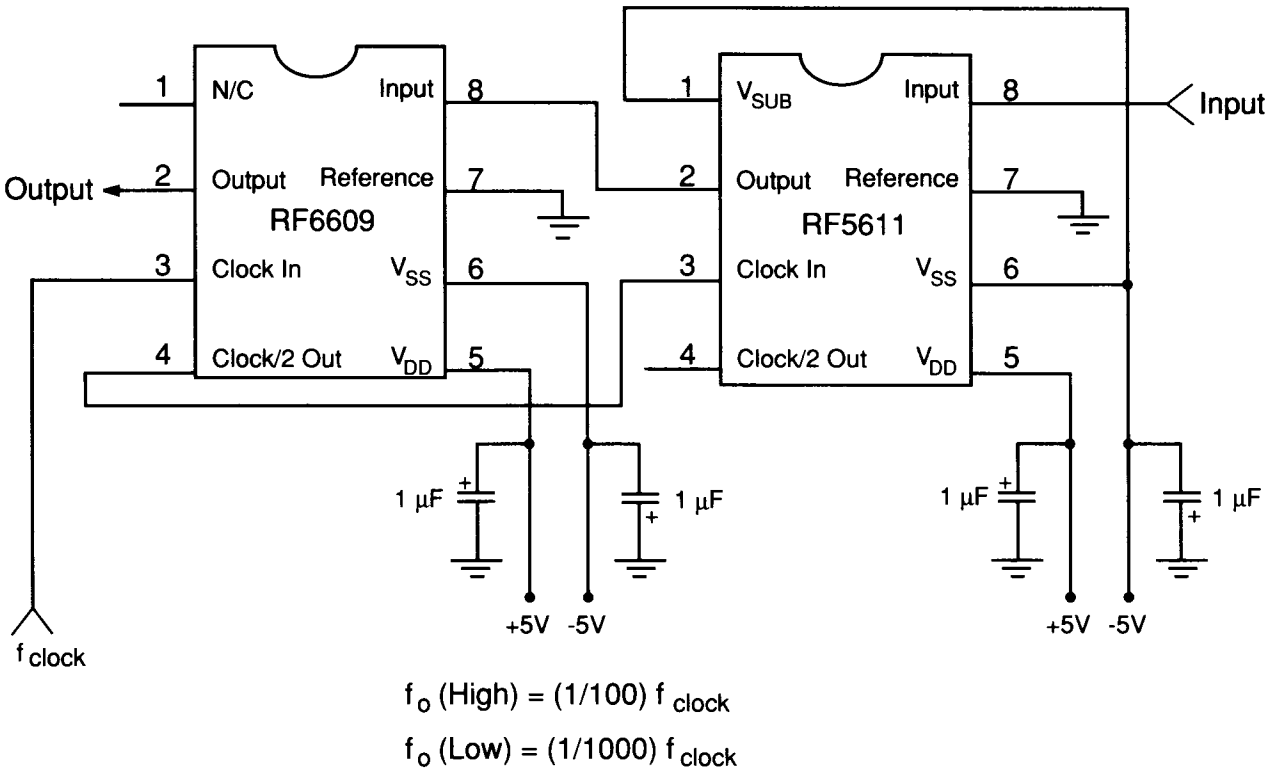


Figure 9. 1-Decade Bandpass Filter characteristics

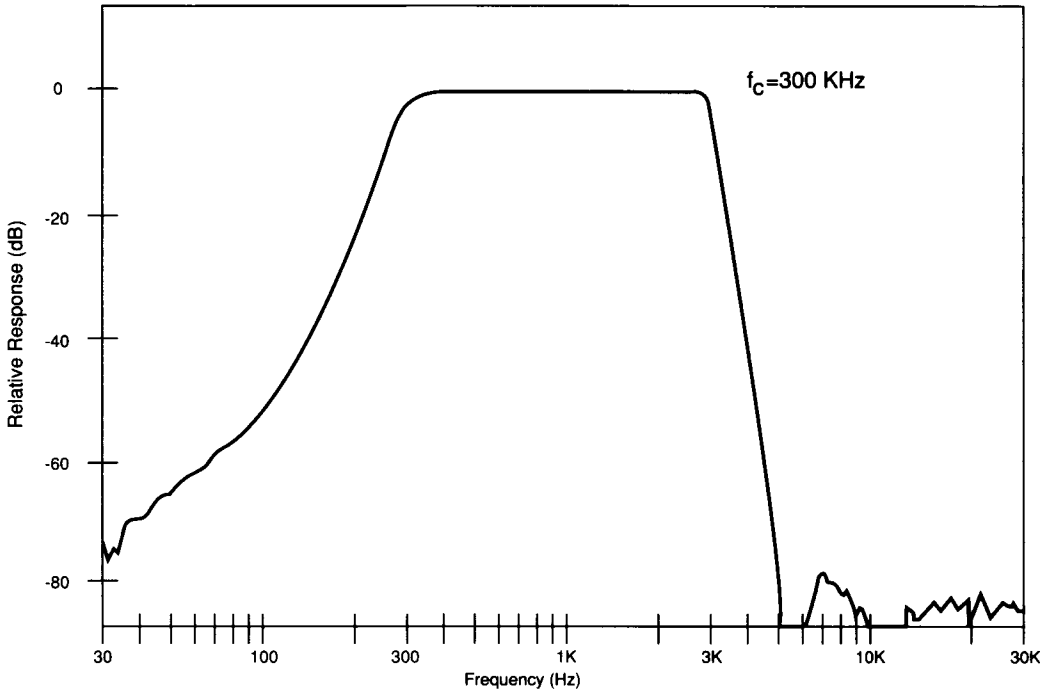


Figure 10. RF6609/RF5611 1-Decade Bandpass Filter Characteristic

Table I. Absolute Minimum/Maximum Ratings

	Min	Max	Units
Input voltage – any terminal with respect to substrate, pin 6 (V_{SS})	V_{SS}-0.4V	V_{DD}+0.4V	V
Output short-circuit duration – any terminal	Indefinite		
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C
Lead temperature (soldering, 10 sec)		300	°C

NOTE: This table shows stress ratings exclusively. Functional operation of this product under any conditions beyond those listed under standard operating conditions is not suggested by the table. Permanent damage may result if the device is subject to stresses beyond these absolute min/max values. Moreover, reliability may be diminished if the device is run for prolonged periods at absolute maximum values.

CAUTION: Observe MOS Handling and Operating Procedures

Although devices are internally gate-protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

Table II. Characteristics and Operating Range Limits [1]

Symbol	Parameter	Conditions and Comments	Min	Typ	Max	Units
±V	Supply voltage	+V = V_{DD}; -V = V_{SS}	±4.5	±5	±5.5	V
f_c	Clock frequency		1		2500	KHz
PW_c	Clock pulse width	T_c = Clock period in nanoseconds	100		T_c-100	nsec
V_{th}	Clock threshold voltage level		0.8		3	V
f_o	Corner frequency	-3 dB cutoff frequency	0.01		25	KHz
R_i	Input resistance [2,3]			≥10		MΩ
C_i	Input capacitance [3]	Bonding pad capacitance			15	pF
R_L	Load resistance		10			KΩ
C_L	Load capacitance				50	pF
R_o	Dynamic output impedance [3]			10	250	Ω
Io	Output current [3]				0.2	mA

Notes:

1 Test conditions: V_{DD} = 5V, V_{SS} = -5V, f_c = 2 MHz, R_L = 10KΩ, C_L = 50 pF, T_A = 25°C unless otherwise noted.

2 $R_i \approx 1/f_s C_{in}$, where f_s = sampling frequency = $f_c/2$, and C_{in} = capacitance of the first switched capacitor of the filter; $C_{in} \approx$ 1pF. $C_i \neq C_{in}$; C_i is the capacitance of the on-chip bonding pad to the substrate.

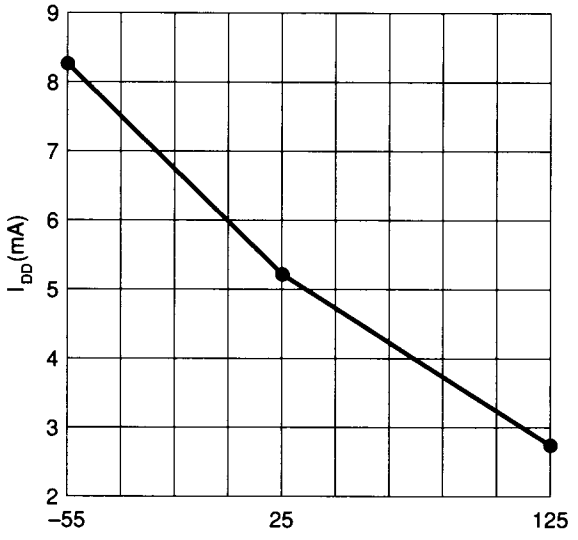
3 Guaranteed by design but not tested.

Table III. Guaranteed Performance Standards

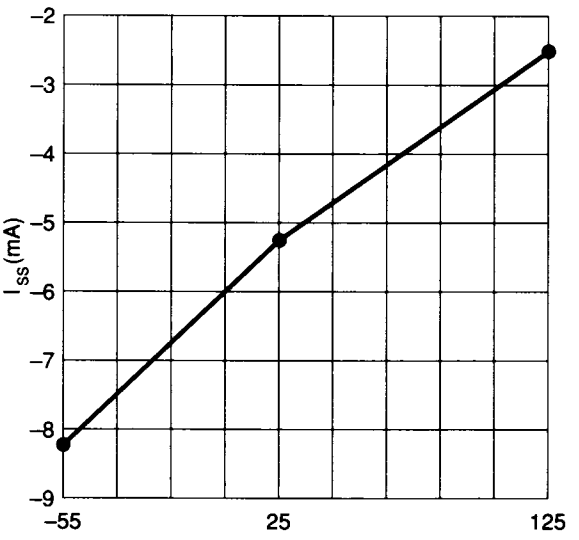
Test Conditions: (V_{DD} = +5V, V_{SS} = -5V, V_{in} = 1V rms and F_c = 2 MHz unless otherwise stated)

Symbol	Parameter	Conditions & Comments	-55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Units
I_{DD}	Supply current	Positive supply		16		9		9	mA
I_{SS}	Supply current	Negative supply	-16		-9		-9		mA
A_v	Passband gain	f_{in} = 10 KHz	-0.5	0.5	-0.25	0.25	-0.5	0.5	dB
	Passband ripple	0 - 10 KHz		0.25		0.2		0.5	dB
		0 - 18.5 KHz		1.0		0.85		2.0	dB
	Stopband rejection	V_{in} = 3Vrms, f_{in} = 1.5 f_o	50		50		50		dB
		V_{in} = 3Vrms, f_{in} = 2.3 f_o [1]	70		70		70		dB
f_c/f_o	Clock-to-corner ratio	-3 dB point	99	101	99	101	99	101	
	Input voltage range		V_{SS}+1	V_{DD}-1	V_{SS}+1	V_{DD}-1	V_{SS}+1	V_{DD}-1	V
	Output voltage range	0.2% THD	5.5		7		5.5		V p-p
DR	Dynamic range		73		78		73		dB
THD	Total harmonic distortion	V_{in} = 1V p-p, f_{in} = 1 KHz		0.2		0.1		0.2	%
		V_{in} = 8V p-p, f_{in} - 1 KHz				0.2			%
V_{off}	Output DC offset		-500	500	-200	200	-500	500	mV
	Clock feedthrough	f_c = 100 KHz		4.5		4		4.5	mVrms
e_n	Output noise	15 KHz bandwidth		0.4		0.35		0.4	mVrms
PSRR	Power supply rejection ratio	f_c = 100 KHz 0.1V rms ripple @ 1 KHz							
		V_{DD} PSRR	10		10		10		dB
		V_{SS} PSRR	3.0		3.5		3.0		dB

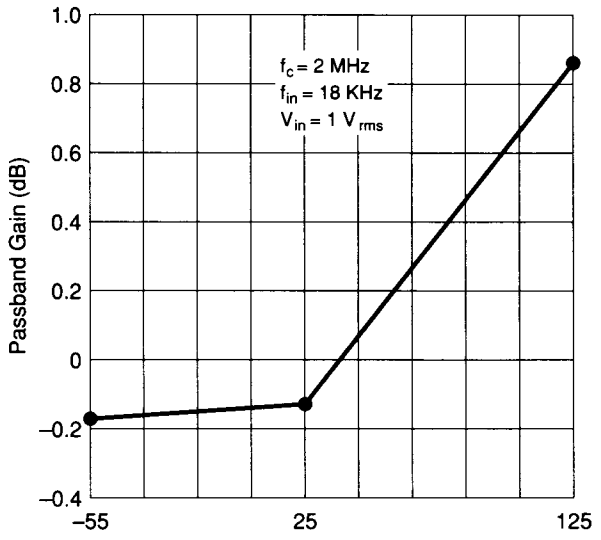
1 Guaranteed by design



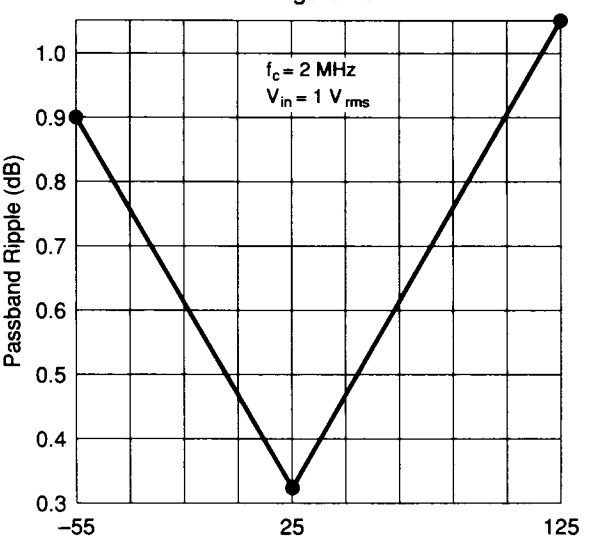
I_{DD} versus Temperature
Figure 12



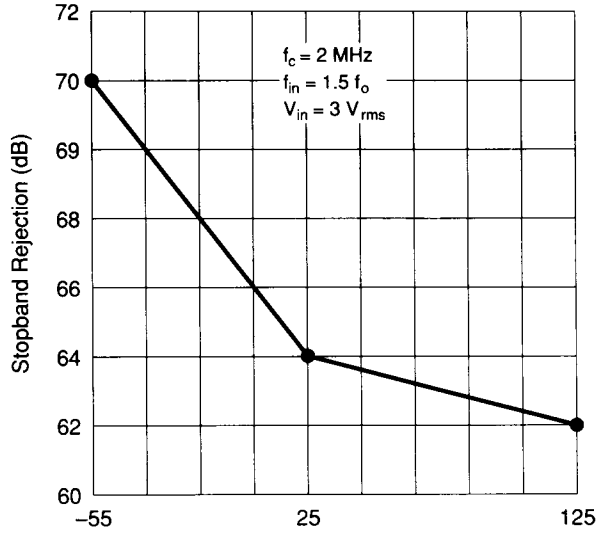
I_{SS} versus Temperature
Figure 13



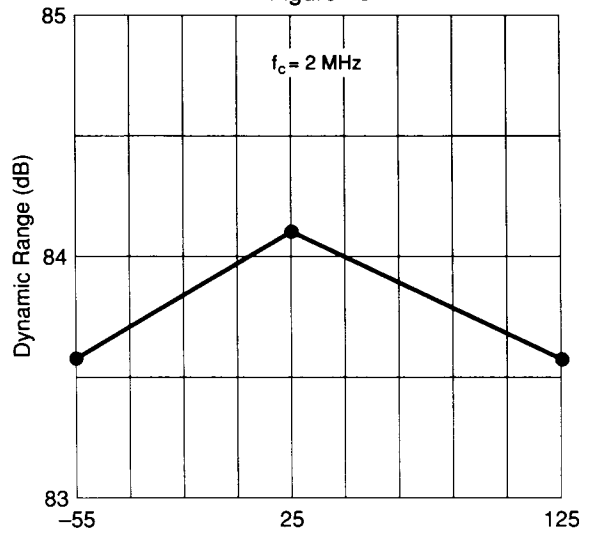
Passband Gain versus Temperature
Figure 14



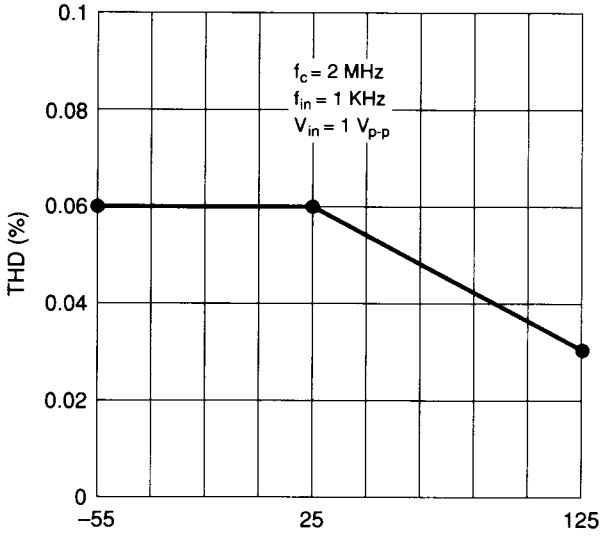
Passband Ripple versus Temperature
Figure 15



Stopband Rejection versus Temperature
Figure 16

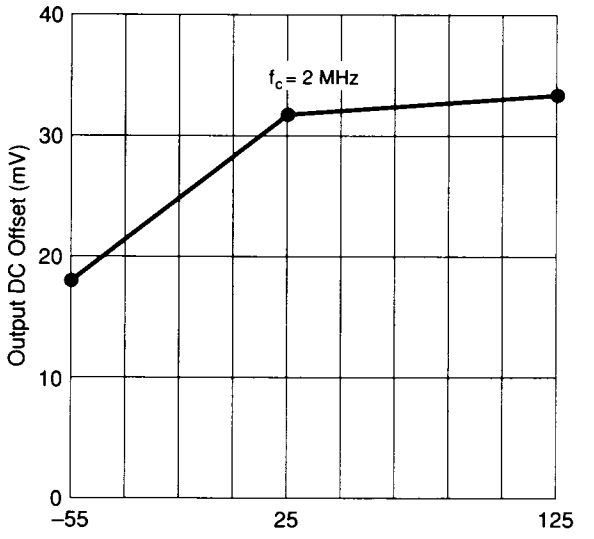


Dynamic Range versus Temperature
Figure 17



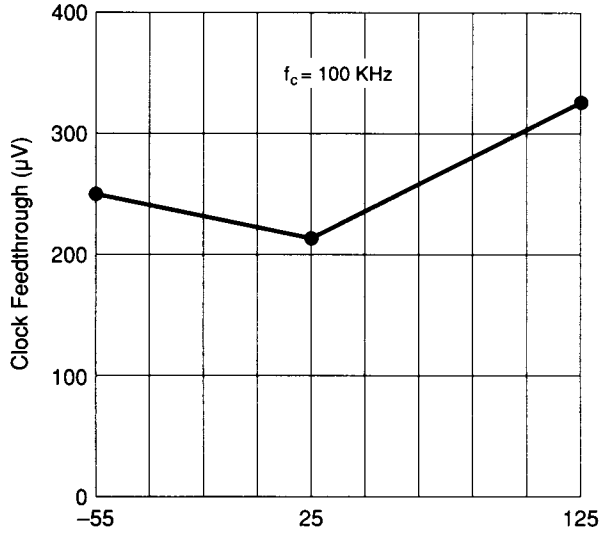
Total Harmonic Distortion versus Temperature

Figure 18



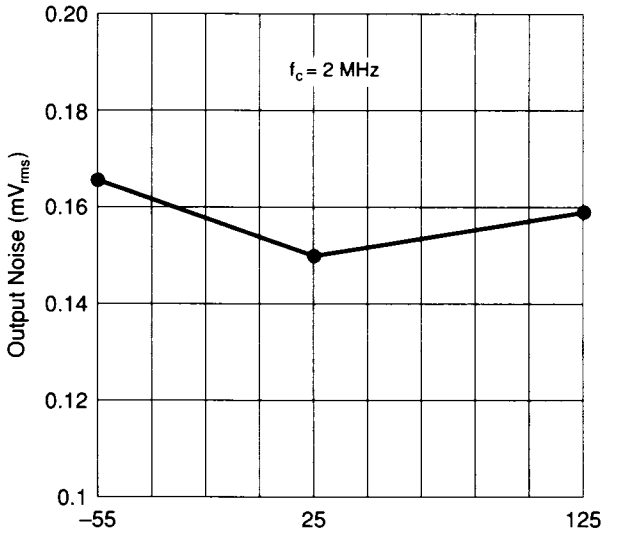
Output DC Offset versus Temperature

Figure 19



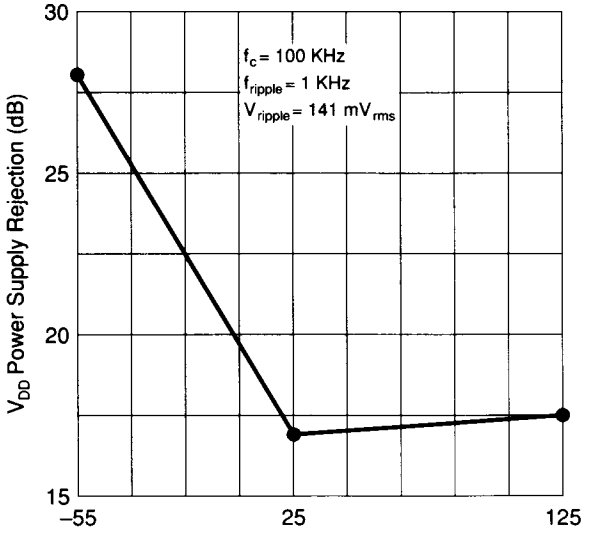
Clock Feedthrough versus Temperature

Figure 20



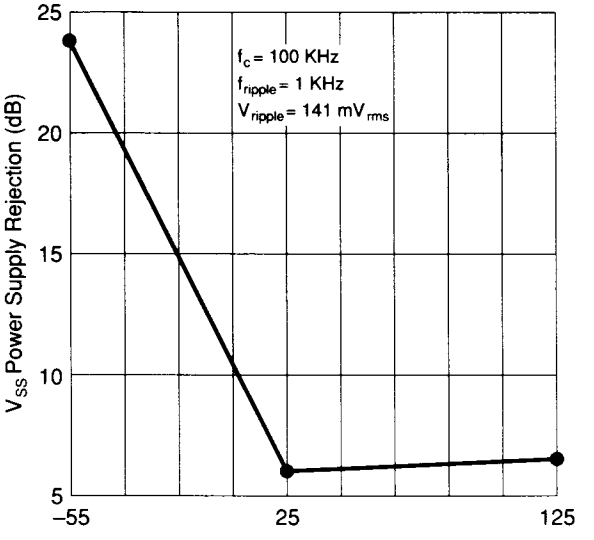
Output Noise versus Temperature

Figure 21



Power Supply Rejection (V_{DD}) versus Temperature

Figure 22



Power Supply Rejection (V_{SS}) versus Temperature

Figure 23

RF6609ANC-015 8-pin cerdip

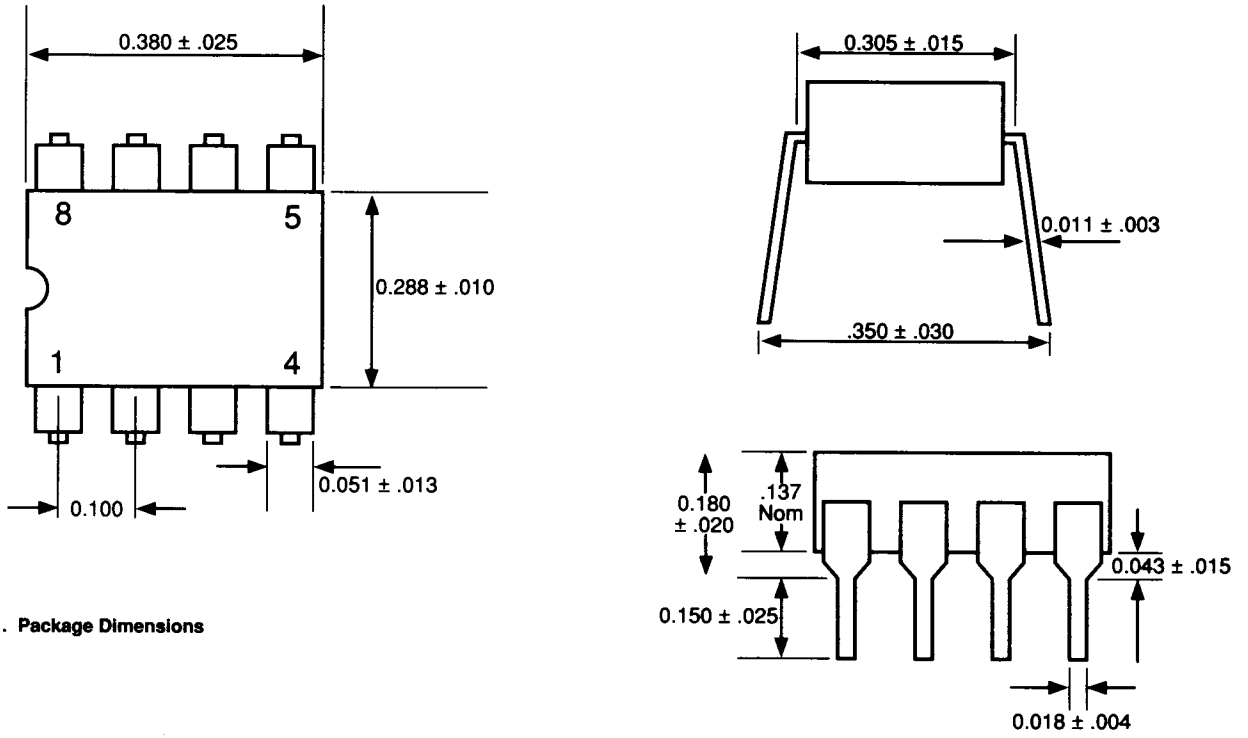


Figure 11. Package Dimensions

Ordering Information

Ordering No.
RF6609ANC-015

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055-0279
January 1990