CHAPTER 2

HARDWARE CONFIGURATIONS

The MGR adapter comes in two configurations which are referred to as the base configuration and the enhanced configuration. The base configuration has 8 frame buffer bitplanes, 2 auxiliary bitplanes and 2 Window ID bitplanes. The enhanced configuration has 24 frame buffer bitplanes, 4 auxiliary bitplanes and 4 Window ID bitplanes. Both wnfigurations may have an optional Z buffer card which contains 24 bitplanes. The base and enhanced configurations both use two identical Micro Channel Architecture (MCA) bus cards. The first MCA bus card contains the Host Interface Subsystem and the Geometry Subsystem. The second MCA bus card contains the Raster Subsystem and part of the Display Subsystem. The difference between the two configurations is in the type of Display Subsystem daughter card that is attached to the second MCA bus card. The base configuration Display Subsystem daughter card contains no extra bitplanes and uses a simpler Display Subsystem. The enhanced configuration contains 16 extra frame buffer bitplanes, 2 extra auxiliary bitplanes and 2 extra Window ID bitplanes. It also contains a 4 K color map that is not present on the base configuration daughter card.

The Micro Channel Architecture requires each card to have a Vital Products Data (VPD) PROM on it. The VPD PROM is 256 bytes and contains various hardware configuration data such as the Serial number, part number and version numbers. The VPD PROM is described in the Host interface subsystem chapter since it is part of the Micro Channel Architecture concepts. It is only mentioned elsewhere as a reference of it's existence on the two MCA cards and the various daughter boards which attach to the second MCA card. The following paragraphs describe the base and enhanced configurations of the MGR adapter.

Base Configuration

The base configuration, as shown in Figure 2.1, consists of the two standard MCA bus cards and the base Display Subsystem daughter board which is attached to the second MCA card. The base configuration provides 12 bitplanes of VRAM of which 8 are used for the image frame buffer bitplanes, 2 are used as overlay bitplanes and 2 are used as Window ID bitplanes. A Z buffer daughter card may also be attached to the second MCA bus card to provide 24 bitplanes of Z buffer for depth comparison calculations. The following paragraphs describe the two MCA bus cards, the Z buffer daughter card and the base configuration Display Subsystem daughter board.

MGE2 Card Description

The MGE2 card contains the Host Interface subsystem the Geometry subsystem and the Vital Product Data (VPD) PROM. The VPD PROM is described in the Host Interface Subsystem chapter and contains various hardware configuration and manufacturing related information.

The Host Interface Subsystem contains the necessary circuitry to provide the proper interface to the MCA bus and to maintain the appropriate stat8 information required by the MCA bus. It also interfaces to the Geometry subsystem over a Local bus which is compatible with the SGI private bus. The Host Interface Subsystem contains the Programmable Option Select (POS) registers which are used to configure the adapter.

The Geometry Subsystem contains almost exactly the same circuitry as the GR1 graphics board in the SGI Personal IRIS system. The Geometry Subsystem is referred to as the GE5 and performs the 3D graphics calculations and does the high level pixel rendering operations.

The MGE2 card has two bus connections to the MRV2 card. The GE bus provides the data path between the Geometry Subsystem and the Raster Subsystem. The Utility bus provides the data path between the Host Interface Subsystem and the Display Subsystem. The GE bus and the Utility bus use ribbon cables to connect the MGE2 card to the MRV2 card.

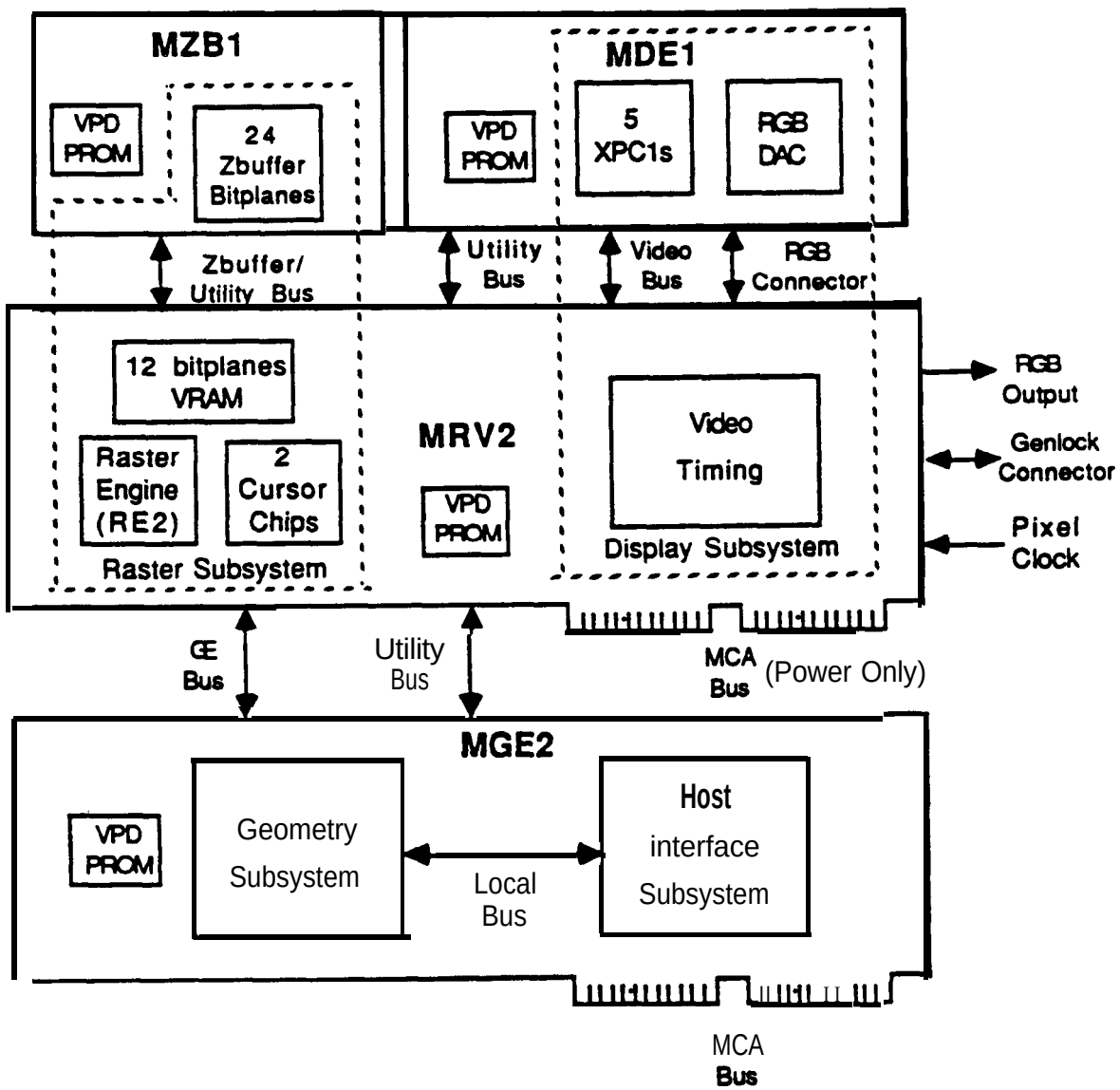


Figure 2.1 Base Configuration Block Diagram

MRV2 Card Description

The MRV2 card contains the VPD PROM, the Raster subsystem, the Video Timing circuitry, the RGB output connector, the genlock connector and the pixel clock input connector. The card plugs into an

MCA bus slot but only uses the power connections. It does not have an interface to the other MCA bus signals.

The Raster subsystem contains the 12 bitpianes of VRAM, the 2 cursor chips and the Raster Engine 2 (RE2) chip. The Raster Subsystem performs the low level pixel rendering and Z buffer calculations. it also provides the necessary signals to control the access to the various bitplanes.

The Video Timing circuitry is a state machine that provides the necessary timing circuitry for the Raster subsystem and the Display subsystem. The video timing is programmable and allows up to four different types of monitors to be connected to the MGR adapter.

The MRV2 card provides the necessary connectors for the MDE1 card to attach to it. There is a connector for the Utility bus to be extended to the MDE1 card. Another connector provides the data path for the Video bus between the Raster subsystem and the Display subsystem. A connection is also provided to route the RGB outputs from the RGB DAC on the MDE1 card to the RGB output connector on the MRV2 card.

A Pixel bus connector is provided for connecting the Raster subsystem to the extended bitplanes but it is only used when the MEV2 card is connected in the enhanced configuration. A Zbuffer bus connection is also provided for the optional MZB1 card when it is attached.

The RGB output connector provides the RGB signals for connection to the high resolution monitor. This connector contains a red color signal, a green color signal and a blue color signal. These signals conform to the RS-343A standard and are capable of driving doubly terminated 75-ohm coaxial cable directly.

The Genlock and Pixel clock connectors provide an interface to an optional genlock card.

MDE1 Card Description

The MDE1 card is a daughter board which connects to the front side of the MRV2 card. It contains the VPD PROM, the five XPC1 chips and the RGB DAC chip which are part of the Display subsystem. These components are described in the chapter on the Display subsystem.

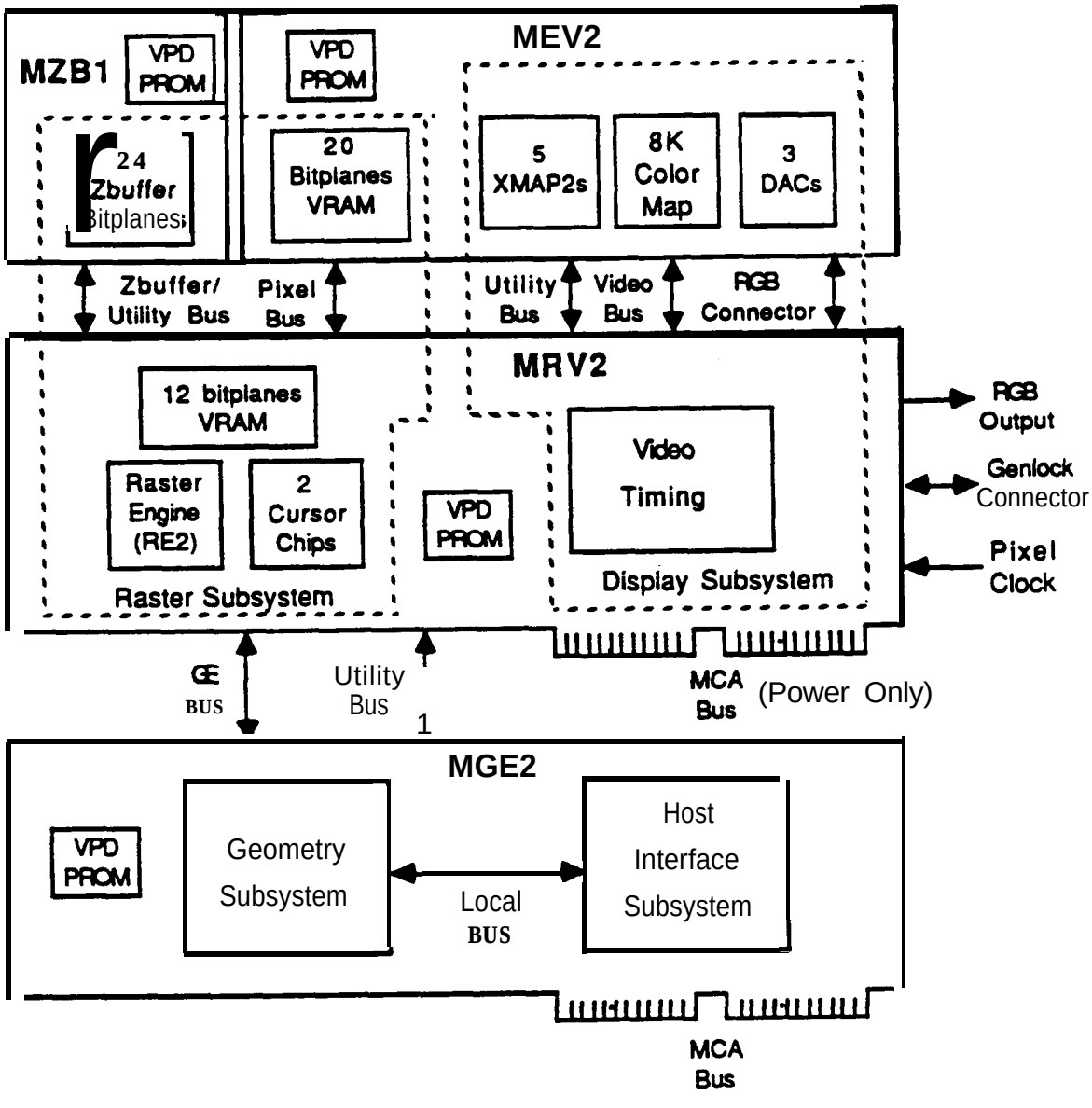
The card has the Utility bus, Video bus and RGB connections described above for the MRV2 card.

MZB1 Card Description

The MZB1 daughter board also attaches to the MRV2 card and provides the 24 bitpfanes of VRAM used for the Zbuffer. The card has a Zbuffer bus connection to the Raster subsystem on the MRV2 card. This bus is part of the Utility bus connector. This card also has a VPD PROM. The Zbuffer is described in greater detail in the chapter on the Raster subsystem.

Enhanced Configuration

The enhanced configuration, as shown in Figure 22, consists of the two standard MCA bus cards, an enhanced Display Subsystem daughter card and the optional Z buffer card. The enhanced configuration contains 24 frame buffer bitplanes, 4 overlay bitplanes, 4 window ID bitplanes and 24 Z buffer bitplanes. The MGE2 card, the MRV2 card and the MZB1 card are the same as in the base configuration. The enhanced Display Subsystem daughter card is described in the following paragraphs.



Rgure 22 Enhanced Configuration Block Diagram

MEV2 Card Description

The **MEV2** card is a daughter board which attaches to the **MRV2** card. It has a VPD **PROM and** provides an additional 20 bitplanes of VRAM which are part of the Raster subsystem. **It also** contains the **five XMAP2** chips, the 8K co&r map chip and the three DAC chips which are part of the Display subsystem and are described in the chapter on the Display subsystem.

The card has the Utility bus, Video bus, Pixel bus and RGB connections described above for the MRV2 card.

The enhanced configuration provides the full 24 bit RGB capabilities as does the SGI Personal IRIS workstation. The enhanced adapter allows both single and double buffer modes of operation in both color index modes and RGB modes.

The following chapters describe the Host Interface Subsystem, the Geometry Subsystem, the Raster Subsystem and the Display Subsystem. Each chapter explains the differences between the base and enhanced configurations for that particular subsystem.