ITT

Technical Reference

ITT XTRA™ Personal Computer

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For the ITT XTRA™ Personal Computer

ITT

ITT INFORMATION SYSTEMS

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DESCRIPTION

1 - Overview Of Major Hardware Components

SYSTEM OVERVIEW

The ITT XTRA Personal Computer system includes three basic components: the system unit, a keyboard, and a monitor.

The system unit is housed in a metal enclosure measuring 5.59" (142 mm) high, 14.00" (356 mm) wide, and 15.57" (395 mm) deep. The system motherboard is the large printed-circuit board that is mounted within the enclosure. Major components on the motherboard include the following:

8088 microcomputer that runs at 4.773 MHz; optional 8087 coprocessor;

128KB of Dynamic Random Access Memory (64K x 1 DRAM chips); expandable to 256K of DRAM on the motherboard (expandable to 512K if 256K x 1 DRAM chips installed);

32KB of Read-Only Memory (27128 ROM) that contains the power-on diagnostics, ROM monitor, bootstrap loader, and the basic input/output system (BIOS) (expandable to 64K);

An 8272A (or NEC uPD765 equivalent) floppy disk drive controller that controls the system's 5.25" floppy disk drive(s).

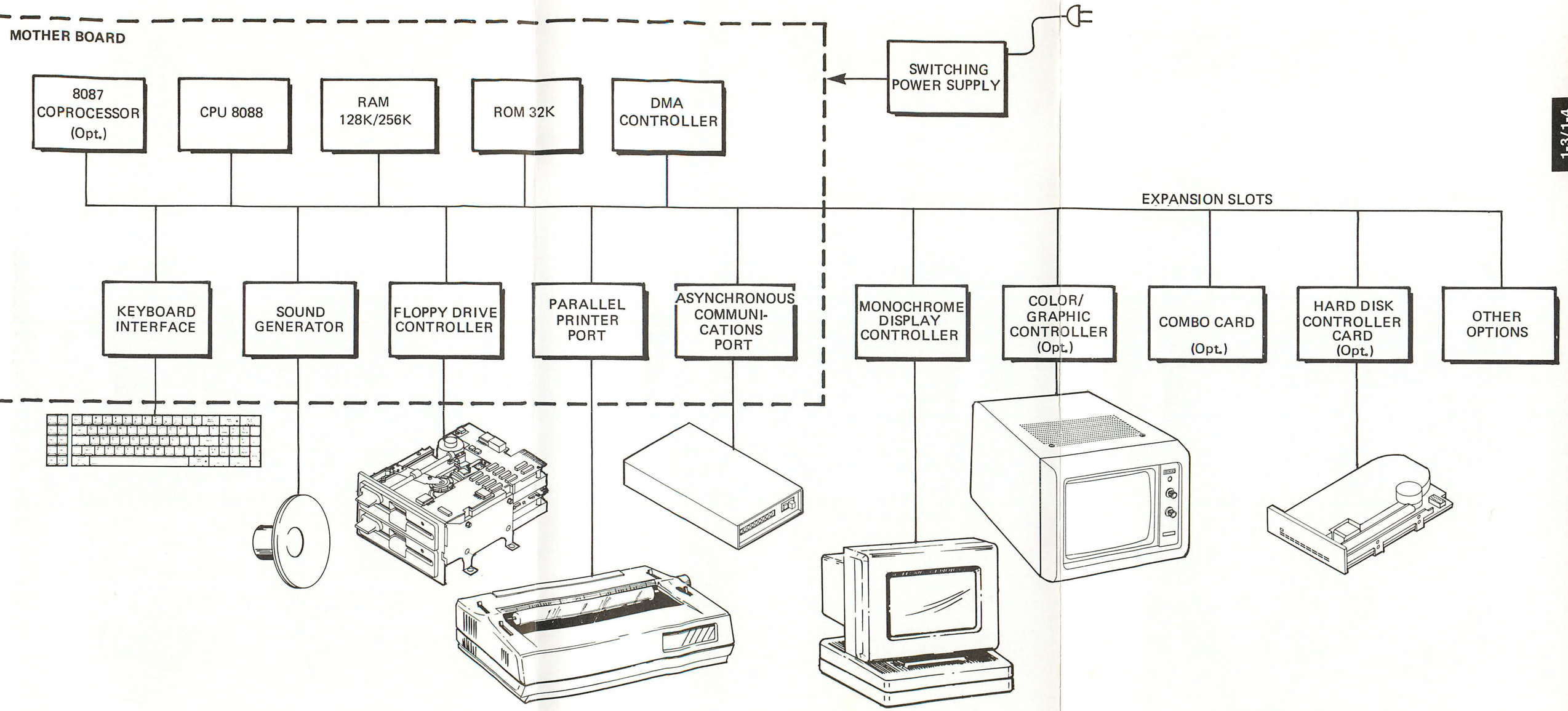
An INS 8250 controlled asynchronous communications port (RS-232-C compatible);

A parallel printer port;

Five expansion slots that provide access to the system bus for a monitor controller card (monochrome and/or color) and a variety of hardware option cards such as a hard disk controller and a Combo board (featuring up to 384K of additional memory, real-time clock, and parallel printer port);

These motherboard features and all other major system components are illustrated in the following figure.

SYSTEM BLOCK DIAGRAM



ITT System Components

The unit's 115 Watt current-limiting switching power supply is also mounted within the system unit. The supply can operate on input voltages ranging from 95 to 132 VAC (110 VAC) and 180 to 264 VAC (220 VAC). It outputs DC voltages of +5V, +12V, -12V, and an unregulated 15 - 20V for the monochrome monitor.

One or two 5-1/4" disk drives are also mounted within the system unit. These drives provide the system with the capability of writing data to and reading from 5-1/4" flexible diskettes. Each diskette can store up to 362,496 bytes of data (double-sided, double density, nine sectors per track, 512 bytes per sector). The optional internal hard disk is also mounted within the system unit. It can store up to 10 Megabytes of data.

The system's low profile, detachable keyboard is connected to the system unit by a six-foot shielded, coiled cord. The keyboard is designed to provide tactile feedback. The 84 sculptured keys are arranged in four basic groups: standard typewriter keys, the numeric keypad, cursor control keys, and special function keys. Ten of the special function keys are completely programmable. When these keys are used in conjunction with the Shift Ctrl and Alt keys, up to 40 unique functions can be assigned.

The monochrome display control card plugs into one of the motherboard's expansion slots. This card supports the system's high resolution monochrome display (available in amber or green phosphor). The 14" diagonal, anti-glare display screen offers a 25-line by 80-character format, contrast adjustment, 256 different characters, and numerous video attributes (e.g., blink, blank, underline, normal/reverse video, and highlight). Characters are formed in a 7 x 9 matrix in a 9 x 14 cell.

The optional color/graphics control card also plugs into one of the motherboard's expansion slots and is designed to operate with a variety of industry standard color monitors. It supports a direct connect port, composite video port, RF modulator, and a light pen interface. The color/graphics board features both text and graphics modes. High resolution (80 x 25) text mode and low resolution (40 x 25) text mode feature eight background colors and sixteen foreground colors. High resolution graphics

mode (640 x 200) is black and white only. Low resolution graphics mode (320 x 200) features four colors. Characters in both text and graphics modes appear within an 8 x 8 cell. Each character measures 5 x 7. One line is dedicated to lowercase descenders.

A 2-1/4" audio speaker is attached to the inside of the system unit. The control circuits which drive the speaker are located on the motherboard.

The optional Combo board plugs into one of the 62-pin motherboard expansion slots and provides an additional 128KB of memory , a battery backup real-time clock, and an 8-bit general purpose port which can be used for a parallel printer. Two "baby" add-on memory cards of 128KB each can also be plugged into the Combo board raising the available memory on the board to 384K.

The optional hard disk controller card plugs into one of the motherboard's expansion slots and interfaces the 10 MB internal hard disk drive to the system.

Optional ITT printers provide letter quality printing at speeds of 20, 40, 55, or 90 characters per second. These printers can use over 100 different types of printwheels in monospace (10, 12, or 15 pitch) or proportional space modes. In addition to printing standard upper and lower case ASCII characters, the printers feature a programmable graphics mode with resolution of up to 5760 points per square inch. Self-test diagnostic procedures and simple paper and ribbon installation procedures are standard. Both serial and parallel printers are supported by ports on the XTRA's motherboard.

2 - System Motherboard

OVERVIEW

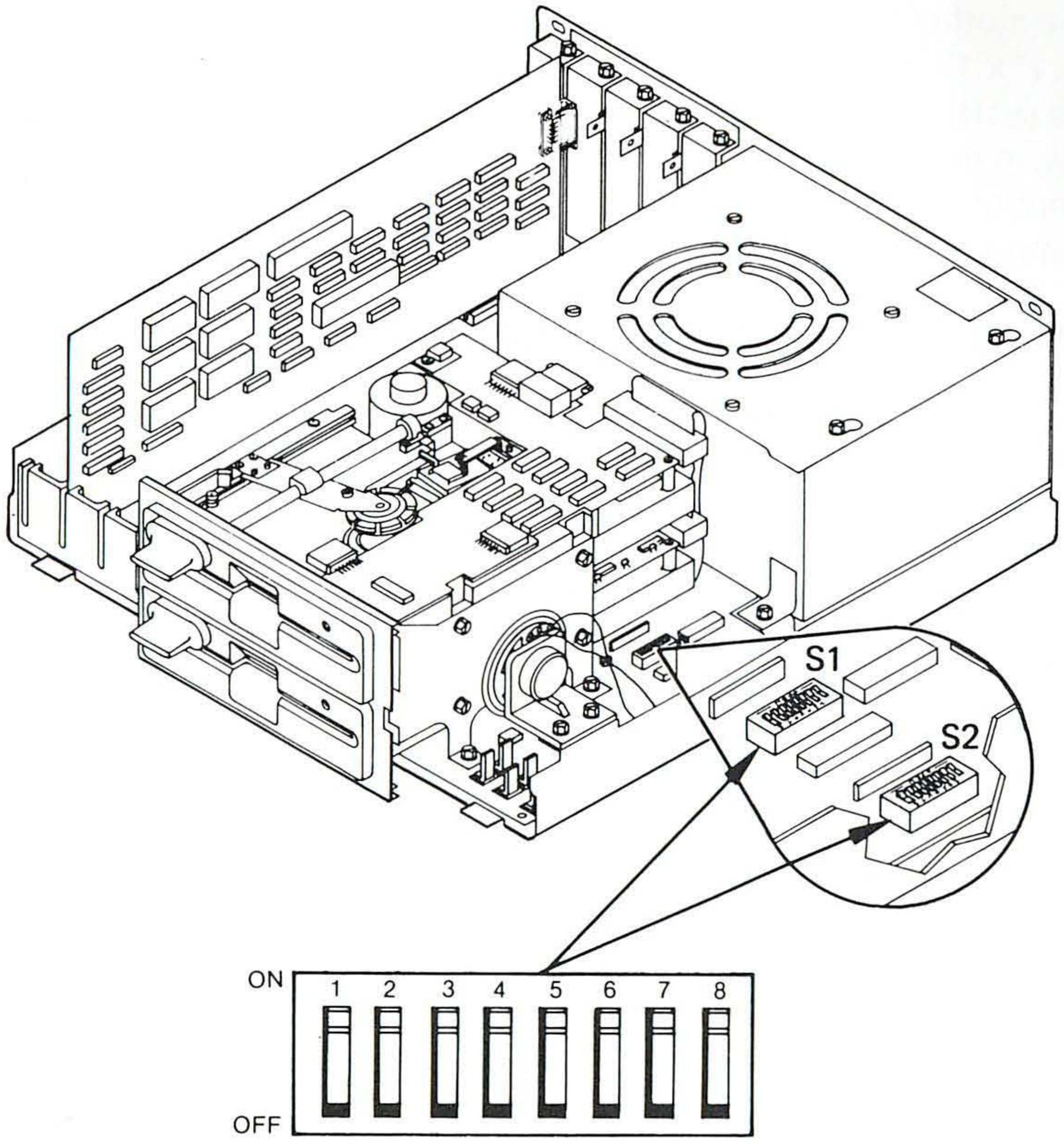
The motherboard is a multilayer printed-circuit board measuring 14.1" x 13.5". As illustrated in the previous block diagram, most of the system's major components are located on the motherboard. It is, in effect, a single board computer. This section provides a functional description of each of the motherboard's major components.

CONNECTORS, DIP SWITCHES, AND JUMPERS

DC power is supplied to the motherboard through a 9-pin connector. Other connectors on the motherboard are provided for the keyboard, the speaker, the two 5-1/4" disk drives, the asynchronous communication port and parallel printer port. Pin assignments for each of these connectors are included with the functional description of the circuit, e.g., see the section titled "Asynchronous Communications Controller" for the pin assignments on connector P19, the asynchronous communications port.

Also mounted on the motherboard are five system expansion slots that provide for the monitor control and hardware option cards. The system's I/O channel is bussed across each of the five 62-pin card edge sockets that comprise this expansion backplane.

Two Dual In-Line Package (DIP) switches, S1 and S2, are mounted on the motherboard.



Motherboard DIP Switches

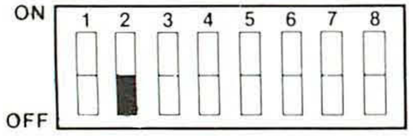
The system software reads these switches to determine the current configuration (i.e., type of display, number of floppy disk drives installed, or amount of installed memory). The DIP switches are set at the factory to indicate the shipped system configuration. If a system addition or deletion is made, these switch settings may need to be changed to reflect the current state of the system.

The following two figures illustrate each correct DIP switch setting for all possible ITT XTRA Personal Computer configurations. The additional settings for the floppy disk drives are for future expansion.

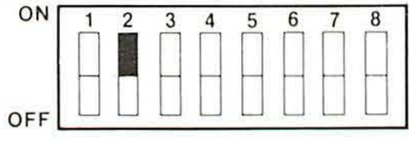
SWITCH 1 SETTINGS

MATH COPROCESSOR

***Math Coprocessor* Installed**

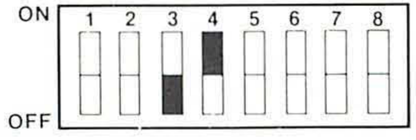


Math Coprocessor Not Installed

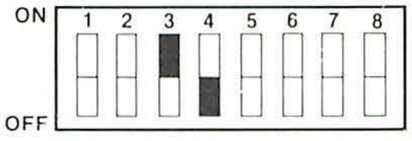


MOTHERBOARD MEMORY

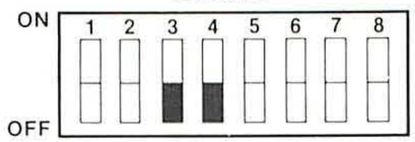
128K



192K

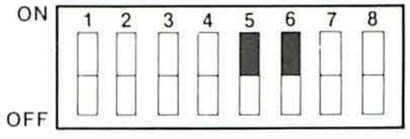


256K

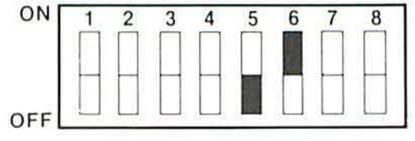


MONITOR TYPE

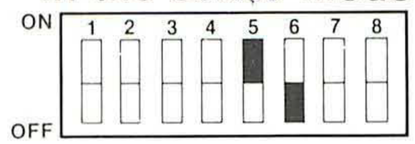
80x25 COLOR



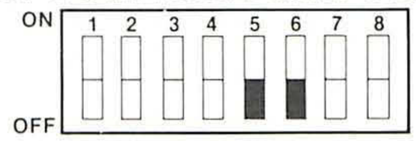
40x25 Color Mode



Color Monitor in the 80x25 Mode

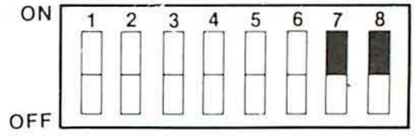


Monochrome Monitor or Both Mono and Color

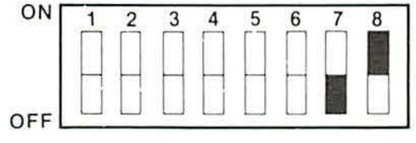


FLOPPY DISKETTE DRIVE

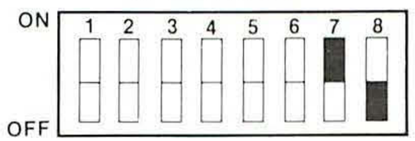
1 Drive



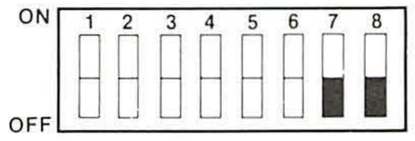
2 Drives



3 Drives



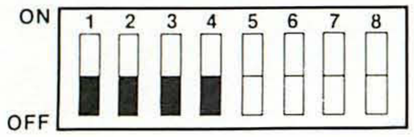
4 Drives



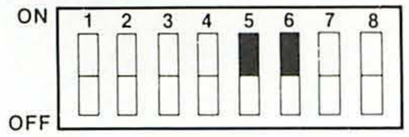
Motherboard DIP Switch Functions, Bank 1

SWITCH 2 SETTINGS

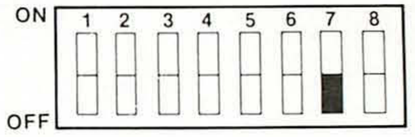
Switches 1-4, Not Used



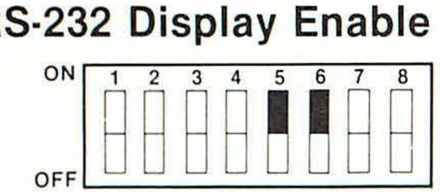
Screen Time Out ON



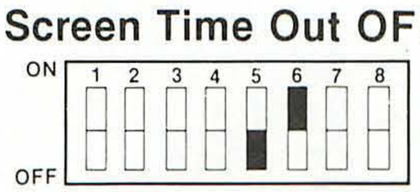
Power Up Self Test OFF



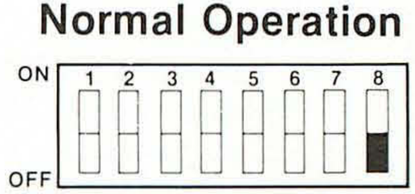
RS-232 Display Enable ON



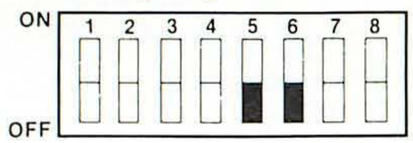
Screen Time Out OFF



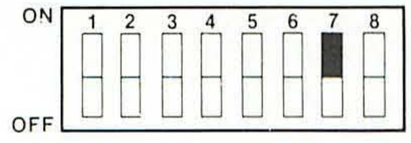
Normal Operation



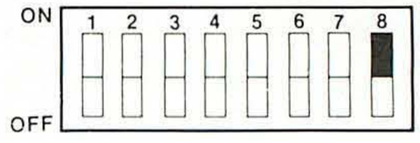
RS-232 Display Enable OFF



Power up Self Test ON

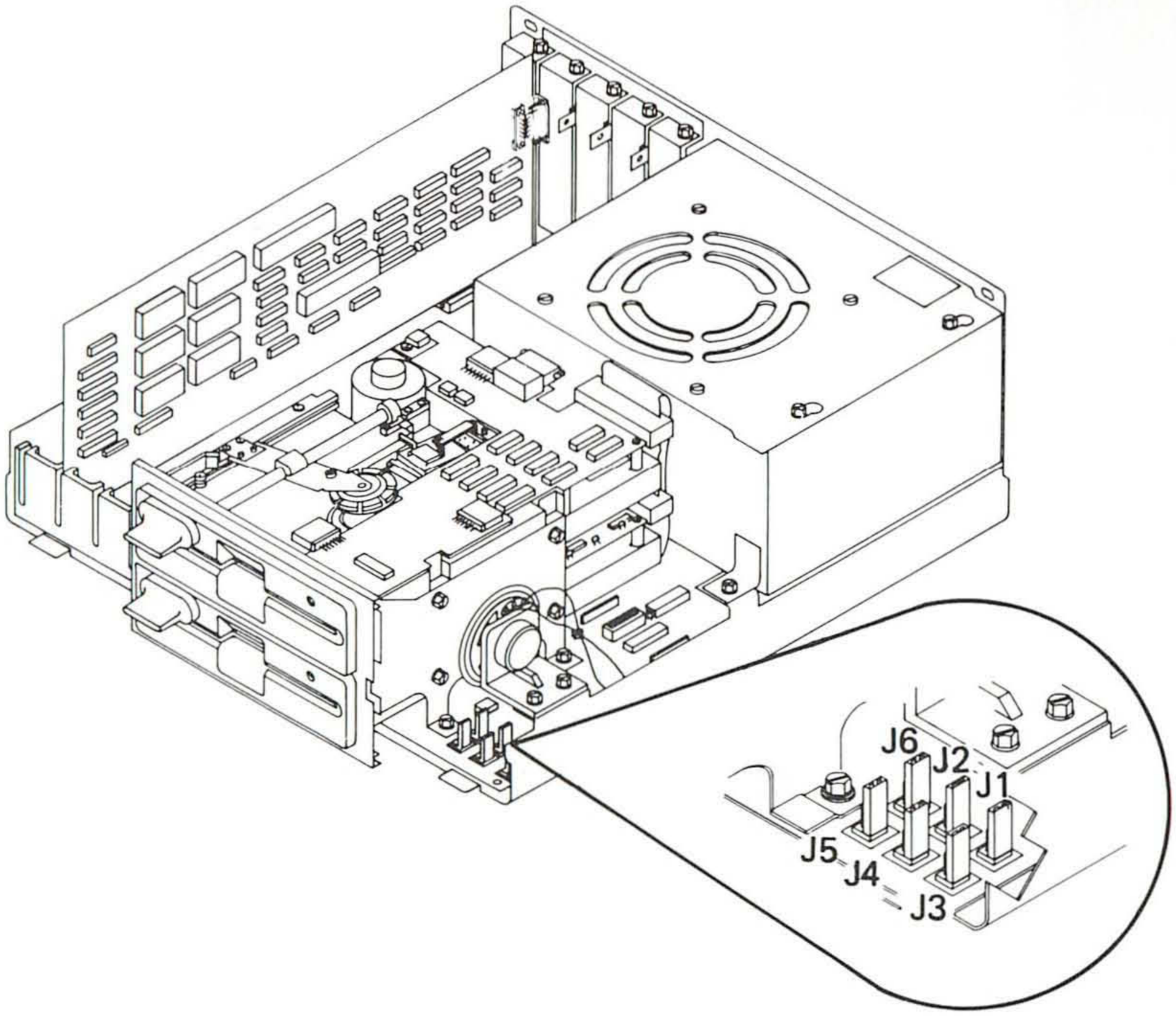


Factory Testing



Motherboard DIP Switch Functions, Bank 2

Jumpers on the right, front corner of the motherboard allow reconfiguration of the board to support future options.



Motherboard Jumpers

MOTHERBOARD JUMPER CONFIGURATIONS

JUMPER	SHORTING PLUG ACROSS PINS	PURPOSE
J1	1 & 2	27128 (16K X 8 EPROMS)
	3 & 4	FUTURE OPTION - 27256 (32K X 8 EPROMS)
J2	1 & 2	27128 (16K X 8 EPROMS)
	3 & 4	FUTURE OPTION - 27256 (32K X 8 EPROMS)
J3	1 & 2	64K X 1 DRAMS
	3 & 4	FUTURE OPTION - 256K X 1 DRAMS
J4	1 & 2	64K X 1 DRAMS
	3 & 4	FUTURE OPTION - 256K X 1 DRAMS
J5	1 & 2	64K X 1 DRAMS
	3 & 4	FUTURE OPTION - 256K X 1 DRAMS
J6	1 & 2	RESERVED
J6	3 & 4	KEYBOARD

Other jumpers on the motherboard, J8 and J10, have no plug installed. J8 is not used. J10 is used at the factory to reset the system.

I/O ADDRESS MAP

I/O ADDRESS MAP

HEX RANGE	9	8	7	6	5	4	3	2	1	0	DEVICE
000H-01FH	0	0	0	0	0	A4	A3	A2	A1	A0	8237A-5 DMA CONTROLLER
020H-03FH	0	0	0	0	1	A4	A3	A2	A1	A0	8259A INTERRUPT CONTROLLER
040H-05FH	0	0	0	1	A5	A4	A3	A2	A1	A0	8253-5 INTERVAL TIMER CONTROLLER
060H-07FH	0	0	0	1	1	A4	A3	A2	A1	A0	8255A-5 PARALLEL PERIPHERAL INTERFACE CONTROLLER
080H-09FH	0	0	1	0	0	A4	A3	A2	A1	A0	DMA BANK REGISTERS
0A0H-OBFH	0	0	1	0	1	A4	A3	A2	A1	A0	NMI MASK REGISTER
378H-37AH	1	1	0	1	1	1	1	A2	A1	A0	PARALLEL I/O PORT (COMBO BOARD)
37BH & 379H	1	1	0	1	1	1	A3	A2	A1	A0	REAL TIME CLOCK
3B0-3BB	1	1	1	0	1	1	A3	A2	A1	A0	6845 MONOCHROME CONTROLLER
3BCH-3BFH	1	1	1	0	1	1	1	1	A1	A0	PARALLEL I/O PORT (MOTHER-BOARD)
3F0H-3F7H	1	1	1	1	1	1	0	A2	A1	A0	765 FLOPPY DRIVE CONTROLLER
3F8H-3FFH	1	1	1	1	1	1	1	A2	A1	A0	8250 SERIAL I/O PORT
3D0H-3DFH	1	1	1	1	0	1	A3	A2	A1	A0	6845 COLOR/GRAPHICS CONTROLLER

SYSTEM MEMORY MAP

START ADDRESS:		
DECIMAL	HEXIDECIMAL	FUNCTION
0	00000	
16K	04000	
32K	08000	
48K	0C000	
64K	10000	28 KB READ/WRITE MEMORY
80K	14000	ON MOTHERBOARD
96K	18000	
112K	1C000	
128K	20000	
144K	24000	
160K	28000	
178K	2C000	
192K	30000	OPTIONAL 128 KB READ/WRITE
208K	34000	MEMORY ON MOTHERBOARD
224K	38000	
240K	3C000	
256K	40000	
272K	44000	
288K	48000	
304K	4C000	
320K	50000	OPTIONAL COMBO BOARD
336K	54000	READ/WRITE MEMORY
352K	58000	
368K	5C000	
384K	60000	
400K	64000	
416K	68000	
432K	6C000	OPTIONAL COMBO BOARD
448K	70000	READ/WRITE MEMORY
464K	74000	
480K	78000	
496K	7C000	
512K	80000	
528K	84000	
544K	88000	
560K	8C000	OPTIONAL COMBO BOARD
576K	90000	READ/WRITE MEMORY
592K	94000	
608K	98000	
642K	9C000	

640K	A0000	
656K	A4000	
672K	A8000	
688K	AC000	
704K	B0000	MONOCHROME DISPLAY BUFFER
720K	B4000	
736K	B8000	COLOR DISPLAY BUFFER
752K	BC000	
768K	C0000	
784K	C4000	
800K	C8000	HARD DISK CONTROL
816K	CC000	
832K	D0000	
848K	D4000	
864K	D8000	
880K	DC000	
896K	E0000	
912K	E4000	
928K	E8000	
944K	EC000	
960K	F0000	
976K	F4000	
992K	F8000	32 KB SYSTEM ROM
1.008M	FC000	

THE 8088 AND 8087 MICROPROCESSORS

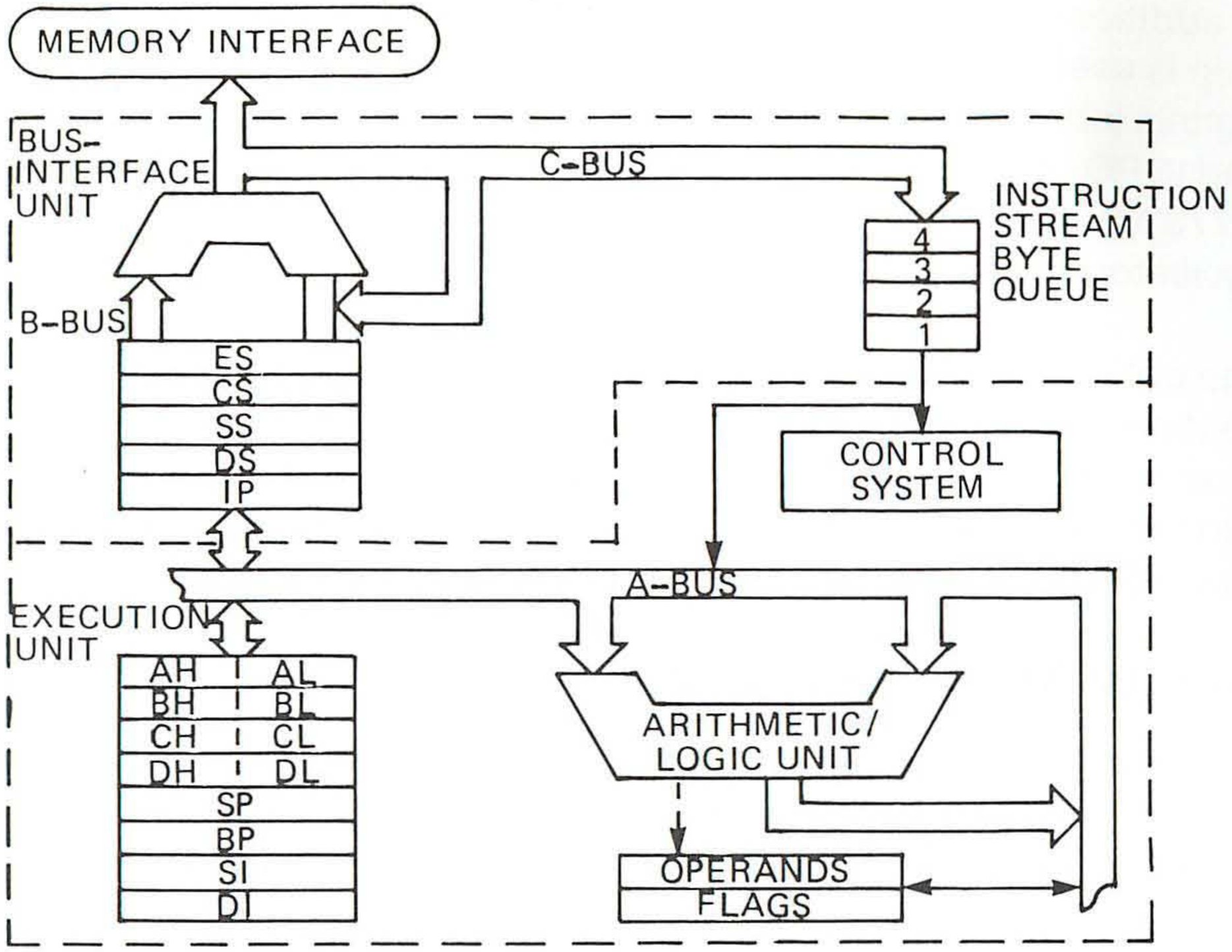
The Intel 8088 microprocessor directs activity on the motherboard. The 8088 uses a 16-bit internal architecture and instruction set and is capable of addressing one megabyte of memory via its twenty address lines. It communicates, however, through an 8-bit rather than a 16-bit external data bus. The first 8 of the 20 address lines are demultiplexed from the address/data signals. Another 8 address lines come directly out of the 8088 to a latch which redrives them onto the address bus. The last 4 address lines are demultiplexed from the address/status signals.

In addition to decoding the status lines, the 8288 bus controller chip is used to decode the 8088's QS1, QS2, TEST, and RQ/GT1 signals into the bus control signals AMWC, INTA, MRDC, AIOWC, and IORC. As the 8088 does not have an on-the-chip clock, the 4.773 MHz operating frequency is developed from a crystal oscillator and an 8284A clock chip.

The optional 8087 numeric data processor provides additional floating point power for the ITT XTRA Personal Computer. This processor monitors the instruction stream directed to the 8088 and executes those instructions it recognizes as its own. The 8087 adds 68 additional machine instructions to the system.

Internal Architecture of the 8088

The following figure illustrates the internal design of the 8088. As shown in the illustration, the processor is organized into two functional units: the execution unit and the bus interface unit.



Internal Architecture of the 8088

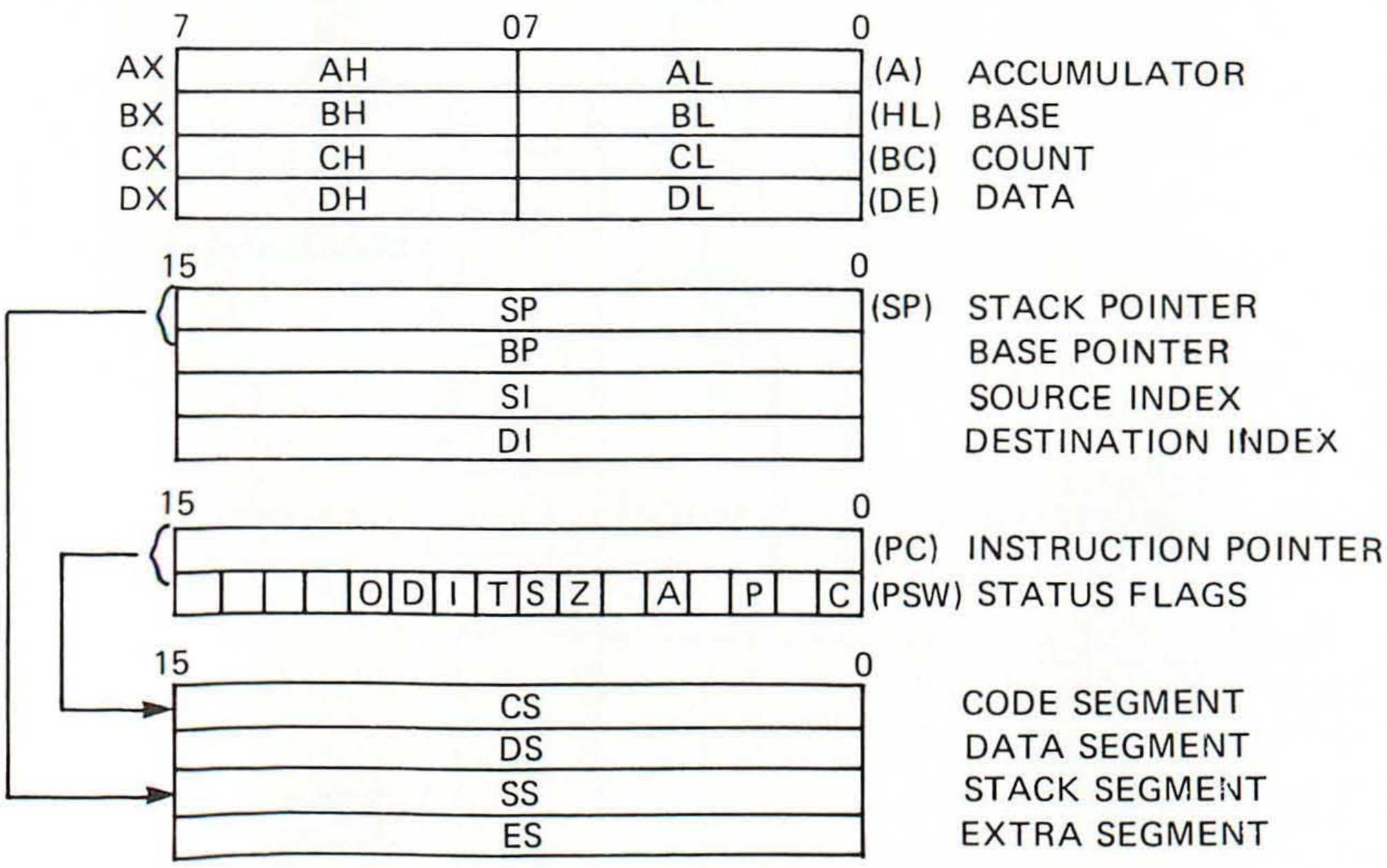
The execution unit contains the arithmetic and logic unit and the registers required to manipulate data, monitor the stack, and temporarily store data. It takes instructions from the bus interface unit, processes them, and issues operand addresses to the bus interface unit. It then processes the operands and returns them to the bus interface unit for storage in memory.

The bus interface unit allows the processor to operate faster by using the bus more efficiently. It fetches instructions before the execution unit needs them and stores them in a 4 byte instruction queue. When the execution unit is ready for the next instruction, it doesn't need to become involved in extensive memory fetches. The required bytes of information will already be in the instruction queue in the bus interface unit. By assuming responsibility for all fetch and storage operations, bus control, and memory relocation, the bus interface unit leaves the execution unit free to concentrate on processing data. The 8088's fourteen 16-bit registers are described in the following paragraph and illustrated in the subsequent figure.

The 8088 internal registers are divided into two groups that coincide with the operating functions of the processor. The two groups are the register file (execution unit) and the relocation register file (bus interface unit). The register file holds the data, pointer and index registers. The relocation register file contains the segment registers and the instruction pointer.

The accumulator (AX), base register (BX), count register (CX) and data register (DX) are the general registers. These registers are sometimes called the high low (HL) registers because they can be divided into high and low bytes.

The stack pointer (SP), the base pointer (BP), the source index (SI) and destination index (DI) can also be used as general registers. They, typically, are used to hold offset addresses when addressing within a general segment of memory. The stack pointer, for example, is used with the segment register (SS) to indicate the current stack location. The function of both the instruction pointer (PC) and the status flags (PSW) are evident within the names assigned.

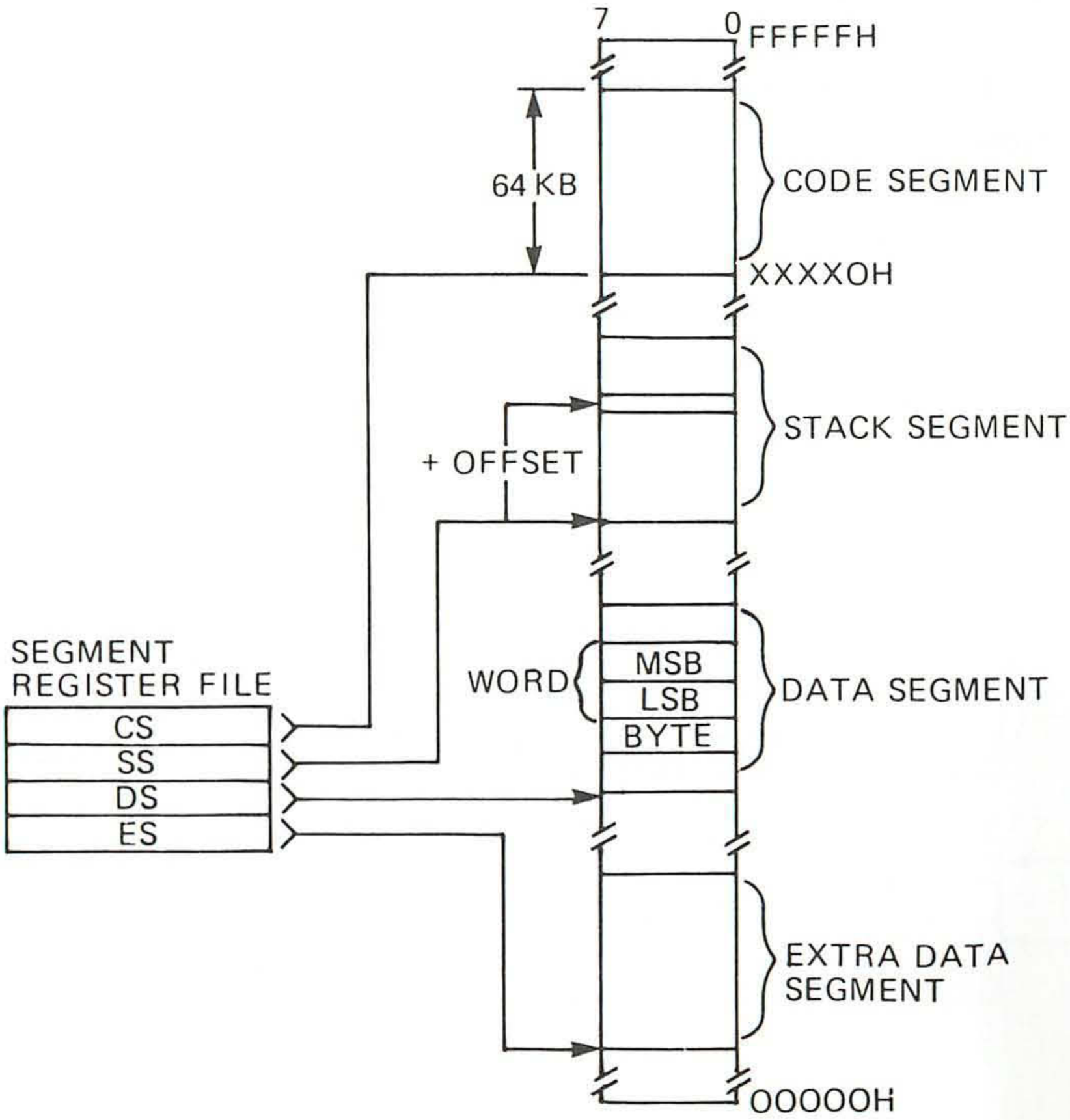


8088 Internal Registers

Memory Segmentation

The memory is logically divided into segments of up to 64K bytes each. Each of the segments will terminate on a 16-byte boundary. All memory references directly coincide with base addresses contained in high speed segment registers. The segment registers are named, from the highest address to the lowest address, code, stack, data and extra data (see Memory Segmentation in the 8088 illustration).

All 16-bit word operands will be located on either even or odd word boundaries. The address and data word operand least significant byte (LSB) is stored in the lower value address location and the most significant byte in the next higher address location. The bus interface unit will automatically perform the proper number of memory accesses to retrieve all data.



Memory Segmentation in the 8088

Memory Addressing

There are two major 8088 addressing concepts that should be understood. These concepts are (1) the formation of the address and (2) the available addressing modes.

An 8088 address is, in essence, a combination of two distinct addresses: the segment address and the effective, or offset, memory address. The segment addresses are pointed to by the segment registers which are acting as base registers. The segment registers can point to any memory location lying within an address boundary that is an even multiple of 16 bytes.

Each address is developed by summing the segment register contents with the effective memory address. Each addressed instruction relates directly to one defined memory area set off by segment registers (see the Memory Addressing figure). The selected segment register, containing the addressed instruction, is then left-shifted four bits and added to the effective memory address to generate the actual memory address. This addressing scheme allows the direct addressing of 1,048,576 external bytes of memory.

No restrictions are placed on the segment register contents. The segment registers do not have to specify overlapping memory locations or be divided into 64K pages. Each segment register will identify any 64K byte memory segment in memory as well as provide the possibility of overlapping one or more segments within memory.

Memory Addressing Modes

An instruction memory address location is developed from the program counter (PC register) and a segment from the CS register. The program counter contents, used to develop the instructions, are normally incremented as the instructions are executed. Jump or Call instructions may modify the program contents in any one of three ways. The modifications are:

Program relative addressing
Direct addressing
Indirect addressing

program relative addressing is an 8-bit or 16-bit immediate data displacement, provided by the instruction, and added to the program counter as a signed number. This intersegment operation will not alter the contents of the CS register.

Direct Addressing is the immediate load of 16-bit addresses' data into both the program counter and CS register. This addressing mode is called an intersegment operation.

Indirect Addressing uses two options to complete operations. First, a single 16-bit word will be read into the program counter. The next Jump or Call will use the word in the program counter to reference a memory location in the current CS segment.

The second form of Indirect Addressing is similar to the first option. A single 16-bit word will be read into the program counter. The next Jump or Call instruction will use the word in the program counter to reference a memory location in the current CS segment. The CS segment memory location is read and directs you to the final memory location.

Data Memory Addressing

There are six modes of data memory addressing. They are (1) Immediate; (2) Direct; (3) Direct, Indexed; (4) Implied; (5) Base Relative; and (6) Stack.

Immediate addressing includes an operand immediately following the instruction object code (opcode).

Direct addressing will add a 16-bit displacement, from the two object code bytes, to the Data Segment register. The sum then becomes the actual memory address.

Direct, Indexed addressing will specify that either the Source Index (SI) or Destination Index (DI) register will be the primary index register. Once the primary index register is established, you will have the option of either adding an 8-bit or 16-bit displacement to the contents of the specified primary index register to generate the effective address.

The 8-bit or 16-bit displacements are taken from object code bytes. The 16-bit displacement is stored in two object code bytes. The displacement order places the low-order byte before the high-order byte exactly as required for direct addressing.

The 8-bit displacement requires the high-order bit of the low-order byte to be placed in the high-order byte to create a 16-bit displacement.

Implied Memory addressing is almost identical to Direct Indexed addressing. The only deviation to the Direct Indexed form is the omission of any displacement value. The omission of a displacement value, therefore, implies an address in the designated primary index register.

Data memory Base Relative addressing, within the DS segment, uses the contents of the BX register to develop the effective memory address. These contents are added to the contents of a selected index register to form the effective memory address.

Data memory addressing options, except immediate addressing, can use the base relative addressing options. For example, Direct addressing will always generate a 16-bit displacement. Base relative addressing will take the displacement and allow it to be the 16-bit displacement, an 8-bit displacement or no displacement at all.

Base Relative Implied addressing will add the BX register contents to the contents of the selected index register to form the effective memory address.

Base Relative Direct Indexed data memory addressing adds the BX register contents to the effective memory address similar to Direct Indexed addressing.

Stack Memory addressing is a variation of Base Relative addressing. The BP register contents are used to establish the effective memory address.

BUS STRUCTURE

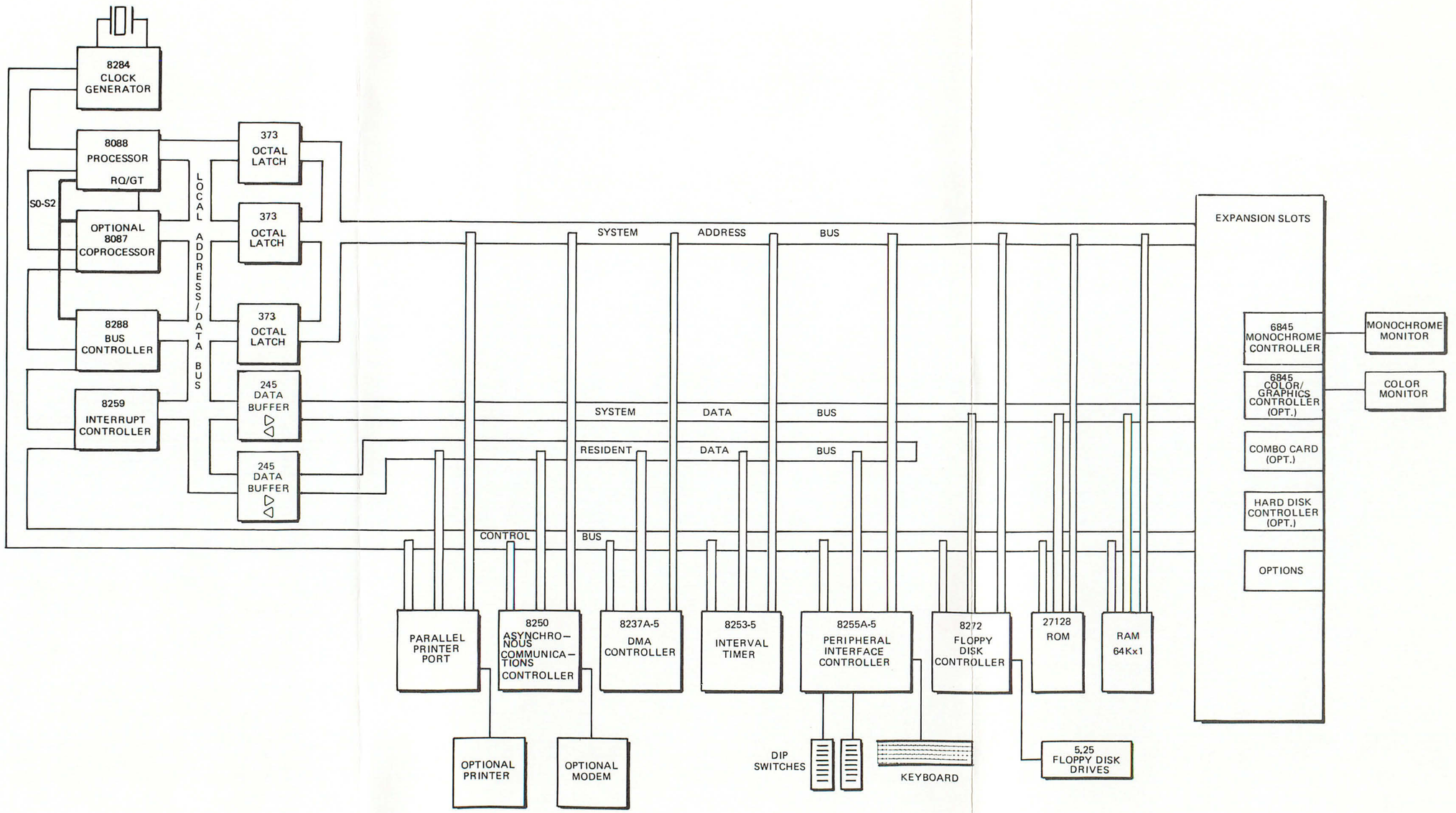
When the 8087 chip is installed, it communicates with the 8088 over a local data/address bus. The 8087 requests use of the bus from the 8088 by using its request (RQ) and grant (GT) arbitration lines. Although the 8088 acts as the master processor, either chip can control the local bus.

The local bus comprises eight multiplexed address and data lines (AD0 - AD7), twelve address lines (A8 - A19), and three status and control lines (S0 - S2). The 8288 bus controller, three 74LS373 octal address latches, and two 74LS245 data transceivers are used to connect the local bus shared by the 8088 and optional 8087 to the system bus and resident bus. The system bus is composed of three subbuses - the control bus, the address bus, and the data bus. The interconnection of the 8088 processor and the local bus to the system bus is shown on the following page

The control bus is composed of a variety of system bus arbitration and bus cycle control lines, clock signals, and interrupt request and DMA request/acknowledge lines.

The system data bus drives the on-board ROM and RAM, the 8272 floppy disk controller, and the five 62-pin I/O expansion slot connectors. All option boards manufactured by ITT will operate in any one of the five I/O expansion slots. The monochrome display controller board, with its 6845 video controller, is normally mounted in slot 5 of the I/O expansion backplane.

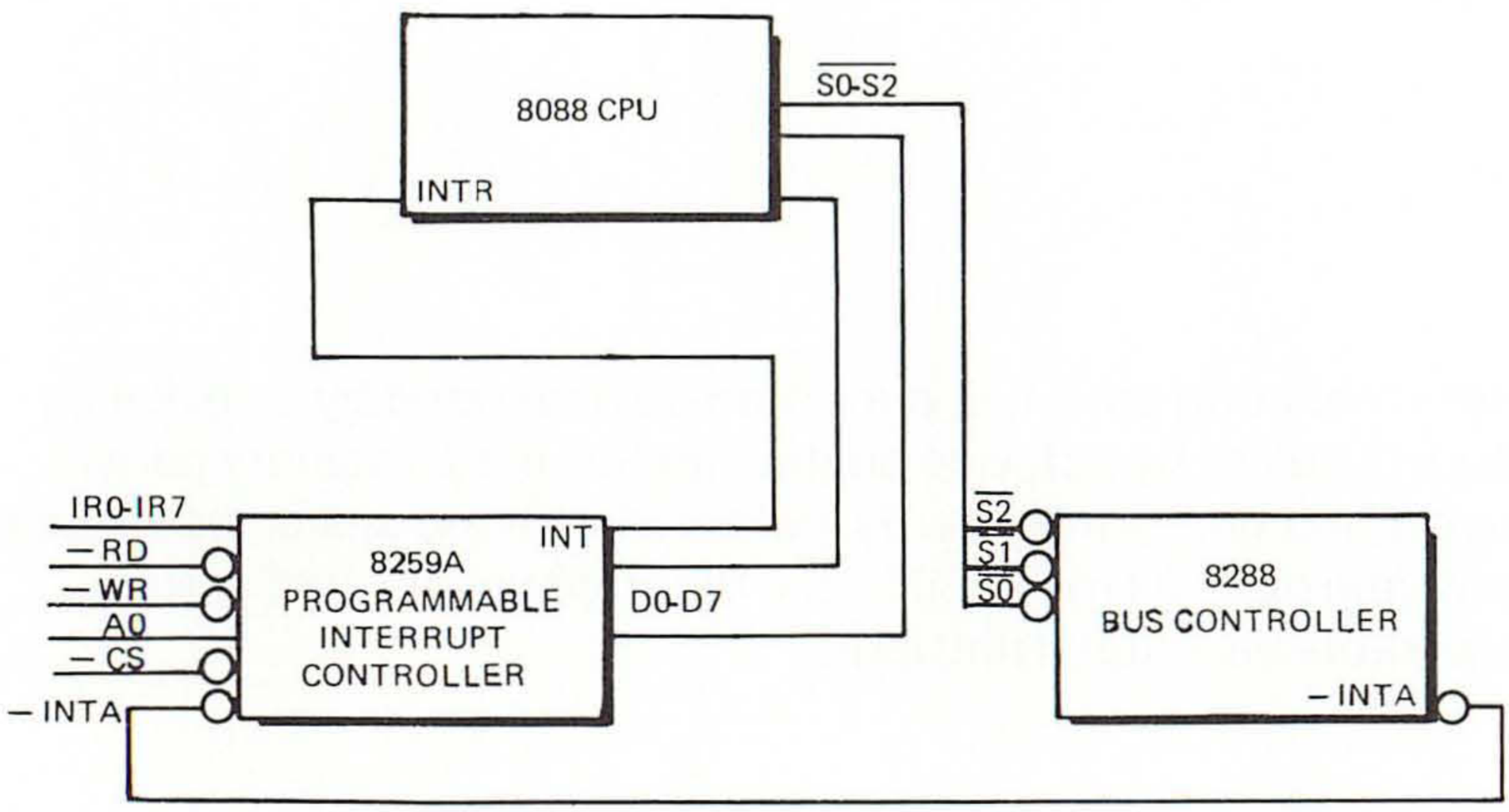
The resident data bus drives the on-board device controller chips (e.g., 8237A-5 programmable DMA controller, 8255A-5 parallel peripheral interface controller, 8253-5 timer controller, and the 8250 asynchronous communications interface chip). These chips control the system's external devices such as the keyboard and printer.



8088 Processor and Support Chip Interconnection

8259A PROGRAMMABLE INTERRUPT CONTROLLER

The 8259A programmable interrupt controller provides eight prioritized levels of interrupts (interrupt 0 has the highest priority). The interrupt system frees the 8088 from the task of constantly polling I/O devices to determine if they require servicing. Under the interrupt scheme, the 8088 need only attend to I/O devices after being notified by an interrupt that a device is ready to be serviced. The following figure illustrates the major 8259A signal lines.



All of the system's interrupt driven peripheral devices, located on the motherboard or in the I/O expansion backplane, are connected via interrupt request lines to the 8259A programmable interrupt controller. Interrupt assignments are listed in the following table.

8259A INTERRUPT ASSIGNMENTS

INTERRUPT	DESCRIPTION
Interrupt 0	Timer interrupt
Interrupt 1	Keyboard data ready
Interrupt 2	I/O bus
Interrupt 3	I/O bus
Interrupt 4	I/O bus or a synchronous communications port (primary)
Interrupt 5	I/O bus
Interrupt 6	I/O bus or floppy drives
Interrupt 7	I/O bus or parallel printer port

Note that interrupts 4, 6, and 7 can be generated by a device on the I/O bus or by a device on the motherboard. Memory parity errors, I/O errors from cards installed in the expansion backplane, and interrupts from the 8087 are reported via the 8088's Non-Maskable Interrupt (NMI) logic.

8259A Functional Description

When the 8259A programmable interrupt controller receives an interrupt request, it first evaluates the request. If the request is not masked, and is of the highest priority of all presently existing interrupts, the 8259A sends an INT to the 8088's INTR input. The 8088 then goes into an interrupt acknowledge sequence. It finishes execution of the current instruction, preserves the contents of the flag registers, the CS register, and the IP register by pushing them on to the stack, and clears the interrupt flag to prevent additional interrupts from occurring. The 8288 bus controller then signals the 8259A interrupt controller via the -INTA line that the interrupt request has been granted. A second pulse on the -INTA line causes the 8259A to place the interrupt type on the data bus. The 8088 multiplies the value of the interrupt type by four. The result provides the address of the device's interrupt vector.

A table of all of the system's interrupt vectors is located at the low end of system memory (00000 to 003FF). Each interrupt vector is composed of four bytes that indicate the address of the appropriate interrupt service routine. Before jumping to the interrupt vector, the system saves the current program address on the stack and disables its interrupt. The address of the service routine is then placed in registers CS and IP, the 8088's program address registers. The computer then runs the interrupt service routine. When the service routine is completed, the 8088 pops the stack, reenables its interrupts, and returns control to the program that was running when the interrupt occurred.

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during -INTA pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8088 input levels.

-INTA (INTERRUPT ACKNOWLDEGE)

-INTA pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (uPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

-CS (CHIP SELECT)

A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

-WR (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

-RD (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the Data Bus.

AO

This input signal is used in conjunction with -WR and -RD signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the ID's of all 8259's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CASO-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive -INTA pulses.

Programming the 8259A

The 8259A accepts two types of command words generated by the 8088:

1. Initialization Command Words (ICWs): Before normal operation can begin, each 8259A in the system must be brought to a starting point by a sequence of 2 to 4 bytes timed by -WR pulses.

2. Operation Command Words (OCWs): These are the command words which command the 8259A to operate in various interrupt modes. These modes are:

   Fully nested mode
   Rotating priority mode
   Special mask mode
   Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.

b. The Interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

d. The slave mode address is set to 7.

e. Special Mask Mode is cleared and Status Read is set to IRR

f. If IC4 = 0, then all functions selected in ICW4 are set to zero.

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1,ICW2)

A5 - A15: Page starting address of service routines. A15 - A11 are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A10 - A5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; AD1 = 0 then interval = 8

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set - ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will enable the corresponding slave to release byte 2 through the cascade lines.

b. In the slave mode (either when -SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, byte 2 of the call sequence is released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode, -SP/-EN becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

uPM: Microprocessor mode: uPM = 1 sets the 8259A for 8088 operation.

OPERATION COMMAND WORDS (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

0	R	SL	EOI	0	0	L2	L1	L0

OCW3

0	0	ESMM	SMM	0	1	P	RR	RIS

OPERATION CONTROL WORD 1 (OCW1)
OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR). M7 - M0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited); M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)
R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L2,L1,L0 - These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)
ESMM - Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0, the SMM bit becomes a “don’t care.”

SMM - Special Mask Mode. If ESMM = 1 and SMM = 1, the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the 8088 issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the 8088 internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IRO has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence -INTA pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: specific and nonspecific. When the 8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a nonspecific EOI command is issued, the 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A nonspecific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0 - L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a nonspecific EOI if the 8259A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 8259A will automatically perform a nonspecific EOI operation at the trailing edge of the last interrupt acknowledge pulse (second pulse). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

The AEOI mode can only be used in a master 8259A and not a slave.

AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait in the worst case until each of seven other devices are serviced at most once.

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

SPECIFIC ROTATION (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; L0 - L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and L0 - L2 = IR level to receive bottom priority).

INTERRUPT MASK

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels' operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

POLL COMMAND

In this mode the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = 1 in OCW3. The 8259A treats the next -RD pulse to the 8259A (i.e., -RD = 0, -CS = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from -WR to -RD.

The word enabled onto the data bus during -RD is:

D7	D6	D5	D4	D3	D2	D1	D0
I	--	--	--	--	W2	W1	W0

W0 - W2: Binary code of the highest priority level requesting service

1: Equal to a 1 if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the -INTA sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0).

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A remembers whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever -RD is active and A0 = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = 0, an interrupt request will be recognized by a high level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for clean up simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes, a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a nonspecific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a nonspecific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on -SP/-EN to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the -SP/-EN output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the -INTA sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during byte 2 of INTA.

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs; no slave inputs leave the cascade line inactive (low).

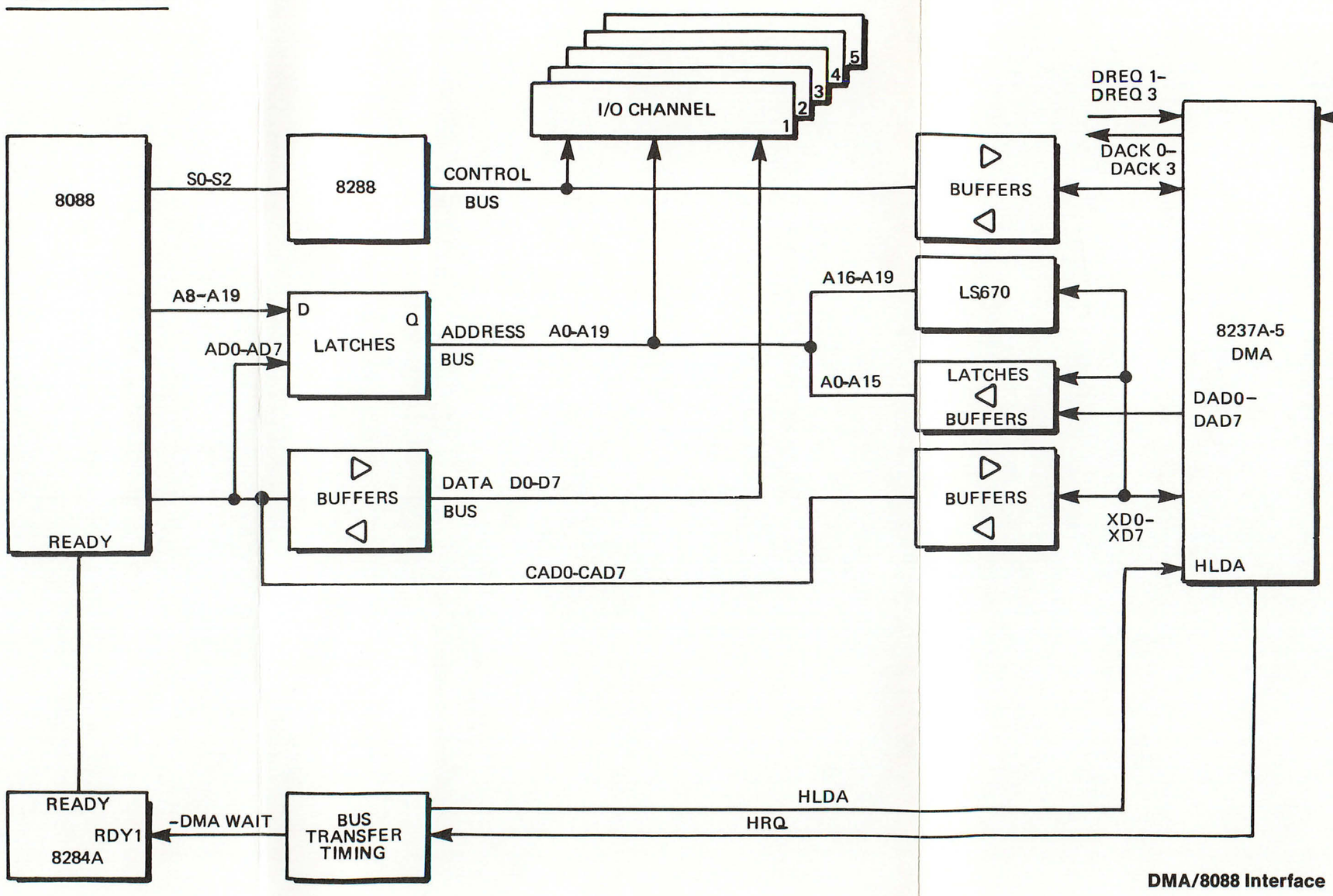
8237A-5 PROGRAMMABLE DMA CONTROLLER

The DMA controller provides direct access to memory for the system's peripheral devices without intervention by the 8088. By allowing these direct transfers, the 8237A-5 substantially improves system performance.

Operational Overview

As shown in the DMA 8088 interface illustration, whenever the DMA controller is given access to the system bus, the bus arbitration circuitry isolates the local bus from the system bus by disabling the address latches and data transceivers that interface the local and system buses (see the following figure). The DMA controller requests control of the bus by issuing a Hold Request (HRQ). If the 8088 is in the process of executing an instruction or is in the midst of an interrupt acknowledge sequence, the status will remain active until the sequence is complete. This prevents the DMA controller from gaining control of the system bus while the 8088 still requires access to the bus. When -LOCK goes inactive the 8088 is in its idle state at the end of a bus cycle, the DMA controller receives a hold acknowledge signal (HLDA), granting it access to the bus. The 8284A clock generator, via the RDY1 line, is used to place the 8088 into a continuous wait state which will keep the local bus isolated from the system bus until the DMA request has been completed.

DMA INTERFACE



DMA/8088 Interface

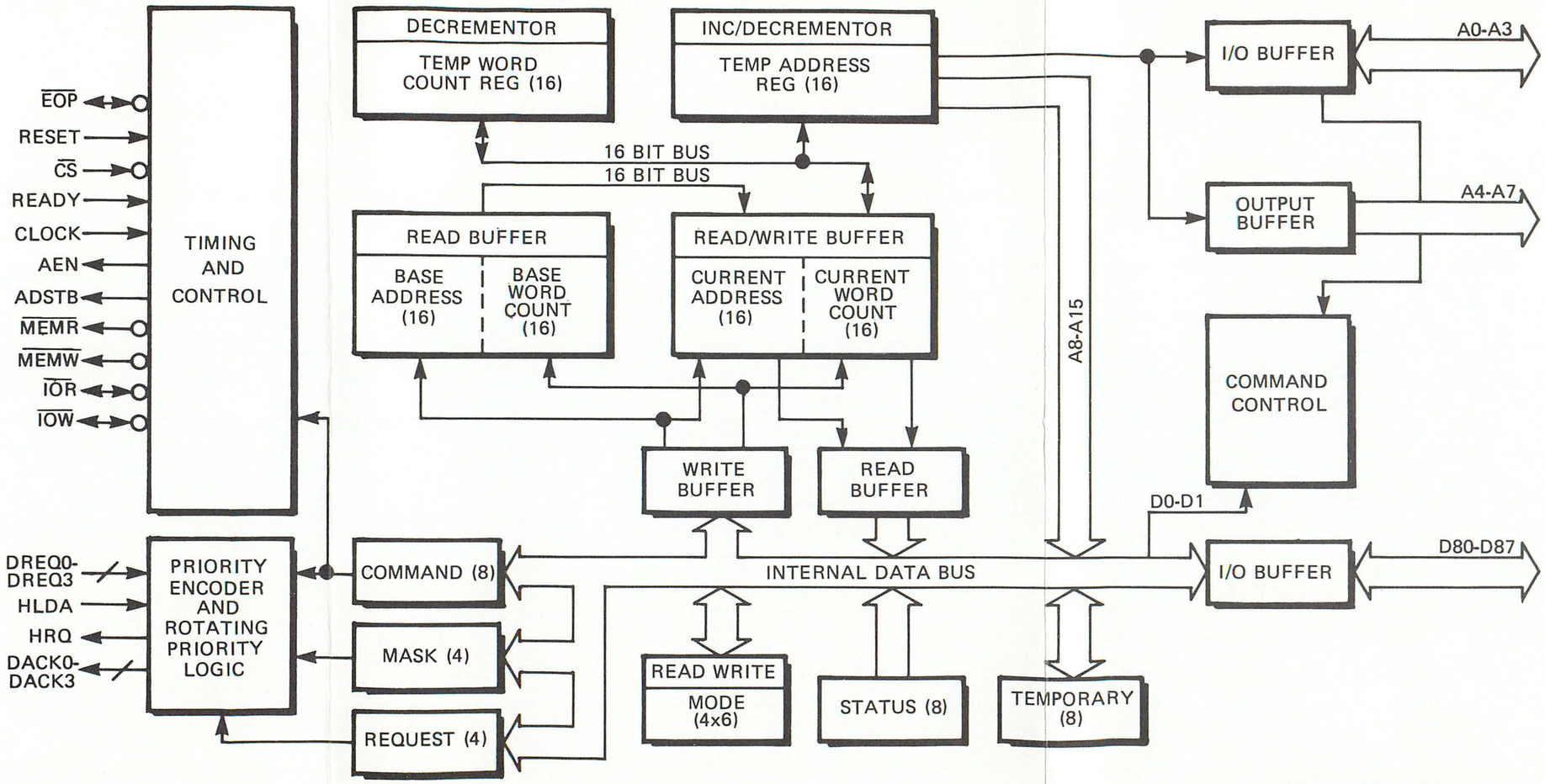
Two of the four 20-bit DMA channels support high speed transfers between memory and the I/O BUS. A third channel is available to the I/O bus or to the floppy drives. The fourth channel is used to implement a memory refresh scheme. Under this scheme a dummy DMA transfer is requested every 15 microseconds via the 8253-5 interval timer, triggering a memory read cycle that refreshes dynamic memory on the motherboard and on any board installed in one of the expansion slots. A memory refresh requires four clock cycles; DMA data transfers require five clock cycles. Specific channel assignments are as listed in the table below:

DMA CHANNEL ASSIGNMENTS

CHANNEL	FUNCTION
Channel 0	Memory Refresh
Channel 1	I/O Bus
Channel 2	I/O Bus and Floppy Drives
Channel 3	I/O Bus

8237A-5 DMA Controller Internal Description

The 8237A-5 major logic blocks, internal registers, and data interconnection paths are shown in the following block diagram.



8237A-5 Block Diagram

As shown in the block diagram, the 8237A-5 contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 8237A-5. The Command Control block decodes the various commands given to the 8237A-5 by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the 8284A's CLK signal.

8237A Detailed Functional Description

The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 8237A can assume seven separate states, each composed of one full clock period. State I (SI) is the inactive state. It is entered when the 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 8237A has requested a hold but the processor has not yet returned an acknowledge. The 8237A-5 may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3, and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 8237A. Note that the data is transferred directly from the I/O device to memory (or vice versa) with -IOR and -MEMW (or -MEMR and -IOW) being active at the same time. The data is not read into or driven out of the 8237A-5 in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

IDLE CYCLE

When no channel is requesting service, the 8237A-5 will enter the Idle cycle and perform SI states. In this cycle the 8237A-5 will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample -CS, looking for an attempt by the microprocessor to write or read the internal registers of the 8237A-5. When -CS is low and HLDA is low, the 8237A-5 enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The -IOR and -IOW lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 8237A-5 in the Program Condition. These commands are decoded as sets of addresses with the -CS and -IOW. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-Flop and Master Clear.

ACTIVE CYCLE

When the 8237A is in the Idle cycle and a non-masked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode - In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer.

When the word count rolls over from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, ensuring one full machine cycle execution between DMA transfers.

Block Transfer Mode - In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, called by word count going to FFFFH, or an external End of Process (-EOP) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode - In Demand Transfer mode the device is programmed to continue making transfers until a TC or external -EOP is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 8237A-5 Current Address and Current Word Count registers. Only an -EOP can cause an Autoinitialize at the end of the service. -EOP is generated either by TC or by an external signal.

Cascade Mode - This mode is used to cascade more than one 8237A-5 together for simple system expansion. The HRQ and HLDA signals from the additional 8237A are connected to the DREQ and DACK signals of a channel of the initial 8237A-5. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 8237A-5 is used only for prioritizing the additional device, it does not output any address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The 8237A-5 will respond to DREQ and DACK but all other outputs except HRQ will be disabled.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write, and Verify. Write transfers move data from an I/O device to the memory by activating -MEMW and -IOR. Read transfers move data from memory to an I/O device by activating -MEMR and -IOW. Verify transfers are pseudo transfers. The 8237A operates as in Read or Write transfers generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. Verify mode is not permitted during memory to memory operation.

Memory-to-Memory - To perform block moves of data from one memory address space to another with a minimum of program effort and time, the 8237A-5 includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The 8237A-5 requests a DMA service in the normal manner. After HLDA is true, the device, using eight-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 8237A-5 internal Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an -EOP output terminating the service.

Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

The 8237A-5 will respond to external -EOP signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Autoinitialize - By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following -EOP. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

Priority - The 8237A-5 has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing - In order to achieve even greater throughput where system characteristics permit, the 8237A-5 can compress the transfer time to two clock cycles. State 3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation).

Address Generation - In order to reduce pin count, the 8237A-5 multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 8237A directly. Lines A0-A7 should be connected to the address bus.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 8237A executes S1 states only when updating A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

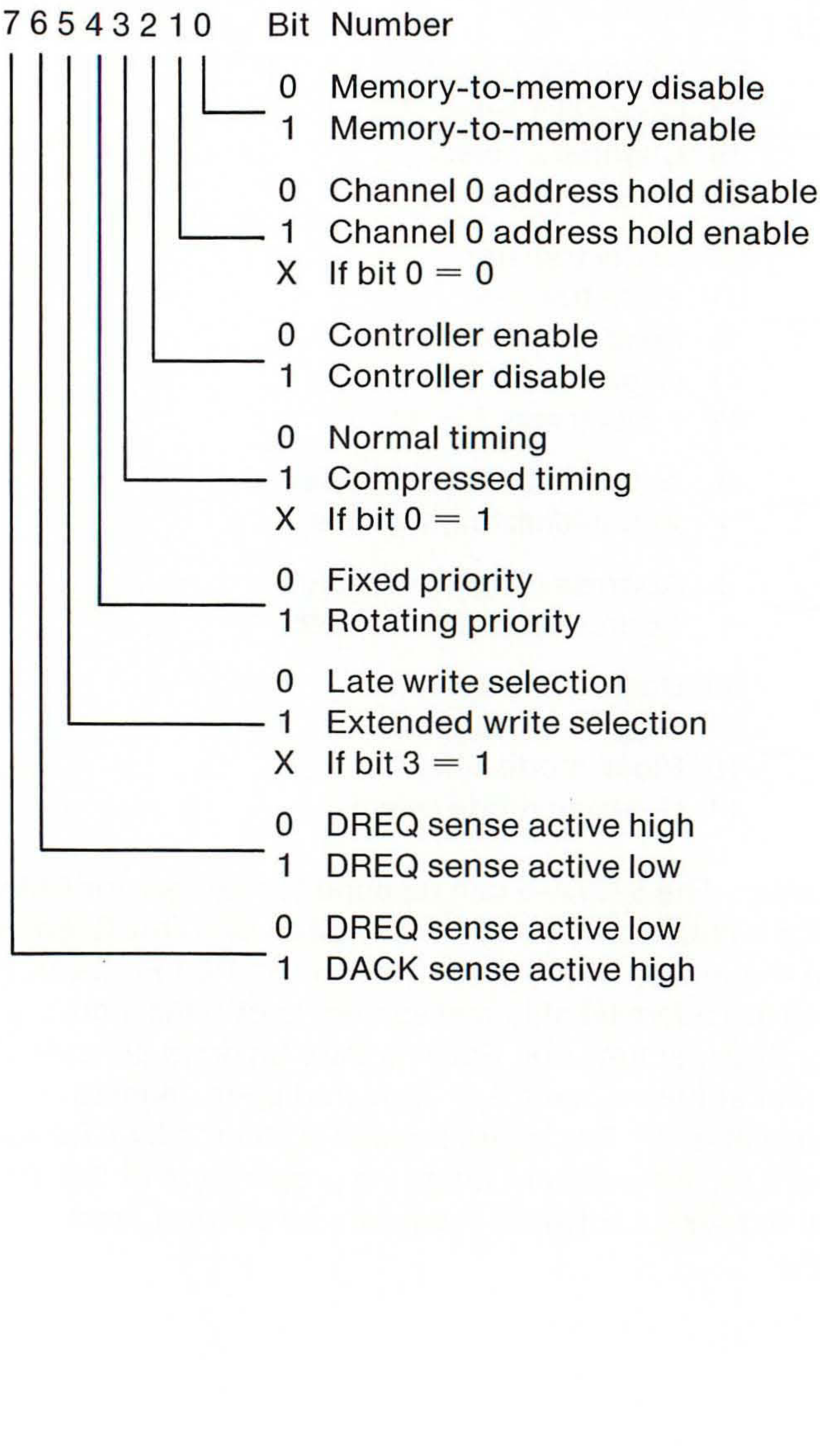
Register Description

Current Address Register - Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an -EOP.

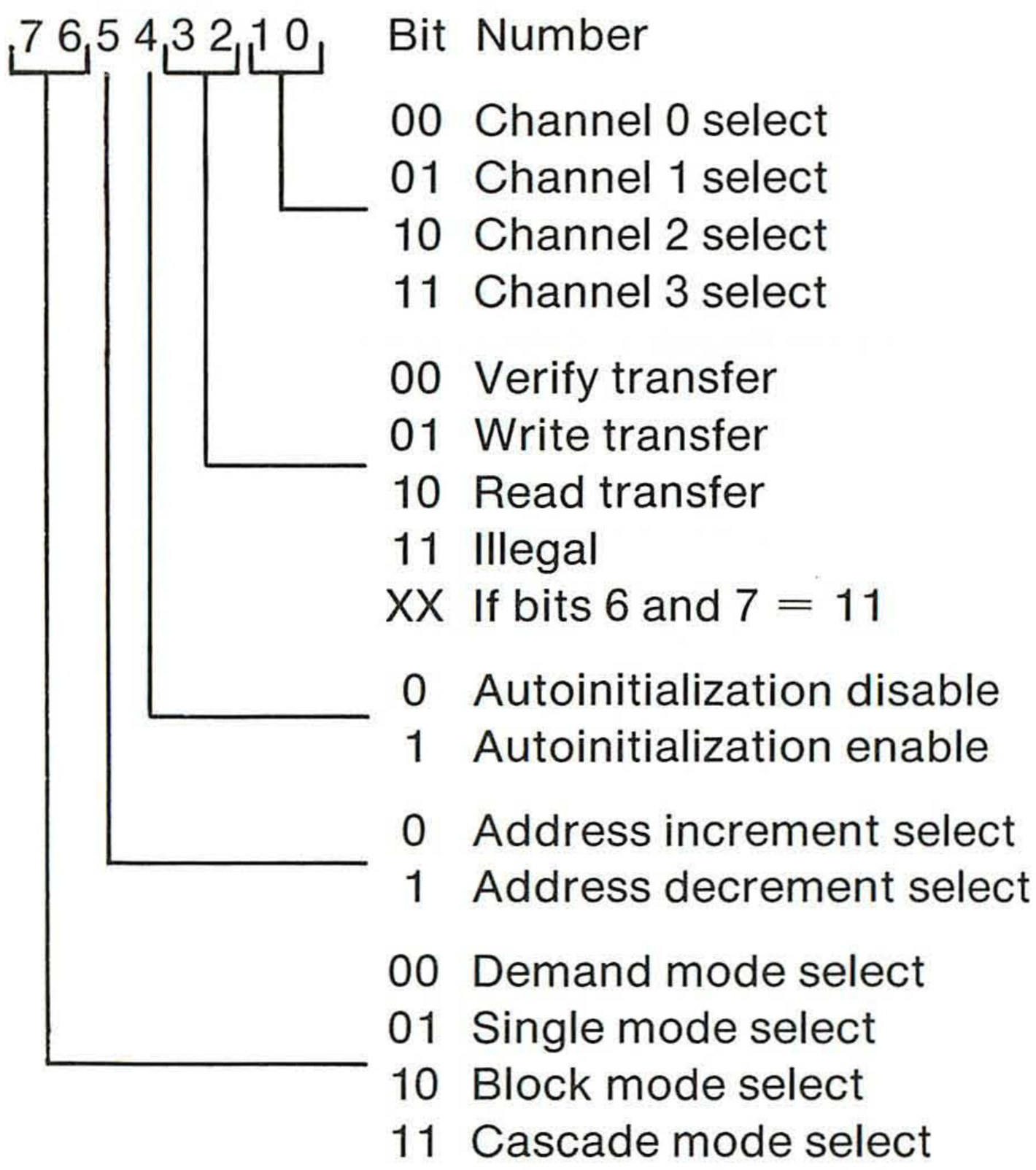
Current Word Register - Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an -EOP occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address And Base Word Count Registers - Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an -EOP.

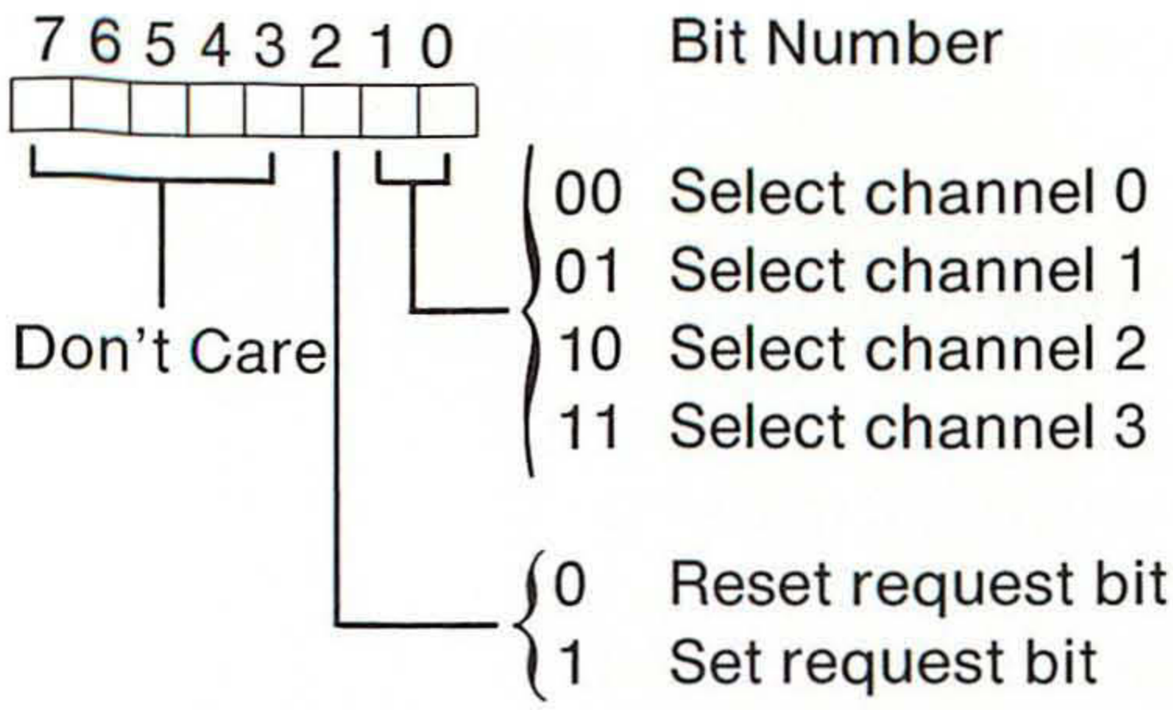
Command Register - This 8-bit register controls the operation of the 8237A-5. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits.



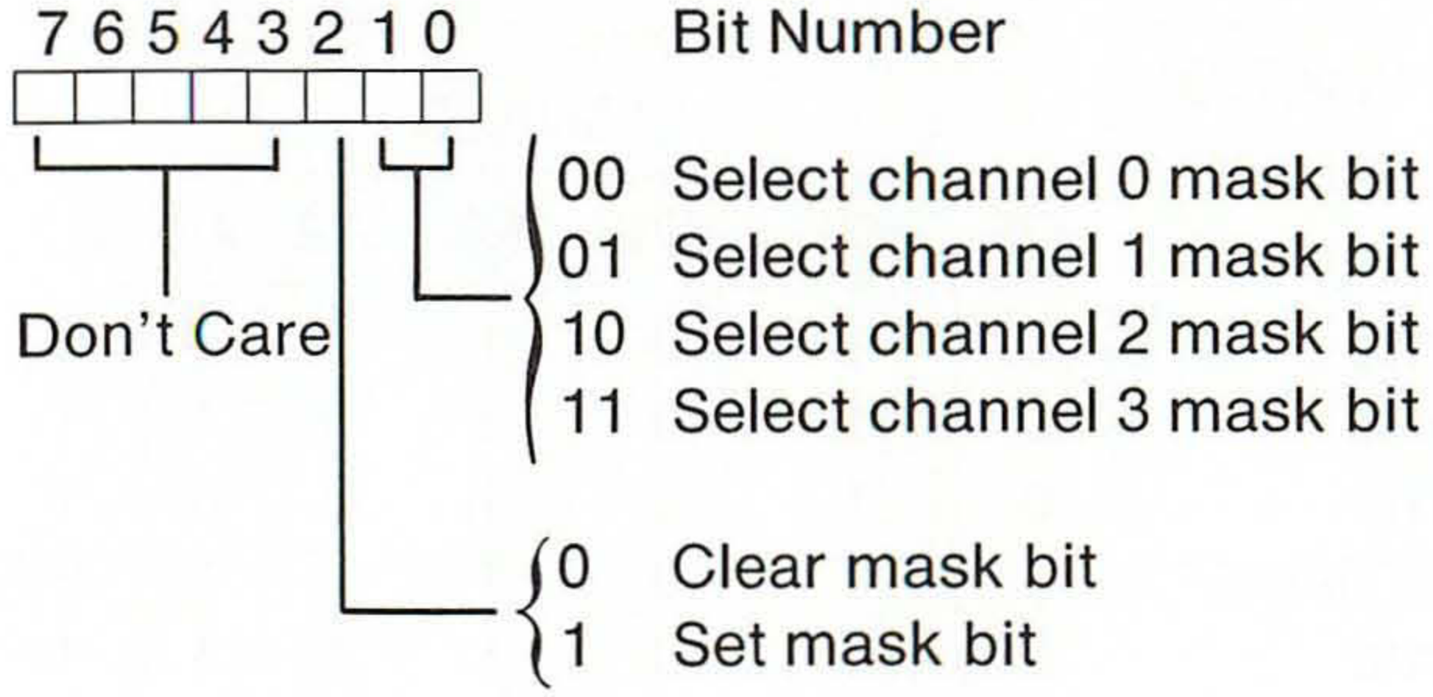
Mode Register - Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.



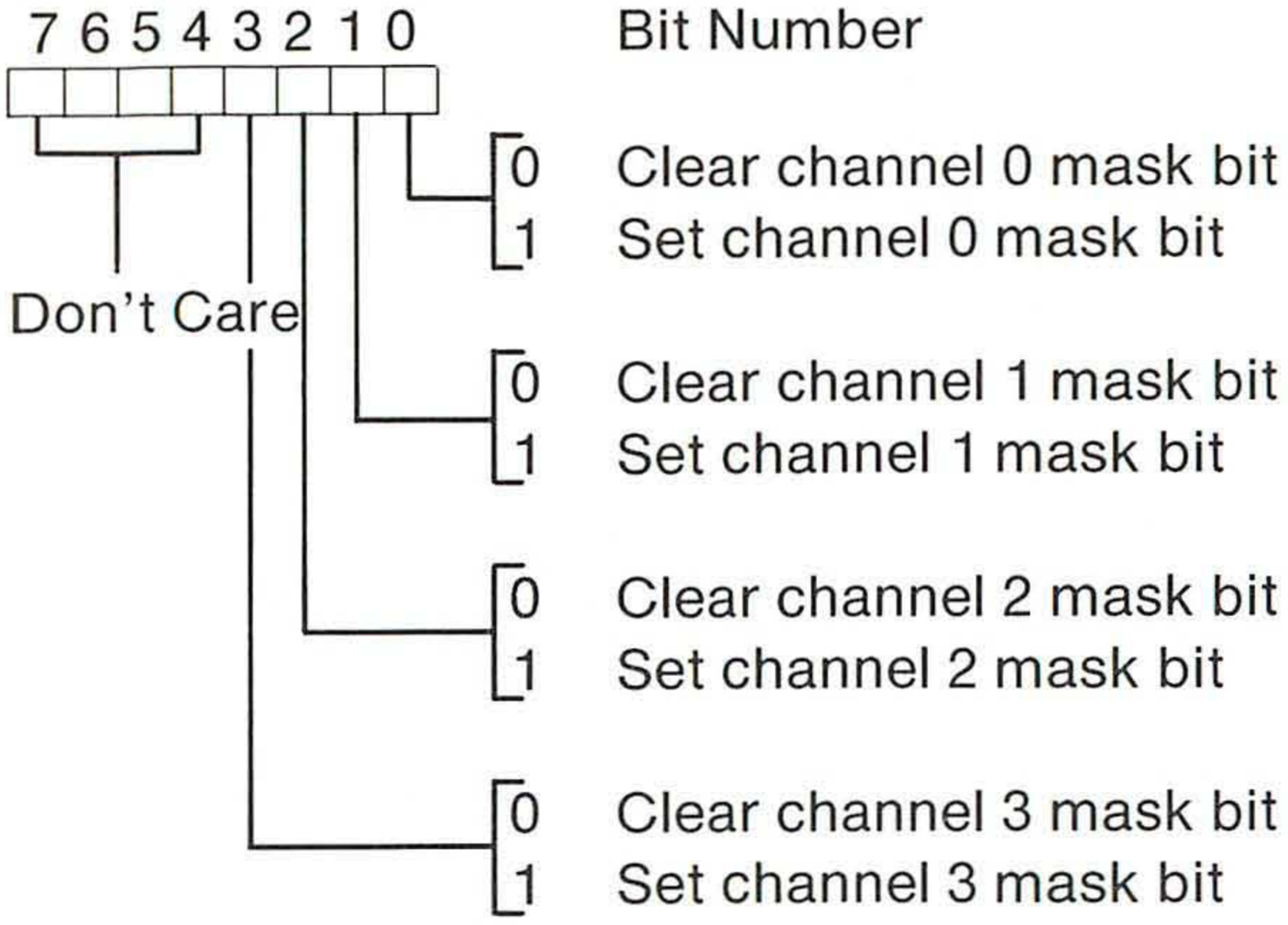
Request Register - The 8237A-5 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external -EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. In order to make a software resquest, the channel must be in Block Mode.



Mask Register - Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an -EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register.



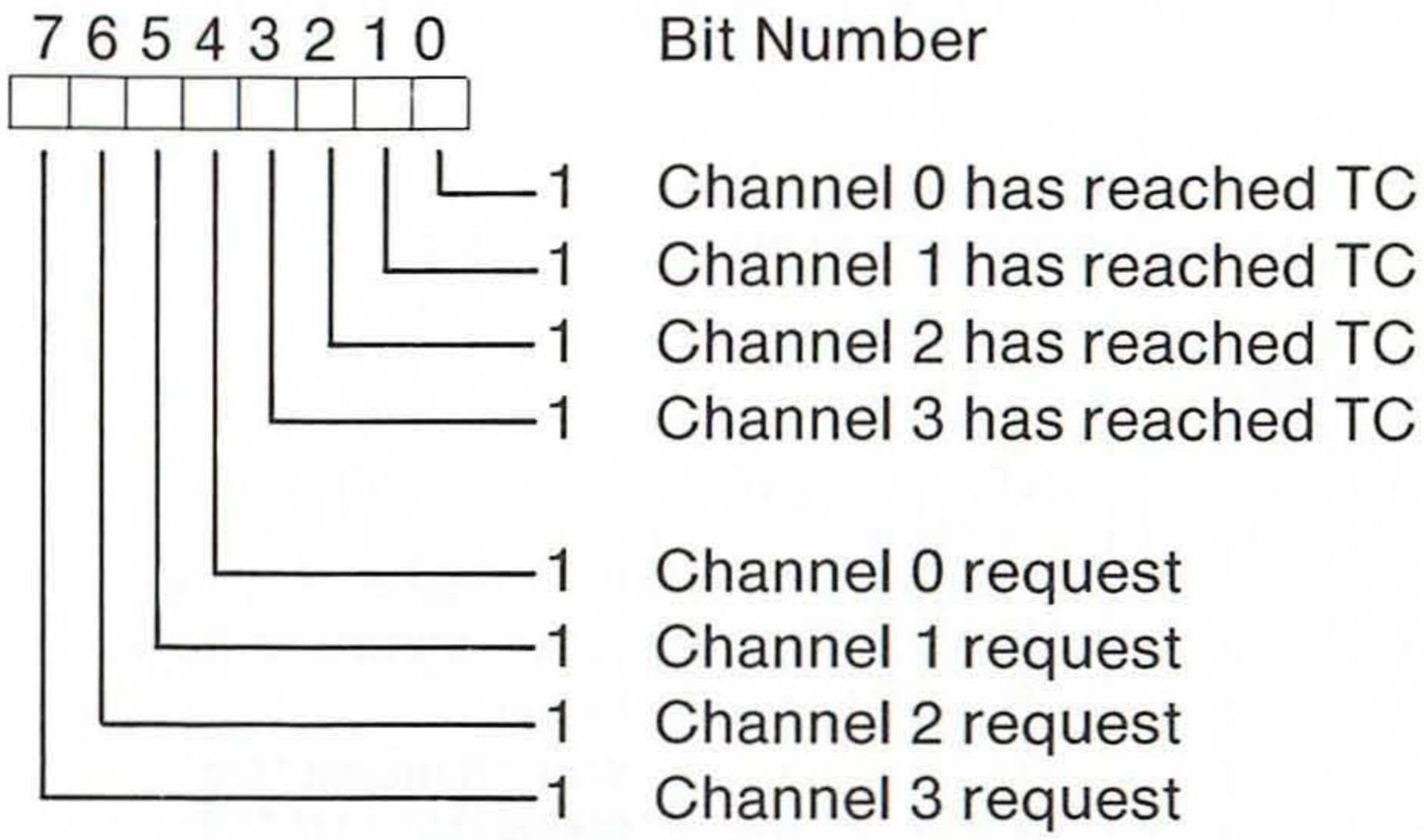
All four bits of the Mask register may also be written with a single command.



Definition of Register Codes

REGISTER	OPERATION	SIGNALS						
		-CS	-IOR	-IOW	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Status Register - The Status register is available to be read out of the 8237A-5 by the 8088. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0 - 3 are set every time a TC is reached by that channel or an external -EOP is applied. These bits are cleared upon Reset and on each Status Read. Bits 4 - 7 are set whenever their corresponding channel is requesting service.



Temporary Register - The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the 8088 in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands - These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two softare commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 8237A-5. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 8237A will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

The following table lists the address codes for the software commands:

SOFTWARE COMMAND ADDRESS CODES

Signals						
A3	A2	A1	A0	-I0R	-IOW	OPERATION
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Programming The 8237A-5

The 8237A-5 will accept programming from the 8088 any time that HLDA is inactive; this is true even if HRQ ia active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the 8237A-5 is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 8237A-5 is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

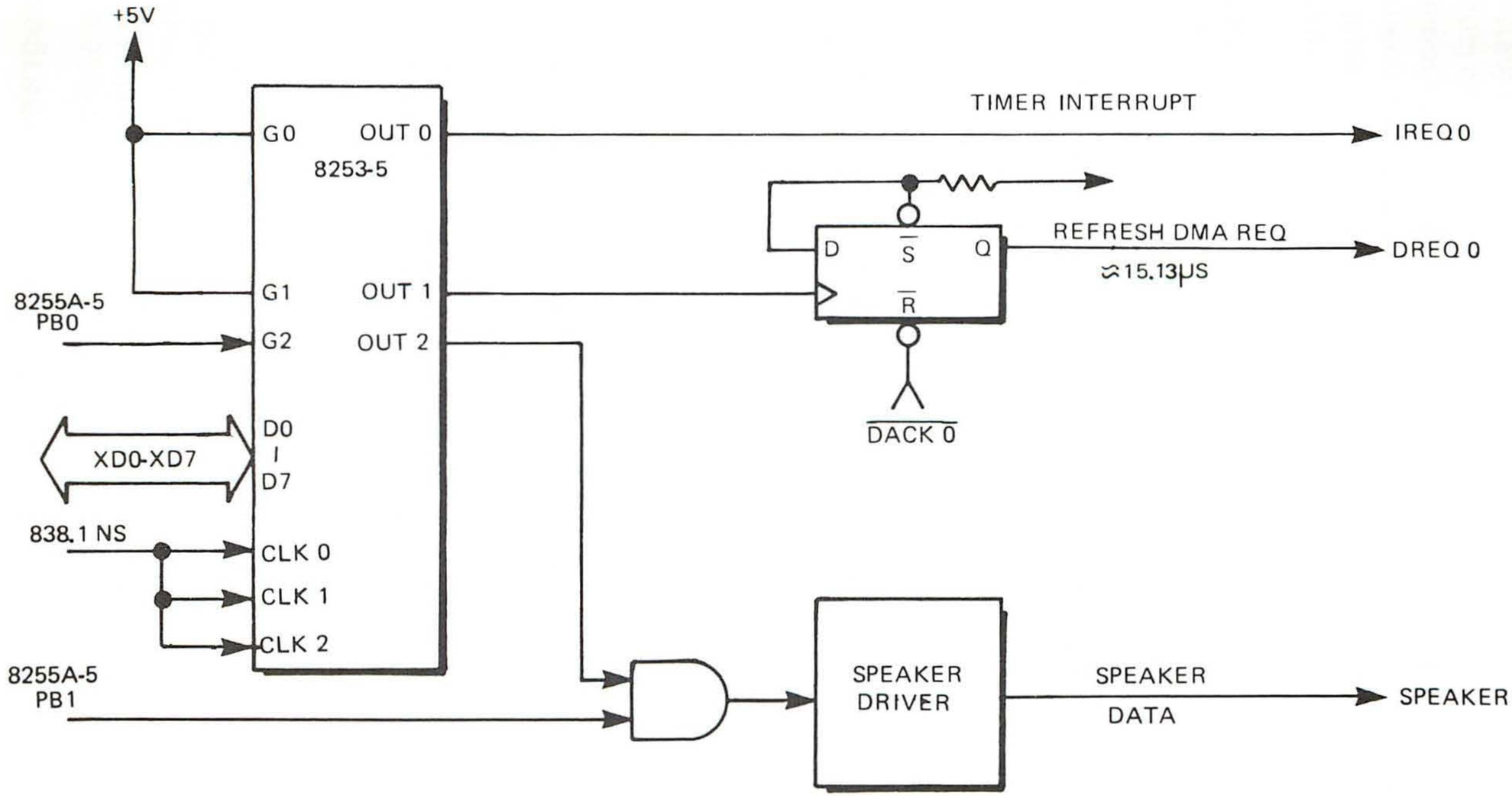
After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

8253-5 PROGRAMMABLE INTERVAL TIMER

The 8253-5 timer controller provides a 1.193 Mhz clock input to three 16-bit timer counter channels. Each of these timers can be initialized with a specific value that represents the length of a desired delay. The 8253-5 can then be commanded to count out the delay. At the conclusion of the count, the 8253-5 can issue an interrupt or otherwise trigger a desired event. This arrangement allows the system to generate accurate time delays without creating the overhead that timing loops in system software would generate.

Timer 0 (OUT 0) is the system's general purpose timer. It connects to Interrupt Request 0 and can be used for an internal clock. Timer 1 connects to DMA Request 0 and is used in the dynamic memory refreshing scheme. Timer 2 is used to develop the audio signal used to drive the speaker. A simplified block diagram of the interval timer circuit is shown in the following figure.

INTERVAL TIMER



8253-5 Interval Timer

Functional Overview Of The 8253-5

DATA BUS BUFFER

A 3-state, bi-directional, 8-bit buffer is used to interface the 8253-5 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253-5.
2. Loading the count registers.
3. Reading the count values.

READ/WRITE LOGIC

The Read/Write Logic accepts inputs from the sytem bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

-RD (READ)

A low on this input informs the 8253-5 that the CPU is inputting data in the form of a counter's value.

-WR (WRITE)

A low on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0,A1

These inputs are connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

-CS (CHIP SELECT)

A low on this input enables the 8253. No reading or writing will occur unless the device is selected. The -CS input has no effect upon the actual operation of the counters.

CONTROL WORD REGISTER

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in the register controls the operational MODE of each counter, selection of binary or BCD counting, and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

COUNTER #0, COUNTER #1, COUNTER #2

These three functional blocks are identical in operation so only a single counter will be described. Each counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent, and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications. In addition, special commands and logic are included in the 8253-5 so that the contents of each counter can be read “on the fly” without having to inhibit the clock input.

Programming the 8253-5

A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence, and selection of binary or BCD counting. Once programmed, the 8253-5 is ready to perform whatever timing tasks it is assigned to accomplish.

All of the modes for each counter are programmed by the system's software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register (A0,A1 = 11).

CONTROL WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
SCI	SCO	RLI	RLO	M2	M1	M0	BCD

DEFINITION OF CONTROL

SC - Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

M - Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RL - Read/Load:

RL1	RL0	
0	0	Counter Latching operation
1	0	Read/Load most significant byte only
0	1	Read/Load least significant byte only
1	1	Read/Load least significant byte first, then most significant byte.

BCD:

0 Binary Counter 16-bits
1 Binary Coded Decimal (BCD) Counter (4 Decades)

COUNTER LOADING

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE DEFINITION

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached, the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

1. Write 1st byte stops the current counting.
2. Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+ 1)/2 counts and low for (N-1)/2 counts.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

GATE PIN OPERATIONS SUMMARY

MODES	SIGNAL STATUS		
	LOW	RISING	HIGH
0	Disables counting	- - - - - -	Enables counting
1	- - - - -	Initiates counting; Resets output after next clock.	- - - - - -
2	Disables counting; Sets output immediately high	Reloads counter; Initiates counting	Enables counting
3	Disables counting; Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	- - - - - -	Enables counting
5	- - - - - -	Initiates counting	- - - - - -

WRITE OPERATIONS

The system's software must program each counter of the 8253-5 with the mode and quantity desired. The programmer must write out to the 8253-5 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent (SC0, SC1).

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0,RL1) are programmed. Then proceed with the restart operation.

READ OPERATION

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity.

Event counters are probably the most common application that uses this function. The 8253-5 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0,A1 inputs to the 8253, the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0,A1 - 11). To ensure a stable count reading, however, this method requires that the operation of the selected counter be inhibited. Controlling the Gate input or using external logic to inhibit the clock input are two methods of inhibiting the counter. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB)

second I/O Read contains the most significant byte (MSB)

Due to the internal logic of the 8253-5, it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read, then two bytes must be read before any loading WR command can be sent to the same counter.

READING WHILE COUNTING

For the programmer to read the contents of any counter without affecting or disturbing the counting operation, the 8253-5 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter “on the fly,” he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter, and the contents of the latched register are available.

MODE Register For Latching Count
A0,A1 = 11

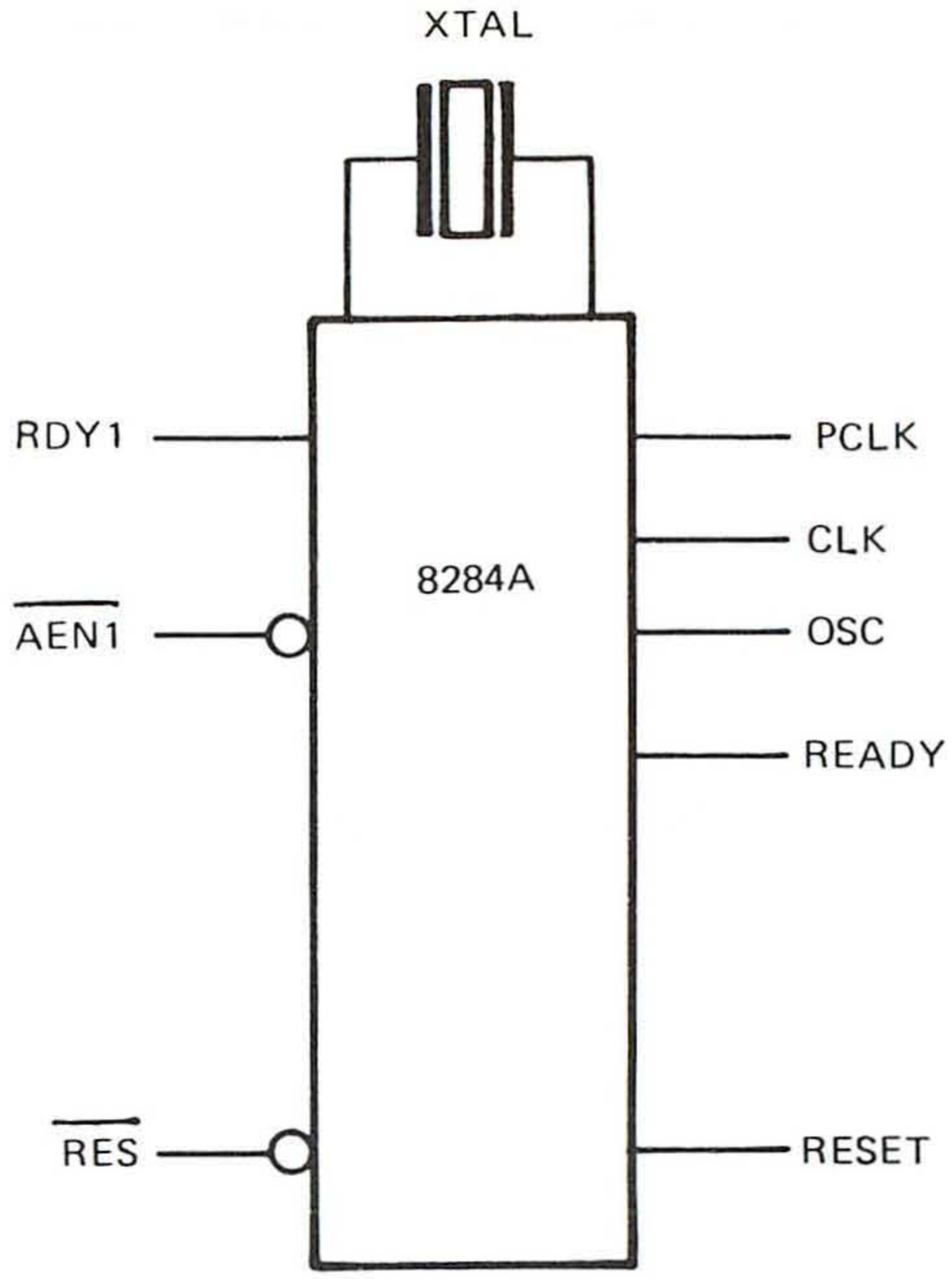
D7	D6	D5	D4	D3	D2	D1	D0
SCI	SCO	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched
D5, D41: - 00 designates counter latching operation.
X - don't care

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

CLOCK CIRCUITRY

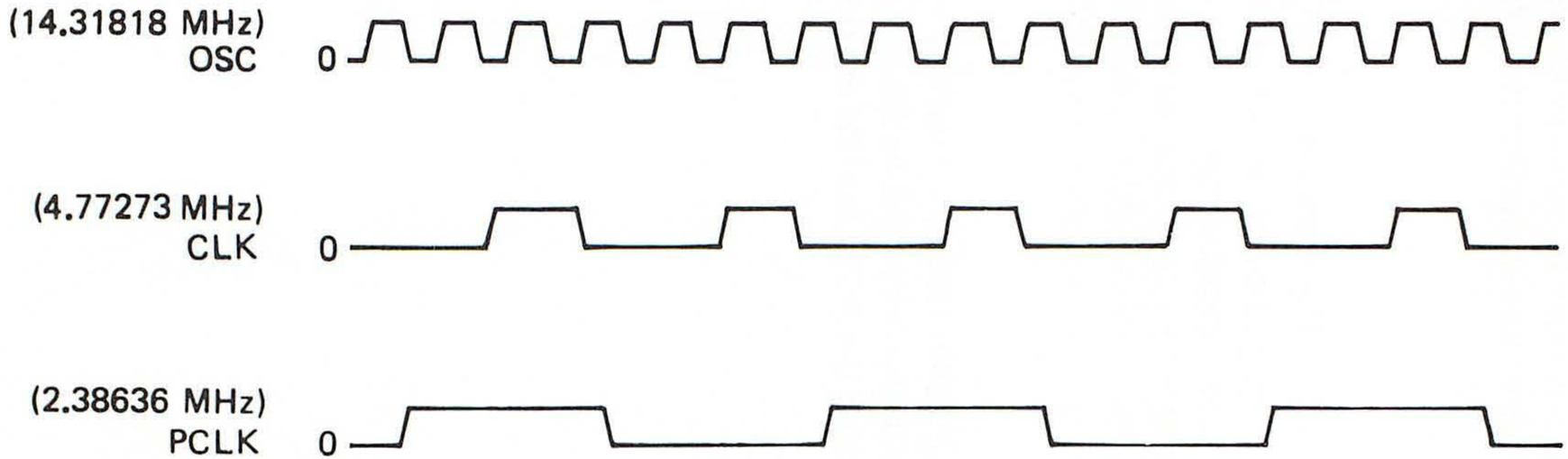
The 8284A clock generator, as shown below, produces all of the system's major required clock pulses. The READY output signal is the synchronized RDY1 input signal. This bus ready indicator is used, as described under the DMA controller, by devices located on the system bus to indicate when they have received data or made data available. RDY1 is validated by the -AEN1 signal. The 8284A is also used to generate the system's power-on reset signal (RESET).



8284A Clock Generator and Driver Circuit

The 8088's 4.773 MHz clock rate is derived by dividing the 14.31818 MHz crystal oscillator frequency by three. This clock signal (CLK) is also used by the optional 8087, the 8288 bus controller, the 8237A-5 DMA controller, and any cards installed in the I/O expansion backplane. The 8284A also produces the OSC clock signal. The frequency of this output is equal to that of the crystal oscillator, 14.31818 MHz. This signal is sent to the I/O expansion backplane and is used on the optional color/graphics controller board to create the required 3.58 MHz color-burst signal. The 8284A's PCLK signal (2.386 MHz) is divided by two to generate the 1.193 Mhz clock rate which is used by the 8253-5 as input to its three timer counter channel.

The relationship between the three clock signals generated by the 8284A is shown below:



Major Clock Signals

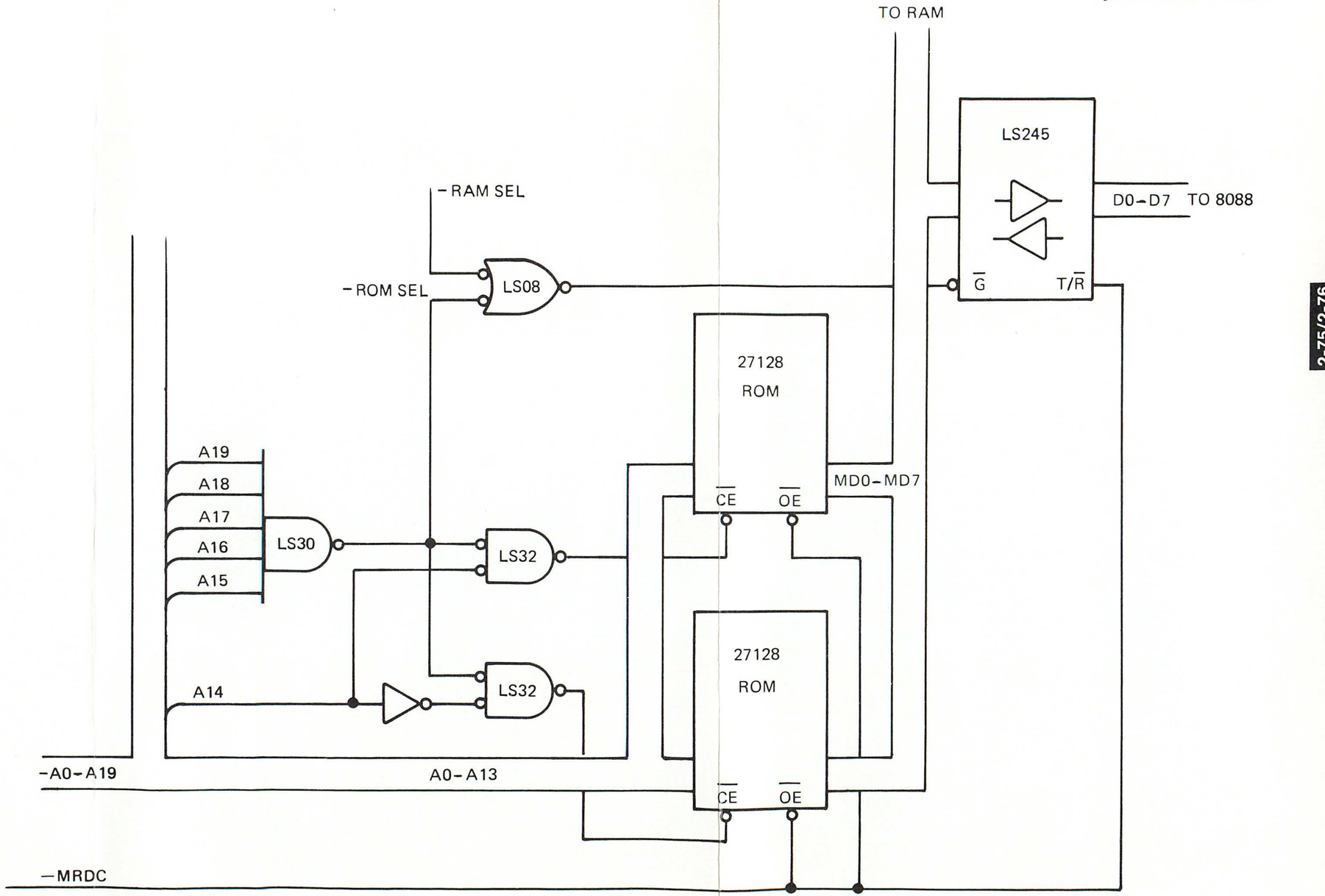
MEMORY DEVICES

The motherboard supports both Read Only Memory (ROM) and Read/Write memory (better known as Random Access Memory - RAM).

ROM

32KB of ROM are located on the motherboard. The ROM contains the diskette bootstrap loader, power-up self-test diagnostics, the ROM monitor, and the basic input/output driver routines. ROM is selected whenever a memory read access at address F8000H or higher is latched on the system address bus. This address activates the -ROMSEL signal and ultimately, the memory data bus transceiver.

When the 8288 bus controller issues a memory read (-MRDC), the requested ROM data becomes available on the data bus. The following figure illustrates the ROM and its associated support components.



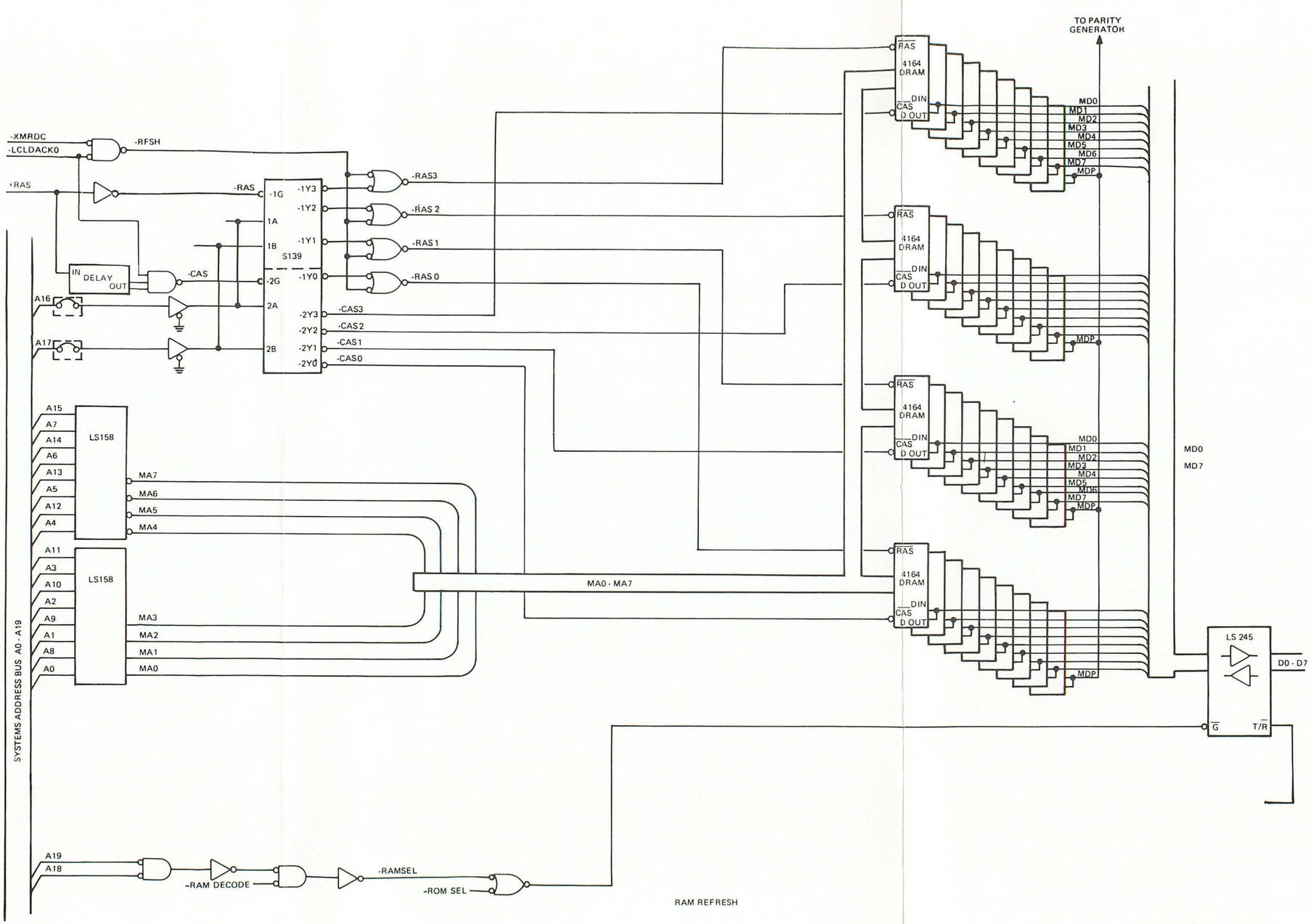
ROM Circuitry

RAM

The motherboard supports up to 256K x 9 of dynamic read/write memory located at hexadecimal address 00000 through 3FFFF. The extra (ninth) RAM chips are used for parity checking. The 64K x 1 chips have an access time of 200 ns and a cycle time of 410 ns. An additional 384KB of memory is available when the optional combo board and two "baby" add-on memory boards are installed in one of the motherboard's expansion slots.

The dynamic RAM is refreshed every 15 microseconds via a memory read cycle triggered by a dummy DMA transfer. The DMA refresh signal -LCLDACK0 disables the RAM column address strobe (CAS) circuitry. The DMA controller then drives -XMRDC active, causing a RAS only read using -RAS3, -RAS2, -RAS1, and -RAS0, the RAM row address strobe (RAS). These signals and the basic components in the RAM circuit are shown on the following page.

With the column address strobe and RAM decoding circuitry disabled, a normal read or write operation cannot occur during a memory refresh operation. Once the DMA refresh signal -LCLDACK0 goes inactive and an address lower than 20000 hex (for 128K systems) is latched on the data bus, -RAMSEL goes active and enables the data bus transceiver. A memory write (-AMWC) or a memory read (-MRDC) can be initiated by the 8288 bus controller. Row and then column addresses are multiplexed onto the 8-bit memory address bus (MA0-MA7). The direction of the data flow is controlled by the -MRDC signal on pin 1 of the memory data bus transceiver. A low signal causes the data to flow from the memory data bus to the system data bus. A high signal sends the data from the system data bus to the memory data bus.



RAM Circuitry

Parity checking is provided by the LS280 parity generator. During a memory write cycle, the parity generator calculates the correct parity bit and writes it into the ninth memory chip in the appropriate bank of memory. During a memory read cycle those stored parity bits are routed back to the parity generator. If a parity error is detected, -PERR goes active and the error is reported via the nonmaskable interrupt logic.

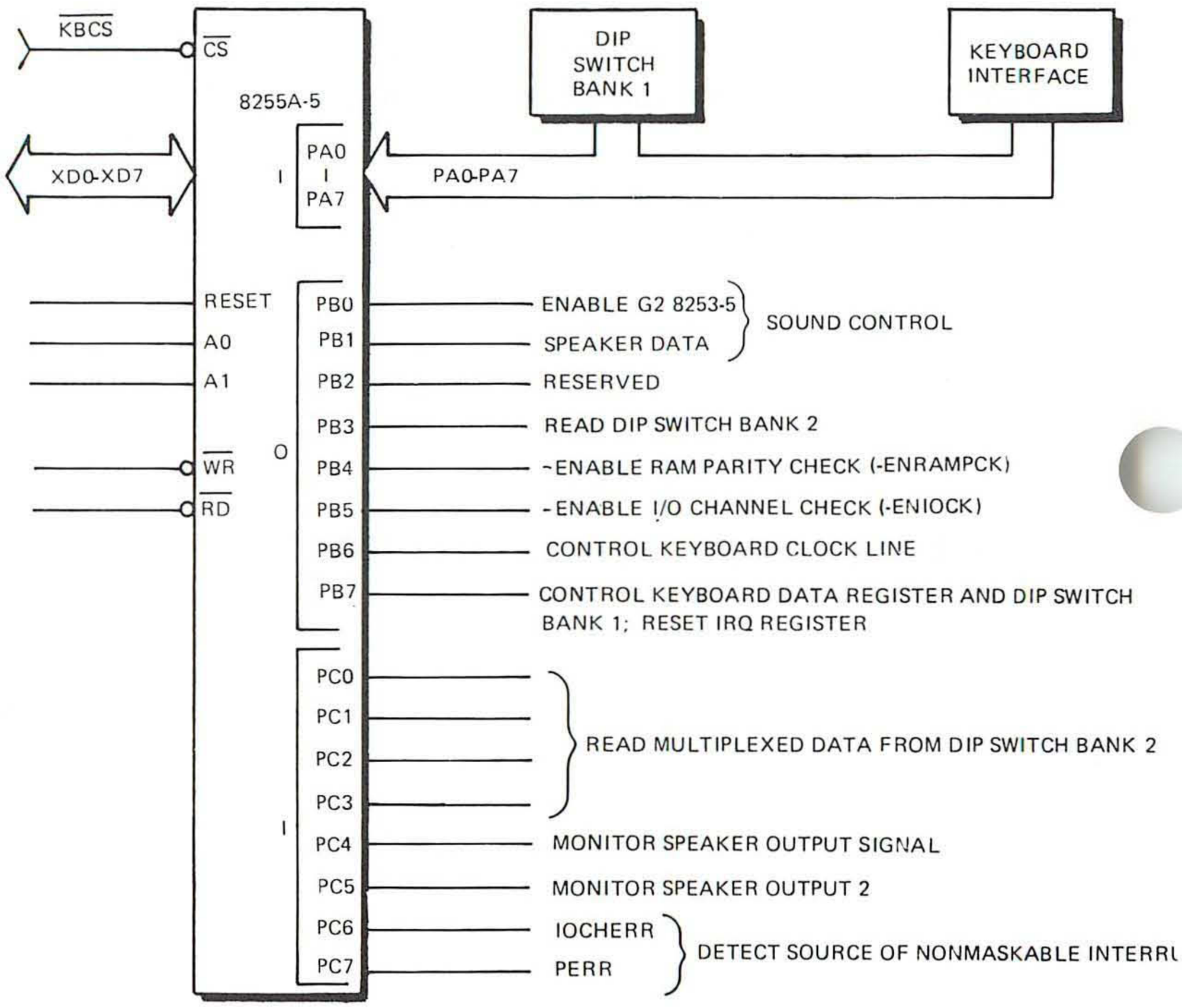
NONMASKABLE INTERRUPTS

The 8088's nonmaskable interrupt input is used to identify memory parity errors, interrupts output by the optional 8087 numeric data processor, and errors occurring on a card in one of the I/O expansion slots (most errors from cards installed in the expansion slots are from memory). These interrupts are nonmaskable once they reach the 8088. But if so desired, any or all of the memory error (-PERR), I/O channel error (-I/O CHERR), and the 8087 (INT) interrupts can be masked via system software before reaching the 8088. An NMI interrupt receives the highest priority of all hardware interrupts.

PARALLEL PERIPHERAL INTERFACE

The 8255A-5 programmable peripheral interface, as shown in the following figure, is a general purpose I/O chip used to interface peripheral devices to the system bus.

8255A-5 Programmable Peripheral Interface



The 8255A-5 provides the interface to devices such as the keyboard, the motherboard DIP switches, and the sound generator. Control words, received from the processor via the 8255A-5's bidirectional data bus, are used to configure each of the 8255A-5's three 8-bit ports. Port assignments are provided below:

8255A-5 PORT ASSIGNMENTS

PORT	BIT	IN/OUT	FUNCTION
Port A: Configured as an input port			
A	0	IN	
A	1	IN	
A	2	IN	
A	3	IN	Used to read DIP switch 1 or the
A	4	IN	8-bit keyboard data
A	5	IN	
A	6	IN	
A	7	IN	
Port B: Configured as an output port			
B	0	OUT	Output to Timer 2 gate input for sound generation.
B	1	OUT	Data from this bit is ANDed with the clock speaker output (timer 2) in the sound generation circuit.
B	2	OUT	Reserved for future use.
B	3	OUT	Used to multiplex the data from the 8-position DIP switch S2 on to the 4-bit switch data bus.

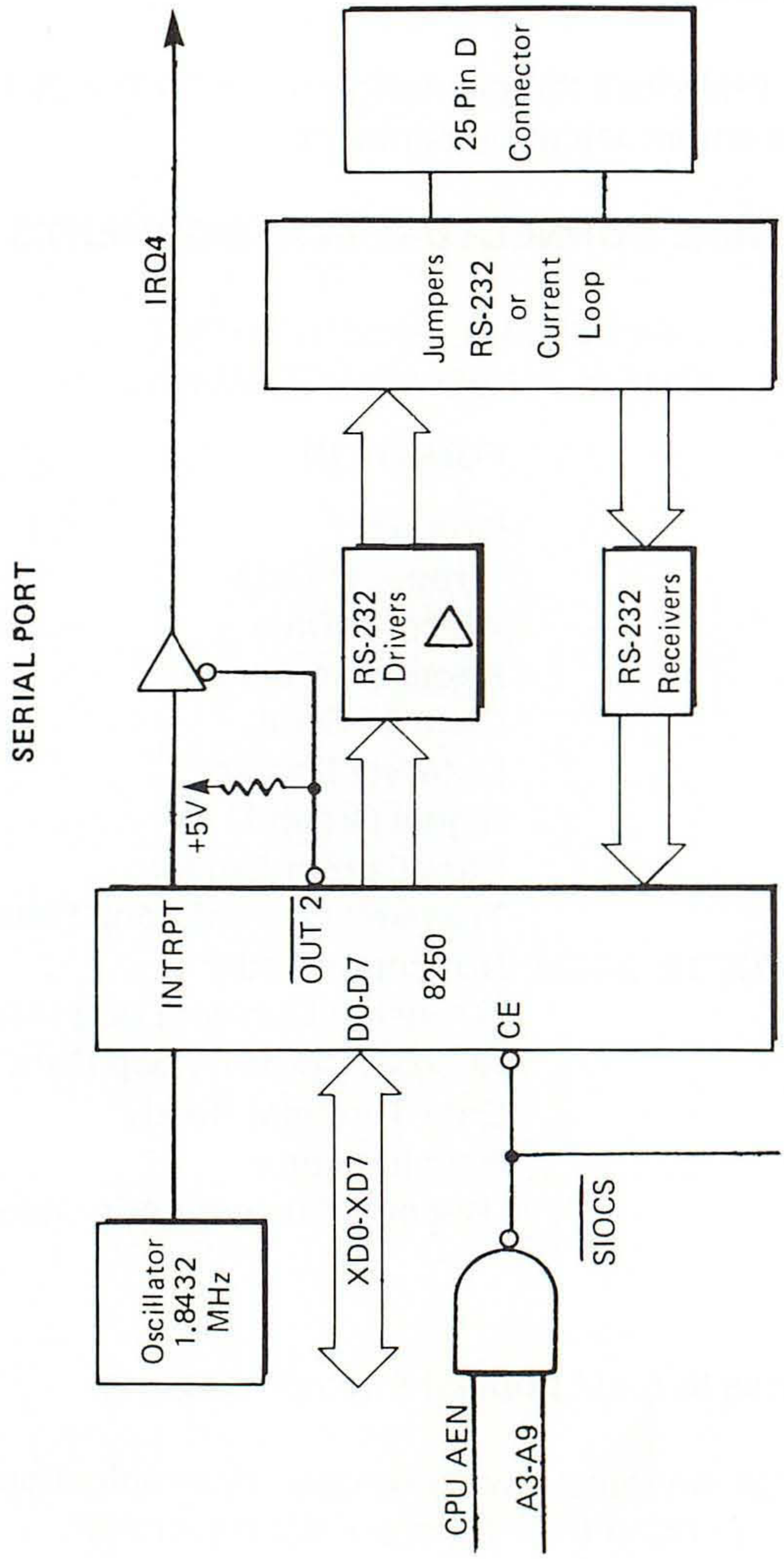
B	4	OUT	Used to enable the RAM parity check. (0 = enable)
B	5	OUT	Used to enable the I/O channel check. (0 = enable)
B	6	OUT	Used to control the keyboard clock line.
B	7	OUT	Used to control the enable line of the keyboard data register and DIP switch S1. Also used to reset the keyboard data register and IREQ 1 register.

Port C: Configured as an input port

C	0	IN	Bits 0-3 are used to read muliplexed data from DIP switch S2.
C	1	IN	
C	2	IN	
C	3	IN	
C	4	IN	Used to monitor the speaker output signal.
C	5	IN	Used to monitor speaker output 2.
C	6	IN	Bits 6 and 7 are used to detect the
C	7	IN	source of nonmaskable interrupts.

ASYNCHRONOUS COMMUNICATIONS CONTROLLER

The system motherboard features an asynchronous communications port, as shown in the following block diagram.



Asynchronous Communications Port Block Diagram

This RS-232-C compatible serial I/O port uses an INS 8250 programmable asynchronous communications interface. The port is configured as a DTE (for host communication). However, an external modem eliminator cable may be used to configure the port as a DCE for interfacing to a serial peripheral device such as a printer or terminal.

The following table lists the pin assignments for the 25-PIN D asynchronous communication connector.

SERIAL CONNECTOR PIN ASSIGNMENTS

P19 SERIAL PRINTER PORT
(CONFIGURED AS A TERMINAL)

PIN	FUNCTION
1	Ground
2	-Transmit Data
3	-Receive Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
7	Signal Ground
8	Data Carrier Detect
9	Transmit Current Loop Data
10, 12-17, 19, 21-24	Not connected
11	-Transmit Current Loop Data
18	Receive Current Loop Data
20	Data Terminal Ready
22	Ring Indicator
25	-Receive Current Loop Data

Features

Easily interfaces to most popular microprocessors.

Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.

Full double buffering eliminates need for precise synchronization.

Independently controlled transmit, receive, line status, and data set interrupts.

Programmable baud generator allows division of any input clock by 1 to (2^{16}-1) and generates the internal 16 x clock.

Independent receiver clock input.

MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).

Fully programmable serial-interface characteristics:

- 5-, 6-, 7-, or 8-bit characters
- Even, odd, or no-parity bit generation and detection
- 1-, 1 1/2-, or 2-stop bit generation
- Baud generation (DC to 56k baud)

False start bit detection

3-STATE TTL drive capabilities for bidirectional data bus and control bus

Complete status reporting capabilities

Line break generation and detection

Internal diagnostic capabilities:

- Loopback controls for communications link fault isolation
- Break, parity, overrun, framing error simulation

Full prioritized interrupt system controls

Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits. Note that in the following descriptions, a low represents a logic O (OV nominal) and a high represents a logic 1 (+2.4V nominal).

INPUT SIGNALS

CHIP SELECT (CSO, CS1, -CS2), pins 12-14: When CSO and CS1 are high and -CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe (-ADS) input. This enables communication between the INS8250 and the CPU.

DATA INPUT STROBE (DISTR, -DISTR), pins 22 and 21: When DISTR is high or -DISTR is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250. Note, only an active DISTR or -DISTR is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the -DISTR input permanently high, if not used.

DATA OUTPUT STROBE (DOSTR, -DOSTR), pins 19 and 18: When DOSTR is high or -DOSTR is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250. Note, only an active DOSTR or -DOSTR input is required to transfer data from the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the -DOSTR input permanently high, if not used.

ADDRESS STROBE (-ADS), pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0 - CS2) signals. Note, an active -ADS input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the -ADS input permanently low.

REGISTER SELECT (A0, A1, A2), pins 26-28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the following table. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

8250 Register Select

ADDRESS (HEX)	DLAB	A2	A1	A0	REGISTER
3F8	0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
3F9	0	0	0	1	Interrupt Enable
3FA	X	0	1	0	Interrupt Identification (read only)
3FB	X	0	1	1	Line Control
3FC	X	1	0	0	MODEM Control
3FD	X	1	0	1	Line Status
3FE	X	1	1	0	MODEM Status
3FF	X	1	1	1	None
3F8	1	0	0	0	Divisor Latch (least significant byte)
3F9	1	0	0	1	Divisor Latch (most significant byte)

MASTER RESET (MR), pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, -OUT1, -OUT2, -RTS, -DTR) are affected by an active MR input (see the following table, "ASYNCHRONOUS COMMUNICATION RESET FUNCTIONS").

ASYNCHRONOUS COMMUNICATIONS RESET FUNCTIONS

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit O is High, Bits 1 and 2 Low; Bits 3-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bits 0-3 Low Bits 4-7 - Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write TAR/MR	Low
INTRPT (MODEM Status Changes)	Read MSR/MR	Low
-OUT 2	Master Reset	High
-RTS	Master Reset	High
-DTR	Master Reset	High
-OUT1	Master Reset	High

RECEIVER CLOCK (RCLK), pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

SERIAL INPUT (SIN), pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

CLEAR TO SEND (-CTS), pin 36: The -CTS signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the -CTS input has changed state since the previous reading of the MODEM Status Register. -CTS has no effect on the Transmitter.

Note that whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

DATA SET READY (-DSR), pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The -DSR signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the -DSR input has changed state since the previous reading of the MODEM Status Register.

Note that whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.

RECEIVED LINE SIGNAL DETECT (-RLSD), pin 38: This signal indicates that the data carrier has been detected by either the MODEM or the data set. The -RLSD signal is a MODEM Control Function input. The condition of this function can be tested by the CPU by reading bit 7 (-RLSD) of the MODEM Status Register. Bit 3 (-RLSD) of the MODEM Status Register indicates whether the -RLSD input has changed state since the previous reading of the MODEM Status Register. -RLSD has no effect on the receiver.

Note that whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

RING INDICATOR (-RI), pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The -RI signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the -RI input has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note that whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status is enabled.

Vcc, Pin 40: +5V supply.

Vss, Pin 20: Ground (0V) reference.

OUTPUT SIGNALS

DATA TERMINAL READY (-DTR), pin 33: When low, informs MODEM or data set that the INS8250 is ready to communicate. The -DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The -DTR signal is set high upon a Master Reset operation. The -DTR signal is forced to its inactive state (high) during loop mode operation.

REQUEST TO SEND (-RTS), pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The -RTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The -RTS signal is set high upon a Master Reset operation.

OUTPUT 1 (-OUT1), pin 34: User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control register to a high level. The -OUT1 signal is set high upon a Master Reset Operation.

OUTPUT 2 (-OUT2), pin 31: User-designated output that can be set to an active low by programming bit 3 (OUT2) of the MODEM Control Register to a high level. The -OUT2 signal is set high upon a Master Reset Operation.

CHIP SELECT OUT (CSOUT), pin 24: When high, indictes that the chip has been selected by active, CS0, CS1, and -CS2 inputs. No data transfer can be initiated until the SCOUT signal is a logic 1.

DRIVER DISABLE (DDIS), pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D7-D0 Data Bus) at all times, except when the CPU is reading data.

BAUD OUT (-BAUDOUT), pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The -BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

INTERRUPT (INTRPT), pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

SERIAL OUTPUT (SOUT), pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

INPUT/OUTPUT SIGNALS

DATA (D7-D0) BUS, pins 1-8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D7-D0 Data Bus.

EXTERNAL CLOCK INPUT/OUTPUT (XTAL1, XTAL2), pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Accessible Registers

The system programmer may access or control any of the INS8250 registers via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
1	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1 1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Generator

The INS8250 contains a programmable Baud Generator that is capable of taking the 1.8432 MHz clock input and dividing it by any divisor from 1 to (2^{16}-1). The output frequency of the Baud Generator is 16x the Baud [divisor # = (frequency input) /(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

The following table illustrates the use of the Baud Generator with a frequency of 1.8342 MHz. For baud rates of 9600 and below, the error obtained is minimal. In no case should the data rate exceed 9600 Baud.

Baud Rates Using 1.8432 MHz Frequency

Desired Baud Rate	Divisor Used to Generate 16x Clock (decimal)	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are described below:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. Note that bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are described below:

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, and interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the table that follows.

Bits 3 through 7: These five bits of the IIR are always logic 0.

8250 INTERRUPT CONTROL FUNCTIONS

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Source	Interrupt Source	Interrupt Reset Control
0	0	1	- - -	None	None	- - -
1	1	0	Highest	Receiver Line Status	Overrun Error, parity error, framing error, or break interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR register (if source of interrupt) or Writing into the Transmitter Holding register
0	0	0	Fourth	MODEM status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the Modem Status Register

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the INS8250 to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status registers. The contents of the Interrupt Enable Register are described below:

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Modem Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated below:

Bit 0: This bit controls the Data terminal Ready (-DTR) output. When bit 0 is set to a logic 1, the -DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the -DTR output is forced to a logic 1. Note, the INS8250 -DTR output may be applied to an EIA inverting line driver (i.e., DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send (-RTS) output. Bit 1 affects the -RTS output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 (-OUT1) signal, which is an auxiliary user-designated output. Bit 2 affects the -OUT1 output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output2 (-OUT2) signal, which is an auxiliary user-designated output. Bit 3 affects the -OUT2 output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs (-CTS, -DSR, -DCD, and -RI) are disconnected; and the four MODEM Control outputs (-DTR, -RTS, -OUT1, and -OUT2) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupt's sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM Control Register must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

Modem Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the -CTS input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the -DSR input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of ring Indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the -DCD input to the chip as changed state. Note, whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status interrupt will be generated if in diagnostic mode.

Bit 4: This bit is the complement of the Clear to Send (-CTS) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready (-DSR) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator (-RI) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.

Bit 7: This bit is the complement of the Received Line Signal Detect (-RLSD) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 of the MCR.

Scratchpad Register

This 8-bit Read/Write Register does not control the INS8250 in any way. It is intended as a scratch pad register to be used by the programmer to hold data temporarily.

Transmit and Receive Data Formats

The asynchronous communication controller can transmit and receive EIA RS-232-C compatible serial data, encoded as specified by ASCII standard No. X3.4-1968 of the American National Standards Institute. Receive and transmit signal voltages are nominally +/-12 Vdc. Each ASCII code includes seven bits of binary data. When an ASCII code is transmitted, three (sometimes four) more bits of binary information must be added for a total of ten (sometimes eleven) bits of binary data. These additional bits of information identify the beginning and end of each code and provide error recognition capability.

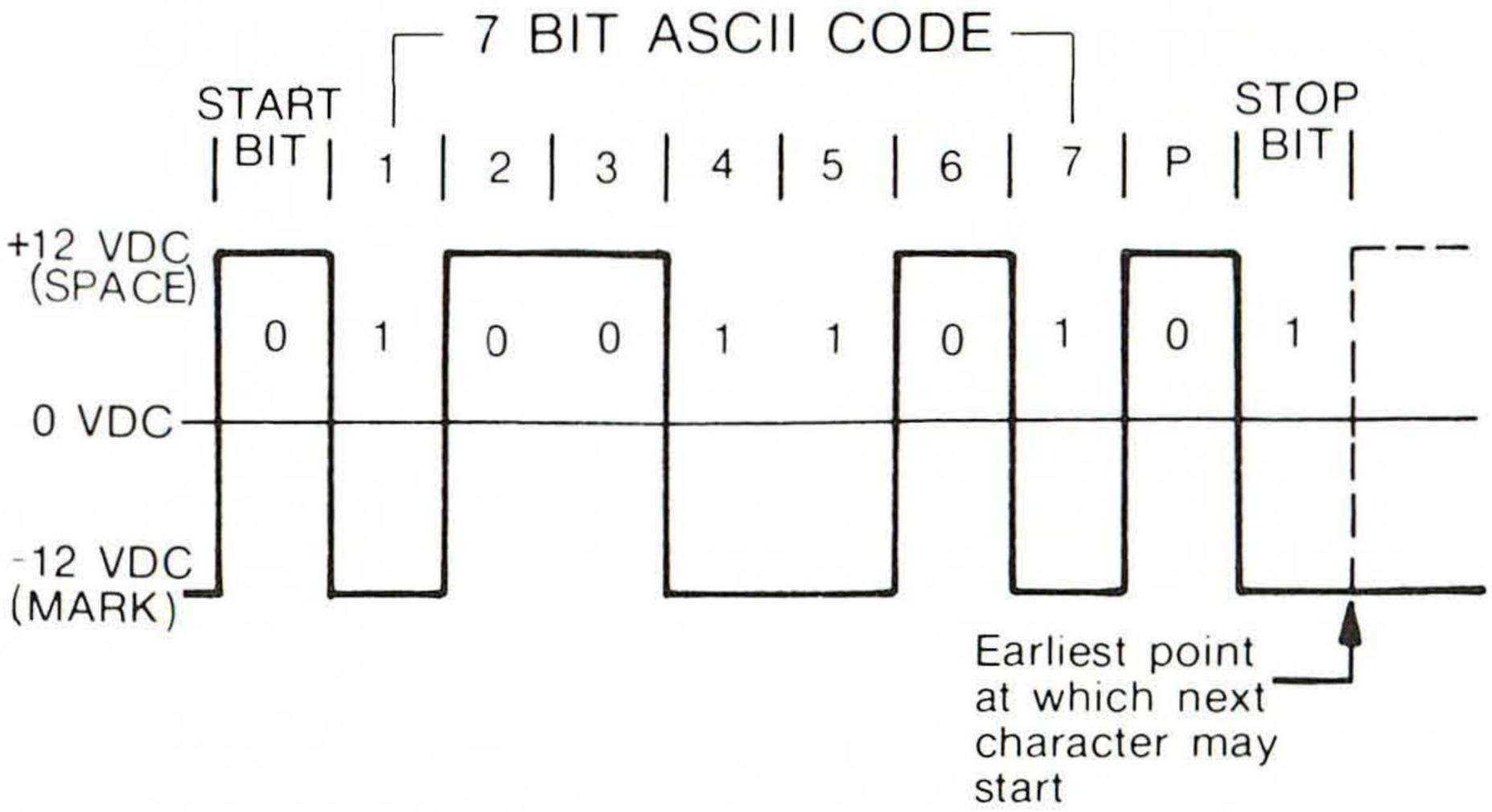
An EIA RS-232-C data line will be in a Mark state (-12 Vdc nominally) between code transmissions. Transmission of a code is begun by the transmitting device raising the data line to a space state (+12 Vdc nominally). The data line is left in the space state for the time period of one bit. This bit time varies depending upon the baud rate selected (e.g., 110 baud equals 9 ms per bit, 1200 baud equals 833 usec per bit). This first bit period is called the start bit and identifies the beginning of a code transmission.

The next seven bits of data are the seven ASCII code bits, least significant bit first. An ASCII code bit that is a logic "1" corresponds to an EIA RS-232-C data line mark state (-12 Vdc nominally).

The next bit (the eighth bit, not counting the start bit) is called the parity bit. Its voltage level during the transmission of any given character depends on the data in the seven ASCII code bits. The 8250 can be programmed for odd, even, or no parity.

The last bit of data transmitted is the stop bit(s). The data line must be brought low to the mark state for a minimum of one bit period (minimum of two stop bit periods for 110 baud or lower operation. Transmission of the next character can begin immediately following the stop bit(s), or the data line can be left idle in the Mark state.

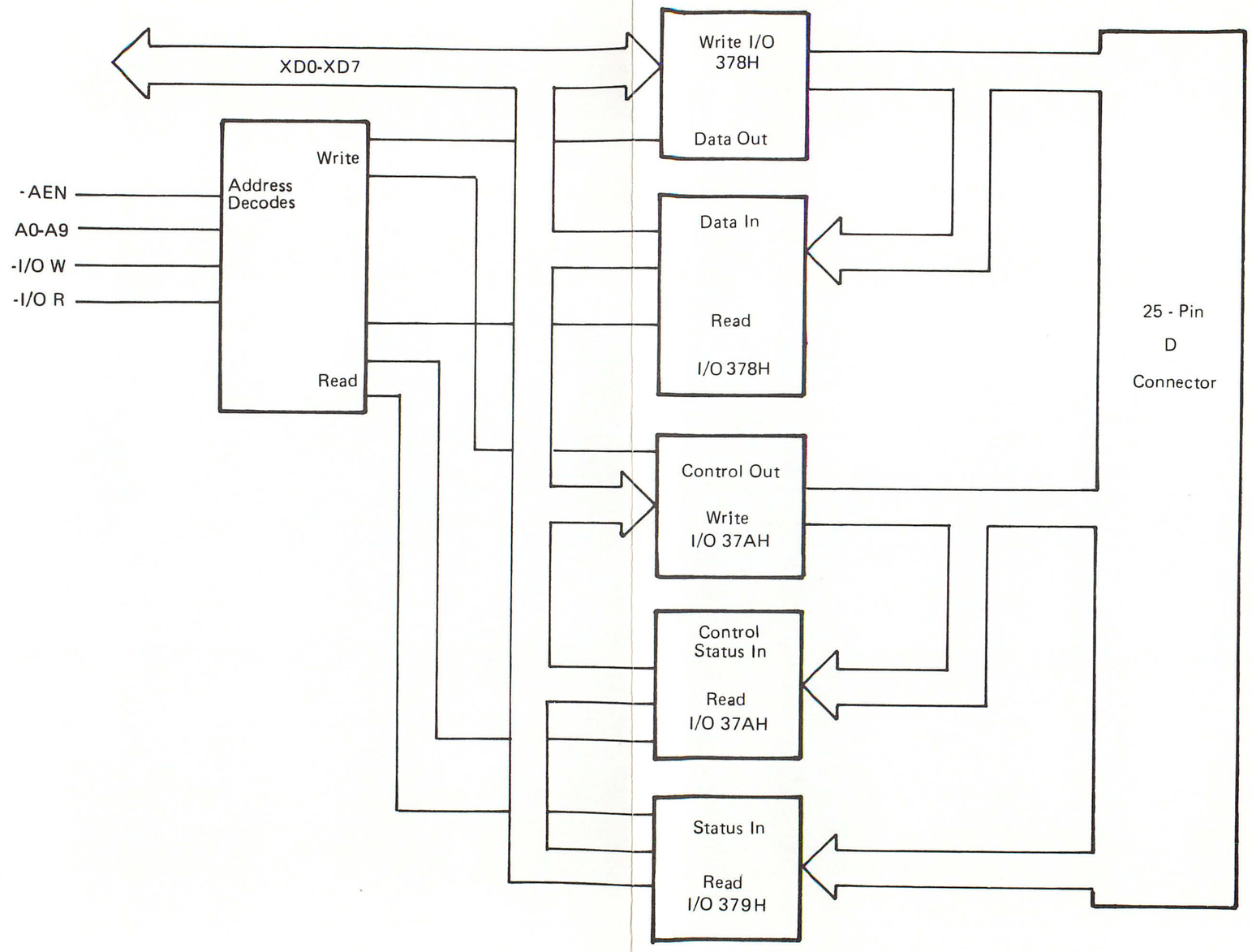
Transmit and receive data formats are shown in the following illustration:



Transmit and Receive Data Format

PARALLEL PORT

The motherboard provides a parallel port via a 25 “D” female connector for interfacing to a parallel printer or other parallel peripheral devices. A simplified block diagram of the parallel interface is shown below:



Motherboard Parallel Interface

Software Instructions

Software instructions can be used in conjunction with the motherboard's parallel interface. These instructions are used to read from or write to the parallel interface latches. A description of each of the five commands follows:

READ 3BC HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
D0	D1	D2	D3	D4	D5	D6	D7

WRITE 3BC HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
D0	D1	D2	D3	D4	D5	D6	D7

READ 3BD HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
UNUSED	UNUSED	UNUSED	-ERROR	SLCT	PE	-ACKNLG	-BUSY

READ 3BE HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
STROBE	AUTO FDXT	-INIT	SLCT IN	UNUSED	UNUSED	UNUSED	UNUSED

WRITE 3BE HEX

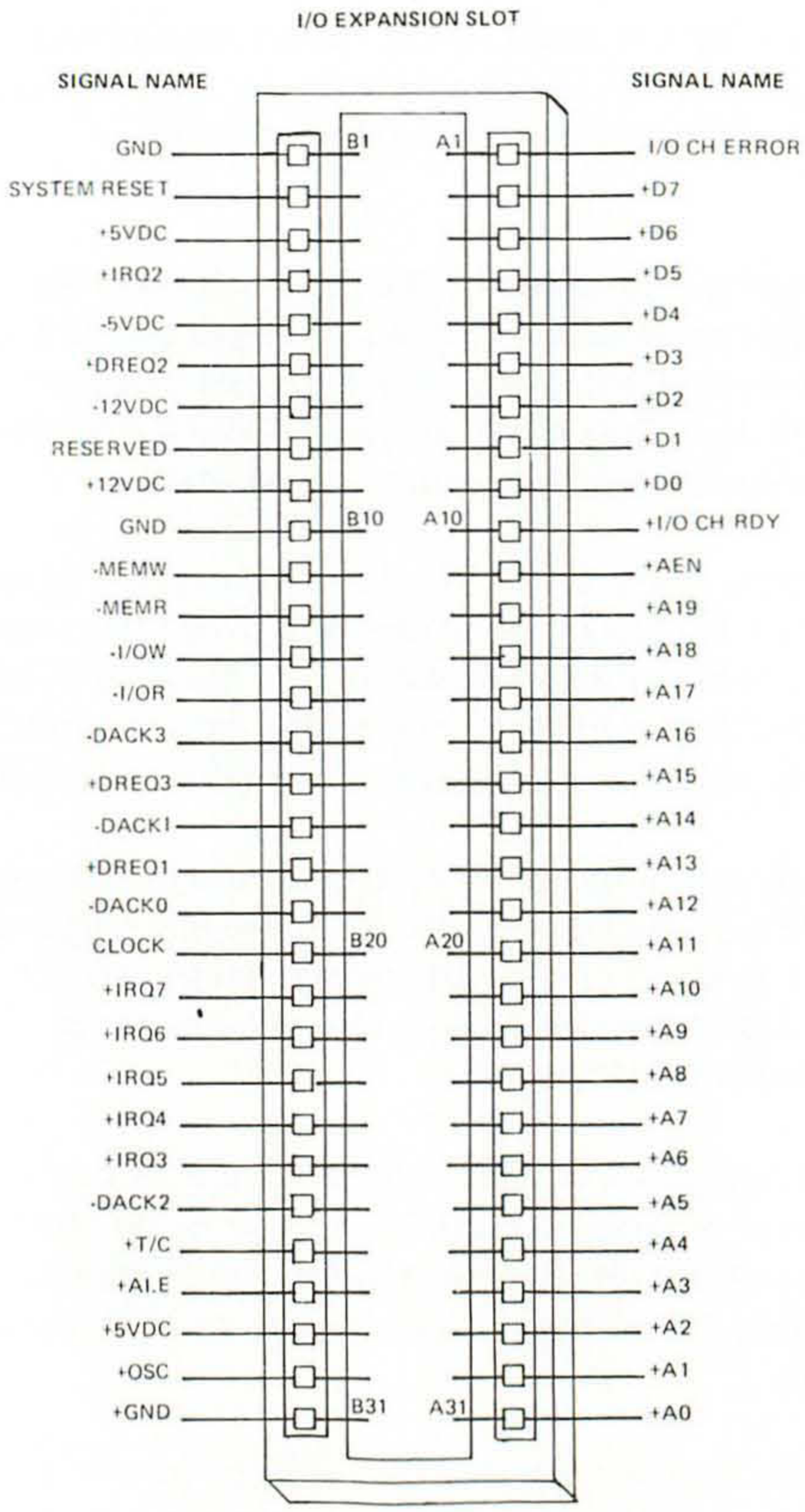
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
-STROBE	-AUTO FD	-INIT	SLCT IN	ON IRQ	UNUSED	UNUSED	UNUSED

PARALLEL INTERFACE CONNECTOR PIN ASSIGNMENTS

PIN NUMBER	SIGNAL	DESCRIPTION
1	-STROBE	Output to printer. A strobe pulse latches data into the printer. Pulse width: from 1.0 to 500 microseconds. May be either active high or low, switch selectable. Strobe must be sent 1.0 microsecond (min.) after valid data.
2	DATA 0	Input data to printer.
3	DATA 1	Data 8 = LSB (Least Significant Bit)
4	DATA 2	Data 1 = MSB (Most Significant Bit)
5	DATA 3	ASCII codes normally use Data 1-7
6	DATA 4	Data 8 not used. Logic 1 high (2.4 - 5.0 Vdc)
7	DATA 5	Logic 0 low (0 to 0.4 Vdc)
8	DATA 6	
9	DATA 7	
10	-ACKNOWLEDGE	Input from printer. A low pulse (5 microseconds) indicates the printer has accepted the input data.
11	BUSY	Input from printer. Printer sets this line high to indicate printer is busy; low indicates printer is not busy and can accept data. A BUSY is sent from the printer after each character is received.
12	OUT OF PAPER	Input from printer. High indicates that the printer is out of paper.
13	SELECT	Input from printer. High indicates printer is selected and ready to receive data.
14	-AUTO FEED	Output to printer. A low indicates that the printer should feed one line of paper.
15	-ERROR	Output to printer. A low indicates that the printer needs attention (ribbon out, cover off, etc.)
16	-INITIALIZE PRINTER	Output to printer. A low pulse (1.0 microsecond minimum) initializes the printer. Clears printer input buffer and sets the printer to default parameters. Performs a Restore function.
17	-SELECT INPUT	Output to printer. This signal must be low before the printer will accept data.
18-25		Signal Grounds

I/O EXPANSION BACKPLANE

The I/O expansion backplane is an expansion of the system bus. Twenty address lines, eight data lines, memory and I/O read or write control lines, a clock, DMA and interrupt control lines, +/- 5V, and +/-12V are all bussed to each of the five expansion slots. The 8237A-5 programmable DMA controller provides three channels of bus request arbitration from cards located on the I/O backplane. The 8259A programmable interrupt controller provides six levels of interrupts to devices on the backplane. Pin assignments for each I/O connector are shown in the following figure:



I/O Expansion Backplane Pin Assignments

A brief description of each of these signals is presented in the following table.

I/O EXPANSION SLOT SIGNAL DESCRIPTIONS

SIGNAL	I/O	PIN #	DESCRIPTION
OSC	O	B30	A buffered version of the main system timing clock with a 70 nsec period (14.31818 MHz); it has a 50% duty cycle.
CLK	O	B20	A buffered version of the system processor clock. Its 4.773 MHz frequency is derived by dividing the oscillator frequency by three; it has a 33% duty cycle.
SYSTEM RESET	O	B2	This line, synchronized to the falling edge of CLK, is used to initialize all system hardware components on power-up or during a low voltage condition.
ALE	O	B28	This signal is provided by the 8288 bus controller to indicate the presence of a valid address on the system bus from the CPU. The address is latched by the falling edge of ALE. This signal is enabled in the I/O channel by the system address enable signal -AEN.
AEN	O	A11	When this signal is inactive (low), the 8088 or optional 8087 has control of the system bus. When this signal is active, the local bus is isolated from the system bus and the DMA controller controls the data bus, address bus, the memory, and I/O read/write command lines.
A0-A19	O	A31- A12	These lines comprise the 20-bit address bus. Driven by the 8088 or the DMA controller, these lines provide access to up to one megabyte of memory. A0 is the Least Significant Bit (LSB) and A19 is the Most Significant Bit (MSB).
D0-D7	I/O	A9-A2	These lines comprise the 8-bit system data bus. D0 is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These bidirectional lines can be driven by the processor, I/O devices, or memory devices.
I/O CH RDY	I	A10	This line is pulled low (NOT READY) by an I/O or memory device to lengthen the bus cycle. By lengthening the cycle, slower devices can attach to the I/O cycle with less difficulty. To ensure that the memory refresh cycle is not interrupted, this line should never be held low for more than 2 microseconds.

I/O EXPANSION SLOT SIGNAL DESCRIPTIONS (Continued)

SIGNAL	I/O	PIN #	DESCRIPTION
-I/O CH ERR	I	A1	This signal is used to generate an interrupt on the NMI input of the 8088. It indicates an error on a device in the I/O channel (typically a memory device).
-I/OR	O	B14	This signal, driven by the processor or the DMA controller, commands an I/O device to place its data on the data bus.
-I/OW	O	B13	This signal, driven by the processor or the DMA controller, commands an I/O device to accept the data on the system data bus.
-MEMR	O	B12	This signal, driven by the processor or the DMA controller, commands the memory to place its data on the system data bus.
-MEMW	O	B11	This signal, driven by the processor or the DMA controller, commands the memory to accept the data on the system data bus.
IRQ2-IRQ7	I	B4, B25-B21	These prioritized interrupt request lines (IRQ2 has the highest priority; IRQ7 the lowest) signal the processor that an I/O device requires attention. These edge triggered request lines must be raised (from low to high) and held high until the interrupt request is acknowledged.
DREQ1-DREQ3	I	B18,B6, B16	These prioritized DMA request lines (DREQ1 has the highest priority, DREQ3 the lowest) are used by peripheral devices to request DMA service. A DREQ line must be held high until the corresponding DACK signal is received.
-DACK0 - - DACK3	O	B19,B17, B26,B15	These lines are used to acknowledge DMA requests (DACK1-DACK3). DACK0 is used to indicate that a DMA controlled memory refresh is in progress.
RE-SERVED	B8	Not used	
T/C	O	B27	This line indicates when the terminal count for any DMA channel is reached.

The following power connections are provided in each expansion connector:

+5 Vdc +/-5%, located on connector pins B3 and B29.
-5 Vdc +/-10%, located on connector pin B5
+12 Vdc +/-5%, located on connector pin B9
-12 Vdc +/-10%, located on connector pin B7 GND located on connector pins B1, B10, and B31.

FLOPPY DISK DRIVE CONTROLLER

An Intel 8272A floppy disk controller/formatter (or NEC uPD765 equivalent), also located on the motherboard, controls the system's 5.25" disk drives. A 9216 chip provides clock and data separation on the read data. A 4-bit shift register is used to provide write pre-compensation. The controller clock frequency is 4 MHz.

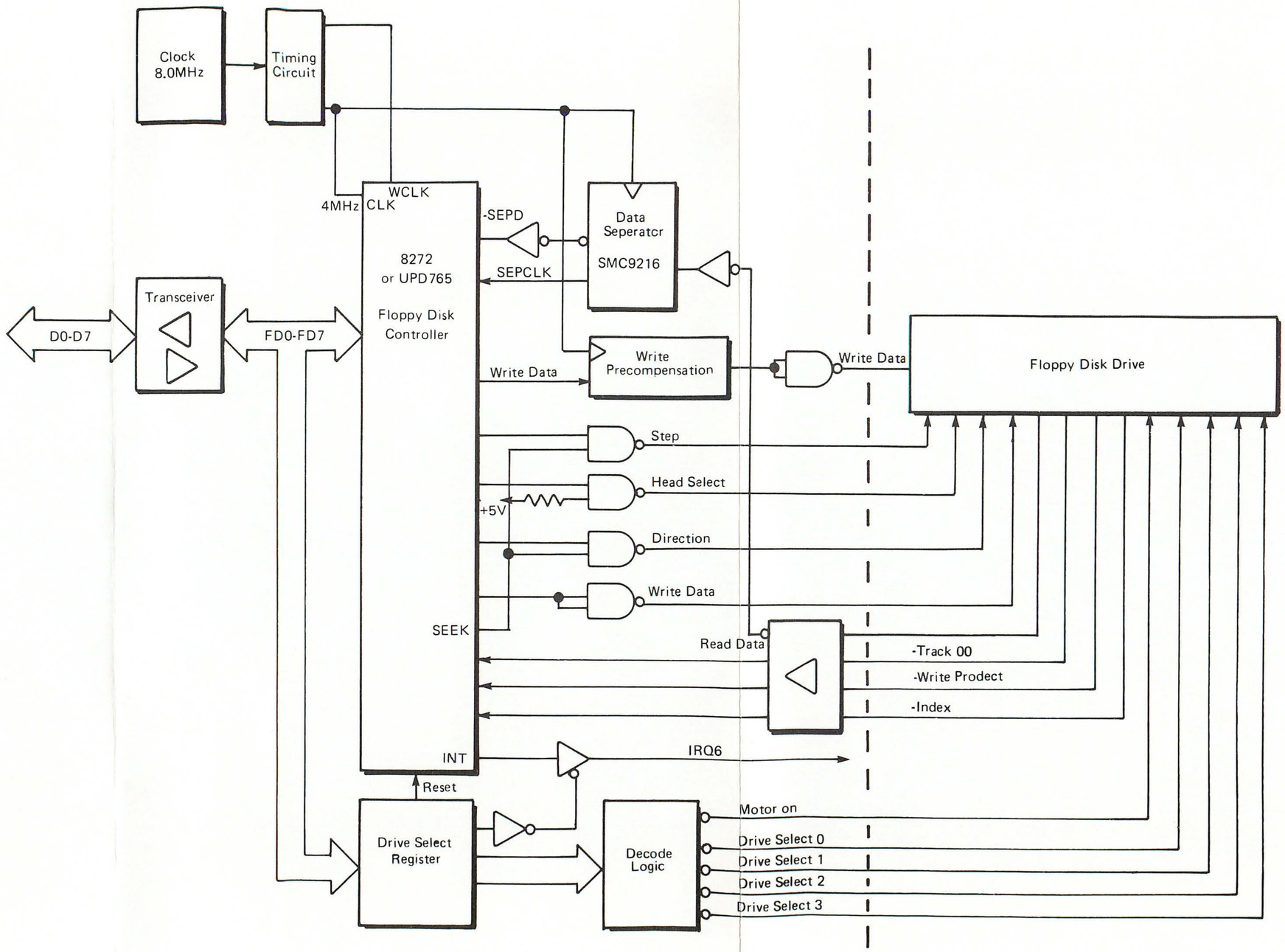
Configured by the system to use the standard IBM 5.25" disk drive format of eight or nine sectors of 512 bytes in double density (Modified Frequency Modulation), the sector lengths of 128, 256, and 1024 bytes are also selectable. The step rate is programmable from 2 to 32 ms in 2 ms increments.

System Interface

The floppy disk controller, as shown in the following block diagram, uses Direct Memory Access (DMA) to transfer data between the disk drives and memory. The system data bus (D0-D7) is buffered via a 245 data transceiver to the 8272A's data access lines (D0-D7). Data is written into or read from the floppy disk controller's Data Register when address 3F5 is placed on the address bus. Data is written into or read from the controller's Status Register when address 3F4 is placed on the address bus.

The data access lines, in addition to interfacing the system data bus to the floppy disk controller, are used to output data from the controller to the LS273 Drive Select Register. The Drive Select Register is an output only register used to control the drive select and motor on signals. Data is written into the Drive Select Register when I/O address 3F2 hex is placed on the system address bus. Bit assignments for the Drive Select Register are as follows:

Bits 0,1	Drive Select 00 - drive A 01 - drive B 10 - drive C 11 - drive D
Bit 2	Master reset for controller
Bit 3	Enable interrupts and DMA request
Bit 4	Motor on drive A
Bit 5	Motor on drive B
Bit 6	Motor on drive C
Bit 7	Motor on drive D



Floppy Disk Drive Controller Block Diagram

The FDC contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDC status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and FDC.

The following table defines the bits in the Main Status Register:

MAIN STATUS REGISTER BIT DESCRIPTION

Bit NUMBER	NAME	SYMBOL	DESCRIPTION
D0	FDD A Busy	DAB	FDD A is in the Seek mode.
D1	FDD B Busy	DBB	FDD B is in the Seek mode.
D2	FDD C Busy	DCB	FDD C is in the Seek mode.
D3	FDD D Busy	DDB	FDD D is in the Seek mode.
D4	FDC Busy	CB	A read or write command is in process.
D5	Non-DMA mode	NDM	The FDC is in the non-DMA mode. This bit is set only during the execution phase in non-DMA mode. Transition to "0" state indicates execution phase has ended.
D6	Data Input/ Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO="1" then transfer is from Data Register to the Processor. If DIO="0", then transfer is from the Processor to Data Register.
D7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

The FDC is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

The following table summarizes the mneumonics (symbols) that appear in the ensuing FDC Command Set Summary.

COMMAND MNEUMONICS

SYMBOL	NAME	DESCRIPTION
A0	Address Line 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1)
C	Cylinder Number	C stands for the current selected Cylinder track number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D7-D0	Data Bus	8-bit Data Bus where D7 is the most significant bit, and D0 is the least significant bit.

COMMAND MNEUMONICS (Continued)

SYMBOL	NAME	DESCRIPTION
DSA,DSB	Drive Select	DS stands for a selected drive number A or B.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number of a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HDS	Head Select	HDS stands for a selected head number 0 or 1 (H=HDS in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MFM	FM or MFM Mode	If MF is low, FM mode is selected and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed (a cylinder under both HD0 and HD1 will be read or written).
N	Number	N stands for the number of data bytes written in a Sector.

COMMAND MNEUMONICS (Continued)

SYMBOL	NAME	DESCRIPTION
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). The same Stepping Rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A0 = 0). ST 0-3 may be read only after a command has been executed and the registers contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.

COMMAND SET SUMMARY

DATA BUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					READ DATA					
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				C					Sector ID information
	W				H					prior to Command
	W				R					execution
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					after command
	R				N					execution

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		READ DELETED DATA								
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				C					Sector ID information
	W				H					prior to Command
	W				R					execution
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					after command
	R				N					execution

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					WRITE DATA					
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				C					Sector ID information
	W				H					prior to Command
	W				R					execution
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					after command
	R				N					execution

DATA BUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					WRITE DELETED DATA					
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				C					Sector ID information
	W				H					prior to Command
	W				R					execution
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					after command
	R				N					execution

		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					READ A TRACK					
Command	W	0	MFM	SK	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				C					Sector ID information
	W				H					prior to Command
	W				R					execution
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main system. FDC reads all of cylinder's contents from index hole to EOT
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					after command
	R				N					execution

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					READ ID					
Command	W	0	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					during execution
	R				N					phase
					FORMAT A TRACK					
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				N					Bytes/Sector
	W				SC					Sectors/Cylinders
	W				GPL					Gap 3
	W				D					Filler byte
Execution										FDC formats an entire cylinder
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					In this case the ID
	R				R					information has no
	R				N					meaning

		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					SCAN EQUAL					
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				C					Sector ID information
	W				H					prior to Command
	W				R					execution
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data compared between the FDD and main system
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					after command
	R				N					execution

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		SCAN LOW OR EQUAL								
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W	C								Sector ID information
	W	H								prior to Command
	W	R								execution
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data compared between the FDD and main system
Result	R	ST0								Status information
	R	ST1								after Command
	R	ST2								execution
	R	C								
	R	H								Sector ID information
	R	R								after command
	R	N								execution

		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		SCAN HIGH OR EQUAL								
Command	W	MT	MFM	SK	1	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				C					Sector ID information
	W				H					prior to Command
	W				R					execution
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data compared between the FDD and main system
Result	R				ST0					Status information
	R				ST1					after Command
	R				ST2					execution
	R				C					
	R				H					Sector ID information
	R				R					after command
	R				N					execution
		RECALIBRATE								
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DSB	DSA	
Execution										Head retracted to Track 0

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		SENSE INTERRUPT STATUS								
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R				ST0					Status information at
	R				PCN					the end of each seek operation about the FDC
		SPECIFY								
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT	
	W	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND	
		SENSE DRIVE STATUS								
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
Result	R				ST3					Status information about FDD
		SEEK								
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DSB	DSA	
	W				NCN					
Execution										Head is positioned over proper Cylinder on Diskette
		INVALID								
Command	W				Invalid Codes					Invalid Command Codes (No Op-FDC goes into Standby State)
Result	R				ST0					STO = 80

Status Register Summary

Status Register 0

NO.	NAME	BIT SYMBOL	DESCRIPTION
D7	Interrupt Code	IC	D7=0 and D6=0 Normal termination of command (NT). Command was completed and properly executed.
D6		D7=0 and D6=1	Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed. D7=1 and D6=0 Invalid Command issue, (IC). Command which was issued was never started. D7=1 and D6=1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track) Signal fails to occur after 77 Step Pulses Recalibrate Command) then this flag is set.
D3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt
D1	Unit Select1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D0	Unit Select0	US 0	

Status Register 1

D7	End of cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D6			Not used. This bit is always 0 (low)
D5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D3			Not used. This bit is always 0 (low).
D2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set. During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set. During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.

Status Register 2

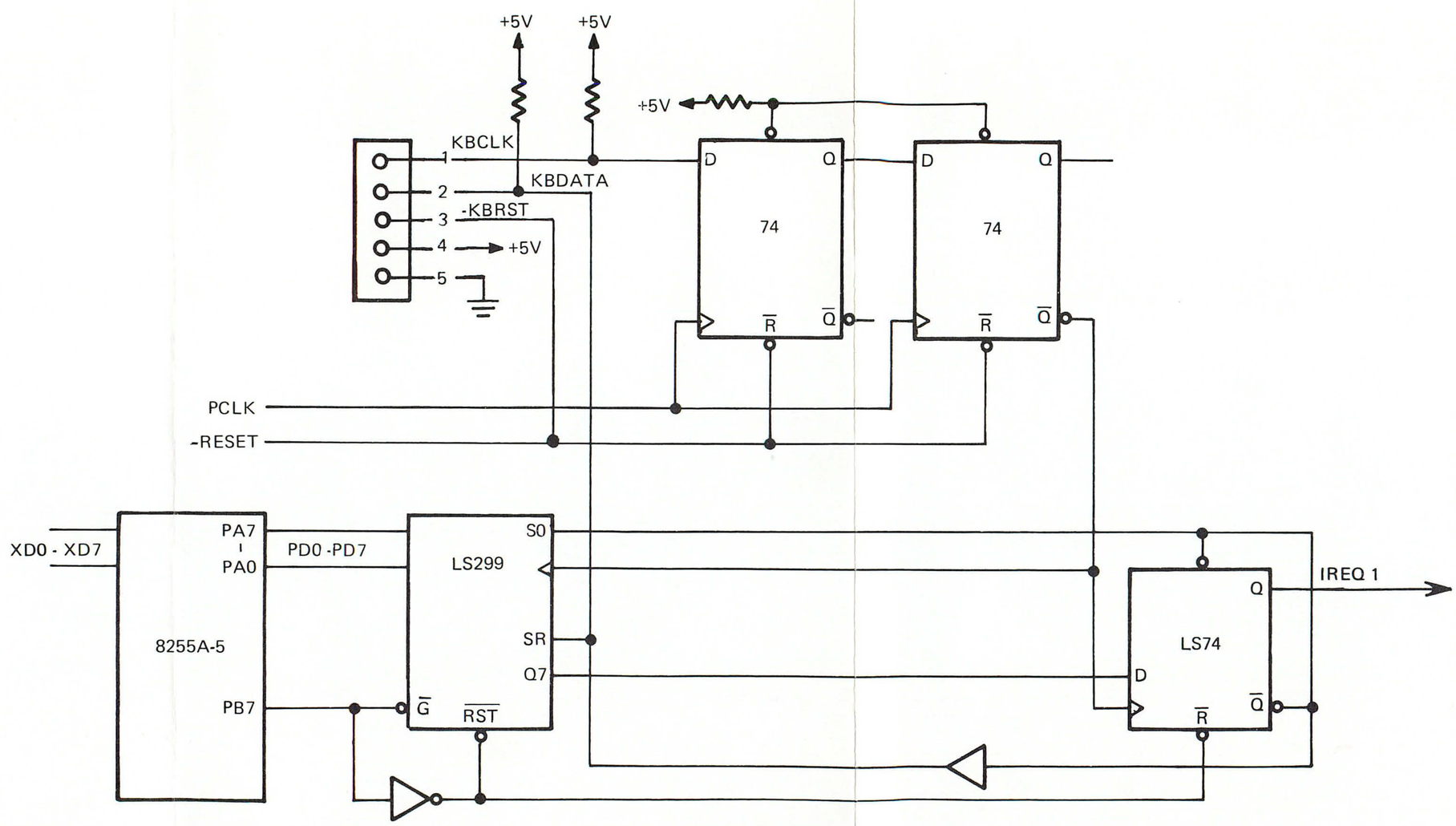
D7			Not used. This bit is always 0 (low).
D6	Control Mark	CM	During execution of the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D2	Scan Not Satisfied	SN	During execution of the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

Status Register 3

D7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D4	Track 0	TO	This bit is used to indicate the status of the Track 0 signal from the FDD.
D3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D1	Unit Select1	DSB	This bit is used to indicate the status of the Drive Select B signal to the FDD.
D0	Unit Select0	DSA	This bit is used to indicate the status of the Drive Select A signal to the FDD.

KEYBOARD INTERFACE

The keyboard interface circuit is illustrated below. A microprocessor within the keyboard assembly scans the keys and generates separate make (when the key is depressed) and break (when the key is released) codes. For example, the letter “Q”, is assigned a make scan code of 10 hexidecimal and a break code of 90 hexidecimal (break codes are formed by adding 80 hexidecimal to the make code. These NRZ scan codes are transmitted on the KBDATA line (via the keyboard’s coiled cable) to the keyboard interface circuitry on the system motherboard. (a complete list of all scan codes is provided in SECTION 3.)



KEYBOARD INTERFACE

Keyboard Interface Circuit

Each bit in a transmitted code is accompanied by a clock pulse on the -KBCLK line. This clock pulse is generated by the keyboard and is only active while scan codes are being transmitted or while the keyboard is undergoing a self-test. Data is transmitted at 9600 baud. When a complete scan code is received from the keyboard, Q7 on the LS299 goes high. This high is input to the LS74 D flip flop and an interrupt (IREQ1) is sent to the 8259A interrupt controller and subsequently to the 8088. The KBDATA line is immediately pulled low, preventing the keyboard from sending another character until the 8088 has processed the interrupt, read the current character, and reset the keyboard interface circuit in preparation to receive another character.

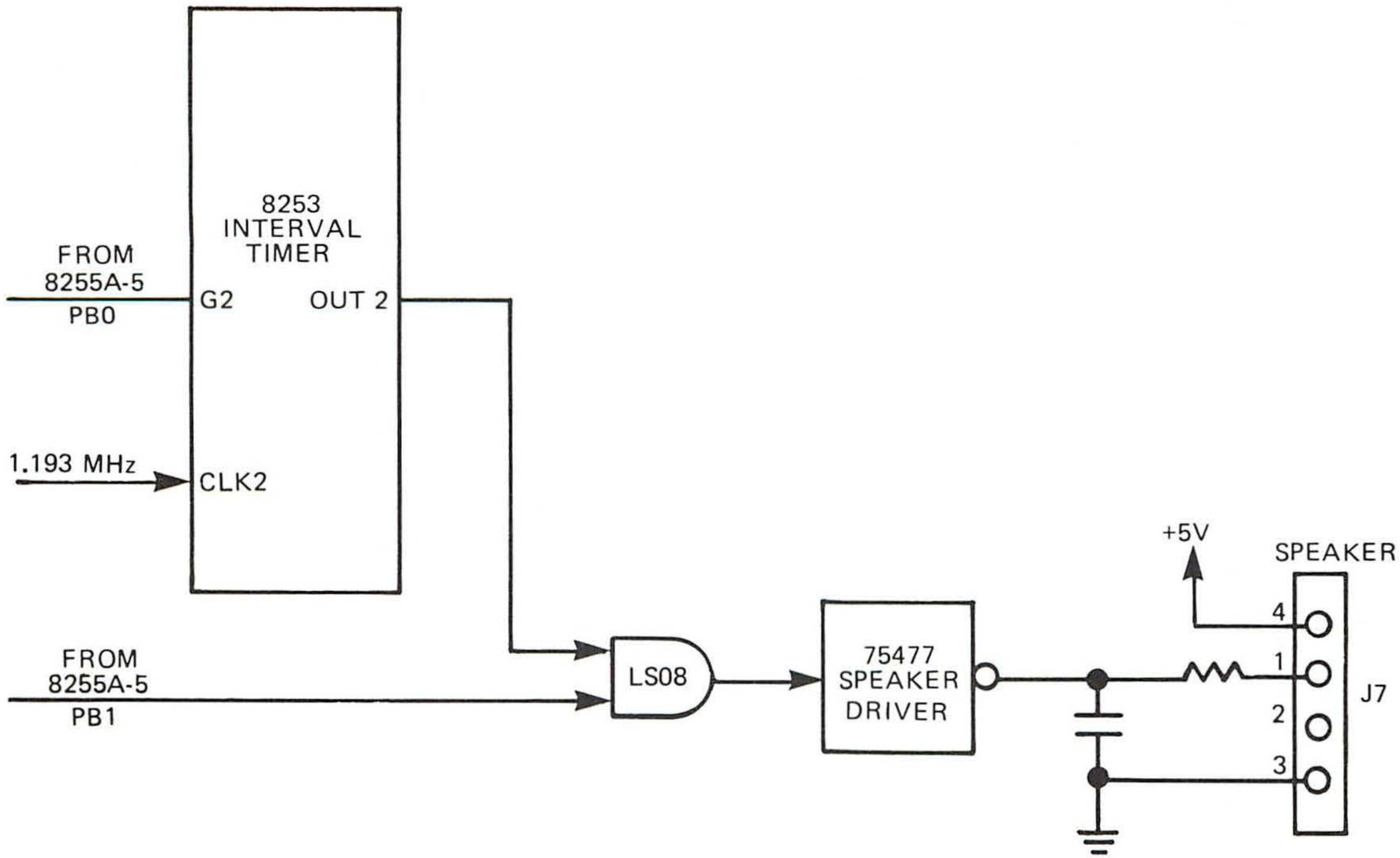
While waiting for the 8088 to become ready, the keyboard microprocessor continues to scan the keyboard switch matrix and to buffer any keypress scan codes. It also continues to monitor the KBDATA line. When KBRST goes inactive and the data line goes high, the keyboard transmits the next scan code.

The motherboard provides a connector for the keyboard on the rear panel of the system unit. Pin assignments for this connector and additional information on the keyboard itself are provided in Section 3.

SPEAKER INTERFACE

The speaker drive system is illustrated on the following page. As seen in the figure, either of two 8255A-5 parallel peripheral interface output bits (PB0 or PB1) can be used to control the output of the speaker. Both bits must be 1 to drive the speaker on.

To control frequency generation, bit PB1 from the 8255A-5 can be turned on and off. An easier method of speaker control, however, is to load a count or divisor value into Timer 2 of the 8253. Both 8253A-5 output bits, PB0 and PB1, are addressable via I/O port 61H.



Speaker Drive System

The 2-1/4" speaker connects to the motherboard via a 4-pin Berg connector. Pin assignments for the connector are as follows:

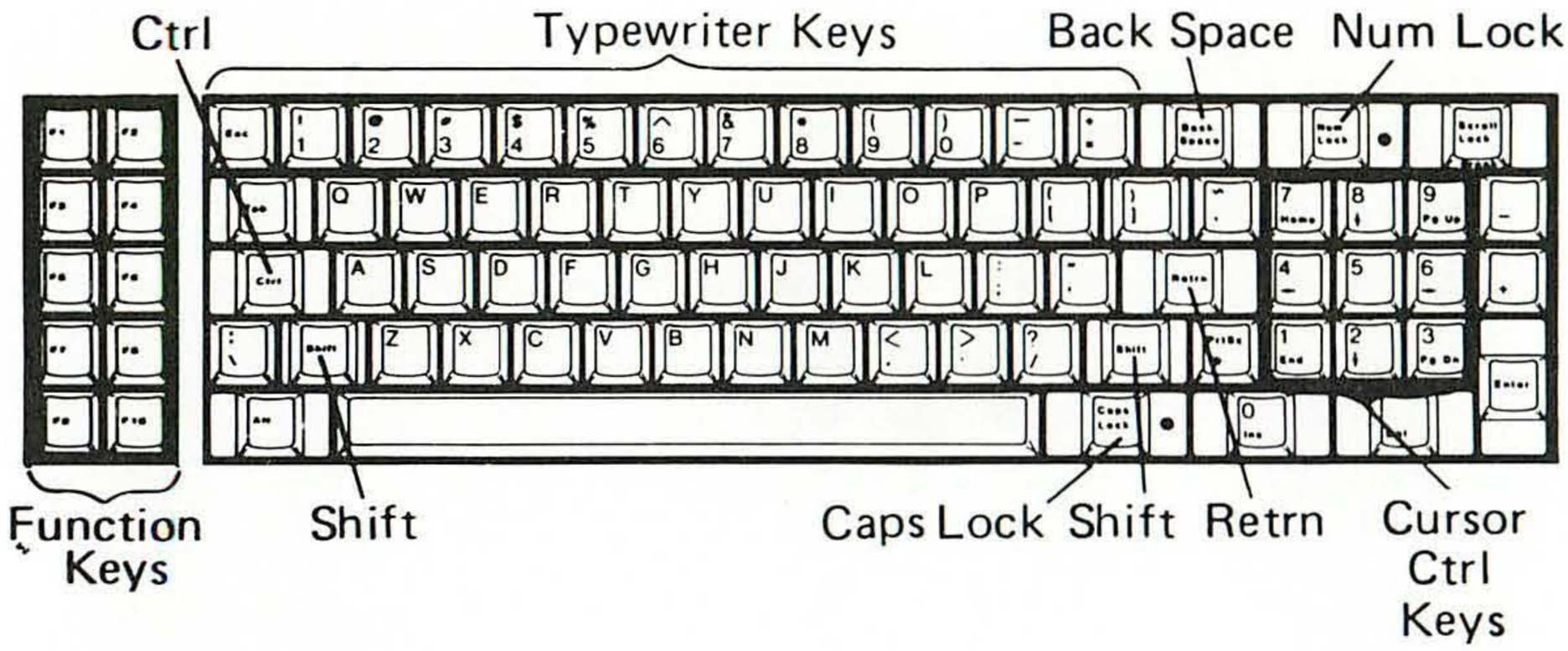
SPEAKER PIN ASSIGNMENTS

PIN	FUNCTION
1	DATA
2	KEY
3	GROUND
4	+5 VOLTS

3 - Keyboard

OVERVIEW

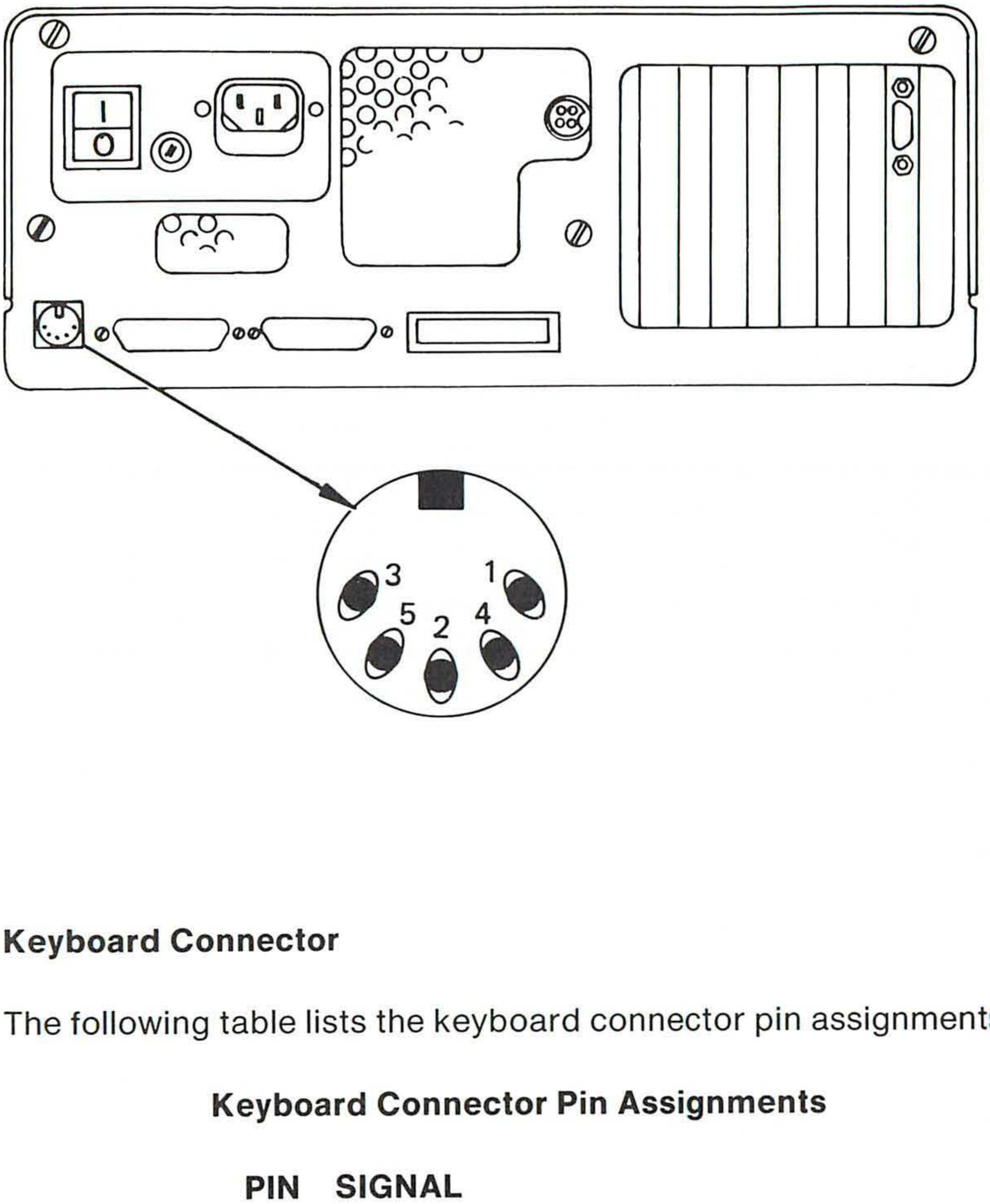
The system's tactile keyboard is a low profile, detachable design. Its 84 sculptured keys are arranged in four basic groups (see figure below). They are: (1) standard typewriter keys; (2) a numeric keypad; (3) cursor control keys and; (4) special function keys. The ten special function keys are completely programmable. When these keys are used in conjunction with the SHIFT, CONTROL, and ALTERNATE SHIFT keys, up to 48 unique functions can be assigned to the keyboard.



The Keyboard

KEYBOARD OPERATION

The keyboard communicates with the system via a six fool coiled cable. This cable mates with a six-pin, DIN connector mounted on the rear panel of the system unit. The following figure shows the location of the keyboard connector.



Keyboard Connector

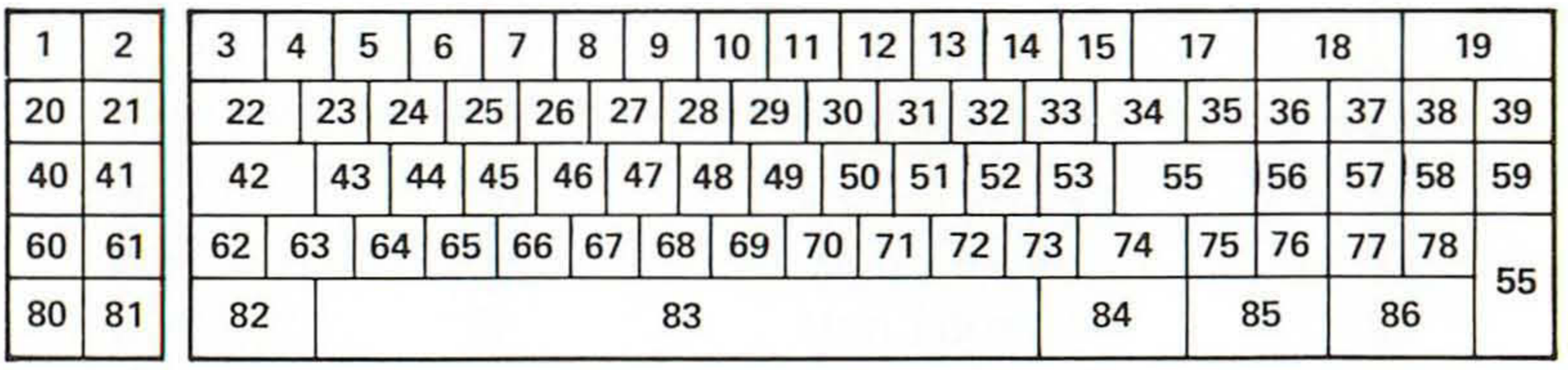
The following table lists the keyboard connector pin assignments.

Keyboard Connector Pin Assignments

PIN	SIGNAL
1	-KEYBOARD CLOCK
2	KEYBOARD DATA
3	-KEYBOARD RESET
4	GND
5	POWER (+5V)

The keyboard uses a capacitive switch technology. All the keys are momentary action keys which produce scan rather than ASCII codes. [Caps Lock] and [Num Lock] are electronically latching keys which use LEDs to indicate their state. The LEDs can only be turned ON or OFF by the keyboard. After power up or keyboard reset, the LEDs are set in the OFF condition.

An 8048 microprocessor within the keyboard assembly scans the key switch matrix on the board and generates separate make and break codes. For example, key #23, the letter "Q", is assigned a make scan code of 10 hexidecimal and a break code of 90 hexidecimal (break codes are formed by adding 80 hexidecimal to the make code). These NRZ scan codes are transmitted serially via the keyboard's coiled cable to the keyboard interface circuit on the system motherboard. Key number assignments are provided in the following illustration. A complete list of all scan codes is provided on the following page:



Key Number Assignments

KEYBOARD SCAN CODES

KEY NUMBER	KEY DESIGNATION	SCAN CODES MAKE	(HEX) BREAK
1	F1	3B	BB
2	F2	3C	BC
3	Esc	01	81
4	1 !	02	82
5	2 @	03	83
6	3 #	04	84
7	4 $	05	85
8	5 %	06	86
9	6 ^	07	87
10	7 &	08	88
11	8 *	09	89
12	9 (	0A	8A
13	0)	0B	8B
14	- _	0C	8C
15	= +	0D	8D
16	not used		
17	Back Space	0E	8E
18	Num Lock	45	C5
19	Scroll Lock	46	C6
20	F3	3D	BD
21	F4	3E	BE
22	Tab	0F	8F
23	Q	10	90
24	W	11	91
25	E	12	92
26	R	13	93
27	T	14	94
28	Y	15	95
29	U	16	96
30	I	17	97
31	O	18	98
32	P	19	99
33	[{	1A	9A
34	] }	1B	9B

KEYBOARD SCAN CODES (Continued)

KEY NUMBER	KEY DESIGNATION	SCAN CODES (HEX) MAKE	BREAK
35	\ ~	29	A9
36	Home 7	47	C7
37	8	48	C8
38	Pg Up 9	49	C9
39	-	4A	CA
40	F5	3F	BF
41	F6	40	C0
42	Ctrl	1D	9D
43	A	1E	9E
44	S	1F	9F
45	D	20	A0
46	F	21	A1
47	G	22	A2
48	H	23	A3
49	J	24	A4
50	K	25	A5
51	L	26	A6
52	; :	27	A7
53	, “	28	A8
54	not used		
55	Retrn/Enter	1C	9C
56	4 ←	4B	CB
57	5	4C	CC
58	6 →	4D	CD
59	+	4E	CE
60	F7	41	C1
61	F8	42	C2
62	\ |	2B	AB
63	Shift	2A	AA
64	Z	2C	AC
65	X	2D	AD
66	C	2E	AE
67	V	2F	AF
68	B	30	B0

KEYBOARD SCAN CODES (Continued)

KEY NUMBER	KEY DESIGNATION	SCAN CODES (HEX) MAKE	BREAK
69	N	31	B1
70	M	32	B2
71	, <	33	B3
72	. >	34	B4
73	/ ?	35	B5
74	Shift	36	B6
75	* PrtSc	37	B7
76	End 1	4F	CF
77	2 ↓	50	D0
78	Pg Dn	51	D1
79	not used		
80	F9	43	C3
81	F10	44	C4
82	Alt	38	B8
83	Space Bar	39	B9
84	Caps Lock	3A	BA
85	Ins 0	52	D2
86	Del .	53	D3

These scan codes are passed through the ROM BIOS keyboard routine where they are converted to the appropriate character and passed to the system or application program.

In addition to identifying and transferring scan codes, the electronic circuitry within the keyboard assembly performs such functions as auto repeat, key debounce, buffering of up to twenty scan codes, monitoring the scan code transfer handshake protocol, and a keyboard self-test.The keyboard performs self-test upon power-up or system reset and when requested by the 8088 CPU. Self-test includes RAM and ROM tests, a check for stuck keys, and a check for loop back errors and buffer overflow conditions. The self-test status byte returned to the system is defined as shown in the following table.

KEYBOARD STATUS AND ERROR CODES

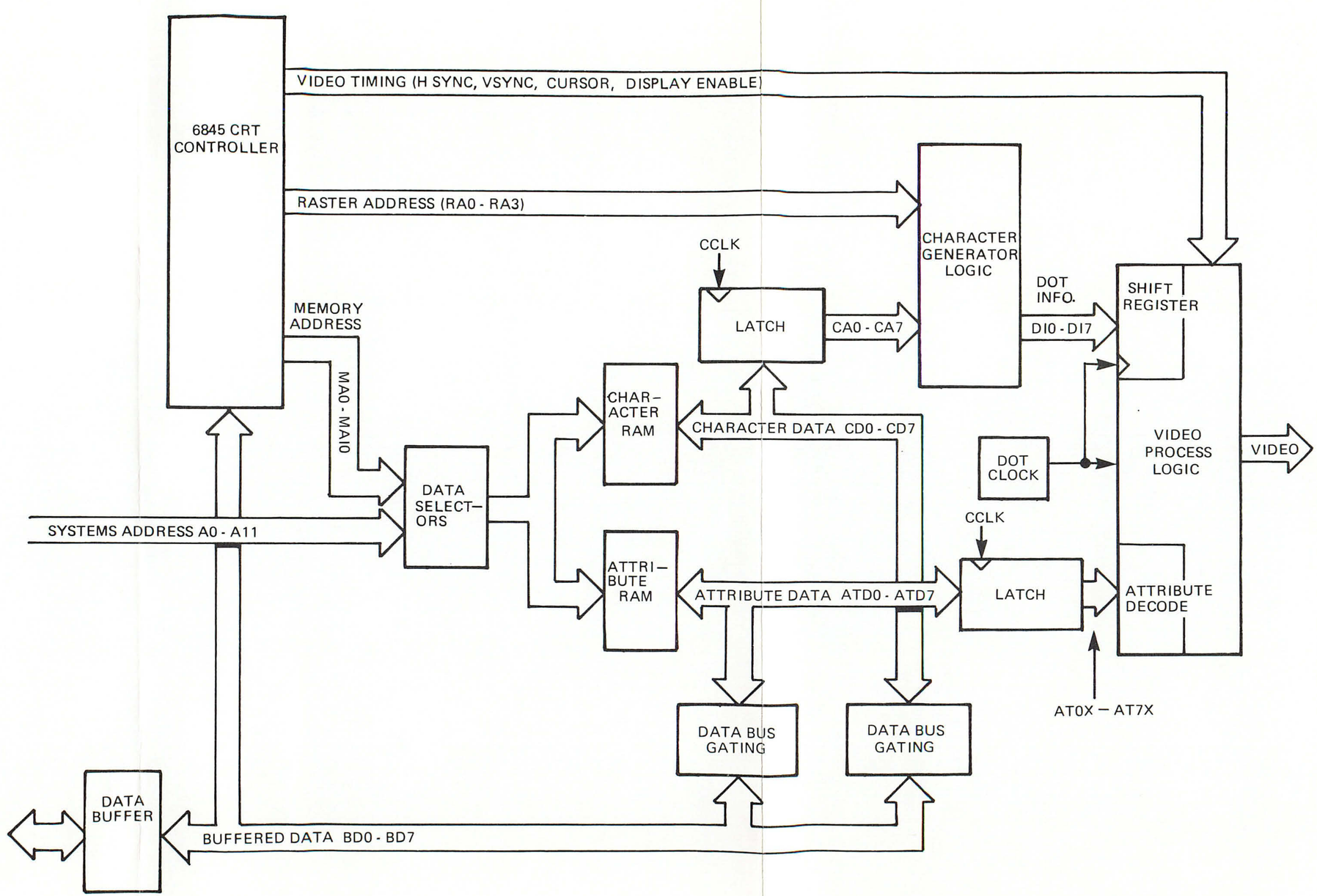
BIT NUMBER	VALUE	DEFINITION
Bit 0	0	Data memory (RAM) OK
	1	Bad data memory (RAM)
Bit 1	0	Program memory (ROM) OK
	1	Bad program memory (ROM)
Bit 2	0	Keyswitches are OK
	1	Keyswitch is stuck
Bit 3	0	Loop back test OK
	1	Loop back test error
Bit 4	0	No buffer overflow
	1	Buffer overflow
Bit 5	0	(not used)
	1	(not used)
Bit 6	0	(not used)
	1	(not used)
Bit 7	0	(not used)
	1	(not used)

4 - Monochrome Monitor

MONOCHROME MONITOR CONTROL BOARD

The monochrome monitor control board interfaces the system motherboard to the monochrome monitor. The control board design includes the MC6845 CRT controller. The display buffer comprises 4K bytes of static memory (no parity checking) that is dual ported and accessed directly from the CPU. The 8K bytes of character generator ROM contain 256 fonts for the character codes. A simplified block diagram of the monochrome monitor control board is shown below.

4-2



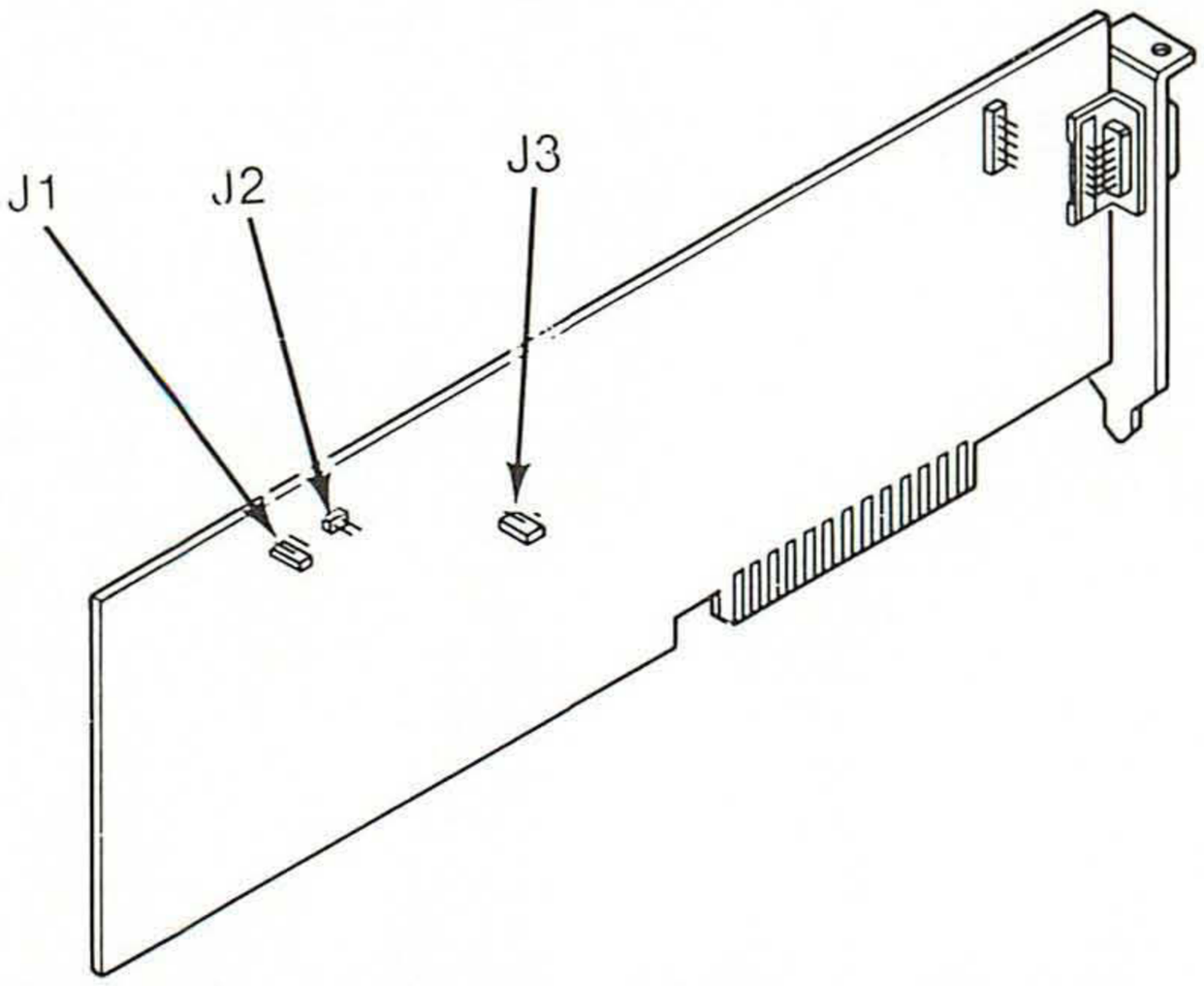
Monochrome Monitor Control Card Block Diagram

The monochrome display and display control board support the following features:

80 character x 25 line screen
9 x 14 character box
7 x 9 characters with descenders
256 characters in masked ROM
Programmable cursor size and blink
Character attributes:
- Reverse Video
- Character blank
- Character blink
- Underline
- Highlight

Jumpers

The monochrome board contains three jumpers, which modify the monochrome board to connect to monochrome or color monitors, and which specify an underline option. The following figure identifies jumper locations on the board.



Monochrome Board Jumper Locations

Jumper configuration is as follows:

JP1: 1 to pin 4: Sets the board dot clock to connect to a monochrome monitor. Leave jumpered in normal operation.

2 to 3: Sets the board dot clock to connect to a color monitor. Leave open in normal operation.

JP2: Sets the vertical sweep clock to drive a color monitor. Leave open for monochrome monitor.

JP3: 1 to 4: Sets the underline to appear at the eleventh row of the twelve-row character font dot matrix. Leave open in normal operation.

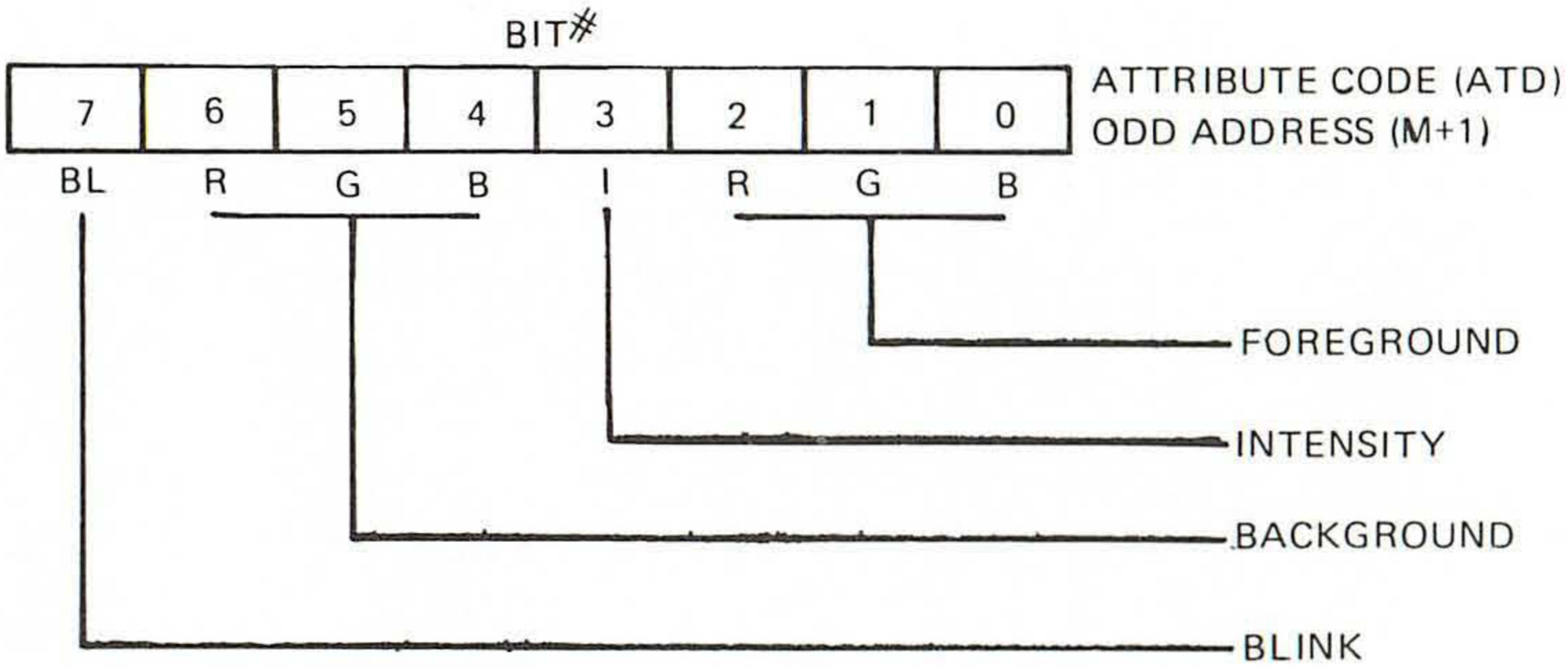
2 to 3: Sets the underline to appear at the twelfth row of the twelve-row character font dot matrix. Leave jumpered in normal operation.

Memory

Memory on the monochrome control card is divided into character memory and attribute memory. The character memory resides in memory locations with even addresses; the attribute memory resides in memory locations with odd addresses. Character memory starts at B0000H and attribute memory at B0001H.

The standard 4K bytes of memory support one screen of 25 rows of 80 characters plus a character attribute for each display character.

Character attribute codes are defined as follows:



BACKGROUND			FOREGROUND			
R	G	B	R	G	B	
0	0	0	0	0	0	NON DISPLAY
0	0	0	0	0	1	UNDERLINE
0	0	0	1	1	1	WHITE CHAR/BLACK BGND
1	1	1	0	0	0	REVERSE VIDEO

Character Attribute Codes

Read/Write Timing

At least one wait state is inserted on all memory accesses from the CPU. The CPU access to memory is synchronized with the character clock on the display control card; therefore, the duration of the wait states varies.

I/O Address

I/O addresses for the display control card range from 3B0H to 3BFH. The following table lists the read and write functions of each decoded address.

MONOCHROME CONTROL BOARD I/O ADDRESS FUNCTIONS

I/O ADDRESS	FUNCTION
3B0H	NOT USED
3B1H	NOT USED
3B2H	NOT USED
3B3H	NOT USED
3B4H	6845 INDEX REGISTER
3B5H	6845 DATA REGISTER
3B6H	NOT USED
3B7H	NOT USED
3B8H	CRT CONTROL PORT 1
3B9H	SET + LPENSTB
3BAH	CRT STATUS PORT
3BBH	CLR + LPENSTB
3BCH	NOT USED
3BDH	NOT USED
3BEH	NOT USED
3BFH	NOT USED

3B4H & 3B5H 6845 Internal Registers

The 6845 index and data registers are used to program the CRT controller to interface with the monitor. The index register is used as a pointer to address one of the remaining eighteen registers.

COLOR/GRAPHICS BOARD 6845 DATA REGISTERS

REGISTER NUMBER	FUNCTION	PROGRAM UNIT	I/O	40X25 ALPHA	80X25 ALPHA	GRAPHIC MODE
0	HORIZONTAL TOTAL	CHARACTER	WR	38H	71H	38H
1	H. DISPLAYED	CHARACTER	WR	28H	50H	28H
2	H. POSITION	CHARACTER	WR	2DH	5AH	2DH
3	H. WIDTH	----	WR	0AH	0AH	0AH
4	VERTICAL TOTAL	CHAR. ROW	WR	1FH	1FH	7FH
5	V. TOTAL ADJUSTMENT	SCAN LINE	WR	06H	06H	06H
6	V. DISPLAYED	CHAR. ROW	WR	19H	19H	64H
7	V. SYNCH POSITION	CHAR. ROW	WR	1CH	1CH	70H
8	INTERFACE MODE	----	WR	02H	02H	02H
9	MAXIMUM SCAN LINE	SCAN LINE	WR	07H	07H	01H
10	CURSOR START	SCAN LINE	WR	06H	06H	06H
11	CURSOR END	SCAN LINE	WR	07H	07H	07H
12	START ADDRESS H	----	RD/WR	00H	00H	00H
13	START ADDRESS L	----	RD/WR	XX	XX	XX
14	CURSOR ADDRESS H	----	RD/WR	00H	00H	00H
15	CURSOR ADDRESS L	----	RD/WR	XX	XX	XX
16	LIGHT PEN ADDRESS H	----	RD	00H	00H	00H
17	LIGHT PEN ADDRESS L	----	RD	XX	XX	XX

3B8H CRT CONTROL PORT (OUTPUT)

BIT	FUNCTION
0	+ HIGH RESOLUTION MODE
1	NOT USED
2	NOT USED
3	+ VIDEO ENABLE
4	NOT USED
5	+ ENABLE BLINK
6	NOT USED
7	NOT USED

Note that for proper initialization of the 6845 monochrome card, the first instruction issued to the card must set the +HIGH RESOLUTION MODE bit on CRT CONTROL PORT 1. The CPU must not access this card if this bit is not set.

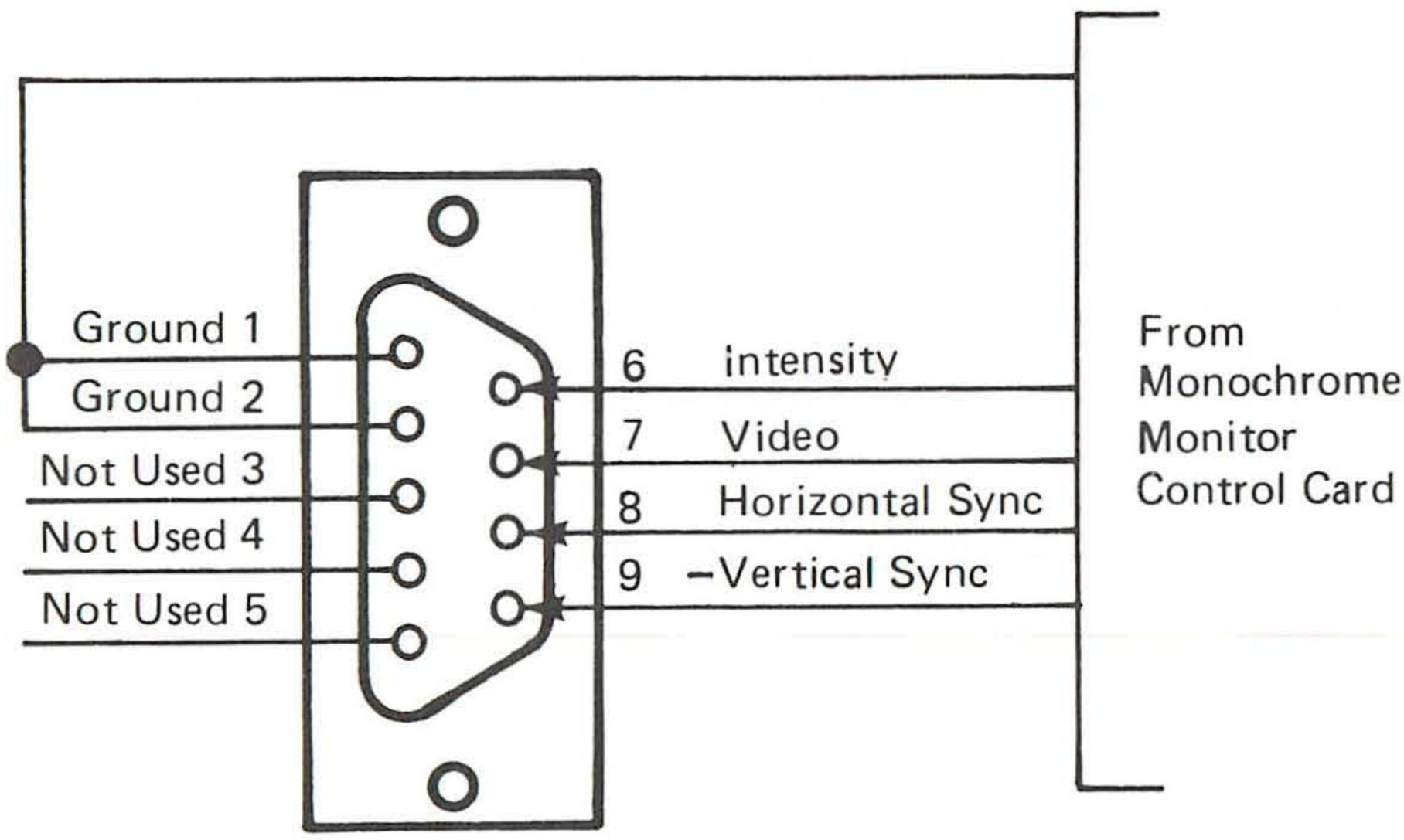
3BAH CRT STATUS PORT (INPUT)

BIT	FUNCTION
0	+ HORIZONTAL DRIVE
1	+ LPENSTB
2	+ LPENSW
3	+ B/W VIDEO
4	NOT USED
5	NOT USED
6	NOT USED
7	NOT USED

MONOCHROME MONITOR

The monochrome display unit uses a 14" (35.6cm), high-resolution raster scan CRT with a 18.432KHz horizontal sweep frequency and a 50 Hz noninterlaced vertical refresh rate to display 720 picture elements (pixels) on each of the 350 display scan lines.

The monochrome display is attached to the system unit via a three-conductor braided shield power cable and a six-conductor braided shield video cable. Both cables measure approximately 3 feet. The signal cable provides Ground, Intensity, Video, Horizontal Sync, and Vertical Sync signals from the monochrome display board typically installed in slot 5 of the system unit's expansion backplane connectors. Pin assignments on the signal connector are shown on the following page.



Monochrome Monitor Signal Connector Pin Assignments

The ITT XTRA switching power supply provides +15 to +18 volts of unregulated dc to the monitor through the power cable. Thus, whenever the switching power supply is powered on, the monitor is automatically turned on. Monochrome display specifications are provided in the following table.

MONOCHROME MONITOR SPECIFICATIONS

DISPLAY CHARACTERISTICS

CRT:	14" (35.6cm) diagonal, 90° deflection angle
Tilt:	From -5 to +25°
Swivel:	+/- 67° from left to right
Phosphor:	H39 (green) with anti-glare etched surface to reduce glare; H134 (amber) available as an option;
Resolution:	Horizonal - 720 dots Vertical - 350 dots
Display ARGA:	Test Pattern - Full screen of "H's" 234 mm +/-3 mm (W) 158 mm +/-3 mm (H)
Display Format:	7 x 9, in 9 x 14 dot matrix with lower case descender
High Voltage:	12.8 KV + 0.5 KV

INPUT SIGNAL

Video:	amplitude: TTL logic level active polarity: positive dot rate: 16.257 MHz pulse width: 61.5ns
Horizontal Drive:	amplitude: TTL logic level active polarity: positive frequency: 18.432KHz pulse width: 8.304us
Vertical Sync:	amplitude: TTL logic level active polarity: negative frequency: 50Hz pulse width: 868 us
Intensity Drive:	H = High intensity L = Half intensity dot rate: 16.25748MHz pulse width: 61.5ns

VIDEO AMPLIFIER

Small signal bandwith:	dc to 20 MHz (at -3dB points)
Gain:	20 + 2 dB
Rise, fall time:	10 ns

POWER SUPPLY

Voltage:	+15V to 18 Vdc
Current:	1.5 A dc max

0.8 A (nominal)

INTERFACE CABLES Six conductor, braided shielded cable with nine-pin D-type shielded connector (female)

Pin	1 GND
Pin	2 GND
Pin	3 NC
Pin	4 NC
Pin	5 NC
Pin	6 + INTENSITY
Pin	7 + VIDEO
Pin	8 + HORIZONTAL SYNC
Pin	9 - VERTICAL SYNC

POWER CABLE Three conductor, braided shield cable with four pin connector

Pin	1 GND
Pin	2 CHASSIS GND
Pin	3 NC
Pin	4 + 15Vdc to + 18 Vdc (unregulated)

5 - Color/Graphics Board and Monitor

COLOR/GRAPHICS CONTROL BOARD

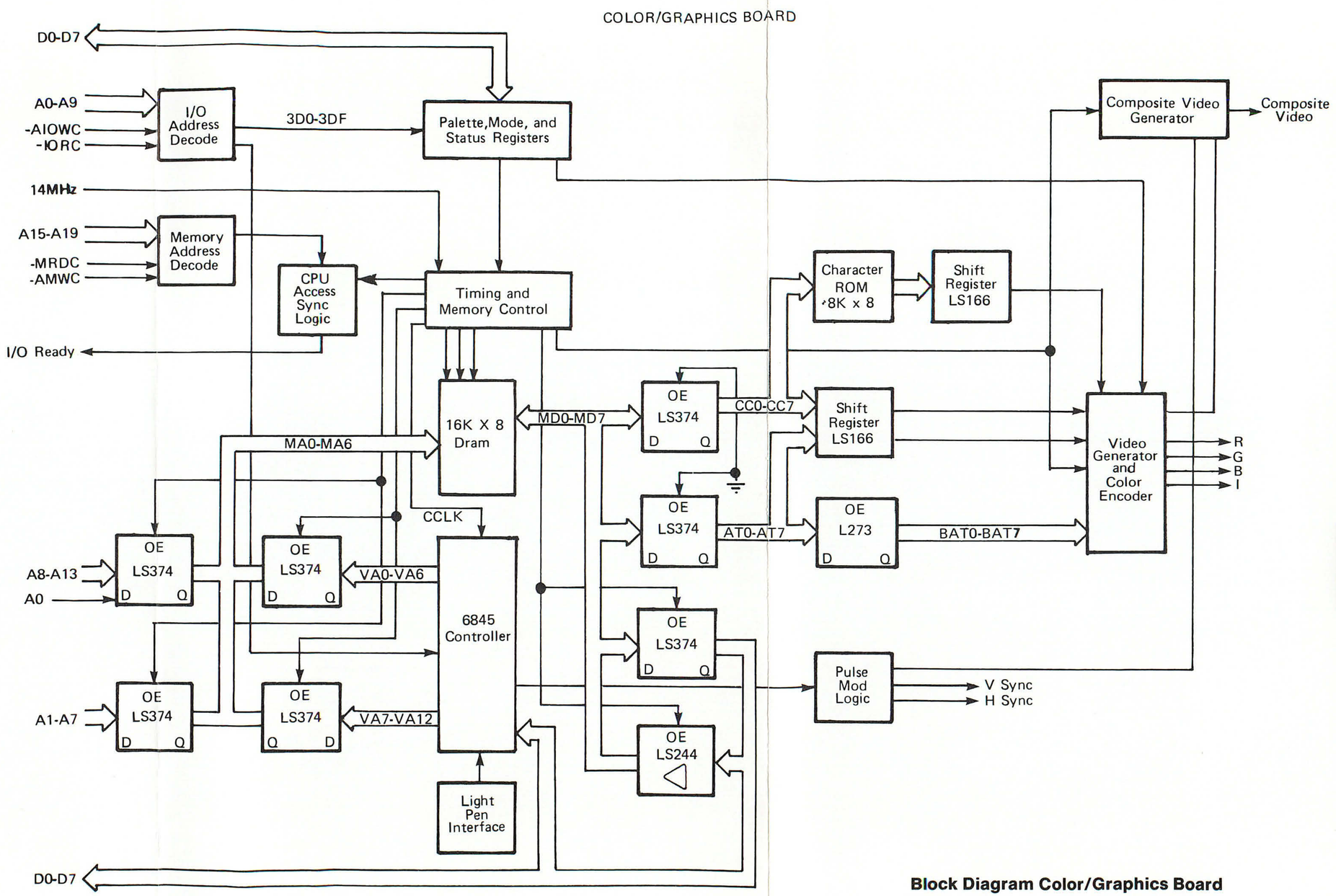
The ITT XTRA Color/Graphics board supports a variety of monitors designed for graphic and/or color presentation. The board features a 9-pin connector for RGB input monitors and a video jack for composite input monitors. An RF modulator interface and a light pen interface are also provided. A functional block diagram of the Color/Graphics board appears below

The color/graphics card provides two software-selectable modes: alphanumerics and graphics. These modes are supported by the use of a 6845 Video Timing Controller (VTC) and 16K bytes of dynamic RAM, starting at address B8000H. Information written into the memory is interpreted and then displayed under the control of the VTC. The interpretation of the data depends upon the currently selected mode.

Alphanumeric Mode

In alphanumeric mode, data in memory is interpreted as a character code and a corresponding attribute code in alternating bytes. One of the 256 character codes are selected to be displayed from a character ROM. Characters measure 7 x 7 in an 8 x 8 character box.

When displayed in Black and White mode, available attributes are Reverse Video, Blinking, and Bold. If displaying the color, up to 16 foreground and 16 background colors are available per character. If the blink enable software switch is set, the number of background colors is reduced to 8 but a blinking attribute becomes available.



Block Diagram Color/Graphics Board

The color/graphics card can be set to display either 25 lines of 40 characters each or 25 lines of 80 characters. Since there are 16K bytes of memory and each character uses two bytes (one for the code and one for the attribute), up to eight screens can be stored in memory in 40 x 25 mode. In 80 x 25 mode, up to four screens can be stored in memory. The border area of the screen can also be set to one of 16 colors.

Bit-Mapped Graphics Mode

In graphics mode two resolutions are available, 320 x 200 or 640 x 200. In 320 x 200 mode, two bits are used per pixel (picture element) and the 16K bytes of memory hold one screen at a time. In 640 x 200 mode, one bit is used per pixel so, again, the memory will hold one screen at a time. Using one bit per pixel means that in 640 x 200 mode, only one foreground and one background color are supported. Through the composite video output, this will appear as Black and White.

In 320 x 200 mode, three foreground colors are available per character from one of two palettes. The background color for the entire screen can be one of 16 colors.

Jumpers

The Color/Graphics board contains the following three jumpers:

JP1 - pin 1 to pin 4 = positive sync (normal setting)
pin 2 to pin 3 = negative sync

JP2 - shorted = single dot font
open = double dot font

JP3 - open (not used)

Software Interface

In addition to the 16K bytes of RAM on the board, starting at address B8000H, there are several I/O ports, starting at address 3D0H. The ports and their addresses are:

6845 I/O PORTS (COLOR/GRAPHICS BOARD)

ADDRESS	FUNCTION
3D1	6845 Data Register
3D2	Same as for 3D0H
3D3	Same as for 3D1H
3D4	Same as for 3D0H
3D5	Same as for 3D1H
3D6	Same as for 3D0H
3D7	Same as for 3D1H
3D8	Mode Control Register
3D9	Color Select Register
3DA	Status Register
3DB	Clear Light Pen Latch
3DC	Set Light Pen Latch
3DD	Not used
3DE	Not used
3DF	Not used

Each of the these ports is described in the following paragraphs (see the description given for ports 3DBH and 3DCH for the status port, bit 1).

6845 Video Timing Controller

The 6845 LSI chip provides most of the signals needed to drive a video display. The 6845 has 19 internal registers. One of these, the Address Register, is used as a pointer to the other 18 registers. To access one of the 18 Data Registers, the register number must first be loaded into the Address Register. The register can then be read or written by accessing the Data Register address. For example, to read Register 14, first write 0EH to address 3D0H, then read from address 3D1H.

The Data Registers, a brief description of their function, and their initialization values are listed in the following table.

COLOR/GRAPHICS BOARD 6845 DATA REGISTERS

REGISTER NUMBER	FUNCTION	PROGRAM UNIT	I/O	40X25 ALPHA	80X25 ALPHA	GRAPHIC MODE
0	HORIZONTAL TOTAL	CHARACTER	WR	38H	71H	38H
1	H. DISPLAYED	CHARACTER	WR	28H	50H	28H
2	H. POSITION	CHARACTER	WR	2DH	5AH	2DH
3	H. WIDTH	----	WR	0AH	0AH	0AH
4	VERTICAL TOTAL	CHAR. ROW	WR	1FH	1FH	7FH
5	V. TOTAL ADJUSTMENT	SCAN LINE	WR	06H	06H	06H
6	V. DISPLAYED	CHAR. ROW	WR	19H	19H	64H
7	V. SYNCH POSITION	CHAR. ROW	WR	1CH	1CH	70H
8	INTERFACE MODE	----	WR	02H	02H	02H
9	MAXIMUM SCAN LINE	SCAN LINE	WR	07H	07H	01H
10	CURSOR START	SCAN LINE	WR	06H	06H	06H
11	CURSOR END	SCAN LINE	WR	07H	07H	07H
12	START ADDRESS H	----	RD/WR	00H	00H	00H
13	START ADDRESS L	----	RD/WR	XX	XX	XX
14	CURSOR ADDRESS H	----	RD/WR	00H	00H	00H
15	CURSOR ADDRESS L	----	RD/WR	XX	XX	XX
16	LIGHT PEN ADDRESS H	----	RD	00H	00H	00H
17	LIGHT PEN ADDRESS L	----	RD	XX	XX	XX

Mode Control Register

This is a 6-bit write-only register. This port is used to switch between the various modes of the color/graphics card and resides at address 3D8H. The following table summarizes the functions of this port.

COLOR/GRAPHICS BOARD MODE CONTROL REGISTER

BIT	FUNCTION
0	Selects between 40 x 25 and 80 x 25 in alphanumeric mode. A "1" set the board to 80 x 25.
1	Selects between alphanumeric and graphics mode. A "1" selects 320 x 200 graphics mode.
2	Selects color or B/W mode. A "1" selects B/W. This bit affects only the composite output, not the RGB outputs.
3	A "1" enables the video signal to the monitor. A "0" disables the video signal.
4	A "1" selects 640 x 200 graphics.
5	This function is active only when in alphanumeric mode. When a "1", the blinking attribute is enabled, and bit 7 of the attribute byte becomes the blink attribute. As a result, the number of background colors is reduced from 16 to 8.

The following table lists the value loaded into the Mode Control Register for each mode.

6845 MODE CONTROL REGISTER

MODE	VALUE
I40 x 25 Alpha B/W	2CH
I40 x 25 Alpha Color	28H
I80 x 25 Alpha B/W	2DH
180 x 25 Alpha Color	29H
320 x 200 Graphics B/W	0EH
320 x 200 Graphics Color	0AH
640 x 200 Graphics B/W	1EH

Color Select Register

This is a 6-bit write-only register at address 3D9H. It is used to modify the colors displayed. The following table lists the functions of the bits.

BIT	FUNCTION
0,1,2,3	These bits select one of 16 colors for the screen border when in alphanumeric mode or the background if in 320 x 200 mode. It also selects the foreground color in 640 x 200 mode. Bit 0 selects blue Bit 1 selects green Bit 2 selects red Bit 3 selects intensity
4	When a "1", this bit will intensify the foreground colors in 320 x 200 graphics mode.
5	Used to select between two foreground palettes in 320 x 200 graphics mode. A "1" chooses the following palette:

C1	C0	COLOR
0	0	Background color selected by bits 0-3 of port 3D9H
0	1	Cyan
1	0	Magenta
1	1	White

A "0" chooses the following palette:

C1	C0	COLOR
0	0	Background color selected by bits 0-3 of port 3D9H
0	1	Green
1	0	Red
1	1	Yellow

C1 and C0 are the bits in memory representing a pixel.

Status Register

This is a 4-bit read-only register at address 3DAH. Bit functions are listed below:

BIT	FUNCTION
0	When this bit is set, the display buffer can be accessed without interfering with the display. This bit will be set for 19 usec at a time and is needed only when in 80 x 25 mode.
1	When this bit is set, it indicates that a positive-going edge from the light pen has set the light pen strobe into the 6845 VTC. This bit can also be set under software control by writing to port 3DCH. It can be reset by writing to port 3DBH. These actions are address decoded, so no specific data is needed.
2	This bit indicates the status of the light pen switch. A "0" indicates that the switch is on. The switch is not latched or debounced by the color/graphics card.
3	When set, this bit indicates that vertical retrace is occurring and, in 80 x 25 mode, a memory access will not disturb the display. This signal will be set for 1.02 msec at a time. After the signal goes low, there is an additional 900 usec in which memory can be accessed without disturbing the video.

Software Considerations in Alphanumeric Mode

To program the Color Graphics Board for alphanumeric mode, the Mode Control Register must first be set up as previously described. The 6845 VTC must also be set up in either 40 x 25 or 80 x 25 mode.

Registers 12 and 13, the Start Address Registers, do not have to be set to 00. They can be set to start the screen anywhere in memory. Note that the address entered into these registers is a word address and not a byte address. For example, if 25 were entered into these registers, the screen would start at word 25, i.e., byte 50. The end of memory is not a concern as the video pointer will wrap back to location 0 when the end of the 16K buffer is reached.

In alphanumeric mode, the memory is organized as alternating character code and attribute bytes. Therefore, each character on the screen corresponds to one word in memory, made up of a character code in the low even byte and an attribute code in the high, odd byte.

Character Code	Attribute Code
Even address, M	Odd address, M + 1

Attribute bits are interpreted as follows:

Bit	7	6	5	4	3	2	1	0
	I	R	G	B	I	R	G	B
	Background Color				Foreground Color			

I - Intensity
R - Red
G - Green
B - Blue

The blink enable bit is set in the Mode Control Register, bit 7 is changed from the intensity bit for background to the blinking attribute.

The available colors are:

I	R	G	B	COLOR
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White (High Intensity)

In Black and White mode, only black, white, and intensified white should be used.

When in 80 x 25 mode, if memory is accessed at any time other than during blanking, the video will be disturbed (see Status Register, bits 0 and 3).

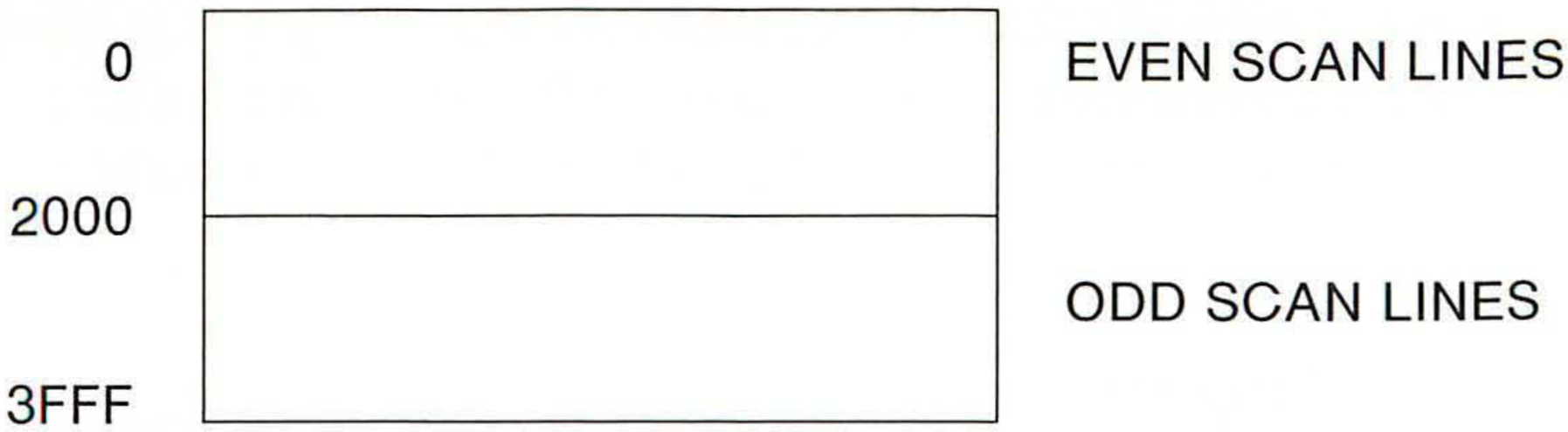
Software Considerations In Graphics Mode

To set up the color/graphics card, the Mode Control Register and the 6845 VTC must be set up properly as previously described. Registers 12 and 13, which set the start address, do not have to be set to 00. The Start address can be any value less than 1000H. This start address is a word address, not a byte address. For example, if 25 is entered into the Address Register, the screen starts at word 25, which is byte 50. This means that the screen can start only at even addresses.

The limit of 1000H in the Start Address Registers is a result of the way in which the Color/Graphics card's memory maps into the graphics screen. Due to limitations of the 6845 VTC, the memory corresponding to each odd scan line on the screen is offset by 2000H bytes from the memory corresponding to the preceding even scan line. The following table shows an example based upon a starting address of 0.

SCAN LINE	MEMORY ADDRESS
0	0H - 4FH
1	2000H - 204FH
2	50H - 9FH
3	2050H - 209FH
4	100H - 14FH

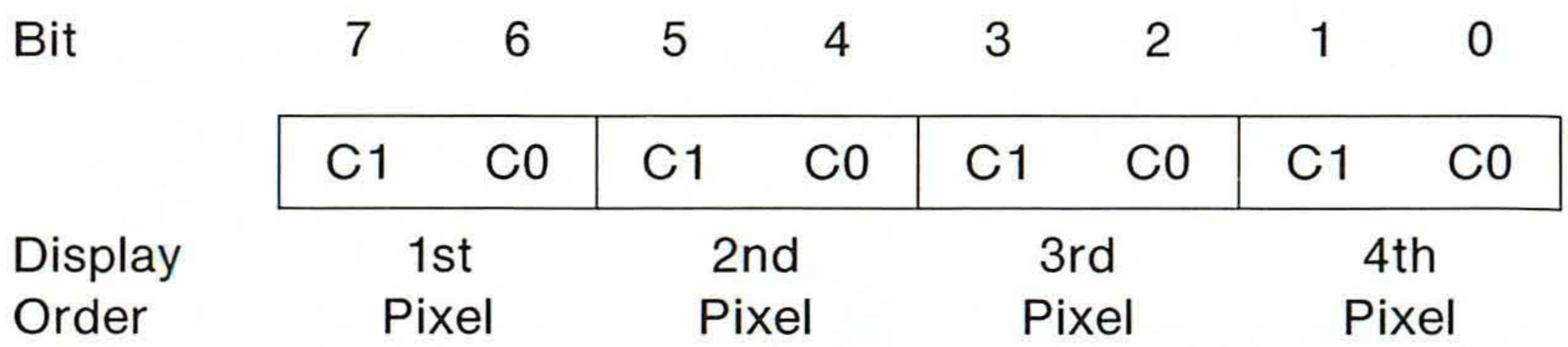
As a result, the memory is split as shown in the following figure:



So the highest starting address can be byte 1FFEH, which is word 0FFFH, and any value less than 1000H can be used in the Start Register. The end of the screen is of no concern as the pointer wraps back to zero when the end of memory is reached.

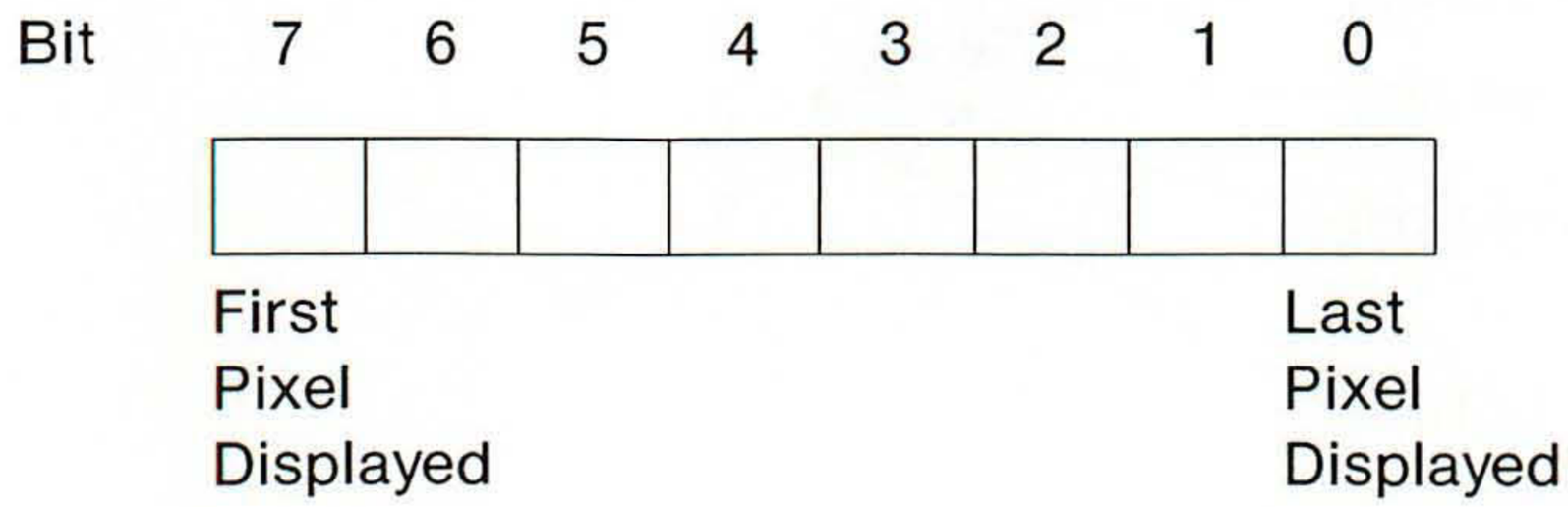
320 x 200 Graphics

When in 320 x 200 mode, two bits are used to encode each pixel, so each byte can represent four pixels as follows:



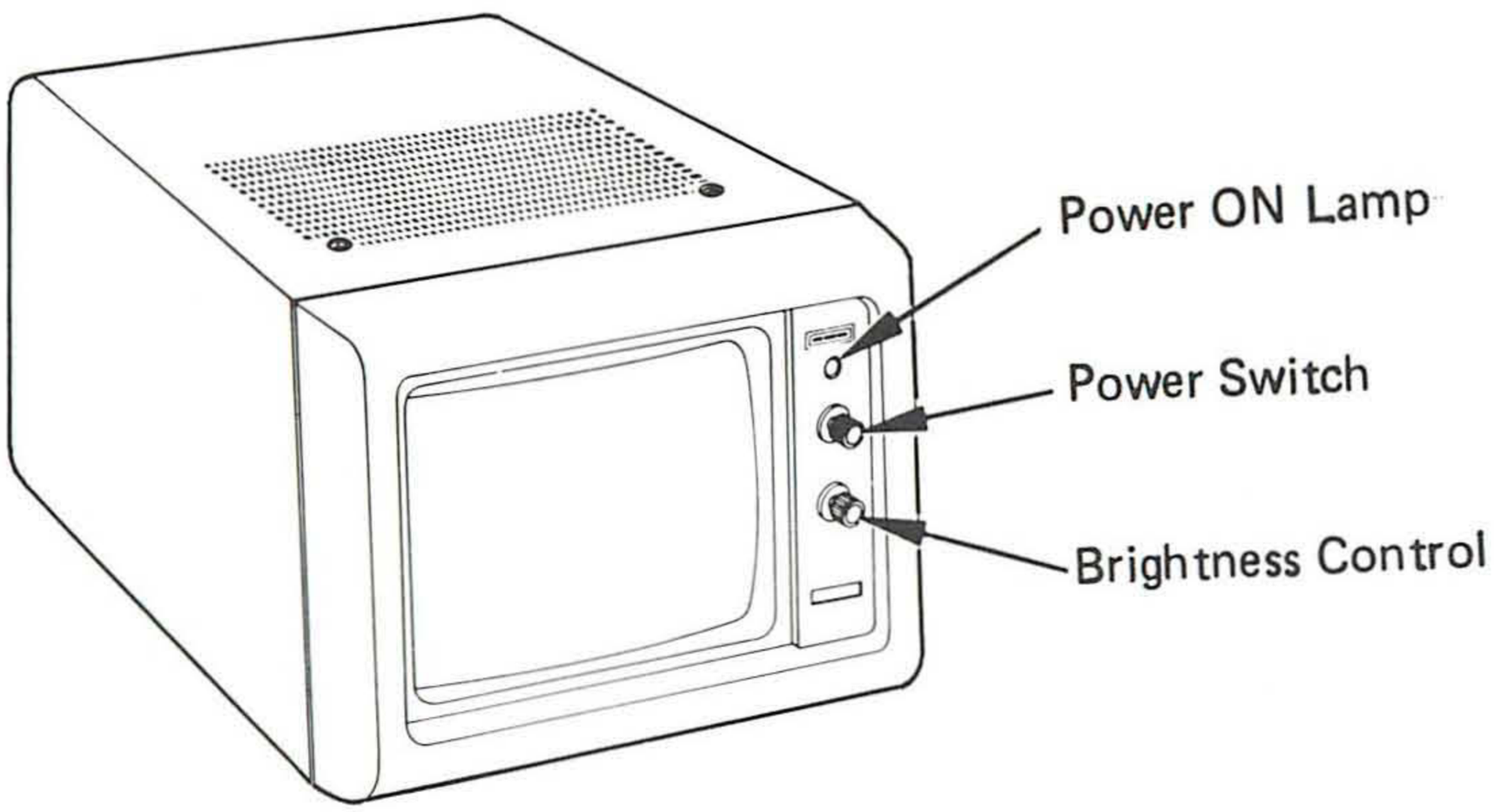
640 x 200 Graphics

In 640 x 200 mode, one bit is used to encode each pixel so each byte represents 8 pixels as follows:

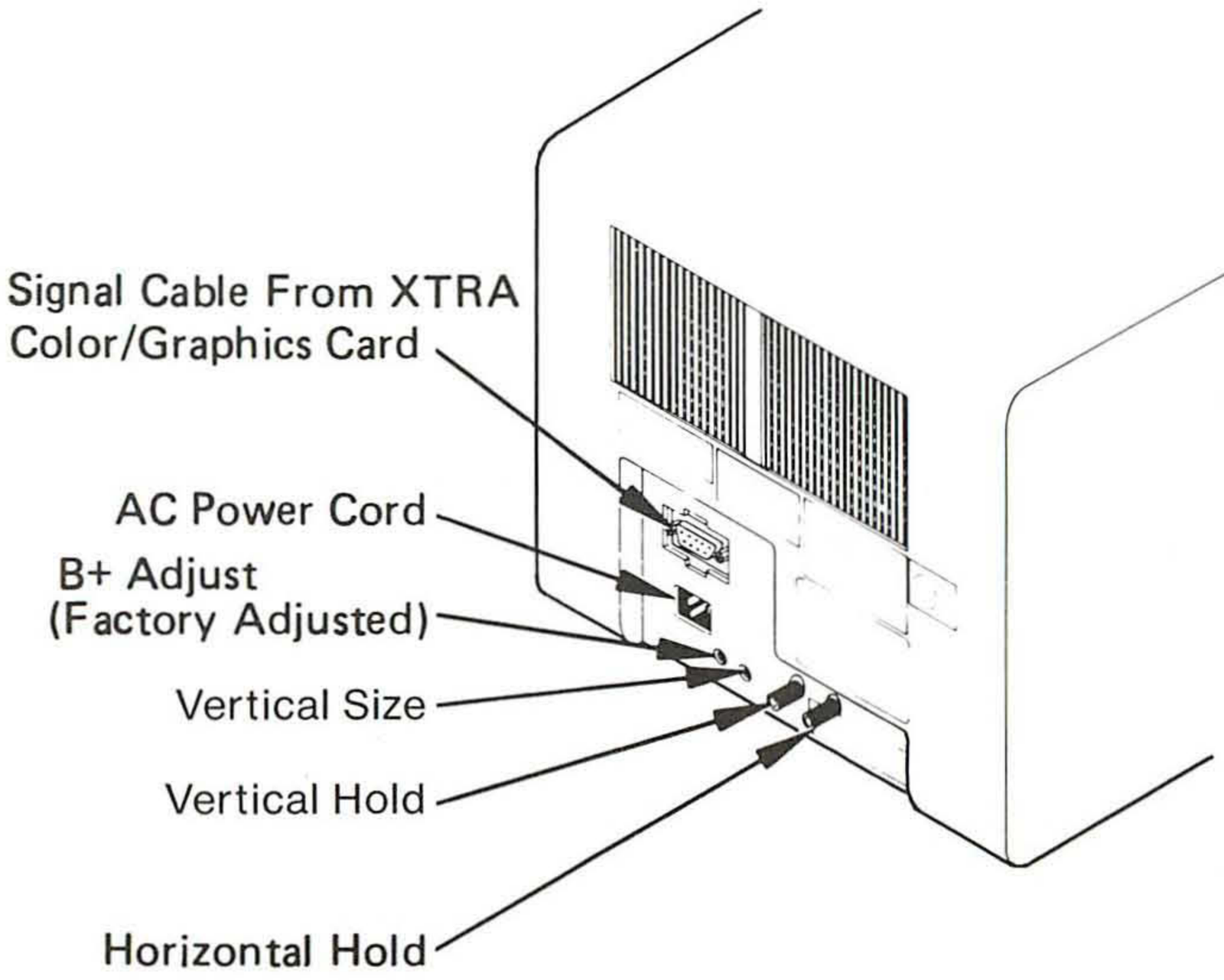


COLOR MONITOR

The ITT XTRA RGB Color Monitor is designed for use with the ITT XTRA Color/Graphics card. A signal cable with a 9-pin connector on each end connects the monitor to the color/graphics card. An AC power cord connects the monitor to a standard wall outlet. Front and rear controls are shown in the following figures:



Color Monitor Front Panel Indicators And Controls



Color Monitor Rear Controls

Color Monitor Specifications

CRT:	12-inch; dot type black matrix, nonglare
CRT Size:	28.1 cm wide, 22.2 cm high, and 32.2 cm diagonal
Active Display Area:	215W x 160H mm
Display Characters:	80 characters with 25 lines - 8 x 8 dots
Display Colors	Red, green, blue, cyan, yellow, magenta, black, white, and two intensity levels.
Dimensions:	37.7W x 28.0H x 41.8D cm
Weight:	12.0 kg
AC Cord:	1.9 m
Input Connector	9-pin "D" subminiature connector
Receivable Frequency Range:	**Video signal frequency**
Input Signal:	RGB direct drive system
Video Signal Input:	TTL level, positive
Ver./Hor. Sync:	TTL level, positive
Intensity:	TTL level, positive
Scanning Frequency:	Horizontal - 15.75kHz Vertical - 60 Hz
Active Video Period:	Horizontal - 48.0uS max Vertical - 14.61ms max
Resolution:	Horizontal - 690 dots Vertical - 240 lines, 480 lines (interlace)
Power Consumption:	67W
High Voltage Output:	24.0 kV
Power Supply:	120V, 60Hz

6 - 5.25" Floppy Disk Drives

SPECIFICATIONS

The ITT XTRA Disk Drive is a slimline double-sided, double-density, 40 cylinder unit. Performance, environmental, and reliability specifications are presented in the following tables:

FLOPPY DISK DRIVE PERFORMANCE SPECIFICATIONS

	SINGLE DENSITY	DOUBLE DENSITY
CAPACITY PER DISKETTE		
UNFORMATTED	250k bytes	500k bytes
FORMATTED	163k bytes	327k bytes
RECORDING DENSITY (Track 39)	2938 BPI	5876 BPI
TRACK DENSITY	48 TPI	48 TPI
NUMBER OF CYLINDERS	40	40
NUMBER OF TRACKS	80	80
RECORDING METHOD	FM	MFM
ROTATIONAL SPEED	300 RPM	300 RPM
TRANSFER RATE	125k bits/sec	250k bits/sec
LATENCY (AVERAGE)	100 ms	100 ms
ACCESS TIME		
AVERAGE	93 ms	93 ms
TRACK-TO-TRACK	6 ms	6 ms
SETTLING	15 ms	15 ms
STEP & SETTLE	21 ms	21
MOTOR START TIME	0.5 sec	0.5
HEAD ASYMMETRY	400 nsec max	400 nsec max

RELIABILITY SPECIFICATIONS

ERROR RATES	
SOFT ERROR RATE	ONE ERROR PER 109 BITS READ
HARD ERROR RATE	ONE ERROR PER 1012 BITS READ
SEEK ERROR RATE	ONE ERROR PER 106 SEEKS
MTBF	8000 POH UNDER TYPICAL USAGE (25% DUTY CYCLE)
PM	EVERY TWO YEARS
MTTR	30 MINUTES
COMPONENT LIFE	5 YEARS
MEDIA LIFE	3 x 106 PASSES/TRACK (30000 INSERTIONS)

ENVIRONMENTAL REQUIREMENTS

DC POWER REQUIREMENTS (AT DC POWER CONNECTOR J2)	VOLTAGE +12VDC +/-5% +5VDC +/-5%	MAX RIPPLE 100MV P-P 50MV P-P	CURRENT 0.8A TYPICAL 0.6A TYPICAL
POWER DISSIPATION	CONTINUOUS: STANDBY:	12.6W TYPICAL 3.5W TYPICAL	
TEMPERATURE	OPERATING +5 TO +43 degrees C 41 TO 111 degrees F	STORAGE* -10 TO +45 degrees C 14 TO 113 degrees F	
ENVIRONMENT RELATIVE HUMIDITY	20 TO 80%	8 TO 80%	
MAXIMUM WET BULB	+29 degrees C	NO CONDENSATION	
MECHANICAL DIMENSIONS (EXCLUSIVE OF FRONT BEZEL)	WIDTH HEIGHT DEPTH WEIGHT	149.3 mm (5.87 in.) 40.0 mm (1.57 in.) 203.2 mm (8.0 in.) 0.9 Kg. (2.0 lbs.)	

* IN ITT SHIPPING CONTAINER

5.25" DISK DRIVE OPERATION

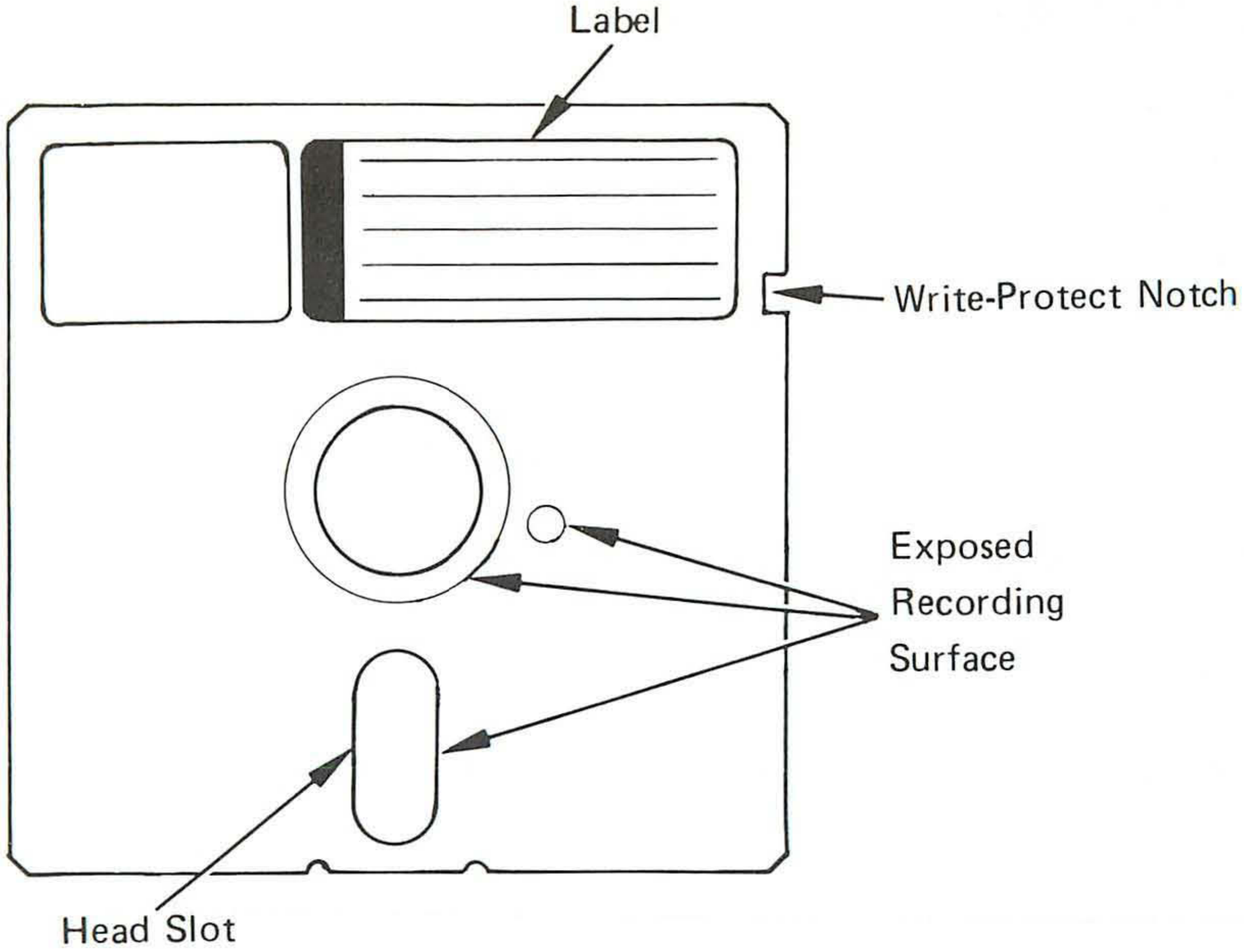
No read or write operation can begin until a diskette has been loaded into the drive. When the drive door lever is closed, the diskette is clamped to the drive hub of the spindle motor and the magnetic Read/Write head contacts the surface of the diskette through the diskette's head slot. A servo system ensures that the DC spindle motor maintains a constant speed of 300 revolutions per minute. An index sensor generates a digital pulse each revolution when it senses the index hole in the diskette.

The read/write head is located over the desired track by a highly accurate positioning mechanism. The Track 00 sensor generates a digital signal when the read/write head is positioned directly over track 0. If a write-protected diskette is inserted in the drive, the write-protect sensor signals the controller and the drive's write circuitry is disabled.

Data is recorded in 0.33 mm tracks. These tracks then undergo a tunnel erase process which reduces their size to 0.30 mm. During a read operation, flux reversals on the diskette are detected via a low-level read amplifier, low pass filter, differentiator, zero-crossing detector, and associated digitizing circuits.

DISKETTES

The disk drives use standard 5.25" (133.4 mm) double-sided, double-density, soft-sectored diskettes. The following figure illustrates the basic parts of a diskette.



Basic Parts of a Diskette

The flexible magnetic recording surface of the diskette is enclosed in a black protective jacket. The soft fabric lining on the inside of the jacket cleans the surface of the diskette as it spins. Openings are provided in the diskette jacket for the index hole, the drive hub, and the read/write head. The write protect notch can be covered with a small adhesive tab to protect the contents of a diskette from being altered or destroyed.

ELECTRICAL INTERFACE

The 142 disk drives interface with the system's motherboard via two connectors: a power connector (J2) which supplies the drives with the required +5 and +12 VDC, and a signal connector (J1) which interfaces the motherboard's floppy disk controller to the drives. Signal interface connections are shown below. A brief description of each of these signals follows:

Input Lines

The following paragraphs describe the eight active low TTL lines input to each 5.25" disk drive.

DRIVE SELECT 0, 1 (pins 6 and 10)

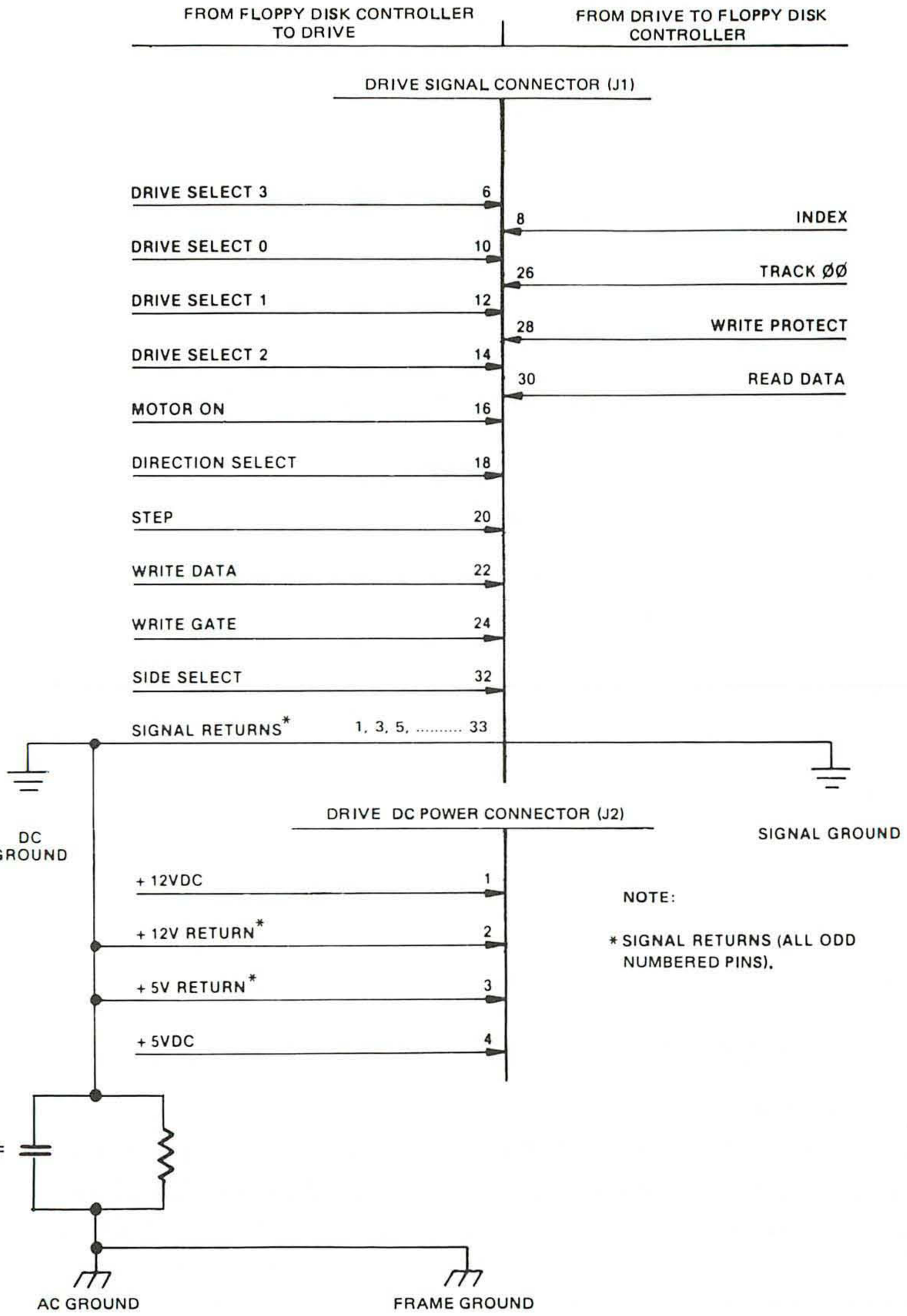
These two lines are used to select disk drive 0 (A) or disk drive 1 (B). Each drive is given its unique drive select address via pluggable jumpers DS0 and DS1. When the two pins of jumper DS0 are shorted, Drive 0 is activated by an active low signal on the DRIVE SELECT 0 line. When the two pins of jumper DS1 are shorted, Drive 1 is activated when the DRIVE SELECT 1 line is active low.

MOTOR ON (pin 16)

An active low level on this line turns on the drive's spindle motor. When the line is deactivated, the motor turns off.

DIRECTION SELECT (pin 18)

DIRECTION SELECT defines the direction of R/W head movement. A low level on this line causes the head positioning mechanism to move the R/W head toward the center of the diskette when the STEP line is pulsed. With the DIRECTION SELECT line at a high level, a pulse on the STEP line causes the head positioning mechanism to move the R/W head away from the center of the diskette.



Disk Drive Interface Connections

STEP (pin 20)

An active low level on this line causes the R/W head to be moved one track. The direction of movement is controlled by the DIRECTION SELECT line.

WRITE DATA (pin 22)

Data to be written on the diskette arrives on this line. Each transition of this line from a high level to an active low level causes the write current direction through the head to be reversed.

WRITE GATE (pin 24)

An active low level on this line enables the write current source, and disables the stepping (head positioning) circuitry. A high level on this line enables the read circuitry.

SIDE SELECT (pin 32)

SIDE SELECT defines which surface of a two-sided diskette is to be accessed for data recording or retrieval. An active low level on the line selects the R/W head for diskette side 1 (the diskette side facing the PCB); a high level selects the R/W head for diskette side 0 (the diskette side facing the disk drive chassis).

Output Lines

The following paragraphs describe the eight active low TTL lines output from each 5.25" disk drive to the disk controller:

INDEX (pin 8)

INDEX is provided by the selected drive once each diskette revolution. The leading (negative going) edge of the INDEX pulse indicates to the controller the beginning of a track.

TRACK 00 (pin 26)

An active low level on this line indicates that the R/W head is positioned at track 0.

WRITE PROTECT (pin 28)

An active low level on this line indicates to the disk controller that a write protected diskette (a diskette with a disable tab covering the write enable notch) is loaded. The drive inhibits write operations when a protected diskette is installed.

READ DATA (pin 30)

Data from the diskette is output to the host system on this line in the same form as it was received on the WRITE DATA line. Each flux reversal that is sensed on the diskette produces a transition to an active low level on the READ DATA line, and a return to a high level later.

7 - 5.25" Hard Disk

HARD DISK CONTROLLER BOARD

The Hard Disk Controller Board controls the operation of the optional 10Mb internal hard disk. The card plugs into one of the five I/O expansion slots on the ITT XTRA motherboard. Features supported by the Hard Disk Controller Board include:

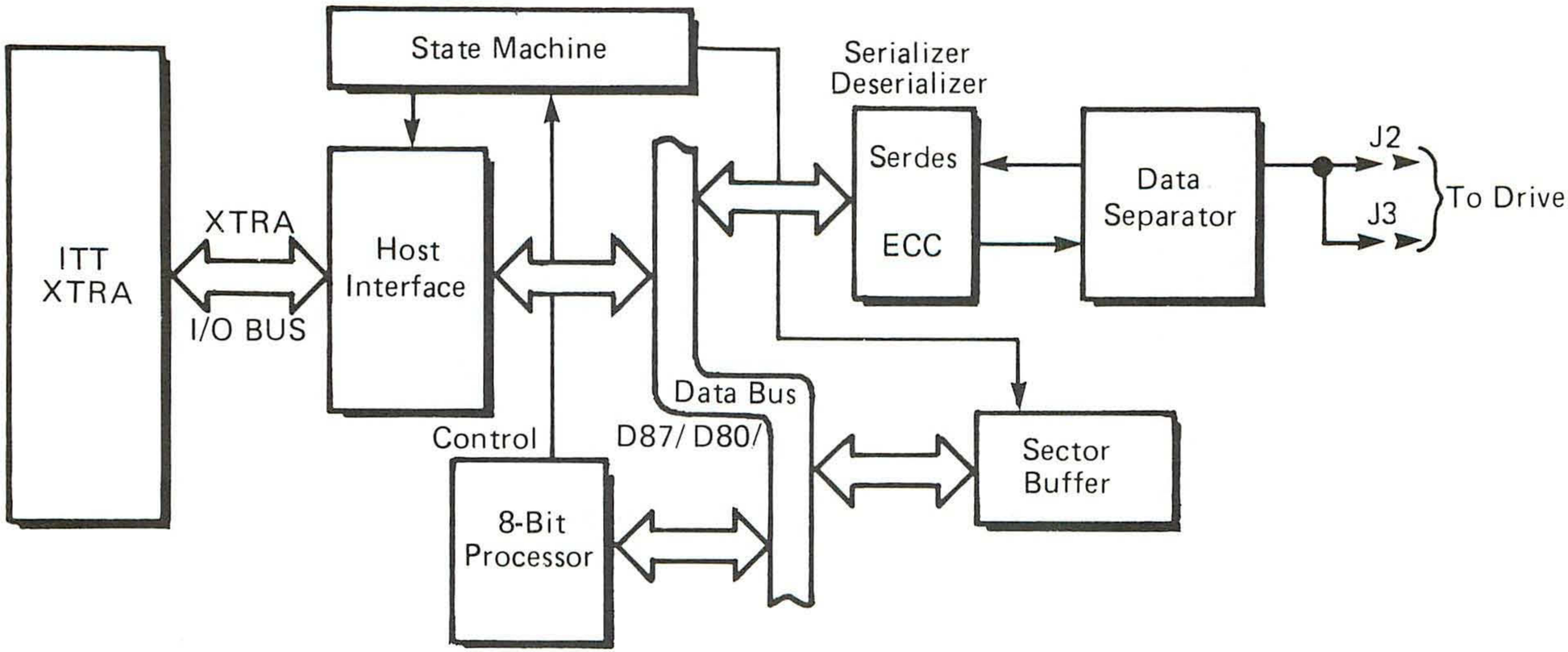
Interlocked data transfer
Microprocessor-based architecture
Full-sector buffering
Hardware 32-bit ECC polynomial with 11-bit burst correction
Data separator
Automatic retries during disk access
Internal diagnostics
Automatic burst error detection and correction
Separate sector format for ID and data fields with individual ECC fields for both the ID and data fields
High level command set
Overlapped seek for buffered-step drive options
ST506 interface to disk drive
Embedded servo support

The hard disk driver is contained in a ROM chip mounted on the hard disk controller card.

The major functional components of the hard disk controller board are shown on the following page. A brief description of each of these functional blocks follows.

HOST INTERFACE - The host interface connects the internal data bus to the ITT XTRA expansion I/O bus. The state machine controls the movement of data and commands through the host interface.

PROCESSOR - The eight-bit processor is the intelligence of the controller; it monitors and controls the operation of the controller.



Hard Disk Controller Board Block Diagram

STATE MACHINE - The state machine controls and synchronizes the operation of the host interface, SERDES, and sector buffer.

SERDES - The serializer/deserializer (SERDES) converts parallel data from the internal data bus to serial data for transfer to a selected disk drive. It converts serial data from the selected disk drive to parallel data which it places on the internal data bus.

DATA SEPARATOR - The data separator converts serial NRZ data to MFM for transfer to the selected disk drive. It converts MFM data coming from the selected disk drive to serial NRZ data for the SERDES.

SECTOR BUFFER - The sector buffer stages data transfers between the disk and the host to prevent data overruns.

Specifications

POWER:

VOLTAGE	RANGE	CURRENT
+5.0 Vdc	4.75 to 5.25 Vdc 2.0 A typ.	2.5 A max.
+12.0 Vdc	10.8 to 13.2 Vdc 48.0 ma typ.	66.0 ma max.

TEMPERATURE: 0 to 50 degrees Celsius

RELATIVE HUMIDITY: 10 to 95 percent noncondensing

ALTITUDE: Sea level to 10,000 feet

I/O Port Decoder

The two least significant bits of the address bus are sent to the host I/O port decoder. There are two sections to the decoder. One section is enabled by the I/O read signal (IOR-) and the other by the I/O write signal (IOW-). Thus, four read ports and four write ports are assigned to the disk controller board.

The AEN signal is asserted by the 8088 when DMA is in control of the data transfer. When AEN is asserted, the I/O port decoder is disabled. Read and write port functions are described in the following table:

HARD DISK CONTROLLER PORT ADDRESSES

READ PORT	FUNCTION
320	Read data (from controller to CPU)
321	Read controller hardware status (controller to CPU)
322	Read option jumpers (controller to CPU)
323	Not used

WRITE PORT	FUNCTION
320	Write data (from CPU to controller)
321	Controller Reset
322	Generate controller select pulse
323	Write interrupt and DMA mask register

Controller Hardware Status Bus Driver (To Host)

The controller hardware status is driven onto the ITT XTRA data bus when an I/O read is issued by the host program to controller read port 321H.

The bits in the controller hardware are defined as follows:

BIT	USAGE
7	Not used (MSB)
6	Not used
5	Interrupt pending (interrupt request flip-flop set)
4	DMA request pending (DMA request flip-flop set)
3	Controller busy (BUSY) This bit is asserted in response to the select signal. Busy remains asserted until 20 microseconds following the input of the status byte at the end of a command. Select must not be set active until Busy is inactive. Busy enables the data path and handshake signals between the controller and the CPU.
2	+Command/-Data 1=Command byte on data bus, 0=Data byte on data bus
1	+Hostin/-Hostout - transfer direction signal from the controller. 0 = Command or data information is being sent to the controller 1 = Status or data information is being sent by the controller
0	Request signal from the controller (REQUEST). If this bit=1, the request line is set by the controller indicating that a data or status byte is available from the controller during an input operation or when set on an output operation, the controller is ready to accept the next byte. The status of this signal is available as part of the hardware status so that the programmed I/O handshakes may be performed by the CPU. When the host transfers the byte of data, Request is cleared within 750 nsec from the end of the transfer. Do not send or receive bytes if REQUEST is not set.

NOTE: Not used bits may be high or low.

DMA And Interrupt Mask Register

This is a two bit register which is written into by the host when it writes to controller I/O port 323H. If neither bit 1 or 0 is active, the selected DMA and interrupt line to the host is set to the high impedance state.

The meaning of the bits in the Interrupt Mask Register is as follows:

BIT	USAGE
2 - 7	Not used.
1	This bit is tied directly to the direct clear of the interrupt request flip flop. When this bit is set it allows the interrupt flip flop to be set by the return status byte sent by the controller at the end of the command. By clearing this bit, the host can acknowledge the interrupt and clear out the interrupt request. The interrupt line (IRQ) is in the high impedance state when this bit is reset. NOTE: The Interrupt mask bit must be enabled before enabling the Interrupt bit on the host CPU. If this is not done, then false Interrupts can occur.
0	This bit is tied directly to the direct clear of the DMA request flip flop. When this bit is set, it allows the REQUEST signal from the controller to activate the DMA request signal to the host (DRQ) to complete a DMA data handshake. If reset, DRQ is in the high impedance state. NOTE: The DMA mask bit must be enabled before enabling the DMA channel on the host CPU. If this is not done, the data request line will not be driven while the host channel is active, and false handshakes can occur.

This register is cleared on a hardware reset (RESET line going high on the ITT XTRA bus) or a programmed reset (write to controller port 1), or by writing 0 into the register bits. Set the interrupt mask bit at beginning of CMD and reset before transfer of the status byte.

Read Option Jumpers

The option jumpers are driven onto the data bus when an I/O read is issued to controller port 322H. When a jumper is installed, it is read as a low (inactive); when a jumper is removed, it is read as a high (active) state.

The option jumpers are defined below:

BIT	USAGE
4 - 7	not used
3	jumper 1
2	jumper 2
1	jumper 3
0	jumper 4

Controller Bus Status Decode

The four possible combinations of the +command-data and +Hostin/-Hostout signals (valid only when REQUEST is active) from the controller's hardware status are as follows:

+C-D	+I-O	CONDITION
High	Low	Command mode, bus driven to the controller. This condition exists when the host is sending command information to the controller.
Low	Low	Data mode, bus driven to the controller. This condition exists when the host is sending data to the controller, by either programmed I/O or DMA modes.

High	High	Status mode, bus is driven by the controller. This condition exists when the controller is sending status information to the CPU. Transferring this byte terminates the command, and BUSY from the controller is set inactive. One byte is transferred at the end of each command. The interrupt line is set if enabled, when the byte is ready to transfer.
Low	High	Data mode, bus is driven by the controller. This condition exists when the controller is sending data to the host, under either programmed I/O or DMA modes.

Interrupt Request Flip Flop

The Interrupt Request flip flop is tied directly to the clear input of the interrupt mask and enabled by bit 1. The output of this flip flop is connected through a tri-state driver to the interrupt request line (IRQ) on the CPU I/O connector. This flip flop is enabled just before the controller transmits the return status byte at the end of each command. It is reset by either a hardware reset (e.g., bus RESET line goes high), programmed reset (e.g., write to controller port 1), or by clearing the interrupt mask bit 1.

DMA Request Flip Flop

This flip flop is set (if enabled by the bit 0 of the interrupt mask register) by the positive-going edge of the request line from the controller when data is being written to or read from the controller. The output of this flip flop is connected to the DMA request line (DRQ) through a tri-state driver. This flip flop is reset by the DMA acknowledge signal (DACK-) from the DMA channel. The flip flop is also reset by clearing the interrupt mask bit 0.

STATUS BYTE

One byte of status is passed to the host at the end of each command. The byte informs the host if any errors occurred during the execution of the command. If interrupts are enabled, then the controller will send an interrupt when ready to transfer the status byte.

After the byte is transferred, the command is completed, and BUSY from the controller is set inactive within 20 microseconds.

COMMAND SEQUENCE

Set busy
Issue six command bytes
Transfer data if required
Interrupt on status
Read status
Command complete

Commands

The following discussion describes communications between the controller and host from the point of view of the codes that are passed. The host sends commands to the controller; the controller then performs the commands and reports back to the host.

DEVICE CONTROL BLOCK

The processor sends a six-byte block, known as the Device Control Block (DCB), to the hard disk controller. This block contains all the information required by the controller to perform the designated command. The followng figure defines the contents of the Device Control Block.

Bit	7	6	5	4	3	2	1	0
Byte 0	Cmd class			Opcode				
Byte 1	LUN			Head Number				
Byte 2	Cyl. High			Sector Number				
Byte 3	Cylinder Low Number							
Byte 4	Interleave or Block Count							
Byte 5	Control Field							

BYTE 0 Bits 7, 6, and 5 identify the class of the command. Bits 4 through 0 contain the opcode of the command.

BYTE 1 Bit 5 identifies the logical unit number (LUN). Bits 4 through 0 contain the disk head number. Bits 7 and 6 are not used.

BYTE 2 Bits 7 and 6 contain the two most significant bits of the cylinder numbers. Bits 4 through 0 contain the sector number. Bit 5 is not used.

BYTE 3 Bits 7 through 0 contain the least significant 8 bits of the cylinder number.

BYTE 4 Bits 7 through 0 specify the interleave or sector count.

BYTE 5 Bits 7 through 0 contain the control field.

STATUS BYTE

At the end of a command, the hard disk controller returns a status byte to the processor. The following figure shows the format of this byte.

Bit	7	6	5	4	3	2	1	0
	0	0	d	0	0	0	ERR	0

Bits 0, 2, 3, 4, 6, and 7 are always set to 0.

Bit 1, when set, indicates that an error occurred during command execution.

Bit 5 shows the logical unit number of the drive (0 or 1).

If bit 1 of the status byte indicates that an error occurred, the controller requests sense status (see command Class 0, Opcode 03) to help identify why the error occurred.

CONTROL BYTE

The control field, byte 5, of the Device Control Block allows the user to select options for several different types and makes of disk drives. The format of this byte is as follows:

Bit	7	6	5	4	3	2	1	0
	r	a	0	0	0	s	s	s

where r = number of retries
a = retry on ECC error
s = step option

Bits 0-3 are used to encode the step option as follows:

Bit 3	2	1	0	OPTION
0	0	0	0	3 ms step rate
0	0	0	1	na
0	0	1	0	na
0	0	1	1	na
0	1	0	0	200 usec buffered step
0	1	0	1	70 usec buffered step
0	1	1	0	msec per step
0	1	1	1	3 msec per step

Bits 4, and 5 are set to zero.

Bit 6 - If set to zero on Read commands and if an ECC error is detected, a reread is attempted. If no error is detected on the reread, then the command completes with no error status. If an ECC error is detected on a reread, correction is attempted, and the result reported to the host. If this bit is set to 1, no reread is attempted, and correction is performed on all ECC errors.

Bit 7 - Disables the four retries by the controller on all disk-access commands. Set this bit only during the evaluation of the performance of a disk drive.

TEST DRIVE READY (CLASS 0, OPCODE 00)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	0
Byte 1	0	0	d	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where d = drive (0 or 1)
x = don't care

This command selects the drive specified by byte 1 of the DCB and reads back the status from that drive. If all status bits are in the correct state, the command will not return an error code. If the drive status is not correct, the command will return an error code, usually DRIVE NOT READY or DRIVE STILL SEEKING.

RECALIBRATE (CLASS 0, OPCODE 01)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	1
Byte 1	0	0	d	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	r	0	0	0	s	s	s	s

where d = drive (0 or 1)
r = retries
s = step option

This command will move the drive arm to the track 00 position. This command should only be used to attempt to correct a drive position error, since it is slower than a direct seek to track 0. Also, if retries are enabled, the controller will recalibrate automatically in case of error. The difference between this command and a direct seek to track 0 is that this command steps the drive one cylinder at a time looking for the signal TRACK 00 from the drive to become active. A direct seek to track 0 is faster because the controller steps the drive at the programmed step rate.

RESERVED (CLASS 0, OPCODE 02) - not used

REQUEST SENSE STATUS (CLASS 0, OPCODE 03)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	0	0	d	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where d = drive (0 or 1)
x = don't care

The status reported by this command corresponds to the drive addressed by Byte 1 of the DCB, i.e., separate status bytes are maintained for each drive. Status is updated after each command, so status clarifying an error previously reported to the host should be read before the next command to the same drive. Four bytes are sent to the host describing drive and controller status; the formats of these four bytes are as follows.

Bit	7	6	5	4	3	2	1	0
Byte 0	v	0	Error Type			Error Code		
Byte 1	0	0	d			Head Number		
Byte 2	Cylinder High					Sector Number		
Byte 3	Cylinder					Low		

where d = drive 0 or 1
v = valid address

When an error occurs on a multiple sector data transfer (read or write), the REQUEST SENSE STATUS command returns the address of the failing sector in bytes 1, 2 and 3. If the REQUEST SENSE STATUS command is issued after any of the FORMAT commands, then the address returned by the controller points to one sector beyond the last track formatted if there was no error. If there was an error, then the address returned points to the track in error.

The address valid bit in the error code byte (bit 7) is set only when the previous command required a disk address, in which case it is always returned as a one; otherwise, it is set to zero. For example, if a RECALIBRATE command is followed immediately by a REQUEST SENSE STATUS command, the address valid bit would be returned as zero since this command does not require a disk address to be passed in its DCB.

The following paragraphs list and describe the returned error codes.

Type 0 Error Codes

HEX CODE\DEFINITION

01 No index signal from the drive. This error occurs during any data transfer or format command if a normal drive select occurs, the drive is ready, but no index signal is detected from the drive within two revolutions of the disk.

02 No seek complete signal from the drive. This error occurs on nonbuffered seek processing if the controller does not receive the seek complete signal from the drive within one second following the last step pulse.

03 Write fault signal received from the drive. This error occurs if the controller detects an active write fault signal from the disk drive either at the completion of a sector data transfer or initially after a successful drive select and the drive indicates ready.

04 Disk drive not ready. This error occurs if the controller fails to receive the select signal from the drive, or the drive indicates not ready after selection.

05 Not used.

06 Track 00 not found. After stepping the drive 200 more steps than the number of cylinders during a recalibrate command, the track 00 signal was not received from the drive.

07 Not used.

08 Disk drive still seeking. This status is returned in response to a test drive ready command if a buffered step seek was issued to a drive and the drive has not returned the seek complete signal. Software must time the seek to insure no system hang occurs if the drive fails to return the seek complete signal. Treat a seek incomplete condition the same as error code 02.

09-0F Not used.

Type 1 Error Codes

10 ID field read error. During a data transfer or format command, address marks were detected, but the target sector was not found and an ECC error occured on one or more ID fields.

Media defects may be overcome by deleting the defective sectors from system use.

11 Uncorrectable data error in the data field. The controller detected a data error that could not be corrected using ECC.

12 Sector address mark not found. The controller did not detect an address mark (AM) from the drive within its timing window. An address mark is a special recording pattern preceeding the ID field of a sector. The AM is only written at format time. The AM tells the controller where a new sector starts. The error may occur during any data transfer or format commands. The error may mean that no address marks were detected on the track, or the target sector address mark was not detected.

13 Not used.

14 Target sector not found. The target sector was not located within two revolutions of the disk. This error usually occurs when there is a media defect in the address mark field of the target sector.

15 Seek error. After a seek, the target disk address did not match the ID address read from the disk. Either the cylinder or head bytes did not match.

16 Not used.

17 Not used.

18 Correctable data error. The controller detected a media error while reading that was corrected by ECC. This error code informs the host software that error correction has taken place. This is the only error where the data is passed to the host before returning the error status.

19 Track is flagged bad. The last data transfer command encountered a track that had been flagged defective using the format bad track command. Host software is responsible for ensuring that deleted tracks are never accessed.

1A-1F Not used.

Types 2 and 3 Error Codes

20 Invalid command. The controller has received an invalid command from the host.

21 Illegal disk address. The controller detected an address that is beyond the maximum range.

22 Illegal parameter. The controller detected an invalid passed parameter.

23-2F Not used.

30 RAM error. The controller detected a data error during the RAM sector-buffer diagnostic. Replace the controller.

31 Program memory checksum error. The controller was unable to obtain a match between the calculated and compare checksum values. This is caused by a defect in the program memory chip of the Controller. Replace the controller.

32 ECC polynomial error. During the controller's internal diagnostic, the hardware ECC generator failed its test. Replace the controller.

33-3F Not used.

FORMAT DRIVE (CLASS 0, OPCODE 04)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	0	0	0	Head Number				
Byte 2	Cyl. Hi			Sector Number				
Byte 3	Cylinder			Number low				
Byte 4	0	0	0	interleave				
Byte 5	r	0	0	v	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option
v = imbedded servo drive
interleave: 1 to 16 for 512 byte sectors

This command recalibrates the drive, then seeks to the starting address specified by bytes 1, 2, and 3 of the DCB. It times the spindle speed, divides the track into equal size sectors, and writes out address mark (AM) and header field for all sectors. The contents of the sector buffer are used for the data pattern of the sector data fields. The sector buffer can be initialized by the write sector buffer command (Opcode 0F) just before any format command. Note that if the format command gets a hard error while formatting a track, the format operation stops immediately and the error is reported. To continue, the host software must provide the data fields for all logical sectors following the sector in error, then continue with the format command at the beginning of the next track. Also note that the format operation always starts at the first sector of track, even though the address specified in the DCB did not point to a track boundry.

If bit 4 is set to one, the controller sets the format timing for an embedded servo drive. If bit 4 is set to zero, format timing is set for a conventional drive. Formatting with the bit set incorrectly will likely result in irrecoverable disk errors. In this case, the drive must be reformatted with bit 4 set properly. If the embedded servo format is selected, the firmware times the disk rotation, subtracts off a 300 microsecond gap for the servo area, and formats the track. This firmware will work properly with drives that have a servo area that is smaller than 300 microseconds preceeding index and 40 microseconds following the leading edge of the index pulse; and the worst-case spindle speed variation falls within 3536 +/- 3.0% RPM for an embedded servo drive, 3600 +/- 3.0% RPM for a conventional drive. All drives must maintain speed tolerance of +/- 1% after format.

READ VERIFY (CLASS 0, OPCODE 05)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	1
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi			Sector Number				
Byte 3	Cylinder					Number low		
Byte 4	Block count							
Byte 5	r	a	0	0	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option
a = retry option data ECC error

This command is identical to the Read command except no data transfer takes place. Starting at the initial address, the command verifies header and data ECC on the specified number of sectors. If an error occurs, the request sense bytes contain the sector number in error.

FORMAT TRACK (CLASS 0, OPCODE 06)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	0
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi			Sector Number				
Byte 3	Cylinder					Number low		
Byte 4	0	0	0	interleave				
Byte 5	r	0	0	v	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option
v = imbedded servo drive
interleave: 1 to 16 for 512 byte sectors

This command recalibrates the drive, seeks to the target track specified in byte 1, 2, and 3 of the DCB, and writes the ID and DATA fields with the interleave value specified in byte 4 of the DCB. This command can be used to clear the defective track bit, or to reformat one track that lacks data integrity on a drive. This command writes the contents of sector buffer as the data pattern of the data field. Note that the v bit must be set for embedded servo drives.

FORMAT BAD TRACK (CLASS 0, OPCODE 07)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi		Sector Number					
Byte 3	Cylinder Number low							
Byte 4	0	0	0	interleave				
Byte 5	r	0	0	v	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option
v = imbedded servo drive
interleave: 1 to 16 for 512 byte sectors

This command is the same as the format track command except that the bad track flag is set in the ID field. Data fields are not written. This command is used to prevent system access to defective tracks. Note that the v bit must be set for embedded servo drives.

READ (CLASS 0, OPCODE 08)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi			Sector Number				
Byte 3	Cylinder Number low							
Byte 4	Block count							
Byte 5	r	a	0	0	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option
a = retry option on data ECC error
interleave: 1 to 16 for 512 byte sectors

This command will read 1 to 256 sectors as specified by byte 4 of the DCB. The starting address is specified by byte 1, 2 and 3 of the DCB. If an error occurs during a multiple sector transfer, the transfer will terminate at the sector where the error occurs. For example, assume the user wants to read 10 sectors starting at sector address 10. If a correctable data error occurs at sector address 15, the controller completes the transfer of 6 sectors, including the sixth one because the data was corrected. It terminates the read operation and set the completion status byte error bit high. The host issues request sense command to determine what error has occured. To continue the operation, the host calculates the difference between sectors desired and sectors completed. In this case, six out of ten are completed; therefore, the host should issue a second read command of four remaining sectors at starting sector address sixteen. If any other error code occurred, the data is not returned to the host, so the retry logical address is one sector less, and the retry sector count one sector more than the continuation after a correctable data error. In the previous example, the restart sector address is 15, and the transfer length is five sectors for any error other than a correctable data error.

RESERVED (CLASS 0, OPCODE 09) - not used.

WRITE (CLASS 0, OPCODE 0A)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	0
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi		Sector Number					
Byte 3	Cylinder					Number low		
Byte 4	Block count							
Byte 5	r	0	0	0	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option

This command will write from 1 to 256 sectors as specified by byte 4 of the DCB, starting at the address specified by bytes 1, 2 and 3 of the DCB. The multiple sector transfer scheme works the same as the READ command. Each sector of data is 512 bytes long.

SEEK (CLASS 0, OPCODE 0B)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	1
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi		x	x	x	x	x	x
Byte 3	Cylinder					Number low		
Byte 4	x	x	x	x	x	x	x	x
Byte 5	r	a	0	0	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option

This command initiates a seek to the track and selects the head number specified in the DCB. The drive must be formatted.

For drives employing buffered step seeks, seek commands can be overlapped. After the controller issues a seek to the drive, it returns with a completion status, not waiting for the drive to complete the seek. If the return status shows no error, then the seek was issued correctly. If there is an error, then the seek was not issued. After transferring the status, another command can be issued to either drive. If a new command is received for a drive with an outstanding seek, then the controller will wait, with busy active, for the seek to complete before executing the new command (Except Drive Ready Command). There is a 500 millisecond timeout on this wait. If the Seek does not complete, a Seek Timeout error (Hex 02) is returned.

The Test Drive Ready command can be used with overlapped seeks to determine when a drive has completed seeking before issuing the next command. If the drive is still seeking, the status byte at the end of the command will indicate an error, and the sense status will indicate drive still seeking (type 0 error, code 8). A sequence of Test Drive Ready commands can thus be used to determine when the drive is ready for the next command.

Byte 5 of the DCB of this command instructs the controller what type of seek algorithm to execute for this drive. There are currently five different seek types supported in this firmware, both buffered and nonbuffered modes. Buffered step drives are supported at 15, 30, 70, or 200 microseconds per step. Buffer step means the drive has seek intelligence built-in. It can accept step pulses at a fast rate, typically under 200 microseconds per step. After the controller stops sending the drive step pulses (i.e., the drive does not receive any more pulses within its timeout limit), the drive seeks based on its own stepping algorithm (typically from firmware built into the drive). This scheme allows the controller to finish the command without having to process the physical seek operation, making overlapped seeks possible. The last step rate is default 3 ms per step. This is used on all nonbuffered drives.

INITIALIZE DRIVE CHARACTERISTICS (CLASS 0, OPCODE 0C)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	0	0
Byte 1	0	0	d	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where d = drive (0 or 1)
x = don't care

This command enables the user to configure the controller to work with drives that have different capacities and characteristics. Drive 1 and Drive 0 can be initialized for different drive parameters.

After the host sends the command (DCB) to the controller, it then sends an eight-byte block of data that contains the drive parameters. Some of the parameters occupy two bytes; all two-byte parameters are transferred with the most significant byte (MSB) first. The eight bytes are listed below.

Maximum number of cylinders (2 bytes)
Maximum number of heads (1 byte)
Starting reduced write current cylinder (2 bytes)
Starting write precompensation cylinder (2 bytes)
Maximum ECC data burst length (1 byte)

When the controller is powered up or reset, the default values listed below are set.

Maximum number of cylinders = 306
Maximum number of heads = 4
Starting reduced write current cylinder = 306
Increase write precompensation cylinder = 306
Maximum ECC data burst length = 11 bits

The parameter for the maximum ECC burst length defines the length of a burst error in the data field that the controller will correct. The burst length is defined as the number of bits from the first error bit to the last error bit. For example, the controller detected a 5-bit ECC error and the erroneous data appeared as C5 (1100 0101) before correction and could appear as D4 (1101 0100) after the correction. However, if the host has set the maximum ECC burst length at 4 bits, the controller would have to flag this data field as uncorrectable. This is a type 1, code 1 error.

READ ECC BURST ERROR LENGTH (CLASS 0, OPCODE 0D)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	0	1
Byte 1	x	x	x	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where x = don't care

This command is only valid following a Correctable Data Error (Error Code 18 Hex). It will transfer one byte to the host indicating the length of the error corrected. The error length is determined by counting the number of bits between the first and the last bit in error, including the first and the last bits.

For example, assume the drive is formatted with the default format data pattern 6C Hex. The first two bytes expanded to the binary level have the pattern - 0110 1100 0110 1100. This is the two byte pattern stored on the disk. Now, if the data read back from the disk has an eror, then:

		ERROR BURST LENGTH
CORRECT PATTERN :	0110 1100 0110 1100	0
READ BACK PATTERN :	0111 1100 0110 1100	1
READ BACK PATTERN :	0111 1100 1110 1100	6
READ BACK PATTERN :	0111 1100 0110 1110	12

Of the three patterns read, the first and second patterns are correctable because the error bit span is less than or equal to 11 bits. The third pattern is uncorrectable since it exceeds the controller's correction capability, which is 11 bits.

READ DATA FROM SECTOR BUFFER (CLASS 0, OPCODE 0E)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	0
Byte 1	x	x	x	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where x = don't care

This command transfers the 512 bytes of data currently residing in the sector buffer to the host.

WRITE DATA TO SECTOR BUFFER (CLASS 0, OPCODE 0F)

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	1
Byte 1	x	x	x	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where x = don't care

This command writes 512 bytes of data from the ITT XTRA CPU into the controller sector buffer.

RAM DIAGNOSTIC (CLASS 7, OPCODE 00)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	0	0
Byte 1	x	x	x	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where x = don't care

This command does walking 1 and walking 0 pattern test of its internal RAM buffer.

RESERVED (CLASS 7, OPCODE 01) - Not used.

RESERVED (CLASS 7, OPCODE 02) - Not used.

DRIVE DIAGNOSTIC (CLASS 7, OPCODE 03)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	1	1
Byte 1	0	0	d	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	r	0	0	0	s	s	s	s

where d = drive (0 or 1)
r = retries

This command tests both the drive and the drive-to-controller interface. The controller sends recalibrate and seek commands to the selected drive and reads sector 0 of each track to verify that both ID and data field are correct. The controller does not perform any write operations during this command; it is assumed that the disk has been previously formatted.

CONTROLLER INTERNAL DIAGNOSTICS (Class 7, Opcode 04)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	0
Byte 1	x	x	x	x	x	x	x	x
Byte 2	x	x	x	x	x	x	x	x
Byte 3	x	x	x	x	x	x	x	x
Byte 4	x	x	x	x	x	x	x	x
Byte 5	x	x	x	x	x	x	x	x

where x = don't care

This command checksums the controller ROM by adding the value of each memory location modulo 256 across the programmed area. The newly calculated checksum is compared to the checksum stored permanently in the ROM. If the checksums do not compare, then a CHECKSUM ERROR (Error Code 31 Hex) is returned. The ECC circuitry is tested by introducing an artificial error to the data and checking that the ECC circuitry detects the error. It also passes a good pattern and sees if the ECC circuitry detects no ECC error.

READ LONG (CLASS 7, OPCODE 05)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	1
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi		Sector Number					
Byte 3	Cylinder Number low							
Byte 4	Block count							
Byte 5	r	0	0	0	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option

This command is used to test the ECC circuitry. When the host issues a write command to the controller (assume 512 bytes/sector), the controller writes to the disk the 512 bytes sent by the host and appends the four bytes generated by the ECC hardware. During a normal read command, the controller reads the 512 data bytes plus the four ECC bytes into the buffer. But the controller sends only the 512 data bytes to the host. The four ECC bytes are used to determine if an ECC data error occured. The only difference between Read Long and Read is that the controller appends the 4 ECC bytes to the data transfer, making the sector transfer 516 bytes long. The method to test the ECC circuitry is as follows:

1. Use the normal Read command to find a sector that does not have any data errors.
2. Use Read Long to read that sector plus ECC into the host.
3. Modify the data pattern in a known way.
4. Use Write Long to write the pattern to the same sector.
5. Use the Read command to read the same sector again.

6. If the pattern change is less than or equal to 11 bits in length, the controller flags it as a correctable data error. If the change is greater than 11 bits in length, the controller will flag it as an uncorrectable data error.
7. Use a Write command to restore the sector for system use.

WRITE LONG (CLASS 7, OPCODE 06)

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	1	0
Byte 1	0	0	d	Head Number				
Byte 2	Cyl. Hi			Sector Number				
Byte 3	Cylinder					Number low		
Byte 4	Block count							
Byte 5	r	0	0	0	s	s	s	s

where d = drive 0 or 1
r = retries
s = step option

When this command is used, the host supplies the four bytes of ECC information following the 512 bytes data. This command is used to test the controller's ECC circuitry only. See the Read Long command for a detailed description of the test.

HARD DISK

Introduction

The ITT XTRA Hard Disk is a half-height random access 5-1/4 inch rigid media disk drive employing Winchester technology. It uses rack-and-pinion actuators, microprocessor control, and open loop stepper head positioning.

The ITT XTRA Hard Disk also features power-up diagnostics, head shipping zone, buffered seek and 5 Mbit/Sec transfer rate. D.C. voltages and physical form factor are the same as those for the 5-1/4 inch half height floppy.

Specifications

Storage Capacity	
Unformatted	
Per Drive	12,749,184 Bytes
Per Surface	6,374,592 Bytes
Per Track	10,416 Bytes
Per Cylinder	20,832 Bytes
Disk	1
Recording Heads	2
Cylinders	612
Data Tracks	1224
Recording Density	
Areal	5.9 X 10^6 bits/sq. in.
Linear	10,000 bpi
Radial	588 tpi

PERFORMANCE SPECIFICATIONS

Rotational Rate	3600 RPM +/- 1%
Data Transfer Rate	5.0 Mbits per second
Access Time	
Average Latency	8.33 ms
Settling Time	15 ms
Seek Time	
Track to Track	3 ms
Average*	155 ms
Maximum*	420 ms
Start Time (Typical)	20.0 sec from power application to ready
Stop Time (Typical)	15.0 sec from power removal

* Buffered including settling time

POWER REQUIREMENTS

DC Input	+12 Volts DC Steady State: +/- 5%, 1.1 amps maximum. Maximum Ripple allowed is 1% with equivalent resistive load. Start Surge: +/- 10%, 2.5 amps maximum. (12 Seconds Typical)
	+5 Volts DC +/- 5%, 1.5 amps Maximum Ripple allowed is 2% with equivalent resistive load.
AC Input	None required.
Power dissipation	20.7W typical

PHYSICAL CHARACTERISTICS

Dimensions (exclusive of front bezel)

Width	149.3 mm (5.76 inches)
Height	41.3 mm (1.63 inches)
Depth	203.2 mm (8.0 inches)
Weight	3.5 pounds
Heat dissipation (typical)	17 watts

ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operative (stabilized)	40°F (4°C) to 115°F (46°C)
Non-operative	-40°F (-40°C) to 135°F (57°C)
Humidity	
Operative and Non-operative	8% to 80% non-condensing
Maximum Wet Bulb	78°F (26°C)

RELIABILITY AND MAINTENANCE

MTBF	8,000 hours (continuous operation)
MTTR	30 minutes
Preventive Maintenance	None
Component Design Life	5 Years
Data Reliability	1 recoverable error in 10^{10} bits read 1 permanent error in 10^{12} bits read (not recoverable in 16 reads) 1 seek error in 10^{6} seeks

Media Defect Criteria (as shipped from ITT)

20 defects maximum
<2 bytes in length
Cylinder zero defect free

Functional Description

The ITT XTRA Hard Disk contains all necessary mechanical and electronic parts to interpret control signals, position the recording heads over the desired track, read and write data, and provide a contaminant free environment for the heads and disks.

READ/WRITE AND CONTROL ELECTRONICS

One integrated circuit is mounted within the sealed enclosure in close proximity to the read/write heads. Its function is to provide 1 of 2 head selection, read preamplification, and write drive circuitry.

The single microprocessor controlled circuit card provides the remaining electronic functions which include:

Read/Write Circuitry
Head Positioning
Stepper Motor Drive
Interface Control
Index Detection
Track Zero Detect
Spin Speed Control
Dynamic Braking

DRIVE MECHANISM

A brushless DC direct drive motor rotates the spindle at 3600 rpm. The motor/spindle assembly is dynamically balanced to provide minimal mechanical runout to the disks. A dynamic brake is used to provide a fast stop to the spindle motor when power is removed.

AIR FILTRATION SYSTEM

Within the sealed enclosure a 0.3 micron filter coupled with a breather filter, provides over the drive life a clean, above atmospheric pressure environment to the heads and disks.

HEAD POSITIONING MECHANISM

Two read/write heads are supported by a carriage mechanism coupled to the stepper motor through a rack-and-pinion motion translator. The rack-and-pinion translator allows for the increased number of data tracks while retaining the full step holding torque and positioning repeatabilty characteristics of the stepper motor.

READ/WRITE HEADS AND DISKS

Data is recorded on one 130 mm diameter disk through two low force, low mass Winchester type ferrite heads.

MECHANICALLY ISOLATED MOUNTING POINTS

Four side mounting points, compatible with a half height floppy disk, are provided. Each mounting point is mechanically isolated from the drive.

TRACK ZERO DETECTOR

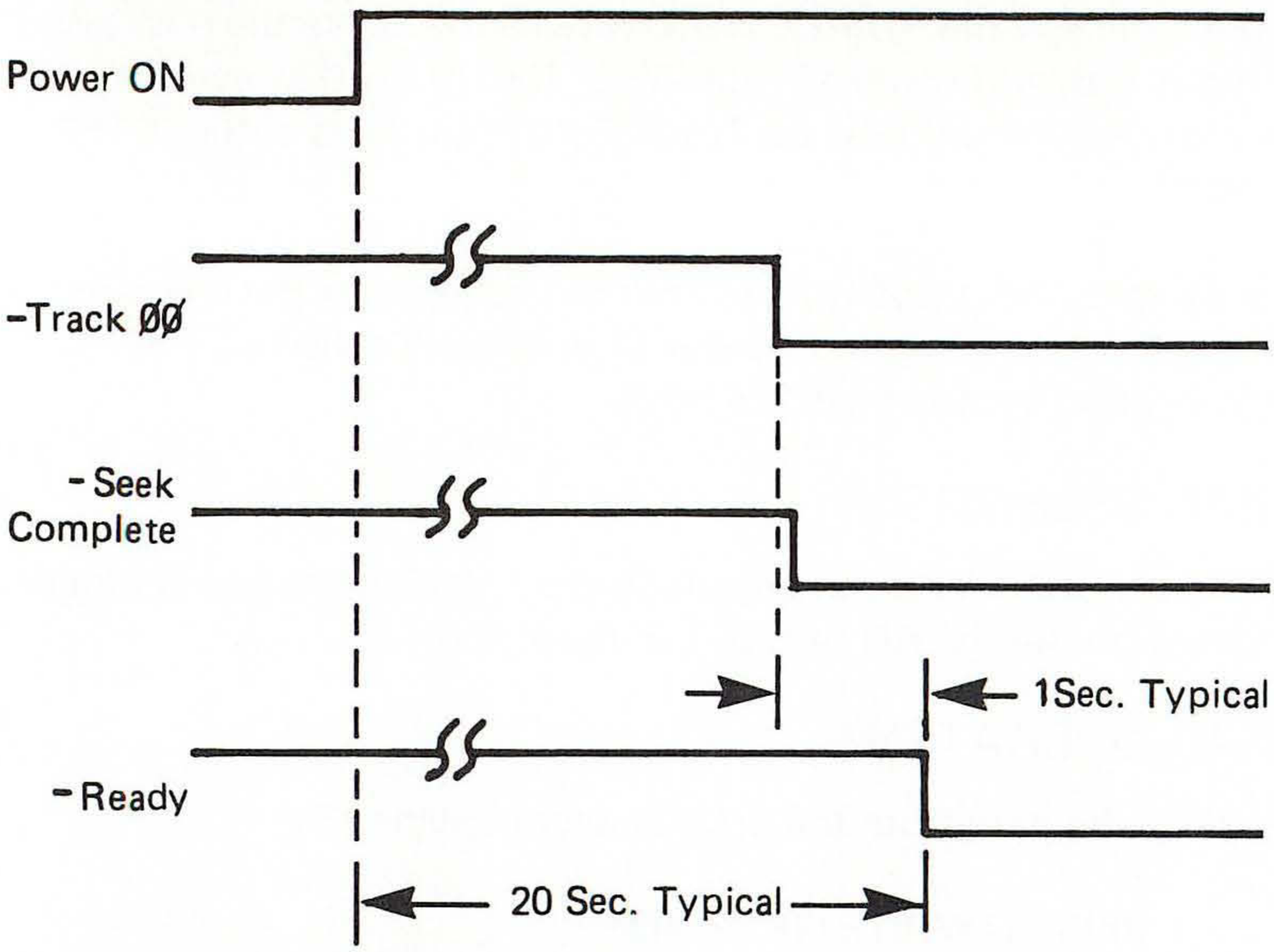
The Track Zero Detector resides on the stepper motor. This optical sensor consists of a light source (activated only when a seek is initiated) and a receiver which when blocked by an interrupter on the motor shaft indicates one of several logical Track Zero positions. The microprocessor determines the physical location of Track Zero from the redundant logical Track Zeros.

Operational Description

POWER SEQUENCING

+5 volts DC and + 12 volts DC may be applied in any order. +12 VDC powers the spindle drive motor. The microprocessor verifies that the disks are spinning at 3600 rpm and then activates the automatic Track Zero positioning.

-Track ZERO, -SEEK COMPLETE, and -READY will become true upon completion of the Track Zero positioning sequence. The following figure illustrates the power-up sequencing.



Hard Disk Power On Timing

DRIVE SELECTION

Drive Selection occurs when one of the -DRIVE SELECT signals is true. Only the drive selected will respond to Control Input Signals, and only that drive's Control Output Signals will be gated to the interface (see "Radial Option" for the exception).

TRACK ACCESSING

Read/Write head positioning is accomplished by:

- Setting -WRITE GATE false
- Setting the appropriate -DRIVE SELECT true
- Selected drive having -READY and -SEEK COMPLETE true
- Setting the appropriate state of -DIRECTION IN
- Pulsing the -STEP

Each -STEP pulse will cause the R/W heads to move either one track in or one track out, depending on the state of -DIRECTION IN. -DIRECTION IN true will cause the R/W head to move inward toward the spindle; -DIRECTION IN false will cause the R/W head to move outward toward Track Zero. The drive will prevent any outward movement beyond Track Zero regardless of the -STEP pulses.

A seek to cylinder 656 will position the heads over the shipping zone. A seek to a higher cylinder than 656 will cause a recalibration sequence in the drive.

HEAD SELECTION

Either of the 2 heads can be selected by placing the heads binary address on the -HEAD SELECT 2^{o} input line.

READ OPERATION

Reading the data from the drive is accomplished by:

Setting -WRITE GATE false
Setting the appropriate -DRIVE SELECT true
Having -READY and -SEEK COMPLETE true on the selected drive
Selecting the appropriate -HEAD SELECT binary address

WRITE OPERATION

Writing data to the drive is accomplished by:

Setting the apropriate -DRIVE SELECT true
Having -READY and -SEEK COMPLETE true on the selected drive
Selecting the appropriate -HEAD SELECT binary address
Assuring -WRITE FAULT is false
Setting -WRITE GATE true and placing the data to be written on the MFM WRITE DATA lines.

Electrical Interface

The interface to the ITT XTRA Hard Disk can be divided into three categories, each of which is physically separated: Control Signals, Data Signals, and DC Power.

All Control Signals are digital in nature (open collector TTL) and either provide signals to the drive (input) or signals to the controller (output). The Data Signals are differential in nature and provide data either to (write) or from (read) the drive.

The following table provides the connector pin assignments for P1 and P2. The interconnect cable between the drive and controller is a flat ribbon cable. The signal return lines and groundlines for P1 and P2 are grounded at the controller.

Connector pin assignments for P3 are also included in the table. The voltage return lines of P3 are grounded at the power supply.

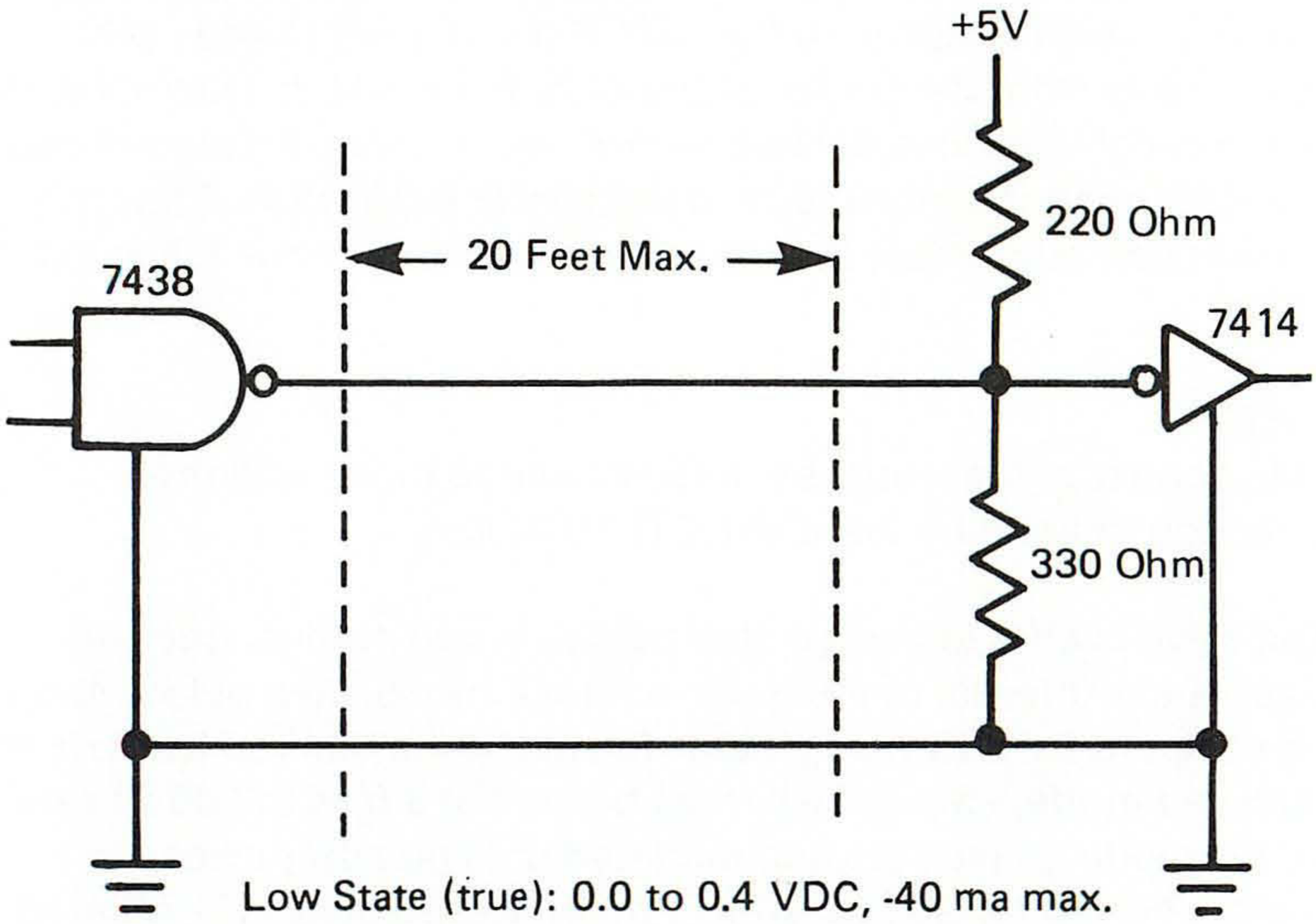
Connector P4 is a spade lug connector tied to frame ground.

P1/P2/P3/P4 CONNECTOR PIN ASSIGNMENTS

Signal	Ground Return	Signal Name
P1-2	P1-1	Reserved
P1-4	P1-3	Reserved
P1-6	P1-5	-Write Gate
P1-8	P1-7	-Seek Complete
P1-10	P1-9	-Track Zero
P1-12	P1-11	-Write Fault
P1-14	P1-13	-Head Select 2^{o}
P1-16	P1-15	Reserved
P1-18	P1-17	Reserved
P1-20	P1-19	-Index
P1-22	P1-21	-Ready
P1-24	P1-23	-Step
P1-26	P1-25	-Drive Select 1
P1-28	P1-27	-Drive Select 2
P1-30	P1-29	-Drive Select 3
P1-32	P1-31	-Drive Select 4
P1-34	P1-33	-Direction In
P2-1	P2-2	-Selected
P2-3	P2-4	Reserved
P2-5	P2-6	Spare
P2-7	P2-8	Reserved
P2-9		Spare
P2-10		Spare
P2-11	P2-12	Ground
P2-13		+MFM Write Data
P2-14		-MFM Write Data
P2-15	P2-16	Ground
P2-17		+MFM Read Data
P2-18		-MFM Read Data
P2-19	P2-20	Ground
P3-1		+12 Volts DC
P3-2		+12 Volts DC Return
P3-3		+5 Volts DC Return
P3-4		+5 Volts DC
P4		Frame Ground

CONTROL INPUT SIGNALS

The Control Input Signals are gated into the drive by the activation of the appropriate -DRIVE SELECT line. The following figure illustrates the driver/receiver circuit and signal level specification. Note that the Control Input Signal is terminated by a 220/330 ohm resistor network in the drive.



Hard Disk Control Signal Driver/Receiver

REDUCED WRITE CURRENT

This line is non-functional on the ITT XTRA hard disk. Write current is controlled by the internal microprocessor.

-WRITE GATE

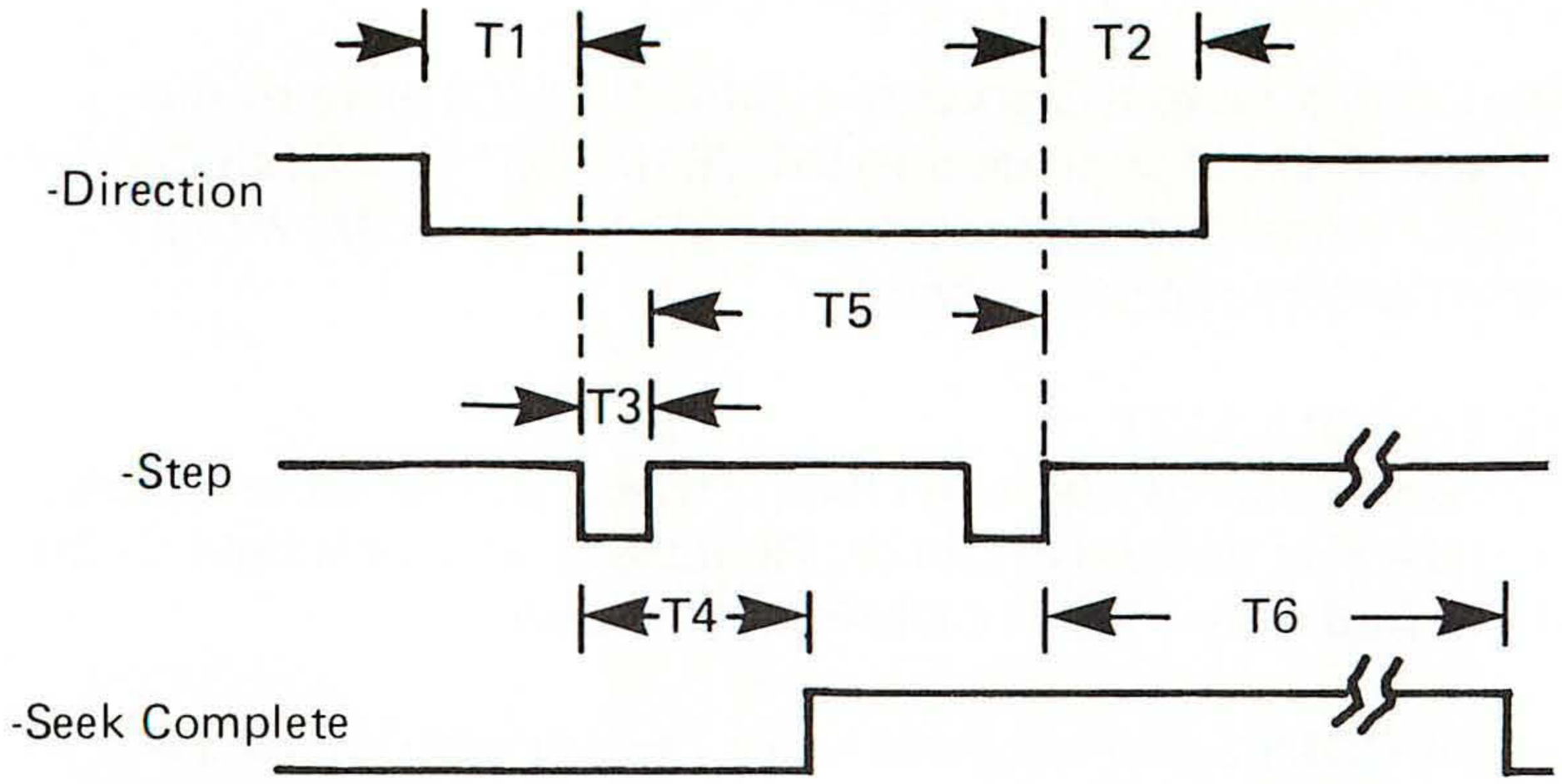
The true state of this signal enables write data to be written on the disk. The false state of this signal enables data to be transferred from the drive.

-HEAD SELECT 2°
-HEAD SELECT 2° signal provides for the selection of one of the two Read/Write Heads. -Head Select 2° being false will select Head 0, and being true will select Head 1.

-DIRECTION SELECT
This signal defines direction of motion of the R/W head when the -STEP line is pulsed. A high level defines the direction as "out" and if a pulse is applied to the -STEP line the R/W heads will move away from the center of the disk. If this line is a low level, the direction of motion is defined as "in" and the step pulses will cause the R/W heads to move toward the center of the disk. Change in direction must meet the requirements shown in the following figure.

-STEP
This control signal causes the R/W head to move with the direction defined by the -DIRECTION IN line.

The drive is able to accept step pulses in two modes, track-to-track and buffered. In the track-to-track mode, step pulses should be sent at a 3 ms rate or greater to access the desired track. In the buffered mode, step pulses must be sent at a 6 us to 200 us rate. In this mode, pulses are accumulated until no new pulses have been received for 200 us. At this point access motion is initiated, and an optimized seek algorothim executed to minimize access time. Pulses that occur after this time and prior to completion of the seek will be ignored. The drive automatically decides which mode to use based on the incoming step pulse rate. The direction line should be maintained at the desired level 100 ns before the first step pulse until 100 ns after the last step pulse has been issued.



TRACK TO TRACK

T5=3ms min

T6=15ms min

SEEK MODE TIMING

T5=100ns min

T2=100ns min

T3=2us min-40us max

T4=500ns typical

BUFFERED SEEK

T5=6us min 200us max

T6=SEEK LENGTH DEPENDENT

Hard Disk Direction Select Timing

-DRIVE SELECT 1, 2, 3 and 4
-DRIVE SELECT, when low, connects the drive to the control lines. Only the drive selected will respond to control input signals, and only that drive's control output signals will be gated to the interface. See the discussion under "OPTIONS" for information on the DIP shunt that controls drive selection.

CONTROL OUTPUT SIGNALS

The Control Output Signals are gated from the drive by the activation of the appropriate -DRIVE SELECT line. Each Control Output Signal should be terminated in the controller with a 220/330 ohm resistor network.

-SEEK COMPLETE
This signal will go true when the R/W heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when -SEEK COMPLETE is false.

-SEEK COMPLETE will go false if a recalibration sequence is initiated (by drive logic) at power on, or 500ns (typical) after the leading edge of a step pulse.

-TRACK ZERO
This interface signal indicates a true state only when the drive's R/W heads are positioned at Track Zero (the outermost data track).

-WRITE FAULT
This signal is used to indicate that a condition exists in the drive which will result in improper writing on the disk. When this signal is true, further writing is inhibited at the drive until the condition is corrected. Once corrected, the controller can reset this line by deselecting the drive. Any of the following four conditions could cause -WRITE FAULT to be true.

1. No write current sensed in the head with -WRITE GATE active and -DRIVE SELECTED.
2. An open head in the drive.
3. No transitions on MFM WRITE DATA line when -WRITE GATE true.
4. DC voltages are out of tolerance.

-INDEX
This 100 microsecond (typical) interface pulse is provided by the drive once each revolution (16.67 ms nominal) to indicate the beginning of the track. Normally, this signal is a high level and makes the transition to the low level to indicate -INDEX. Only the transition from high to low is valid.

-READY
This interface signal when true together with -SEEK COMPLETE, indicates that the drive is ready to read, write or seek, and that the I/O signals are valid. When this signal is false, all writing and seeking are inhibited.

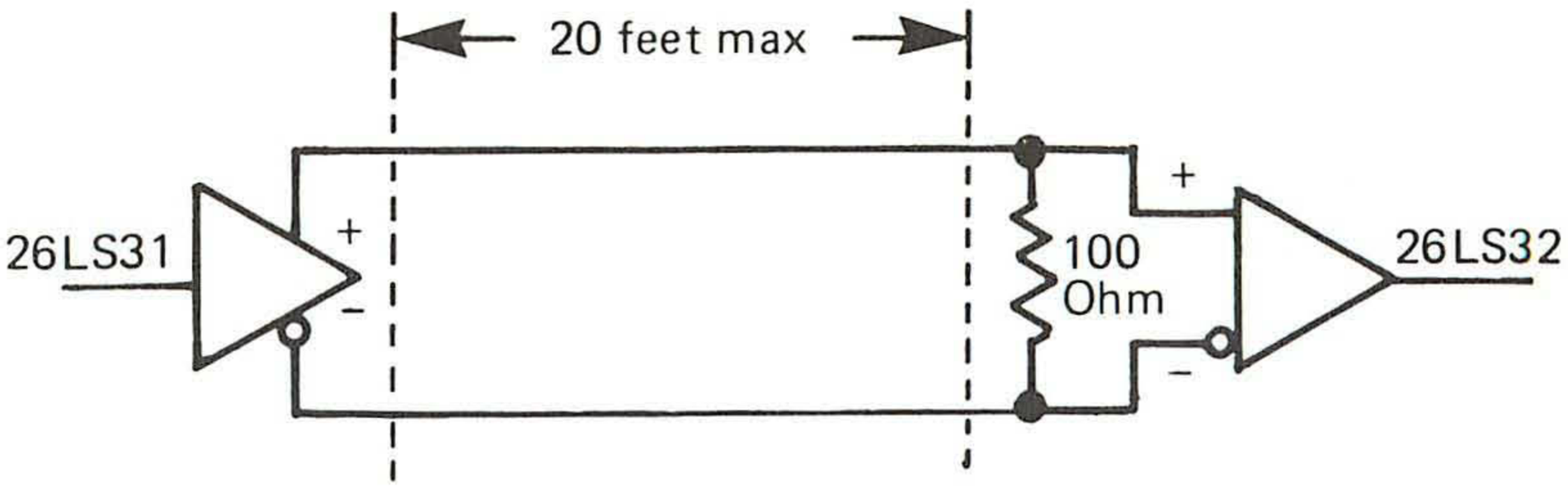
The typical time after power on for -READY to be true is 20 seconds.

-DRIVE SELECTED
The -DRIVE SELECTED signal will go true only when the drive is programmed as drive X (X = 1, 2, 3, or 4) and the -DRIVE SELECT X line is activated by the controller.

DATA TRANSFER SIGNALS

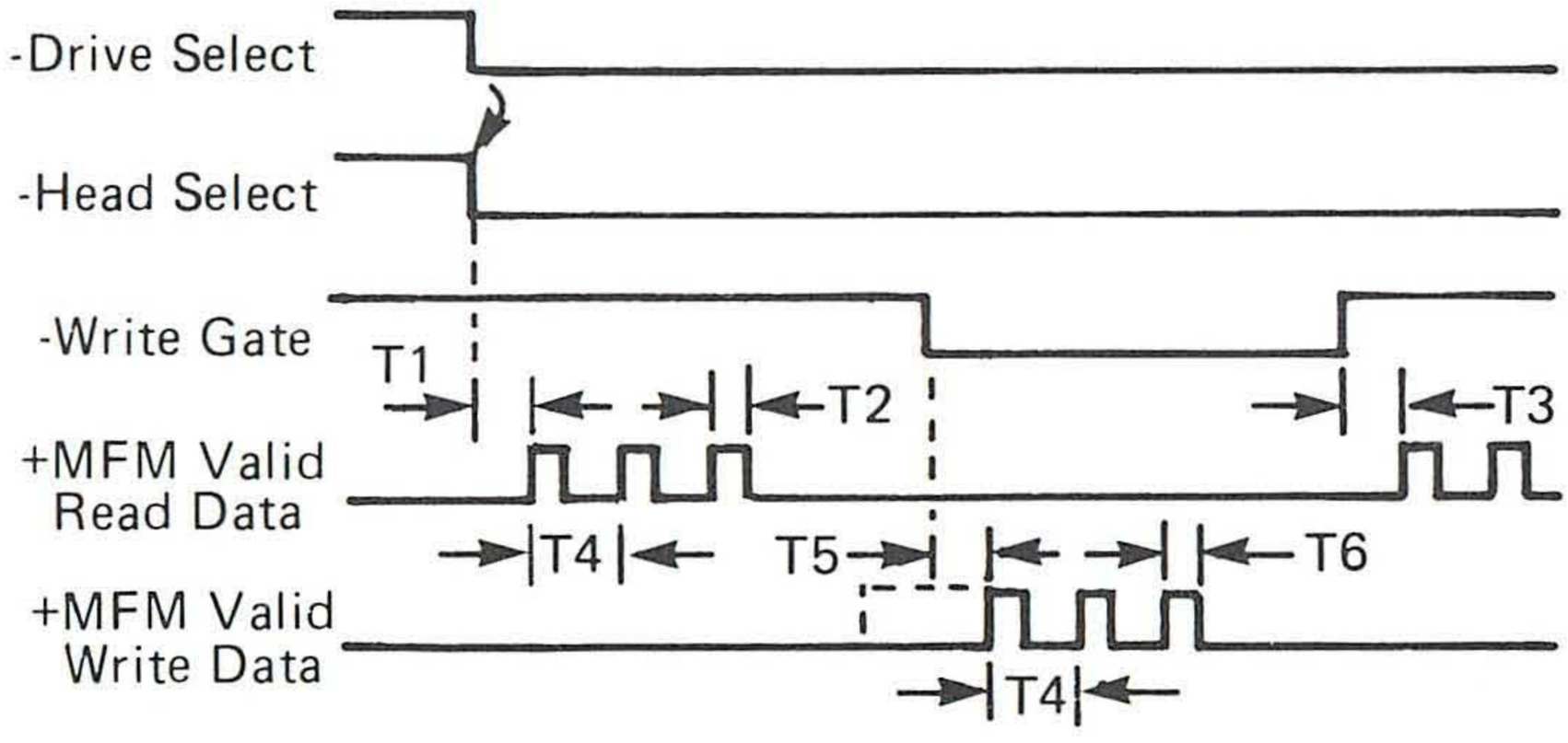
All signals associated with the transfer of data between the drive and the controller are differential in nature and are gated by -DRIVE SELECT except in the radial mode.

Two pairs of balanced signals are used for the transfer of data: MFM WRITE DATA and MFM READ DATA. The following figure illustrates the driver/receiver combination used in the ITT XTRA Hard Disk for data transfer signals.



Hard Disk Data Signal Driver/Receiver

MFM WRITE DATA
This is a differential pair that defines the transitions to be written on the track. The transition of +MFM WRITE DATA line going more positive than the -MFM WRITE DATA line will cause a flux reversal on the track provided -WRITE GATE is true. The timing of the write operation is illustrated in the following figure.



T1=20 us max (head switch)
T2=25 - 50 ns
T3=20 us max (read after write)
T4=200 ns typical bit cell
T5=400 ns max
T6=50-150 ns

Hard Disk Read/Write Timing

In MFM recording, to optimize data integrity and meet the error rate specified, the write data presented by the controller may be precompensated on all tracks, but must be precompensated from track 128 through track 612. +/-MFM Write Data pulses bounded on one side by a 200 ns period (1/2F) and bounded on the other side by 300 ns (1/1.5F) or 400 ns (1/F) period must be precompensated by 12 ns towards the side of the 200 ns (1/2F) period. The precompensation is illustrated in the following table.

WRITE PRE-COMPENSATION RULES

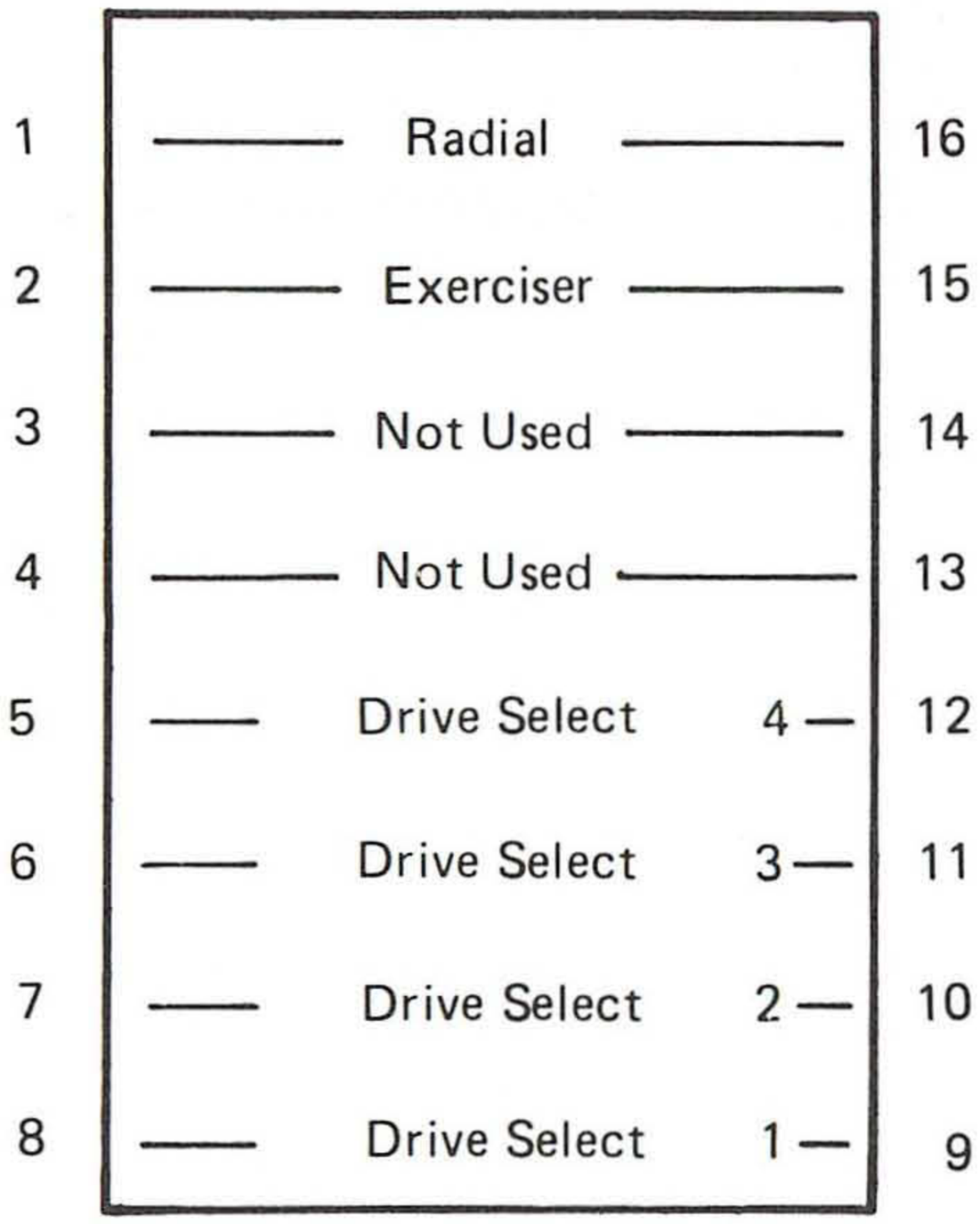
Bit	1	2	3	4	Compensation
	1	0	0	0	12nsec late on first clock
	0	0	0	1	12nsec early on second clock
	0	1	1	X	12nsec late on first data
	1	1	0	X	12nsec early on second data

MFM READ DATA

The data recovered by reading a pre-recorded track is transmitted to the controller via the differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head. The timing of the read operation is illustrated in the previous figure.

OPTIONS

Optional features are implemented via a shunt block on the hard disk printed circuit card. The layout of the shunt block is shown below.



Shunt Block

-DRIVE SELECT

As shipped, the 16-pin shunt block has pin pair 8/9 shorted, resulting in Drive Select 1 being selected. To select a different drive number in a daisy-chain operation, refer to the following table.

DRIVE SELECTION CONFIGURATION

			DRIVE SELECT NUMBER			
Pin		Pair	1	2	3	4
8	-	9	short	open	open	open
7	-	10	open	short	open	open
6	-	11	open	open	short	open
5	-	12	open	open	open	short
1	-	16	open	open	open	open

"RADIAL" OPTION

If the 16-pin shunt block has pin pair 1/16 shorted resulting in a radial operation, then all input and output signals are enabled, even if the drive is not selected. However, the front panel LED will not be on. -DRIVE SELECT must be active to light the LED. When pin pair 1/16 is open the drive is in a daisy chain mode where input and output signals are enabled when the appropriate -DRIVE SELECT line is activated.

DRIVE EXERCISE OPTION

As shipped, the 16-pin shunt block has pin pair 2/15 open. This shunt, when shorted, will initiate drive exercise routines.

TERMINATORS

Each drive is shipped with a terminator pack providing the 220/330 ohm termination for the Control Input Signals. If multiple drives are configured in a daisy chain configuration, the terminator pack must be removed from all drives except the last unit on the daisy chain.

ERROR MESSAGES

The microprocessor performs wake up diagnostcs on power up. Additionally, some operations are monitored during normal operations. If an error is detected, the microprocessor will flash a warning by blinking the activity LED. An explanation of the hard disk diagnostics and error codes is contained in the **ITT XTRA Maintenance** manual.

Physical Interface

The electrical interface between the disk drive and the host controller and DC power supply is via four connectors: P1-Control Signals, P2-Read/Write Signals, P3-DC Power Input and P4-Frame Ground.

J1/P1 CONNECTOR - CONTROL SIGNALS

Connection to P1 is through a 34-pin PCB edge connector. The pins are numbered 1 through 34 with the odd pins located on the component side of the printed circuit card. A key slot is provided between pins 4 and 6.

The recommended mating connector (P1) is AMP Ribbon Connector P/N 88373-3.

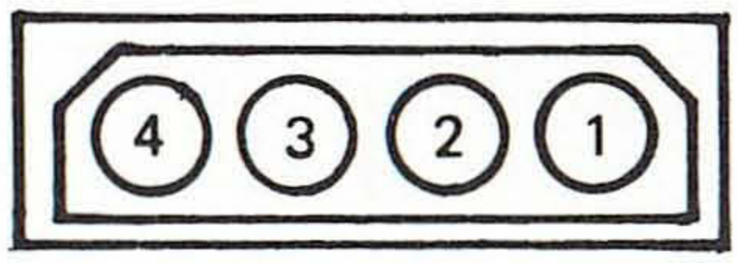
J2/P2 CONNECTOR - DATA SIGNALS

Connection to P2 is through a 20-pin PCB edge connector. The pins are numbered 1 through 20 with the odd pins located on the component side of the printed circuit card. A key slot is provided between pins 4 and 6.

The recommended mating connector (P2) is AMP ribbon connector P/N 88373-6.

J3/P3 CONNECTOR - DC POWER

DC power connector (P3) is a 4 pin AMP Mate-N-Lok connector, mounted on the PCB. The recommended mating connector (P3) is AMP P/N 1-480424-0 utilizing AMP pins P/N 350078-4. P3 pins are numbered as shown in the following figure.



DC Power Connector

J4/P4 CONNECTOR - FRAME GROUND

Faston AMP P/N 61761-2

Recommended mating connector is AMP 62187-1. If used, the hole in P4 will accommodate a wire size of 18 AWG max.

Track Formatting Guidelines

The purpose of a format is to organize a track into smaller addressable records called sectors. The ITT XTRA Hard Disk is a soft sectored device allowing the customer to define the sector format. When establishing the track format, you should observe certain rules to accommodate the physical timing relationships within the drive.

GAP 1

If head switching occurs at index time, then, to reliably read the content of the first sector, Gap 1 must be provided to allow the read amplifier to stabilize. The minimum length of Gap 1 is 12 bytes.

SYNC

A sync field precedes each addressable record (ID or record) and should be of a length to accommodate the "lock up" characteristics of the phase-lock-loop within the data separator portion of the controller.

GAP 2

Following each sector it is recommended that a gap be placed to accommodate spindle speed variations between write operations on the same track to insure that overwrite will not occur on adjacent recorded data. To accommodate the +/-1% speed tolerance of the disk drive, Gap 2 should be a minimum of 1 byte for each 32 bytes of data within the sector. Additionally, the gap must be increased to accommodate the spin speed-asynchronous frequency variation of the controller generated MFM WRITE DATA signals.

GAP 3

This gap is a speed tolerance buffer for the entire tract to insure that the last sector does not overflow beyond the index. Gap 3 preceeds index and should be of a length to accommodate the spin speed variations of the disk drive (+/-1%) and the frequency variation of the controller generated MFM WRITE DATA signals.

8 - The Switching Power Supply

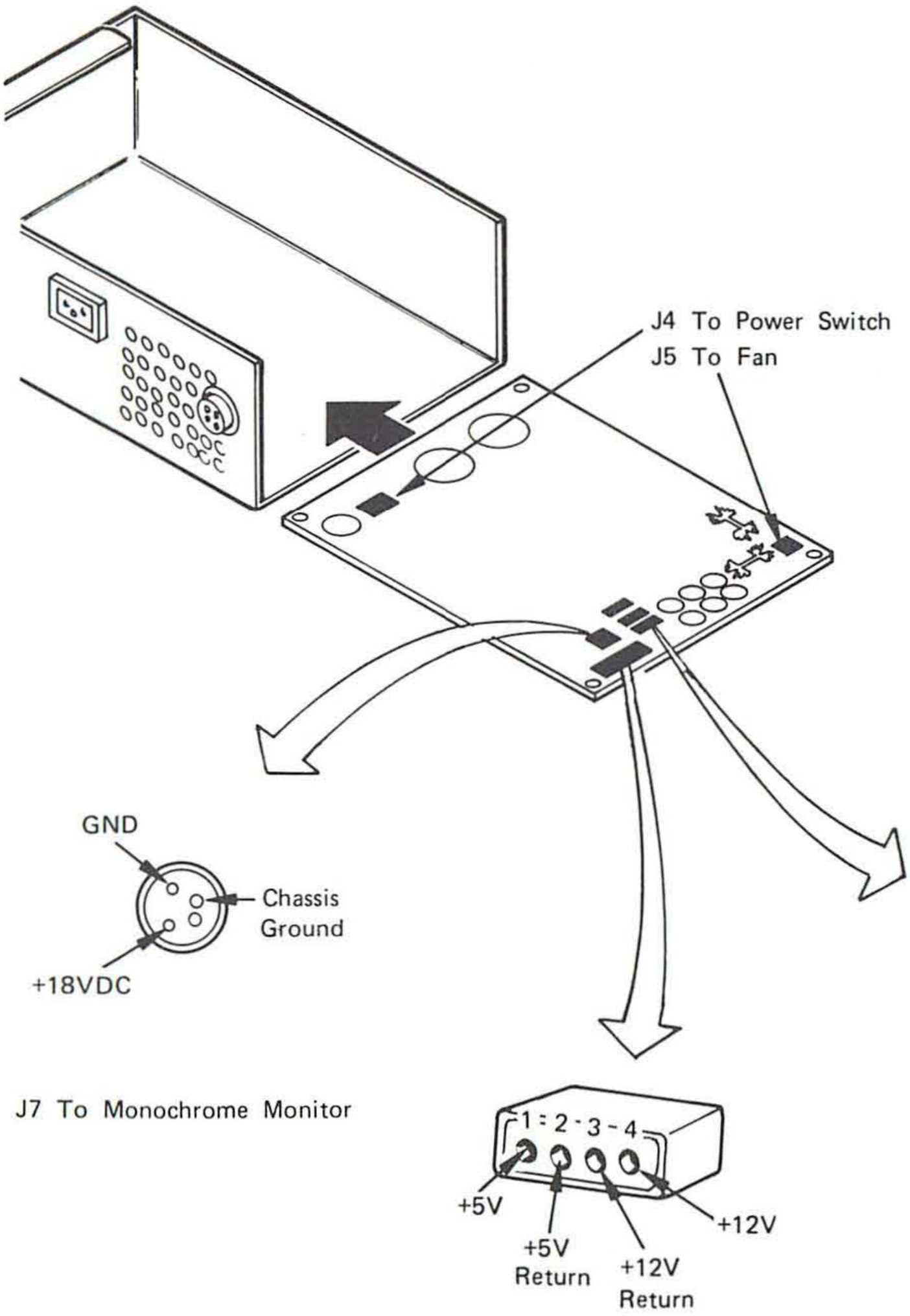
INTRODUCTION

The switching power supply is located on the right rear corner of the system motherboard. This compact and highly efficient supply is switch-selectable for 115 or 230 VAC operation. It provides operating DC voltages to the motherboard, the video monitor, the floppy disk drive(s), the optional hard disk drive, and any printed-circuit boards installed in the expansion backplane. The power supply is designed for continuous operation at 115 watts. Electrical and environmental specifications for the power supply are provided in the following table:

SPECIFICATIONS FOR THE SWITCHING POWER SUPPLY

INPUT VOLTAGE:			90 to 132 for 115 VAC 180 to 264 for 230 VAC		
FREQUENCY:			47 to 63 Hz		
AC LINE FUSE:			2 amp fast blow, 250 V for 230 VAC 3 amp fast blow, 250 V for 115 VAC		
OUTPUT VOLTAGE:					
	+5V	+12V		-12V	CRT
Min Voltage	4.75	11.4		10.2	15.0
Max Voltage	5.25	12.6		13.8	20.0
Ripple	50mv	100mv		150mv	n/a
Min Load	2A	.3A		.1A	0.0A
Max Load	10A	2.5A @70% duty cycle		.85A	1.5A
Peak	10A	10A		1.5A	1.5A
TEMPERATURE:					
Operating	10°C to 55°C, at maximum rated load				
Storage	5°C to +85°C (noncondensing)				

POWER SUPPLY CONNECTORS AND PIN ASSIGNMENTS

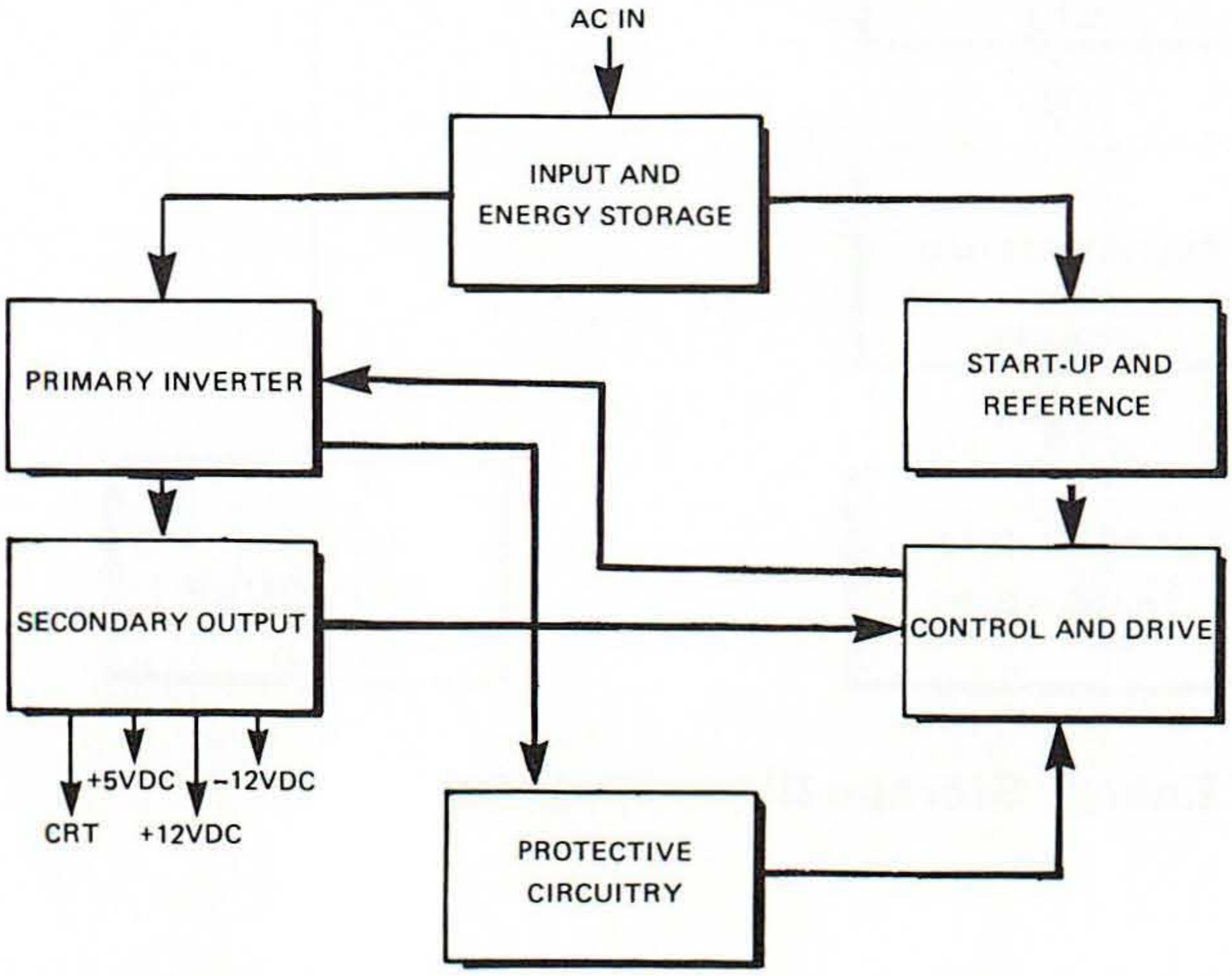


SWITCHING POWER SUPPLY OPERATION

The power supply has six major circuits: (1) Input and Energy Storage, (2) Start-up and Reference, (3) Control and Drive, (4) Primary Inverter, (5) Protection, and (6) Secondary Output. The following paragraphs describe the basic function of each of these circuits. To better follow the discussion, reference the power supply schematics located at the end of this manual.

As shown in the following simplified block diagram, AC power is input through the Input and Energy Storage circuit to both the Start-up and Reference circuit and the Primary Inverter circuit. The Start-up and Reference circuit supplies the initial input to the Control and Drive circuit. The output of the Control and Drive circuit provides a second, controlling input to the Primary Inverter circuit. The Primary Inverter circuit provides input for both the Protection circuit and the Secondary Output circuit.

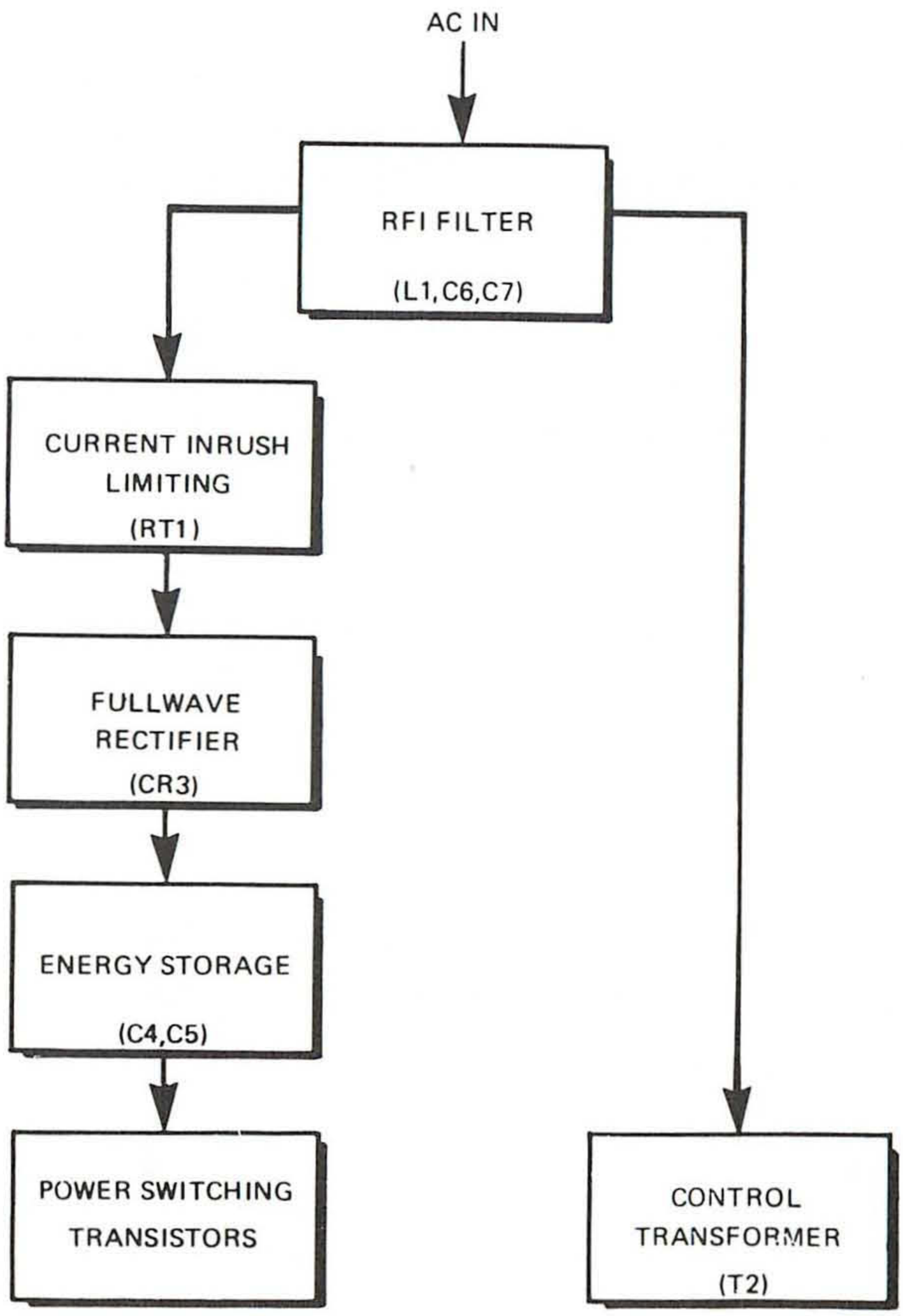
The Protection circuit supplies a controlling signal to the Control and Drive circuit. The Secondary Output circuit provides feedback to the Control and Drive circuit for +5V regulation. It also provides +5, +12, and -12 VDC to the system motherboard, and +15 to +18 unregulated DC to the video monitor.



Simplified Block Diagram of the Switching Power Supply

Input and Energy Storage

The Input and Energy Storage circuit has five major functions: (1) prevent RFI from entering the AC line, (2) supply AC input to the Start-up and Reference circuit, (3) provide in-rush current limiting, (4) provide the capability to switch from 110 to 220 VAC, and (5) store and supply a rectified, unregulated DC voltage to the Primary Inverter circuit.

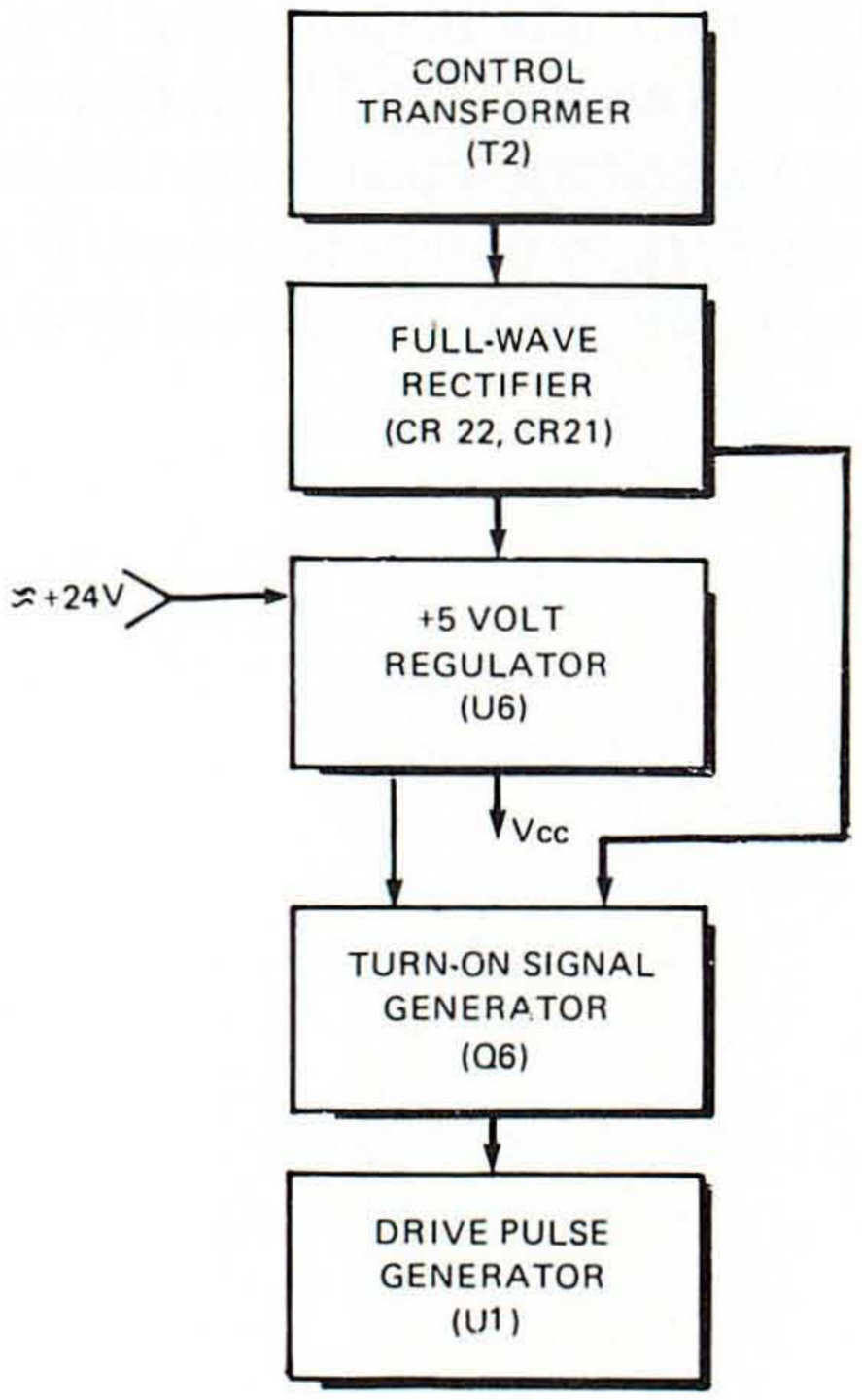


Input and Energy Storage Block Diagram

Switch S1 configures the circuit for 110 or 220 VAC. The AC input from the power line is passed through an RFI filter. This AC voltage drives the primary of the control transformer resulting in the transformer's secondary driving the Start-up and Reference circuit. AC is also passed through a current inrush limiting thermistor and input to a full-wave rectifier diode bridge. This rectified, unregulated DC is passed on to an energy storage capacitor. The energy storage capacitor provides DC storage of rectified AC and short term operational power during brief AC line interruptions. DC power passes from the storage capacitor to the power switching transistors in the Primary Inverter circuit.

Start-up and Reference Circuit

The Start-up and Reference circuit has three main functions: (1) supply a DC unregulated voltage source, (2) supply a +5V reference source, and (3) provide a trigger voltage to the drive pulse generator for circuit start-up.



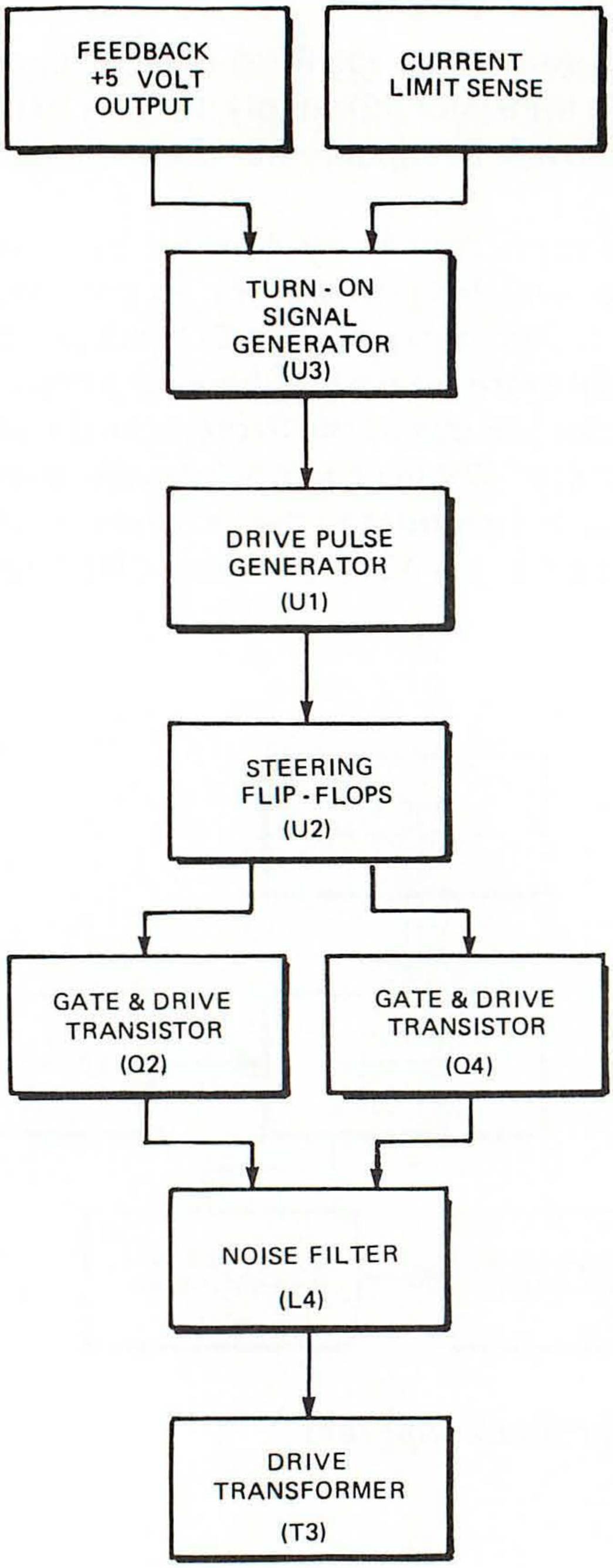
Start-up and Reference Block Diagram

The AC voltage from the Input and Energy Storage circuit is coupled through the control transformer, stepped down, and rectified. This unregulated DC voltage is passed to a +5 volt regulator, whose output provides a +5 volt reference and internally powers several IC's. Once the regulator is providing a constant +5 volt output, causing the Primary Inverter circuit to run, the Secondary Output circuit supplies approximately +24 volts to the regulator input for the +5 volt reference. The regulator output provides a reference for the turn-on signal generator and provides a pull-up on the trigger pin of the drive pulse generator in the Control and Drive circuit.

Control and Drive Circuit

The Control and Drive circuit has three main functions: (1) control power pulse generation with feedback from the +5 V output, (2) control power pulse generation during current limiting, and (3) direct the generated pulses to the drive transformer and into the Primary Inverter circuit.

The output from the turn-on signal generator to the drive pulse generator, in conjunction with the +5 V feedback and current sense signals, triggers a voltage pulse from the generator through a steering flip-flop, to one of two drive transistors. These transistors drive the Primary Inverter circuit through the drive transformer.

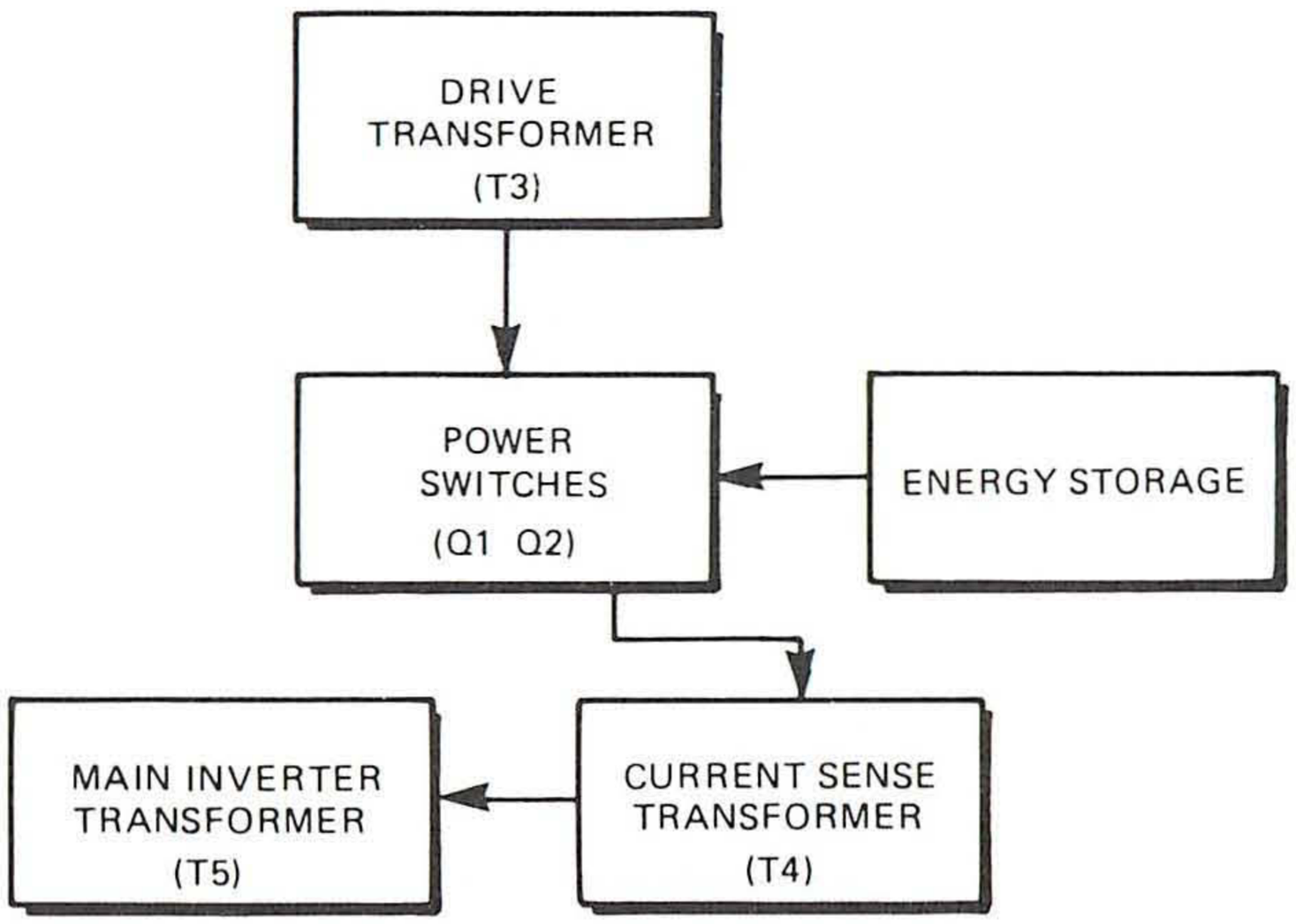


Control and Drive Block Diagram

Primary Inverter Circuit

The Primary Inverter circuit has three main functions: (1) drive the power switching transistor, (2) supply an input to the Protection circuit and (3) provide an input to the Secondary Output circuit.

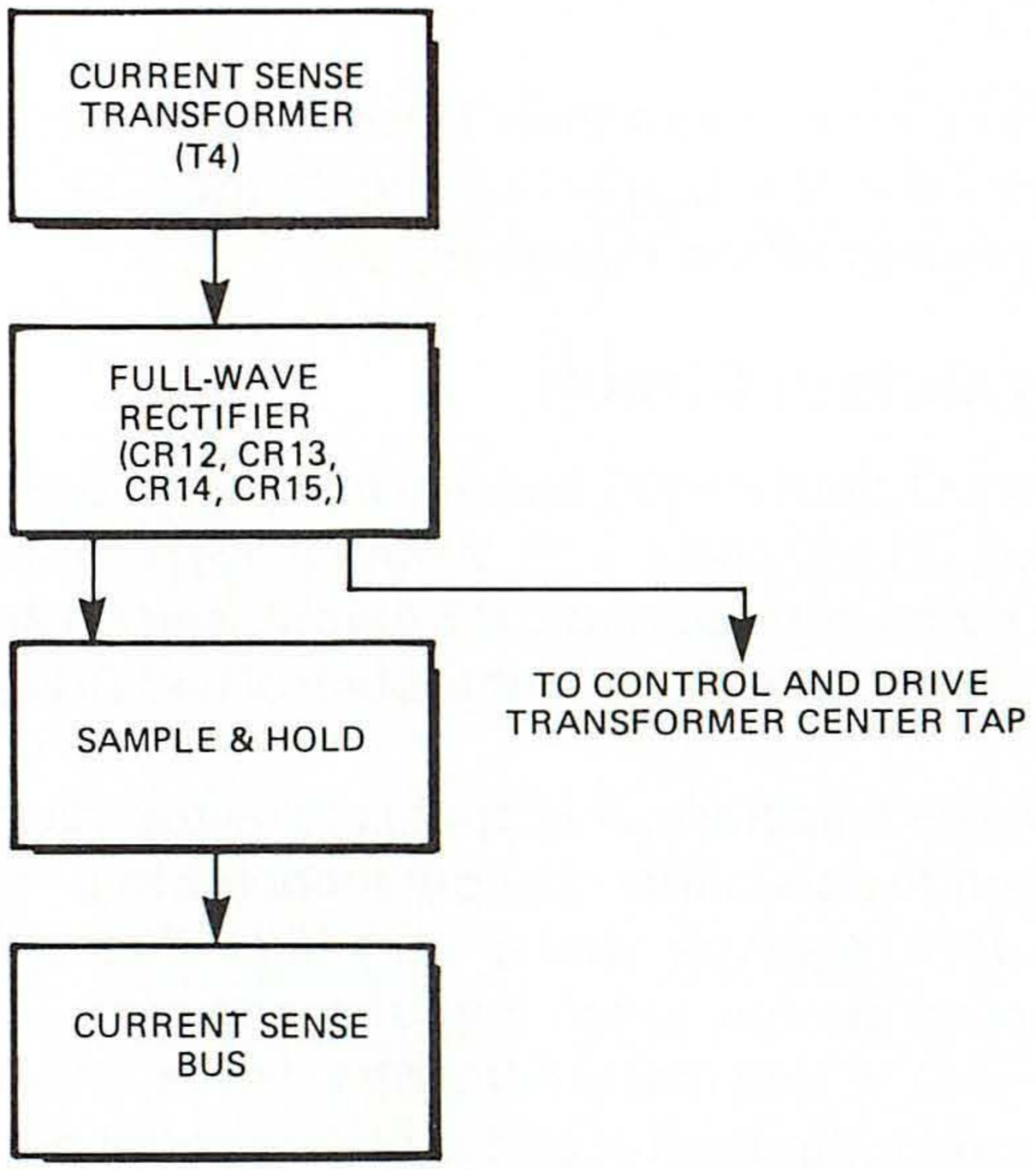
The drive transformer secondary provides an input to turn on one of the two power switching transistors. As one transistor or the other is turned on and conducts, the DC voltage stored in the Input and Energy Storage circuit is applied across the current sense transformer (for use by the Protection circuit) and the main inverter transformer. These power pulses are coupled across the main inverter transformer to the Secondary Output circuit to produce the supply's +/- 12V, +5V, and CRT output voltages.



Primary Inverter Block Diagram

Protection Circuit

The Protection circuit has three basic functions: (1) detect and limit high primary current, (2) detect and protect an overvoltage on the +5V output, and (3) detect and protect in case of an over temperature condition within the supply.



Primary Current Limiting Block Diagram

The current sense transformer secondary provides input to a full-wave rectifier diode bridge. The rectified DC is proportional to the primary current being switched by the power switch transistors and is supplied to two places: (1) the center tap of the drive transformer in the Control and Drive circuit as positive feedback and (2) the sample and hold subcircuit that compares the rectified DC with a fraction of the +5 V reference. This comparison generates a negative current sense bus voltage and is used, if necessary, to inhibit drive pulse generation providing current limiting.

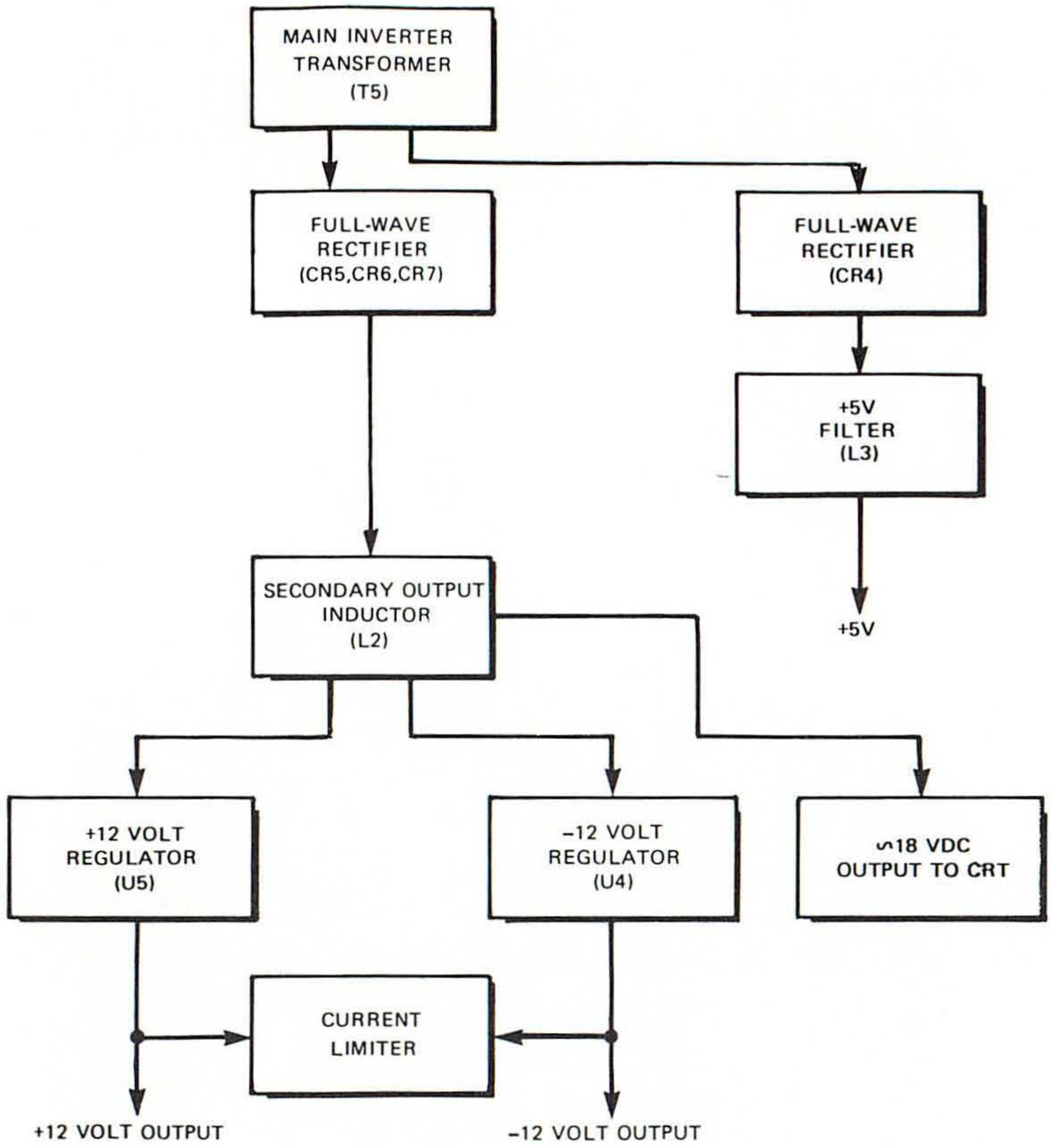
Overvoltage protection is provided for the +5 V output via a zener diode and SCR OVP crowbar. If the output voltage exceeds 5.6 volts, the zener goes into an avalanche condition and triggers the SCR crowbar. When the SCR fires, it clamps the center tap of the current sense transformer to ground, effectively turning off the power switching transistors. A small resistor is used to provide holding current to the SCR to keep the over voltage protection circuit latched on.

The Protection circuit uses a thermistor to detect excessive temperatures within the supply and trigger the SCR used for overvoltage to latch off the power supply.

Secondary Output Circuit

The Secondary Output circuit has five main functions: (1) provide a +5 V output, (2) provide a +12 V output, (3) provide a -12 V output, (4) provide unregulated CRT output, and (5) provide feedback for +5 V regulation to the Control and Drive circuit.

The main inverter transformer output is full-wave rectified and passed through the secondary output inductor to a +12 V regulator, a -12 V regulator, and a +5 V filter. These voltages are then supplied directly to the output connectors: +/-12 V to the fan; +5, +12 V, and GND to the disk drives; +/- 12 V, +5V, and GND to the motherboard; and an unregulated output of +15 to +20 V to the video display.

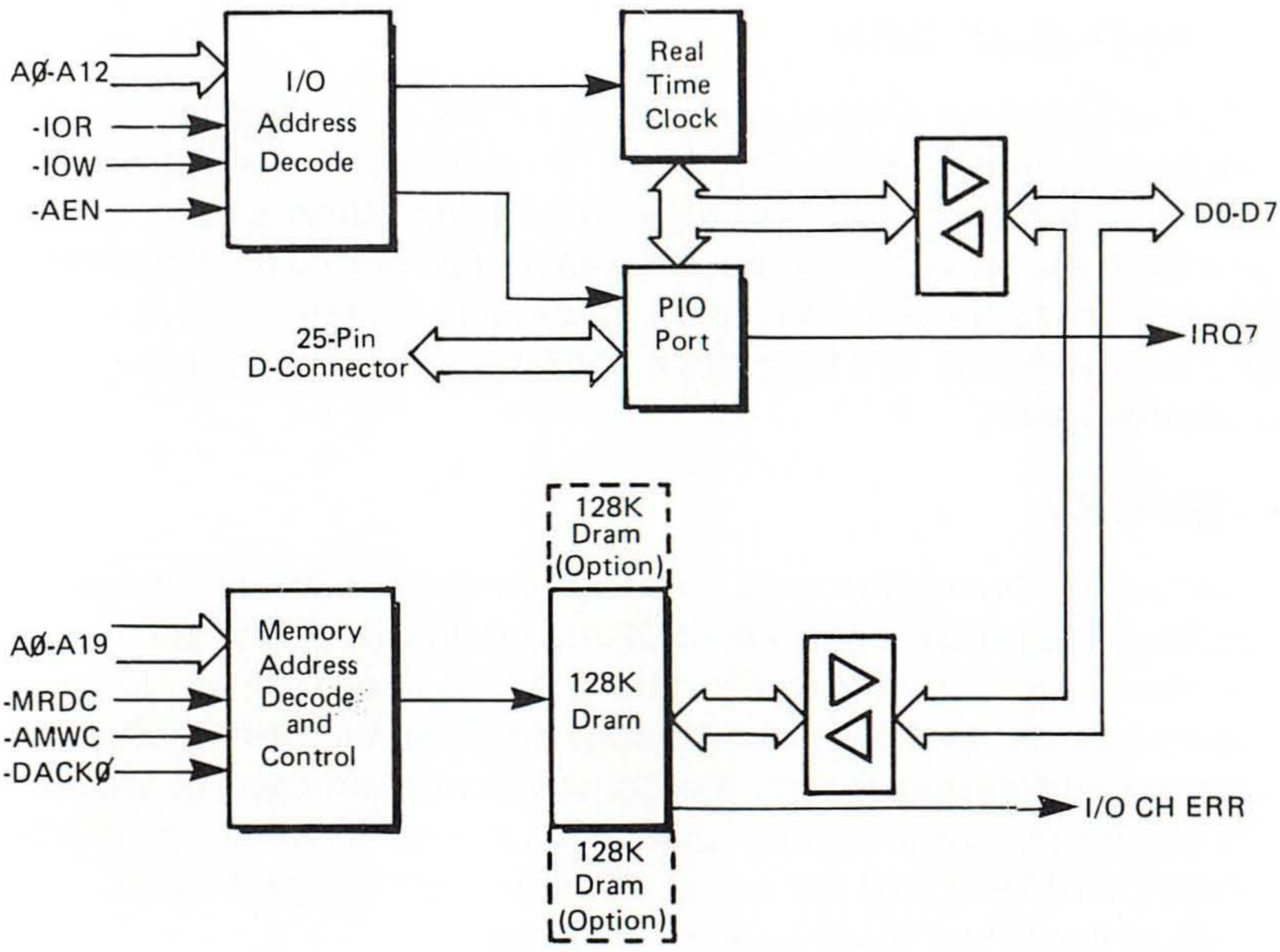


Secondary Output Circuit

9 - Combo Board

INTRODUCTION

The ITT XTRA Combo Board is an optional device that may be installed in any of the I/O expansion slots on the system motherboard. The Combo Board features three different circuits on one board: 128K to 384K of add on memory, a parallel port, and a real-time clock. A block diagram of these major circuits appears below:



Combo Board Block Diagram

BOARD SWITCHES

The DIP switches on the Combo Board are used to establish the address range occupied by the the board's add on memory. Note in the following table that only switches 1-4 are currently used.

AMOUNT OF MEMORY ON MOTHER-BOARD	COMBO BOARD DIP SWITCH SETTINGS				ADDRESS RANGE OCCUPIED BY COMBO BOARD MEMORY
	SWITCH 4	SWITCH 3	SWITCH 2	SWITCH 1	
128K	OFF	OFF	ON	OFF	20000 - 3FFFF HEX
192K	OFF	OFF	ON	ON	30000 - 4FFFF HEX
256K	OFF	ON	OFF	OFF	40000 - 5FFFF HEX

BOARD JUMPERS

JP2 is a three-pin jumper. Jumpering pin 2 to pin 3 disconnects the battery from the real time clock. When the board is shipped or stored for long periods of time, this configuration is used to preserve the life of the battery. Jumpering pin 1 to pin 2 connects the battery to the real time clock. Under this configuration, the battery keeps the real time clock operating when the system is powered down.

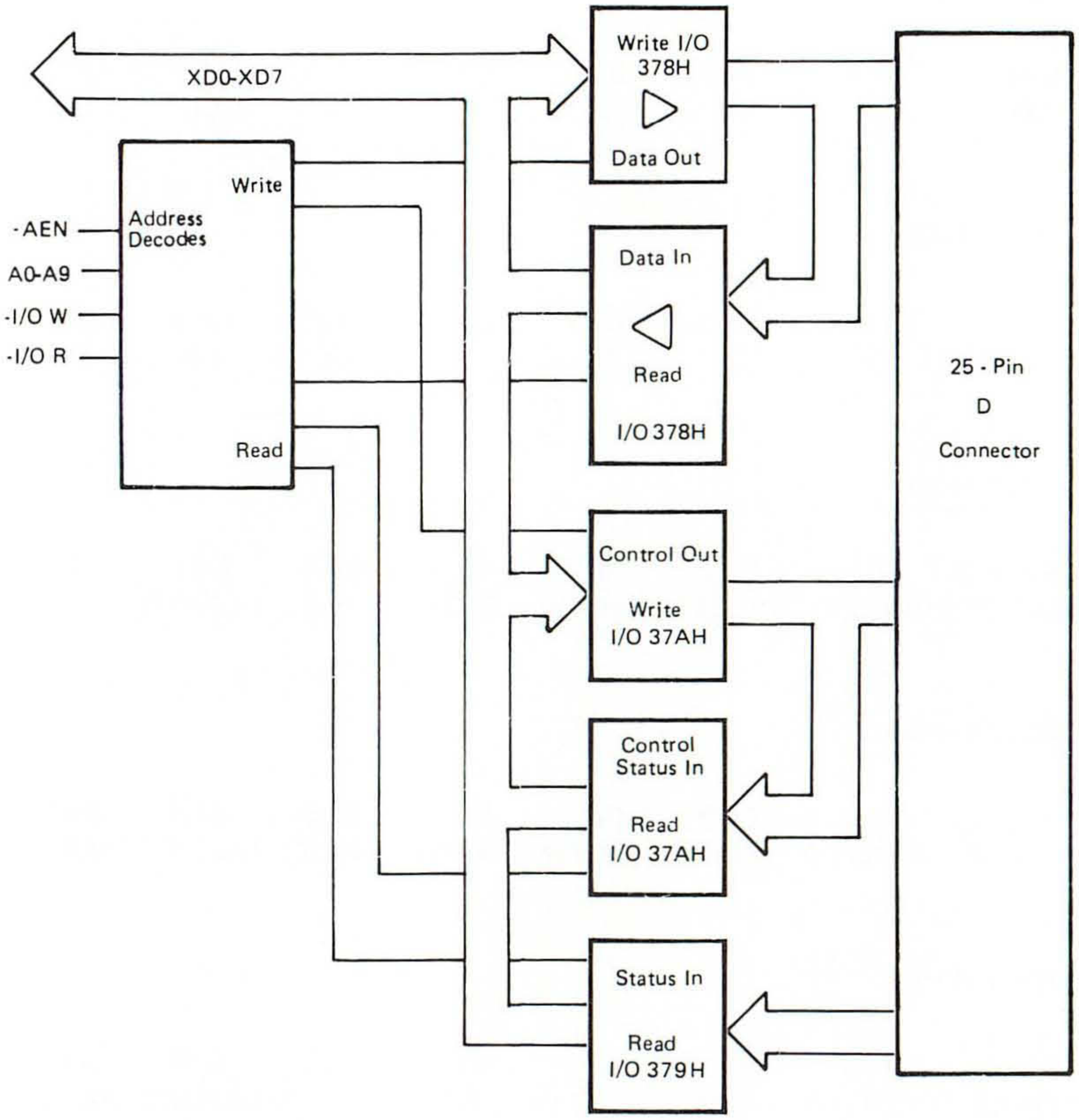
MEMORY

The Combo Board supports three 128K banks of DRAM. The first additional addressable bank of DRAM will always reside on the Combo Board. The second and third DRAM banks will reside on "baby boards" that are placed "piggy back" on the Combo Board. Correct addressing of both the Combo Board and baby board are critical for maximum system utilization. Any break in the continuity of the DRAM will void the use of all other DRAM placed either physically or electrically behind the break.

Each Combo and baby board memory byte is parity checked like all other XTRA memory. The system appends the parity bit and checks this bit each time a read or write operation takes place. If a parity error should occur, the IO bus IOCHERR line will be pulled low. This line will remain low until either a valid memory read or write operation occurs.

PARALLEL PORT

The combo board provides a parallel port via a 25-pin "D" female connector for interfacing to a parallel printer or other parallel peripheral device.



Combo Board Parallel Port Block Diagram

Software Instructions

Five software instructions can be used in conjunction with the combo board's parallel interface latches. A description of the five commands follows:

READ 378 HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
D0	D1	D2	D3	D4	D5	D6	D7

WRITE 378 HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
D0	D1	D2	D3	D4	D5	D6	D7

READ 379 HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
UNUSED	UNUSED	UNUSED	-ERROR	SLCT	PE	ACKNLG	BUSY

READ 37A HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
-STROBE	-AUTO FD	-INIT	-SLCT IN	IRQ EN	UNUSED	UNUSED	UNUSED

WRITE 37A HEX

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
-STROBE	-AUTO FD	-INIT	-SLCT IN	IRQ	UNUSED	UNUSED	UNUSED

Parallel Interface Connector Pin Assignments

PIN NUMBER	SIGNAL	DESCRIPTION
1	-STROBE	Output to printer. A strobe pulse latches data into the printer. Pulse width: from 1.0 to 500 microseconds. May be either active high or low, switch selectable. Strobe must be sent 1.0 microsecond (min.) after valid data.
2	DATA 0	Input data to printer.
3	DATA 1	Data 8 = LSB (Least Significant Bit)
4	DATA 2	Data 1 = MSB (Most Significant Bit)
5	DATA 3	ASCII codes normally use Data 1-7
6	DATA 4	Data 8 not used. Logic 1 high (2.4
7	DATA 5	- 5.0 Vdc); Logic 0 low (0 to 0.4
8	DATA 6	Vdc)
9	DATA 7	
10	-ACKNOWLEDGE	Input from printer. A low pulse (5 microseconds) indicates the printer has accepted the input data.
11	BUSY	Input from printer. Printer sets this line high to indicate printer is busy; low indicates printer is not busy and can accept data. A BUSY may be sent under certain printer operating modes or error conditions. This depends upon the type of printer used.

Parallel Interface Connector Pin Assignments (Continued)

PIN NUMBER	SIGNAL	DESCRIPTION
12	OUT OF PAPER	Input from printer. High indicates that the printer is out of paper.
13	SELECT	Input from printer. High indicates printer is selected and ready to receive data.
14	-AUTO FEED	Output to printer. A low indicates that the printer should feed one line of paper.
15	-ERROR	Input from printer. A low indicates that the printer needs attention (ribbon out, cover off, etc.)
16	-INITIALIZE PRINTER	Output to printer. A low pulse (1.0 microsecond minimum) initializes the printer. Clears printer input buffer and sets the printer to default parameters. Performs a Restore function.
17	SELECT INPUT	Output to printer. This signal must be low before the printer will accept data.
18-25		Signal Grounds

REAL-TIME CLOCK

The Real-Time Clock circuit uses an OKI MSM5832IRS CMOS chip which features real-time clock/calendar function with a battery backup function for use as a microcomputer timer. The timer functions are seconds, minutes, hours, day-of-the-week, date, month, year, 12/24 hour time selection, and automatic leap year setting. The real time clock chip uses an external 32,768Hz quartz crystal as its time base. A trimmer capacitor in the oscillator circuit can be adjusted to set the accuracy of the real time clock.

Programming Suggestions

To the 8088, the real-time clock appears as one and a half ports. The clock can be read from and written to via port address 37BH. It may also be written to via port address 379H. Port address 379H is also used by the parallel port as a status input. Therefore, although writing to this port accesses the real-time clock, reading from it accesses the parallel port.

A write to port 379H will cause whatever is on the real-time clock's data lines to be strobed into the 58321 as a register address. Since the system data bus is not used, anything can be output on the data bus. A read to port 37BH will read whatever is on the data lines of the 58321 and also the BUSY status from the 58321.

Bits are assigned as follows:

BIT	FUNCTION
0	RTC D0
1	RTC D1
2	RTC D2
3	RTC D3
4	------
5	------
6	------
7	BUSY status

A write to port 37BH will write to the control register. The low four bits of this register latch data to be written to the 58321. The top four bits are latched control bits. Assignment is as follows:

BIT	FUNCTION
0	WRT DATA BIT 0
1	WRT DATA BIT 1
2	WRT DATA BIT 2
3	WRT DATA BIT 3
4	DATA INPUT BUFFER ENABLE
5	58321 READ INPUT
6	58321 WRITE INPUT
7	58321 STOP INPUT

The steps needed to transfer information into and out of the RTC are outlined below. There are two ways to write data into the 58321: using the STOP input to the 58321 or polling the BUSY status.

To write using STOP:

A. OUT 37BH, 1000AAAAB
This will set the STOP input into the 58321 and enable the input buffer. AAAA is the 4-bit address of the 58321 register to be written into.

B. OUT 379H, XXXXXXXXB
This will strobe the register address into the 58321. The Data used is irrelevant.

C. OUT 37BH, 1000DDDDB
This outputs the data to be written to the 58321. DDDD is the 4 bits of data.

D. OUT 37BH, 1000DDDDB
This enables the write strobe. DDDD is the same as in C above.

E. Wait at least 2 microseconds.

F. OUT 37BH, 1001XXXXB
This completes the write by disabling the write strobe and the input buffer. XXXX can be anything.

G. OUT 37BH, 0001XXXXB
This is done to allow the 58321 to start keeping time by disabling the STOP input.

The second method of writing to the RTC is by polling the BUSY status, bit 7 of input port 37BH until it is high. Then the same steps as listed above are followed, but the STOP bit is kept disabled. Thus, when writing to port 37BH, bit 7 is kept low.

Polling BUSY is a slower way to write to the RTC, but it does not disturb the 58321 from keeping time.

There are also several different methods of reading from the RTC. The three methods discussed below are using STOP, using BUSY, and making a comparison.

The first two methods correspond to the methods used when writing to the RTC. The only difference between the two methods is that when BUSY is polled, STOP does not have to be enabled during the access; therefore, the chip will keep counting.

Using BUSY, the following steps are necessary:

A. Wait for BUSY to go high.
Poll port 37BH until bit 7 is high

B. OUT 37BH, 0000AAAAB
This enables the input buffer and latches the register address. AAAA is the 4-bit register address.

C. OUT 379H, XXXXXXXXB
This will strobe the register address into the 58321. The data used is irrelevant.

D. OUT 37BH, 0011XXXXB
   This enables the 58321 read strobe and disables the input buffer. XXXX can be anything.

E. Wait at least 6 microseconds.

F. DATA = INP(37BH) MOD 16
   The data will be in the low 4 bits of port 37BH.

G. OUT 37BH, 0001XXXXB
   This disables the read strobe into the 58321 and completes the read. XXXX can be anything.

Using STOP, a read is accomplished in the same way with two exceptions: step A is skipped and in steps B through F, the STOP bit is enabled. Thus, when writing to port 37BH, bit 7 is kept high in steps B through F.

The third method for reading the 58321 is comparison. This method is the same as a read by polling BUSY except that step A is skipped and steps B through G are repeated until the data from two consecutive reads match. This guarantees the data to be valid.

10 — ROM Diagnostics And Monitor

INTRODUCTION

The ITT XTRA's Read Only Memory (ROM) features several levels of diagnostic and monitoring capability. Diagnostics are divided into two parts: (1) an automatic self-test that runs whenever the system unit is powered on; and (2) a menu-driven series of diagnostic tests that can be individually selected from the keyboard.

The ROM monitor offers a third highly sophisticated level of system test, providing commands that allow you to examine, modify, and move memory and to access I/O port devices. Diagnostic test and monitor commands can be accessed at any time by pressing the Ctrl Alt and ESC keys. Once the ROM ==> cursor appears, press H (for help) to display test and command menus.

The sections that follow describe the power-on self tests, the menu- driven diagnostic tests, and the monitor commands in greater detail.

POWER-UP SELF TEST

Power-Up Description

On Power-up, the processor performs a series of confidence or self-tests on the devices located on the System Motherboard. These tests are designed to indicate whether or not all devices respond and appear to be functional. After performing the confidence check, all devices are initialized to their required states for the system boot.

The memory portion of the power-up diagnostics is activated by setting SW2, position 7 on the System Motherboard to the ON position. If SW2, position 7 is in the OFF position, the system will boot without performing the memory portion of self-test. The power-up screen message indicates if the memory test is disabled.

The bootstrap process will first attempt to boot from floppy disk drive A. If the floppy disk boot fails, then an automatic boot attempt is made on the hard disk. If no hard disk is present or should the hard disk also fail, an error message will be displayed on the screen (or other selected output device) and a prompt for insertion of a diskette will be issued. If the boot is successful, the application or system software is executed out of the dynamic RAM.

The monitor on which the self-test routine displays is selected by setting SW1, positions 5 and 6 on the System Motherboard as follows:

SW1 POSITION	5	6	DEVICE SELECTED
	OFF	OFF	Monochrome Monitor or both monochrome & color monitors
	ON	OFF	Color Monitor, 80 x 25 mode
	OFF	ON	Color Monitor, 40 x 20 mode
	ON	ON	Not Used

During the entire self-test, the following message will be sent to the selected display or output device:

```
The XTRA Personal Computer
Self Test in Progress
```

or

```
The XTRA Personal Computer
Memory Test Disabled
```

The amount of memory tested during the power-up self-test is controlled by the setting of SW1, positions 3 and 4 on the System Motherboard as follows:

SW1 POSITION 3	4	AMOUNT OF MEMORY TESTED
OFF	OFF	256K and expansion RAM
ON	OFF	192K
OFF	ON	128K
ON	ON	64K

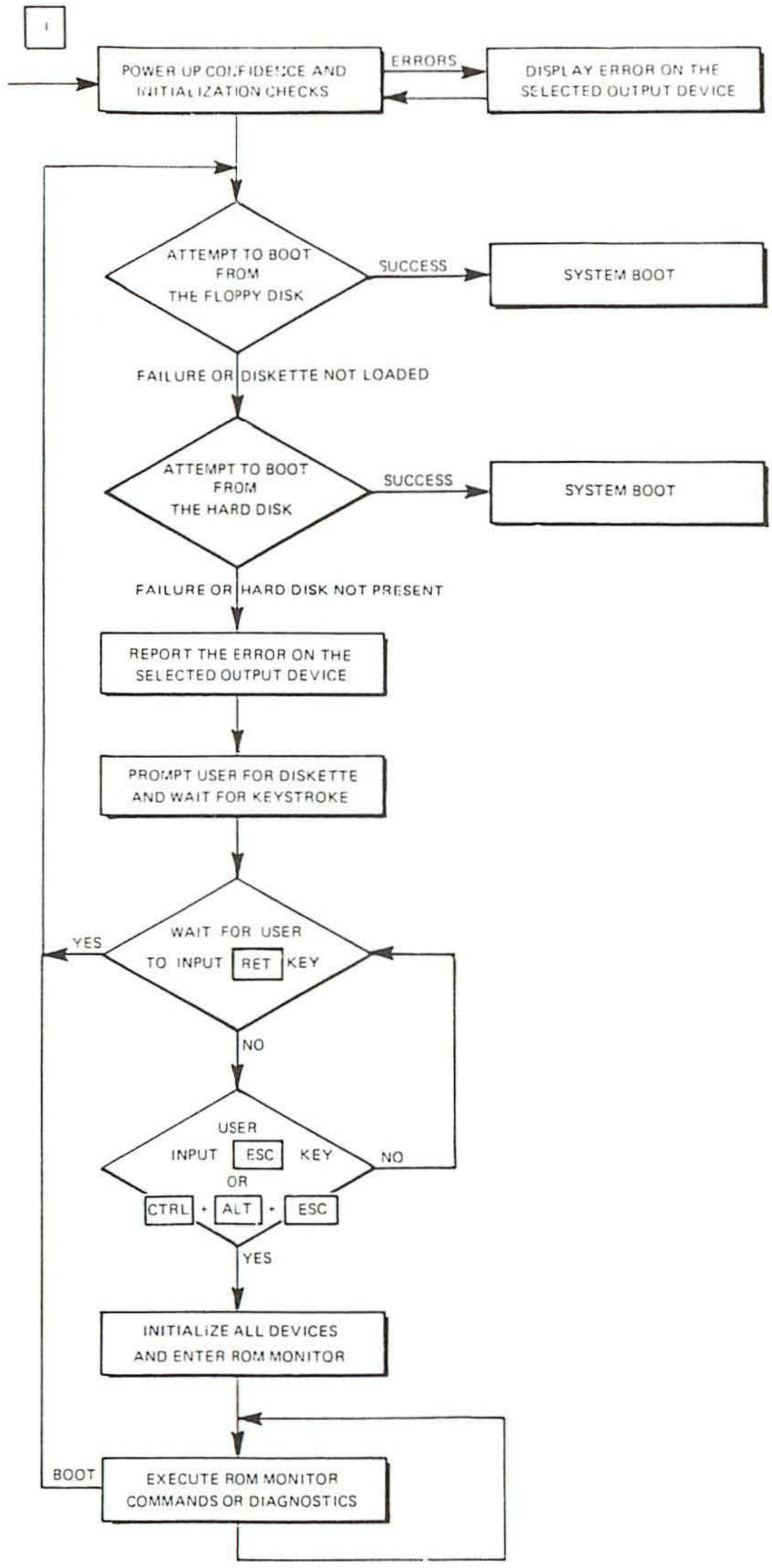
If 256K memory size is selected, then a search for the presence of expansion memory will also be performed. At the end of each 64K block of memory tested, the corresponding results are sent to the monitor (or other selected output device) in the form of one of the following status messages (nnnK will correspond to selected memory size):

```
nnnK Memory Checks OK
```

or

```
nnnK Memory Error Detected
```

If an error is detected, the check will continue to the next block. The reason for any failure of memory is not indicated. The processor will check each 64K block for write/read capability to determine the maximum amount of contiguous RAM available to the operating system.



Block Overview Of Power-Up Sequence

POWER-UP FUNCTIONAL CHECKS

The following functional checks are made at power-up time:

Check 1. Processor Registers, Flags, and Conditional Jumps

Check 2. Checksum of ROM #1 and #2

Check 3. 8255 Port Registers

Check 4. 8253 Timer 1 RAM Refresh Counter

Check 5. 8237 Port Registers

Check 6. All available Memory

Check 7. 8259 Port Registers

Check 8. 8259 Interrupt Masking

Check 9. 8253 Timer 0 Real Time Clock

Check 10. Monochrome RAM if switch selected

Check 11. Color Card RAM if switch selected

Check 12. 8087 Coprocessor if switch selected

Check 13. Keyboard Self-test

Check 14. Serial Channel 8250 Port Registers

Check 15. Parallel Port

Check 16. Real Time Clock (reserved)

Check 17. Floppy Disk Controller Port Registers

POWER-UP CHECK DESCRIPTIONS

CHECK 1 — Processor Registers, Flags, and Conditional Jumps

A check of the 8088 Processor is performed by validating the data retention of all the internal general purpose registers. The processor flags and conditional jumps are tested for functionality.

CHECK 2 — Checksum of ROM #1 and #2

Each ROM in the system is checked by adding all bytes of the ROM into one 8 bit sum. The result of the summation should always be zero. During summation, overflow carries are ignored.

The checksum byte at the end of each ROM is generated at the time the ROM based software is released.

CHECK 3 — 8255 Port Registers

The 8255 PPI is initialized to operate as three output ports. Then each of the three ports is written with unique data patterns. Each port is then read and the data is verified for accuracy. Then the opposite data pattern is written and verified.

First Pass:	0AAH -> 8255 Port A
	055H -> 8255 Port B
	05AH -> 8255 Port C
Second Pass:	055H -> 8255 Port A
	0AAH -> 8255 Port B
	0A5H -> 8255 Port C

After this check, the 8255 is configured and assumed to be functional.

CHECK 4 — 8253 Timer 1 RAM Refresh Counter

Timer 1 of the 8253 Programmable Timer is initialized as a down counter. An initial value is programmed into the counter and the processor waits for the counter to go to zero. The processor then reinitializes the counter and waits for it to go to 0FFFFH. This ensures that the data path to the 8253 is open. After its registers are checked, the 8253 is initialized for use by the 8237 DMA controller for Dynamic RAM refresh.

CHECK 5 — 8237 Port Registers

The 8237 Register bank is checked by first writing 0AAH to each port and then writing the opposite data pattern 055H. Verification is performed after each write. After the registers are checked, the DMA controller is set up for dynamic RAM refresh.

CHECK 6 — All RAM Check

Assuming the 8253 and the 8237 are in operation at this point, the dynamic RAM is checked for functionality by only checking the first 1.5K. If the first 1.5K checks out, then the processor can use this 1.5K of memory to check out the remaining RAM as selected. All expansion memory found is also tested.

All RAM is cleared to zeros upon check completion. The minimum number of interrupt vectors is initialized in the lower 1K.

CHECK 7 — 8259 Port Registers

The 8259 interrupt mask port is checked for data retention by writing 055H and 0AAH and verifying the results.

CHECK 8 — 8259 Interrupt Masking

A temporary interrupt vector is established and all interrupts are masked off at the 8259 level. Then the processor waits for approximately 2 ms and then checks for any spurious interrupts that occurred even though the interrupt mask was set. If any interrupt is received, the 8259 is not functioning properly.

CHECK 9 — 8253 Timer 0 Real Time Clock

Timer 0 of the 8253 is initialized for use as a real time clock. The interrupt vector is then established.

CHECK 10 — Monochrome RAM if switch selected

If the switches (SW1 5,6) indicate that the Monochrome card is present, a call to the video reset function is performed. This function first initializes the video controller and then does a video RAM test of the screen and attribute memory.

CHECK 11 — Color Card if switch selected

If the switches (SW1 5,6) indicate that the Color card is present, a call to the video reset function is performed. This function first initializes the video controller and then does a video RAM test of the screen memory.

CHECK 12 — 8087 Co-processor if switch selected

If the switches (SW1 position 2) indicate that the 8087 Co-processor is present, then it is initialized. It is tested for functionality by executing commands to read and write the entire 8087 register set from common system RAM. All registers and all bit patterns are tested.

CHECK 13 — Keyboard Self-test

The keyboard is issued a reset pulse to force the keyboard processor to execute a self test and return its status. If the status is bad, a message is reported and processing continues.

CHECK 14 — Primary Serial Channel Registers

The command registers on the 8250 are verified for proper data retention by writing the patterns 055H and 0AAH.

CHECK 15 — Primary Parallel Printer Port

The on-board parallel printer port is checked by ensuring that all twelve (12) bidirectional lines are operational. Ports 3BC and 3BE are considered the primary printer port.

CHECK 16 — Real Time Clock (reserved)

CHECK 17 — Floppy Disk Controller Port Registers

The 765/8272 registers are checked for data retention and addressability by writing the patterns of 055H and 0AAH to the control registers.

POWER-UP ERRORS

Catastrophic Failures

If at any time during power-up, initialization, or booting, an error is detected, the initialization code will pass an error code to the ROM Monitor for display on the selected output device. If the error is considered catastrophic, then the ROM Monitor will place the processor into a hard loop with the error code in the BP register and interrupts totally disabled. The effect is a processor halt without going into a true halt state. The low byte of the BP register is the error number indicating the failured test, and the high byte is the status byte of the failing device if available. In addition, the Video RAM and the Color card RAM located at B000:0 and B800:0, respectively, will contain the contents of the BP register if the Monochrome and/or the Color card is on the bus. The beeper will be initialized, and, if functional, a single short beep should be heard every 5 seconds. If there is a catastrophic error and no beep is heard, there are problems in the 8255 PPI and/or the 8253 Programmable Timer areas. A qualified technician, using an in-circuit emulator or similiar such device, can get to the BP register or the video static RAM containing the failure code. The first eight checks made at power-up time are considered catastrophic. The error codes are defined as follows:

1 8088 Processor
2 ROM #1
3 ROM #2
4 8255 PPI
5 8253 (Not Counting to 0)
6 8253 (Not Counting to 0FFH)
7 8237 DMA
8 Dynamic RAM (lower 1.5K)

Non-Catastrophic Failures

Certain errors that are detected are considered not catastrophic but may or may not prevent the processor from booting the system or application. For example if a serial port is defective, the operating system will still boot from the boot device. These errors are reported by the ROM Monitor and control is returned to the power-up code to continue with further initialization until a hard error or a successful bootstrap occurs.

POWER-UP ERROR MESSAGES

The following messages will appear on the display device and the processor will not halt but continue to initialize other devices and attempt to boot the system from the boot device:

System Unit Error Detected

Keyboard Error Detected

nnK Memory Error Detected

Monochrome Video Error Detected

Color Video Error Detected

Floppy Controller Error Detected

Hard Disk Controller Error Detected

Option Card Error Detected, Status is:

With any error detected, the system may or may not boot, depending on the actual reason for the failure.

ROM DIAGNOSTICS

ROM Based Diagnostic Commands

Included in the ROM based software is a diagnostic package to test the System functions that are standard in all systems. The diagnostic test areas are:

```
DIAGNOSTICS

1. System Board
2. Memory
3. Floppy
4. Keyboard
5. Video
6. All Tests [Repeat]
```

Each of these diagnostics is selected by entering the desired menu number (1-6) and pressing Retrn. When one of these diagnostics is selected, a secondary menu will be displayed along with a prompt that indicates that the current menu is a diagnostic and not part of the ROM monitor. To return to the ROM monitor, press Esc and the ROM monitor prompt => will return.

While you are in a diagnostic menu, the Help command will display the current diagnostic menu and not the main ROM monitor menu. All ROM monitor commands, as described later in this section, remain available while in a diagnostic menu.

SYSTEM BOARD DIAGNOSTICS DESCRIPTION

Upon selecting the System Board Diagnostic option (diagnostic menu number 1), the following menu will be displayed and a new prompt will be issued:

```
                    MOTHERBOARD

                1. 8259 Interrupt [Repeat]
                2. 8253 Timer [Repeat]
                3. ROM [Repeat]
                4. 8255 PPI [Repeat]
                5. 8087 Coprocessor [Repeat]
                6. Sound [Repeat]
                7. Parallel Printer Port [Repeat]
                8. Serial Communication Port [Repeat]

SB=>
```

1. 8259 Interrupt Test

The 8259 Interrupt Controller is tested by verifying that all registers are functional and that all interrupts can be masked off. The 8253 Timer is then used to generate interrupts to check the actual interrupt vector generation.

2. 8253 Timer Test

The 8253 Timer Controller is tested by verifying that all registers are functional and that all three channels are able to count down.

3. ROM Test

The system ROMs #1 and #2 are checked by summing all the bytes in each ROM and verifying that the result is zero.

4. 8255 PPI Test

The 8255 PPI is tested by initializing all ports to be output ports. Then each port register is checked for proper data retention.

5. 8087 Co-Processor Test

The 8087 is tested only if switch SW1, position 2 is OFF. This switch indicates whether the 8087 Coprocessor is present on the motherboard. The test consists of simply issuing commands and data to the 8087 and verifying that the answer is correct and that the 8087 handshake is operational. Note that if the 8087 is not physically present on the board, or not responding, the 8088 processor will hang in a permanent wait state waiting for the ESC release from the 8087.

6. Sound Test

Sound is tested by running through a series of eight tones, each lasting one half second, with a one half second pause between tones.

7. Parallel Printer Port Test

The parallel printer port is tested by checking all 12 I/O lines for proper operation and that the correct interrupts are generated. The final test uses a special external loop- back connector to test all drivers and receivers.

8. Serial Communications Port Test

The 8250 registers are checked for functionality. Next, the UART is programmed to operate in local loop-back mode and is tested with a unique data stream.

MEMORY DIAGNOSTICS DESCRIPTION

Upon selecting the Memory Diagnostic option (diagnostic menu number 2), the following menu will be displayed and a new prompt will be issued:

```
MEMORY

   1. Memory Map
   2. Motherboard Memory [Range]
      [Repeat]
   3. Expansion Memory [Range] [Repeat]
   4. All Contiguous Memory [Repeat]

ME=>
```

1. Memory Map

The System Memory Map function will search the entire 1 megabyte address space and report where valid RAM was found.

Example display:

System Memory Map	Comments
00000 to 3FFFF	256K
B0000 to BFFFF	Monochrome and Color Card

2. Motherboard Memory

The motherboard memory may consist of up to 256K of RAM located on the system motherboard. All RAM tests are performed using the same algorithm. First, a data pattern is written based on a random number generator. Then the entire pattern is verified for data retention. During the verification pass, the data pattern is complemented in place to check the opposite bits. A final pass is done to verify that complemented data is still valid. Finally, the RAM is cleared to zeros.

Example Display:

```
  64K Memory Checks OK
 128K Memory Checks OK
 192K Memory Checks OK
 256K Memory Checks OK

ME =>
```

In the event of a memory error, the following error message will be reported:

```
Memory Error Detected at SEG:OFF Should be xx is yy
```

The actual message will contain the expected data instead of xx and the erroneous data instead of yy. An optional Range parameter may be used to narrow down a failing device or memory cell.

3. Expansion Memory

Testing of the Expansion Memory is done using the same algorithm as in the System RAM test. The expansion RAM must start after the 256K of system RAM and must be contiguous up to the one megabyte addressing domain. The amount of expansion RAM is controlled by a memory search done at power- up time. An optional Range parameter may be used to isolate a failing device or memory cell.

Example display:

```
320K Memory Checks OK
384K Memory Checks OK
448K Memory Checks OK
512K Memory Checks OK
576K Memory Checks OK
640K Memory Checks OK
```

4. All Contiguous Memory

Testing of all contiguous RAM at the same time can be done using this test. The amount of expansion RAM tested is controlled by the memory search done at power-up time.

```
 64K Memory Checks OK
128K Memory Checks OK
192K Memory Checks OK
256K Memory Checks OK
320K Memory Checks OK
384K Memory Checks OK
448K Memory Checks OK
512K Memory Checks OK
576K Memory Checks OK
640K Memory Checks OK
```

FLOPPY DISK DRIVE DIAGNOSTICS DESCRIPTION

Upon selecting the Floppy Disk Diagnostic option (diagnostic menu number 3), the following menu will be displayed and a new prompt will be issued:

```
   FLOPPY DISK

1. Read [Drive] [Repeat]
2. Write/Read [Drive] [Repeat]
3. Random Read [Drive] [Repeat]
4. Random Write/Read [Drive] [Repeat]
5. Format [Drive]

FD=>
```

1. Read Test

This test will read the entire previously formatted diskette starting with the current drive Side 0, Track 0, Sector 1, and continue through the entire diskette as defined by the configuration parameters.

2. Write/Read Test

This test will write and read the entire diskette, starting with track 0, side 0, sector 1, and continue through both sides of the diskette as defined by the configuration parameters.

After selecting test 2 the following message will appear on the selected output device:

```
WARNING - This test will DESTROY data on the diskette!

Insert formatted scratch diskette in drive 0
Press the RETURN key to continue
```

3. Random Read Test

This test will read the previously formatted diskette, using a random track, sector, and side. This test is nondestructive as only a read is performed.

4. Random Write Test

This test will write and read the diskette, using a random track, sector, and side.

After selecting test 4 the following message will appear on the selected output device:

```
WARNING - This test will DESTROY data on the diskette!

Insert formatted scratch diskette in drive 0
Press the RETURN key to continue
```

5. Format Test

This test will format an entire diskette, starting with track 0 and extending through the maximum number of tracks as definded in the Config command. All other parameters, including tracks per disk, number of sides, sectors per track, and sector size, are also defined by the Config parameters.

After selecting test 5 for formatting, the following message will appear on the selected output device:

```
Insert diskette to be formatted in drive 0
Press the RETURN key to continue
```

KEYBOARD DIAGNOSTICS DESCRIPTION

Upon selecting the Keyboard Diagnostic option (diagnostic menu number 4), the following menu will be displayed and a new prompt will be issued:

```
KEYBOARD

1. Reset/Status
2. Key Positions
3. Interactive Test

KB=>
```

1. Reset/Status

This test issues a reset command to the keyboard processor and displays the status returned from the keyboard. The keyboard processor performs a self test and returns a status to the CPU for processing. If the keyboard returns a valid status, the following message will be printed:

```
Keyboard Checks OK
```

2. Key Positions

The key positions test is a manual display of the scan codes being returned from the keyboard. The selected output device will indicate the key position number and will indicate whether the key was pressed or released. The repeat function of any key can be tested by holding that key down. The repeating key should send repeated presses without any releases. To exit this diagnostic, press [Esc]. [Esc] is the only key that cannot be fully checked with this test.

Example Display:

```
Press a key -> key n Pressed
Press a key -> key n Released
```

3. Interactive Test

The interactive keyboard test is designed as an intensive user test to check that the position numbers correspond to the correct physical locations on the keyboard. Upon selecting the test, the following prompt will be issued:

```
Press Key Number 1 ->
```

Press the key prompted for. If the test is successful, an OK will be displayed. If the test is unsuccessful, then the following message will appear:

```
That was Key n
```

The user will then be reprompted for the correct next key.

The test may be terminated by pressing [Esc] twice.

VIDEO DISPLAY DIAGNOSTICS DESCRIPTION

Upon selecting the video diagnostic option (diagnostic menu number 5), the following menu will be displayed and a new prompt will be issued:

```
VIDEO DISPLAY

1. Alignment
2. Character Set
3. Character Attributes
4. Video RAM [Repeat]

VD=>
```

1. Alignment Test

The alignment display will simply fill the entire screen with upper case H's. This test provides vertical and horizontal reference points for image alignment. Press Esc to exit the test.

2. Character Set Test

To display the character set, select menu item 2. The entire primary and secondary character set will be displayed along with its corresponding hex code.

3. Character Attributes Test

To display the character attributes of the Video Display, select menu item 3. Starting at the top, several lines of text will be placed on the screen. Each line of text will state and actually perform the selected character attribute for that line. The character attributes are:

Normal Intensity,
High Intensity,
Blinking (normal and high intensity),
Reverse Video (normal and high intensity and blinking),
Underlining (normal and high intensity and blinking).

This test can also be used in conjuntion with the VIDEO command and a color monitor to display the available colors. See the example under VIDEO for additional details.

4. Video RAM Test

To test the Video RAM, select menu item 4. This will perform the same memory test on the video RAM as on the System RAM. Reports back "Video RAM - OK".

ALL TESTS DIAGNOSTICS DESCRIPTION

When the All Tests Diagnostic option is selected (diagnostic menu number 6), test results similar to the following are automatically displayed:

```
8259 Interrupt Controller - OK
8253 Timer Controller - OK
ROM 1 - OK
ROM 2 - OK
8255 PPI Controller - OK
8087 Math Coprocessor Not Present
Sound Test Complete
Parallel Printer Port - OK
Serial Communications Port - OK
 64K Memory Checks OK
128K Memory Checks OK
Keyboard Checks OK

=>
```

These test routines have already been described under the respective Diagnostic Description heading.

ROM BASED MANUFACTURING DIAGNOSTICS

There is a set of manufacturing tests that can be activated by using Switch Pack 2 (SW2) position 8. If this switch is on, the normal power-up diagnostics and bootstrapping are not performed. Instead, diagnostic 6, (All Tests), is executed continuously until the switch is turned off. The devices tested during these routines are located on the system board only and are listed below:

8259 Interrupt Controller
8253 Timer
System ROM Checksums
8255 PPI Controller
8087 Co-processor (if switch indicates)
Sound
Parallel Port
Serial Port
System RAM
Keyboard Reset/Status

ROM MONITOR

ROM Monitor Description

The ROM Monitor is designed for use by knowledgeable personnel and is not recommended for use by the end user. The ROM Monitor can be used to examine system functions. Included in this monitor are commands to examine, modify, and move memory as well as commands to access the I/O port devices. A special function has been added to each command to allow the command to be repeated a number of times or continuously. This feature is useful to a technician who is trying to troubleshoot a failed unit.

The ROM Monitor initialization code assumes that all devices are functional and simply initializes them blindly before attempting to use them. Therefore, if the boot process fails, it may not be possible to get into the ROM Monitor.

The ROM monitor can be activated in two ways:

First, when the normal power-up sequence is executed and the boot fails for whatever reason, the user may activate the ROM Monitor by pressing the Escape key in response to the Insert Diskette prompt. The ROM Monitor startup message and prompt => will appear on the screen (or selected output device).

The second method to activate the ROM Monitor is by simultaneously pressing the Ctrl + Alt + Esc keys. This 3-key command will always place the ROM Monitor into execution, as long as the ROM keyboard interrupt service routine is in use.

The output of the ROM Monitor may be directed to the parallel port for a hard copy printout by pressing Ctrl + P. All messages will be displayed on the selected output device at the parallel port. To stop output to the parallel port, push Ctrl + P again. If the printer is not ready, the keyboard will hang after pushing Ctrl + P; push Ctrl + P again to free up the keyboard.

ROM MONITOR DEFINITIONS

[ ] Any command option enclosed in braces is optional

Address — Address is a standard 8088 segmented address of the form SEG:OFF, where **SEG** is a 16 bit hexadecimal number representing the **seg**ment register value, and **OFF** represents a 16 bit hexadecimal **off**set value. If an address is not specified in an optional parameter, it is defaulted to zero.

Value — Value is a 16 bit decimal or hexadecimal value. Hexadecimal values are numbers followed by the letter 'H'. If a value is not specified in an optional parameter, it is defaulted to zero.

Range — Range is defined as a starting address followed by either a length specification or an offset from the starting address. A **length** specification is a 16 bit value preceded by the letter **L**. An **off**set specification is a 16 bit value with no preceding letters, e.g. 1234 is an offset and L1234 is a length in bytes. If no offset or length is specified, the default is 64K length. A user entry may take this form:

[<SEG:OFF>] or
[<SEG:OFF>L<nn>]

Repeat — Repeat is defined as the number of times the command or diagnostic is to be repeated. The format is the letter **R** for **repeat**, followed by the decimal repeat count. If the repeat count is omitted, then the repeat is performed continuously until stopped by other action, e.g. R1234 will cause the command to be repeated 1234 times then stop, while R only will repeat the command continuously. If the entire repeat option is omitted then an implied count of 1 is used. A user entry may take this form:

[R[<nn>]]

Port	Port is a 16 bit hexadecimal value representing the I/O port address of a physical device.
Drive	Drive defines a physical diskette drive number in the range of 0 to 3. Unless specified, the default is 0.
Side	[Side] represents the diskette side (or R/W head number) in the drive. Valid entries are 0 or 1. The default is side 0.
Track	[Track] represents a track or cylinder number (on the diskette) in the diskette drive. Valid entries, using current hardware, must be in the range of 0 to 39.
Sector	[Sector] represents a physical sector number on the diskette. Current media uses sector numbers in the range of 1 to 9. Default is sector 1.
Count	[Count] represents the number of sectors to transfer, starting with the specified sector up to the maximum number of sectors per track. Default is 1 sector.
	Represents the Retrn key. All command lines are terminated with a return (Carriage Return).
	Represents the Esc key. Pressing Esc when in the ROM monitor will abort the current command line and reissue the prompt =>. Pressing Esc when in a diagnostic menu will terminate the current command and return to the ROM Monitor prompt. If a diagnostic is in progress, pressing Esc will stop the test and return to the diagnostic menu.

ROM MONITOR COMMAND ERROR MESSAGES

No Such Command

The user selected an invalid ROM Monitor command or a diagnostic selection that is not in the current menu.

Syntax Error

The user did not supply the correct parameter syntax for a ROM Monitor command or for a diagnostic option. Use the Help command to see the current menu.

BOOT

Syntax: =>B

Description: Boot will attempt to boot from floppy disk drive A. If drive A is not ready, a boot will be attempted from the hard disk, if present. No power-up diagnostics are performed before attempting to boot from the device.

Examples: =>B

Note that there are no messages or status on the screen after using the boot command. This command is a complete exit from the ROM Monitor and does not return unless the boot fails and the user uses the Esc key to reactivate the Monitor.

Syntax: =>C [S]

Description: The Config command allows the user to display or modify the floppy disk parameters. If the set option [s] is not specified, Config will display the current floppy disk parameters and motherboard DIP switch settings. By specifying the set [s] option, the user can change the drive parameters as they are prompted for. If an invalid parameter is entered in response to a parameter prompt, the user will be reprompted for the same parameter until a valid parameter is received. The prompting sequence can be aborted by using the Esc key; however, all parameters modified up to that point are in effect. If the parameter is not to be modified, then press Retrn to indicate no modification and the next parameter will be prompted for. When all parameters have been exhausted, the ROM monitor will return.

Examples: To display the current parameters use: (the values are the current defaults)

```
=>C

Sector Size . . . . . .   512 Bytes
Sectors per Track . . .   8
Tracks per Disk . . . .   40
Number of Sides . . . .   2
Seek Step Rate  . . . .   6 ms
Head Settle Time  . . .   16 ms
Motor Startup Time  . .   500 ms

Current Switch Settings

12345678  0 = ON, 1 = OFF
SW1  =  10111100
SW2  =  11111001

=>
```

CONFIG

To set new parameters use:

```
=>C S
Sector Size              =>512
Sectors per Track        =>10
Tracks per Disk          =>40
Number of Sides          =>1
Seek Step Rate:          =>6

Head Settle Time         =>40

Motor Startup Time       =>2

=>
```

Valid Selections
256, 512, 1024
1 to 255
1 to 255
1 or 2
2 to 32 in 2 ms increments
1 to 255 ms in 2 ms increments
from 1 to 255 in units of 250 ms

Syntax: =>D [[Address] or [Range]] [Repeat]

Description: Dump will display memory in hexadecimal bytes and in printable ASCII. The display is formatted at 16 bytes per display line and will always be a minimum of 16 bytes even if the length or offset is less. On a long dump the display scrolling can be stopped by pressing the Space bar once. To continue with a long dump press the Space bar again. Pressing Esc will abort the dump. Note that the largest dump is a 64K segment. The offset register will wrap around to 0000H if the offset exceeds 0FFFFH.

Examples: To start dumping memory at 0000:0 use:

```
=>d

0000:0000 4B FF 00 F0 4B FF 00 F0 - 5F F8 00 F0 4B FF 00 F0 K...K._.K..
0000:0010 4B FF 00 F0 54 FF 00 F0 - 4B FF 00 F0 4B FF 00 F0 K..T..K..K..
0000:0020 A5 FE 00 F0 87 E9 00 F0 - 23 FF 00 F0 23 FF 00 F0 .....#...#...
0000:0030 23 FF 00 F0 23 FF 00 F0 - 57 EF 00 F0 23 FF 00 F0 #..#..W..#..
0000:0040 65 F0 00 F0 4D F8 00 F0 - 41 F8 00 F0 59 EC 00 F0 e..M..A..Y..
Esc
=>
```

To begin dumping at 400:0 use

```
=>d 400:0

0400:0000 05 00 47 B9 08 00 AB 04 - 93 B0 20 74 04 03 F9 33 ..G..t..3
0400:0010 C9 F3 AA B1 03 F6 C3 08 - 74 04 03 F9 33 C9 F3 AA ...t..3..
0400:0020 91 AB AB 83 EF 10 F6 C3 - 01 74 09 E8 73 00 E8 80 ...t..s..
0400:0030 01 75 04 46 E8 6A 00 E8 - 49 01 76 16 80 3C 75 .u.F.j..I.v..<:u
0400:0040 11 46 2C 40 76 07 36 3A - 06 00 01 76 02 B2 FF AA .F,@v.6:...v..
Esc
=>
```

DUMP

To dump 30 decimal bytes starting at 500:0 use:

```
=>d 500:0 L 30

0500:0000 03 F6 45 1B C0 75 17 FF - 75 02 E8 FD F0 5B 36 88 .E..u..u..[6.
0500:0010 1E 45 03 E8 FD EB 3C FF - 75 04 B0 02 EB C7 E9 6C .E..<.u..1
=>
```

To dump 8 bytes starting at 600:0 and repeat it 5 times use:

```
=>D 600:0 L 8 R 5

0600:0000 73 69 6E 67 20 43 6F 6D - 6D 61 6E 64 20 49 6E 74 sing Command Int
0600:0000 73 69 6E 67 20 43 6F 6D - 6D 61 6E 64 20 49 6E 74 sing Command Int
0600:0000 73 69 6E 67 20 43 6F 6D - 6D 61 6E 64 20 49 6E 74 sing Command Int
0600:0000 73 69 6E 67 20 43 6F 6D - 6D 61 6E 64 20 49 6E 74 sing Command Int
0600:0000 73 69 6E 67 20 43 6F 6D - 6D 61 6E 64 20 49 6E 74 sing Command Int
=>
```

To dump the memory block from 700:0 thru 700:30 use:

```
=>D 700:0 0700:30

0700:0000 82 09 E8 8D 06 0E 1F E9 - 0C FB E8 FD FE 81 3E 7C ...>|
0700:0010 08 00 F0 75 06 C7 06 7C - 08 FF FF E9 96 F8 E8 76 ..u..v
0700:0020 00 E8 04 01 56 E8 F2 00 - 5E 75 01 C3 E8 DA 00 E8 ..v..u..
0700:0030 E8 00 EB 36 E8 E3 00 74 - 3B 33 DB 56 AC 3C 0D 74 .6.t;3.V.<.t
=>
```

Syntax: **=>E Value [+/-] [Value]**

Description: Evaluate displays the result of either adding the first value to the second value or subtracting the second value from the first value. The input values may be decimal, or hexadecimal with an H suffix. The results are displayed in both decimal and hexadecimal. The operation code is optional in which case it defaults to addition. If only one number is used, the number is given in hexadecimal and decimal. The Evaluate command is useful in computing offsets when dealing with relative code.

Examples: To find the decimal and hexadecimal result of 12 + 34, use:

```
=>E  12  +  34
46  002EH
=>
```

To find the result of 12H and 34, use:

```
=>E  12H  +  34
52  0034H
=>
```

To find the difference between 12H and 34H, use:

```
=>E  34H  -  12H
34  0022H
=>
```

To find the decimal value of 0ABCDH, use:

```
=>E  0ABCDH
43981  ABCDH
=>
```

FILL

Syntax: **=>F Range [Hex Value] [Repeat]**

Description: Fill will deposit the specified value into the memory block specified by the range. No check is made to ensure that there is valid memory at the specified memory address.

The user must be very careful in specifying the address of the memory block. For example, the first 1.5K of RAM at physical address 00000H is reserved for interrupt vectors and data. Should this area get overwritten by the fill command, or any other memory manipulation command, the results are unpredictable.

Examples: To fill memory from 1000:0 thru 1000:4F with AAH, use:

```
=>F  1000:0  1000:4F  AAH
=>
```

To fill 256 decimal bytes starting at 0:800 with 55H, use:

```
=>F  0:800  L  100H  55
=>
```

To fill 4K bytes starting at 1000:0 and repeat it 10 times, use:

```
=>F  1000:0  L  1000H  A5  R  10
```

Syntax: **=>G Address**

Description: Go will cause an absolute jump to the mandatory address specified. No provision for examining or modifying the 8088 registers is provided. The screen will display the address that the processor is jumping to since this is a complete exit from the Monitor.

The user should be very careful in using this command since an incorrect jump can result in program destruction and/or cause the processor to enter an infinite loop.

Examples: The most common use of this command is to perform a processor reset by jumping to address FFFF:0. Location FFFF:0 will always contain a valid reset vector. Jumping to FFFF:0 will cause the processor to reset the system as if a power-up reset had been performed.

```
=>G FFFF:0

Jumping to FFFF:0
```

Note

As in the Boot command, the Monitor will no longer be functional after executing a Go command.

HELP

Syntax: =>H

Description: Help will display a complete menu to assist the user in the correct usage of the commands and diagnostics available in the ROM Monitor. The help command functions differently depending upon what the current menu is. When in the ROM Monitor, (prompt is =>), the help menu will display the diagnostic menu and the ROM Monitor commands. When using a selected diagnostic, the help command will only display the current diagnostic menu even though all of the ROM Monitor commands are usable at all times.

Example 1: =>H

```
   DIAGNOSTICS

1. System
2. Memory
3. Floppy
4. Keyboard
5. Video
6. All Tests [Repeat]

   MONITOR COMMANDS

Boot      B
Config    C [S]
Dump      D [ [Address] or [Range] ] [Repeat]
Evaluate  E Value [ [+] or [-] ] [Value]
Fill      F Range [Hex Value] [Repeat]
Go        G Address
Help      H
Move      M Range Address [Repeat]
Port      P Port [Hex Value] [Repeat]
Read      R Address [Drive] [Side] [Track] [Sector]
          [Count] [Repeat]
Sub       S Address [Hex Value] [Repeat]
Video     V Mode
Write     W Address [Drive] [Side] [Track] [Sector]
          [Count] [Repeat]

=>
```

Example 2: ME=>H

```
   Memory

1. Memory Map
2. Motherboard Memory [Range] [Repeat]
3. Expansion Memory [Range] [Repeat]
4. All Contiguous Memory [Repeat]

ME=>
```

MOVE

Syntax: **=>M Range Address [Repeat]**

Description: Move will move all data from the source block specified by the range parameter to the destination block specified by the address parameter. The move command will allow overlapping intrasegment blocks to be moved with no data loss due to overwrite caused by the direction of the data movement. The move command will allow inter-segment data moves. However, there is no checking for overlapping segments and the user must be aware that data overwrite can occur if the segments overlap. It is recommended that only intrasegment moves be used. The repeat option allows a block to be repeatedly copied from one location to another.

Examples: To move 4K bytes from 0000:0 to 0000:1000, use:

```
=>M 0000:0 L1000H 0:1000
=>
```

To move memory from 1000:0 thru 1000:3F to 700:0, use:

```
=>M 1000:0 1000:3F 700:0
=>
```

To move an overlapping block of 8K bytes from 0000:0 to 0800:0, use:

```
=>M 0000:0 L2000H 0800:0
=>
```

Syntax: **=>P Port [Hex Value] [Repeat]**

Description: Port will display the current contents of the specified I/O port and then wait for any value to be output to that port. After displaying the current value the user has the option to change the value or to leave it unchanged. A [Retrn] will leave the location unchanged and the contents of the port will be redisplayed. If a value is specified on the syntax command line, the value is written to the I/O port before being displayed. When the repeat option is used, the I/O port being examined is either read repeatedly or written repeatedly depending on whether a value was specified on the invocation command line. To terminate the Port read mode use the [Esc] key. This will return the user to the ROM Monitor prompt.

Examples: To simply examine an I/O port at 00H, use:

```
=>P 00
Port 0000 = 00 [Esc]
=>
```

To write the value 0AAH to the I/O port at 3F0H, use:

```
=>P 3F0H 0AAH
Port 03F0 = 00 [Esc]
=>
```

To write the value 55H to port 20H continuously, use:

```
=>P 20 55 r
```

READ

Syntax: **=>R Address [Drive] [Side] [Track] [Sector] [Count] [Repeat]**

Description: Read allows the user to read a specific sector from the disk into a RAM location. The RAM address is mandatory and if no options are specified, they will default to the following:

Drive	0	Drive 0
Side	0	Side zero
Track	0	Track zero
Sector	1	Sector one
Count	1	Read one sector
Repeat	1	Do command once

Note

When using the Count option, it is not possible to read past the last sector on the selected track, i.e., the maximum count will be the number of sectors per track. Track wrap-around is not performed.

Examples: To read drive 0, side 0, track 10, sector 2 into location 1000:0, use:

```
=>R  1000:0  0  0  10  2
=>
```

Note

Use the dump command to look at the sector read.

To read 4 sectors starting at drive 0, side 1, track 2 sector 3, use:

```
=>R  1000:0  0  1  2  3  4
=>
```

Syntax: **=>S Address [Hex Value] [Repeat]**

Description: Substitute will display the current contents of the specified address and then wait for a value to be deposited at that location. After the current value is displayed, the user has the option to change the value or to leave it unchanged. Pressing [Retrn] will leave the location unchanged and the contents of the next logical address will be displayed. Typing a - (minus symbol) followed by [Retrn] will cause the contents of the previous logical address to be displayed. If a value is specified on the invocation command line, the value is written to the memory before being displayed. When the repeat option is used, the location being examined is either read repeatedly or written repeatedly depending on whether a value was specified on the invocation command line. To terminate the substitute mode use the [Esc] key. This will return the user to the current prompt.

Examples: To simply examine a memory location at 800:0, use:

```
=>S 800:0
0800:000 00 [Esc]
=>
```

To write the ASCII string 'ABC' starting at location 900:0, use:

```
=>S 900:0
0900:0000 00 41
0900:0001 00 42
0900:0002 00 43
0900:0003 00 [Esc]
=>
```

VIDEO

Syntax: **=>V mode**

Description: This command to select one of the following modes:

```
0      40 x  25 BW      ALPHA
1      40 x  25 Color   ALPHA
2      80 x  25 BW      ALPHA
3      80 x  25 Color   ALPHA
4     320 x 200 Color   GRAPHICS
5     320 x 200 BW      GRAPHICS
6     640 x 200 BW      GRAPHICS
```

Example: To switch from a monochrome to a color display, type v 3 and press Retrn. This will cause the monitor prompt => to display on the color monitor. If you then select the video display diagnostic test and run test 3, "Character Attributes," the sixteen available colors will appear on the monitor.

Syntax: **=>W Address [Drive] [Side] [Track] [Sector] [Count] [Repeat]**

Description: Write allows the user to write a specific sector from a RAM location to the Disk. The RAM address is mandatory and if no options are specified, they will default to the following:

Drive	0	Drive zero
Side	0	Side zero
Track	0	Track zero
Sector	1	Sector one
Count	1	Read one sector
Repeat	1	Do command once

Note

When using the Count option, it is not possible to read past the last sector on the selected track, i.e., the maximum count will be the number of sectors per track. Track wrap-around is not performed.

Examples: To write drive 0, side 0, track 10, sector 2 from location 1000:0, use:

```
=>W  1000:0  0  0  10  2
=>
```

To write 4 sectors starting at drive 0, side 1, track 2 sector 3, use:

```
=>R  1000:0  0  1  2  3  4
=>
```

11 — ROM Bios

INTERRUPT VECTORS

ADDRESS (HEX)	INTERRUPT NUMBER	NAME	BIOS ENTRY
0-3	0	Divide by Zero	INTR_TRAP
4-7	1	Single Step	INTR_TRAP
8-B	2	Nonmaskable	NMI_INT
C-F	3	Breakpoint	INTR_TRAP
10-13	4	Overflow	INTR_TRAP
14-17	5	Print Screen	PRINT_SCREEN
18-1B	6	Reserved	INTR_TRAP
1D-1F	7	Reserved	INTR_TRAP
20-23	8	Timer	TIME_INT
24-27	9	Keyboard (hardware)	KB_INT
28-2B	A	Reserved	INTR_TRAP
2C-2F	B	Reserved	INTR_TRAP
30-33	C	Reserved	INTR_TRAP
34-37	D	Reserved	INTR_TRAP
38-3B	E	Floppy Disk	FD_INT
3C-3F	F	Parallel Printer	PRT_INT
40-43	10	CRT Video I/O	VIDEO_IO
44-47	11	Equipment Check	EQUIP_CHK
48-4B	12	Memory Check	MEMORY_CHK
4C-4F	13	Disk I/O	FD_IO/HD_I/O
50-53	14	RS232 Communications	RS232_IO
54-57	15	Reserved	INTR_TRAP
58-5B	16	Keyboard I/O	KB_IO
5C-5F	17	Parallel printer I/O	PRT_IO
60-63	18	ROM Monitor Entry	INTR_TRAP
64-67	19	IPL/bootstrap Loader	IPL/CODE
68-6B	1A	Return Time of Day	TIME-OF-DAY
6C-6F	1B	Keyboard Break Address	INTR_TRAP
70-73	1C	Timer Break Address	INTR_TRAP
74-77	1D	Video Parm Block Ptr	0
78-7B	1E	Disk Parm Block Ptr	0
7C-7F	1F	Video Graphics Chars	0

BASIC AND DOS RESERVED INTERRUPTS

ADDRESS (HEX)	INTERRUPT (HEX)	FUNCTION
80-83	20	DOS Program Terminate
84-87	21	DOS Function Call
88-8B	22	DOS Terminate Address
8C-8F	23	DOS Ctrl Break Exit Address
90-93	24	DOS Fatal Error Vector
94-97	25	DOS Absolute Disk Read
98-9B	26	DOS Absolute Disk Write
9C-9F	27	DOS Terminate, Fix in Storage
A0-FF	28-3F	Reserved for DOS
100-103	40	Floppy Disk I/O (for Hard Disk System)
104-107	41	Hard Disk Parameter Table
108-17F	42-5F	Reserved
180-19F	60-67	Reserved for User Software Interrupts
1A0-1FF	68-7F	Not Used
200-217	80-85	Reserved by XBASIC
218-3C3	86-F0	Used by XBASIC Interpreter while XBASIC is Running
3C4-3FF	F1-FF	Not Used

RESERVED MEMORY LOCATIONS (400-5FF)

INTERRUPT DESCRIPTIONS

INT 5H - PRINT SCREEN

This routine supports the print screen function. The routine saves the starting position of the cursor and starts printing from the upper left hand corner of the screen after obtaining the pertinent video information such as the number of columns and the current page. The routine replaces unprintable characters with a space. When the entire screen has been printed, the original cursor is restored.

INT 8H - TIMER INTERRUPT

This routine processes interrupts generated by the 8253 timer controller which runs at a rate of 19.2 interrupts per second. A counter for the real time clock is maintained. When this 32-bit count reaches one day, it is reset to zero and the overflow count is incremented. In addition, a timer for the floppy motor is maintained. When this counter reaches zero, the floppy spindle motor is turned off.

INT 10H - CRT VIDEO I/O

This I/O driver supports both the monochrome and color 6845 CRT controllers. It provides a basic driver to the interface cards and a programatic interface to the system and its users. The following features are provided:

General functions:

1. Set mode
2. Set cursor type
3. Set cursor position
4. Read cursor position
5. Read light pen position
6. Select active display page
7. Scroll active page up
8. Scroll active page down

Character handling functions:

9. Read attribute & character at cursor position
10. Write attribute & character at cursor position
11. Write character at cursor position

Graphics functions:

12. Set color: pallette or background/border color
13. Write dot
14. Read dot

ASCII teletype function:

15. Write teletype

Status function:

16. Current video status

Extended functions for Advanced BASIC support:

17. Generalized video display move
18. Generalized video display fill
19. Convert (page, row, column) to (segment:offset)
20. Convert offset to (page, row, column)

Functions:

1. Set mode

(AH) = 0 character modes:

(AL) = 0	40 x 25 BW
(AL) = 1	40 x 25 color
(AL) = 2	80 x 25 BW
(AL) = 3	80 x 25 color

graphics modes:

(AL) = 4	320 x 200 color
(AL) = 5	320 x 200 BW
(AL) = 6	640 x 200 BW

If bit 7 AL is set on input, then Set Mode assumes that the caller desires to use two video cards at once, and that the setting of mode should not clear the cursors, nor the video ram, nor reinitialize the video controller. The feature assumes that typical use will be switching between monochrome text and color graphics modes for simultaneous use.

2. Set cursor type

(AH) = 1 (CH) = bits 4-0 = start line for cursor
(CL) = bits 4-0 = end line for cursor

3. Set cursor position

(AH) = 2 (DH, DL) = row, column address
(BH) = page number (ALPHA modes only)

Notes

(0,0) is the upper left corner. If the page given is the active page, the hardware cursor registers are reset.

4. Read cursor position

(AH) = 3 (BH) = page number (ALPHA modes only)

On return:

(DH, DL) = row, column address of cursor position
(CH, CL) = current cursor type (see #2)

5. Read light pen position

(AH) = 4

(AH) = 0 - light pen switch not down/not triggered
(AH) = 1 - valid light pen value in registers
(DH, DL) - row, column of character light pen position
(CH) - raster line (0-199)
(BX) - pixel column (0-319, 639)

Note

This function returns raster and pixel of the upper left corner of a character. It also returns the column coordinate of the next left pixel in high resolution graphics mode, if the light pen is pointed to an odd- column character cell.

6. Select active display page

(AH) = 5 (AL) = new page value 0-7 for modes 0 & 1
0-3 for modes 2 & 3

7. Scroll active page up

(AH) = 6 (AL) = number of lines, input lines blanked at bottom of window; 0 means blank entire window

(CH,CL) = row, column of upper left corner of scroll

(DH,DL) = row, column of lower right corner of scroll

(BH) = attribute to be used on blank line

Note

In medium and high resolution graphics mode, the attribute value represents a dot/color background pattern to be used literally in filling up the blank lines.

8. Scroll active page down

(AH) = 7 (AL) = number of lines, input lines blanked at top of window; 0 means blank entire window

(CH,CL) = row, column of upper left corner of scroll

(DH,DL) = row, column of lower right corner of scroll

(BH) = attribute to be used on blank line

See note for Scroll Active Page UP, above.

Character handling functions:

9. Read attribute character at cursor position

(AH) = 8 (BH) = display page (alpha modes only)

On return:

(AL) = character read
(AH) = attribute of character read (alpha modes only)

10. Write attribute character at cursor position.

(AH) = 9 (BH) = display page (alpha modes only)
(CX) = count of characters to write
(AL) = character to write
(BL) = attribute of character (alpha mode)
color of character (medium resolution mode)
(attribute ignored in high resolution graphics mode

11. Write character at cursor position

(AH) = 10 (BH) = display page (alpha modes only)
(CX) = count of characters to write
(AL) = character to write

Graphics functions:

12. Set color

(AH) = 11 (BH) = color ID being set (0 or 1)
(BL) = background color 0 - 15 (ID = 0)
pallette 0 or 1 (ID = 1)

Meaningful only in color modes

13. Write dot

(AH) = 12 (DX) = row number (0-199)
(CX) = column number (0-319 or 0-639)
(AL) = color value

14. Read dot

(AH) = 13 (DX) = row number
(CX) = column number
(AL) = returns the dot read

ASCII teletype function:

15. Write teletype:

(AH) = 14 (AL) = character to write
(BL) = foreground color (for graphics mode)
(BH) = display page to write on (ALPHA modes only)

Status function:

16. current video status

(AH) = 15

On exit:

(AL) = mode currently set
(AH) = number of character columns on screen
(BH) = current active display page

Extended functions for BASIC support (all of the following functions implicitly use the current mode setting as an input parameter)

17. Generalized Move Video Character Display

(AH) = -1 (DH,DL) = source row, source column
(CH, CL) = destination row, column for move
(BH,BL) = row, column size of area to move (0 means no move)

high byte
(DI) attribute to use in filled lines

On exit: All registers preserved and screen updated

18. Generalized Fill Video Character Display

(AH) = -2 Function Code
(DH) = Attribute to use in the fill
(DL) = Data to use in the fill
(CH) = Destination row
(CL) = Destination column
(BH) = Number of row to fill
(BL) = Number of column to fill

On Exit: All registers preserved and screen updated

19. Convert (page, row, column) into (segment, offset)

(AH)=-3 (DH,DL) = row, column
(BH) = display page

On exit:

(AX) = segment address of display RAM
(BX) = offset of character in display RAM
(CX) = offset of attribute in display RAM (valid for alpha modes only)

20. Convert character offset into (page,row,column)

(AH)=-4 (BX) = offset of character in display RAM (in graphic's mode, use the address of the character's upper left corner)

On exit:

(DH, DL) = row, column
(BH) = display page

INT 11H - EQUIPMENT CHECK

This routine allows the user to verify the hardware configuration as determined at initialization time. The interface is as follows:

EXIT:	REGISTER	BIT	DESCRIPTION
	(AH)	0	Reserved
		1-3	# of serial channels
		4	Game adapter present
		5	Reserved
		6-7	# of printer channels
	(AL)	0	Floppy drive present
		1	8087 coprocessor present
		2-3	Motherboard RAM size
		4-5	CRT state
		6-7	# of floppy drives

INT 12H - MEMORY CHECK

This routine allows the user to verify the amount of RAM in the system. The interface is as follows:

ENTRY: NONE
EXIT: (AX) = the amount of total RAM in the system, in units of 1K bytes.

INT 13H - FLOPPY DISK DRIVER

Inputs:

AH = command code
0 = reset floppy disk controller
1 = get last status
2 = read sectors
3 = write sectors
4 = verify sectors
5 = format a track
AL = number of sectors to transfer, if applicable
CH = cylinder number
CL = sector number
DH = head number
DL = drive number
ES:BX = floppy disk IO transfer address

Outputs:

CARRY = 1, if any error
AH = error code
AL = number of sectors actually transfered; all other registers preserved
FDISK_STATUS = error code, see equates

INT 14H - ASYNCHRONOUS COMMUNICATIONS DRIVER

COMMAND FUNCTION

(AH)=0 Initialize asynchronous communication port

On entry:

(AL) = communications parameters

Bit 0-1 word length
- 00 = 5 bits
- 01 = 6 bits
- 10 = 7 bits
- 11 = 8 bits

2 # of stop bits
- 0 = 1 bit
- 1 = 1.5 bits when 5-bit word
- = 2 bits when 6, 7, or 8- bit word

3-4 parity
- 00 = none
- 01 = odd
- 10 = none
- 11 = even

5-7 baud rate
- 000 = 110 baud
- 001 = 150 baud
- 010 = 300 baud
- 011 = 600 baud
- 100 = 1200 baud
- 101 = 2400 baud
- 110 = 4800 baud
- 111 = 9600 baud

On exit:

(AH) = Line Status

(AL) = MODEM Status

(See command (AH) = 3 for description)

(AH)=1 Send A Character to Communication Port

On entry:

(AL) = Character
(DX) = RS-232-C port number (0 - 3)

On exit:

(AL) = Character
(AH) = Bit Description

0	Data Ready	(DR of LSR)
1	Overrun Error	(OE of LSR)
2	Parity Error	(PE of LSR)
3	Framing Error	(FE of LSR)
4	Break Interrupt	(BI of LSR)
5	Transmitter Holding Register Empty	(THRE of LSR)
6	Transmitter Empty	(TEMT of LSR)
7	Time Out Error When time out error occurs, bits 0- 6 are undefined	

(AH)=2 Receive A Character From Communication Port

On entry:

(DX) = RS-232-C port number (0 - 3)

On exit:

(AL) = Character
(AH) = Bit Description

Bit	Description	
0	0	
1	Overrun Error	(OE of LSR)
2	Parity Error	(PE of LSR)
3	Framing Error	(FE of LSR)
4	Break Interrupt	(BI of LSR)
5	0	
6	0	
7	Time Out Error. When time out error occurs, bits 0-6 are undefined.	

(AH)=3 Read Communication Port Status

On entry:

(DX) = RS-232-C port number (0-3)

On exit:

(AH) = Line status

Bit	Description	
0	Data Ready	(DR)
1	Overrun Error	(OE)
2	Parity Error	(PE)
3	Framing Error	(FE)
4	Break Interrupt	(BI)
5	Transmitter Holding Register Empty	(THRE)
6	Transmitter Empty	(TEMPT)
7	0	

Note

Bits 1, 2, 3, 4, and 7 are error flags and should be zero in normal condition.

(AL) = MODEM Status

Bit	Description	
0	Delta Clear To Send	(DCTS)
1	Delta Data Set Ready	(DDSR)
2	Trailing Edge Ring Indicator	(TERI)
3	Delta Data Carrier Detect	(DDCD)
4	Clear To Send	(CTS)
5	Data Set Ready	(DSR)
6	Ring Indicator	(RI)
7	Data Carrier Detect	(DCD)

Note

Bits 0-7 correspond to bits 0-7 of the 8250A MODEM Status Register (MSR)

INT 15H - DUMMY CASSETTE ROUTINE

If called, this routine returns the invalid command error message.

INT 16H - KEYBOARD DRIVER

This software routine interacts with the keyboard driver. The calling sequences are as follows:

(AH) = 0 Read character from buffer

On exit:

(AH) = keyboard hardware scan code
(AL) = character or 0FFH if in kbd_raw_mode
The keyboard buffer pointer is incremented and the circular buffer pointer is maintained

(AH) = 1 Buffer empty ?

On exit:

(ZFL) = 1, keyboard buffer empty
(ZFL) = 0, keyboard buffer not empty
(AH) = keyboard hardware scan code
(AL) = character
The keyboard buffer pointer is not incremented and the circular buffer pointer is not updated.

(AH) = 2 Read keyboard status

On exit:

(AL) = keyboard status

INT 17H - PRINTER INTERRUPT

This routine interacts with the printer I/O driver.

INPUT:

AH = 0 Output character to printer
1 Clear/Reset/Initialize Printer
2 Input Printer Status

AL = Character to print (case AH = 0 only)

DX = Printer number (0, 1, or 2)

OUTPUT:

AH = Printer Status

BIT 0	1 = timeout
1	not used
2	not used
3	1 = error
4	1 = printer selected
5	1 = paper error
6	1 = acknowledge
7	0 = printer busy

INT 19H - BOOTSTRAP

This routine loads and, if the load is successful, executes DOS.

ON ENTRY: None

ON EXIT: If successful, track 0 sector 1 is read into the boot location of 0:7C00 and control is transferred there.
Otherwise, the carry flag is set to indicate an error.

INT 1AH - TIME OF DAY

This routine is used to read or set the timer counter. The interface is as follows:

AH = 0		Read real time clock
	ON ENTRY:	AH = 0
	ON EXIT:	DX=RTC_LOW CX=RTC_HIGH AL=RTC_OVERFLOW
AH = 1		Set real time clock
	ON ENTRY:	AH = 1 DX = RTC_LOW CX = RTC_HIGH
	ON EXIT:	RTC_OVERFLOW CLEARED

12 — Physical and Environmental Specifications

System Unit

Width 14.00" (356mm)
Depth 15.57" (395mm)
Height 5.59" (142mm)
Weight: 21.50 lbs (9.57KG)

System Motherboard

Microprocessor: 8088 - 5 MHz
Dynamic Random Access Memory: 128K (expandable to 256K on motherboard using 64K DRAM; optional combo card adds up to 384K additional DRAM)
Read Only Memory: 32K (expandable up to 64K)
Communications port: RS-232-C serial interface, asynchronous protocol, up to 9600 baud; DB-25P male connector
Printer port: Centronics-compatible parallel interface; DB-25P female connector
Floppy Disk Controller: supports up to four 5 1/4" drives; single or double density; FM or MFM formats in sector size of 128, 256, 512, or 1024 bytes
Five expansion slots: support display adapter card and a variety of hardware option cards

Speaker Keyboard

Width 18.00" (457mm)
Depth 8.05" (204mm)
Height 1.44" (37mm)
Weight 4.5 lbs. (2.04KG)

84 key, low profile, detachable keyboard
6 coiled cord
Tactile feedback,
10 special function keys,
10 key numeric keypad
5 editing keys
5 cursor control keys
Indicator lights for numerical lock and caps lock keys
Serial interface feedback.

Disk Drives

Internal 5 1/4" floppy disk drive, 352K, 6ms access
Second floppy disk drive (optional)
10MB integrated hard disk (optional)

Monochrome Monitor

Height 15.25" (387 mm)
Depth 12.50" (318 mm)
Width 14.00" (356 mm)
Weight 27 lbs. (12.25 Kg)

14" diagonal CRT
High resolution display (H134 amber or H39 green phosphor)
Operator controlled contrast adjustment
Tilt -5° or +25°; swivel plus or minus 67°
Anti-glare screen
25-line by 80-character format, 256 different characters
Video attributes - blink, blank, underline, normal/reverse video, and half intensity)
Characters formed in a 7 x 9 matrix in a 9 x 14 cell
dc power provided by system unit via shielded dc power cable
Shielded video signal cable.

Color Monitor

Height 11" (279 mm)
Width 14.75" (375 mm)
Depth 15.50" (394 mm)
Weight 26.46 lbs. (12 Kg)

12" diagonal CRT
RGB input
.31 mm DOT pitch
Black matrix, non-glare surface
640 x 200 high resolution graphics
320 x 200 medium resolution
25 lines by 80 columns
8 x 8 characters
Red, green, blue, cyan, yellow, magenta, black, white colors (at two intensity levels)

Mouse

Connected through keyboard port
Detects movement over normal table top
Keyboard still usable

Expansion Boards

Monochrome Monitor Controller Card: 4K video buffer

Color/Graphics Monitor Controller Card (optional): 16K video buffer; features 16 colors in text mode; in graphics mode features 4 colors at medium resolution (320 h x 200 v) or 2 colors at high resolution (640 h x 200 v)

Combo Board (optional): Real-time clock, second parallel port, and up to 384K additional memory

Switching Power Supply

Input Voltage: switch-selectable for 95 to 132 Vac or 180 to 264 Vac;
Input Line Frequency: 47 - 63 Hz
115 Watt

Operating System

ITT DOS 2.11 by Microsoft
CP/M-86 1.1 by Digital Research (opt.)

Languages

Advanced BASIC, MACRO Assembler

Diagnostics

Power-on self-testing and parity checking; comprehensive ROM- based diagnostic monitor; interactive diskette-based diagnostics

Environment

Temperature

Operating 10 - 35° C (50 - 95° F)
Storage 5 - 45° C (41 - 113° F)

Humidity

Operating 20% to 80% (noncondensing)
Storage 5% to 95% (noncondensing)

Altitude

Operating 8000' (1 hour after stabilization)
Storage 12,000'

Electrostatic Discharge

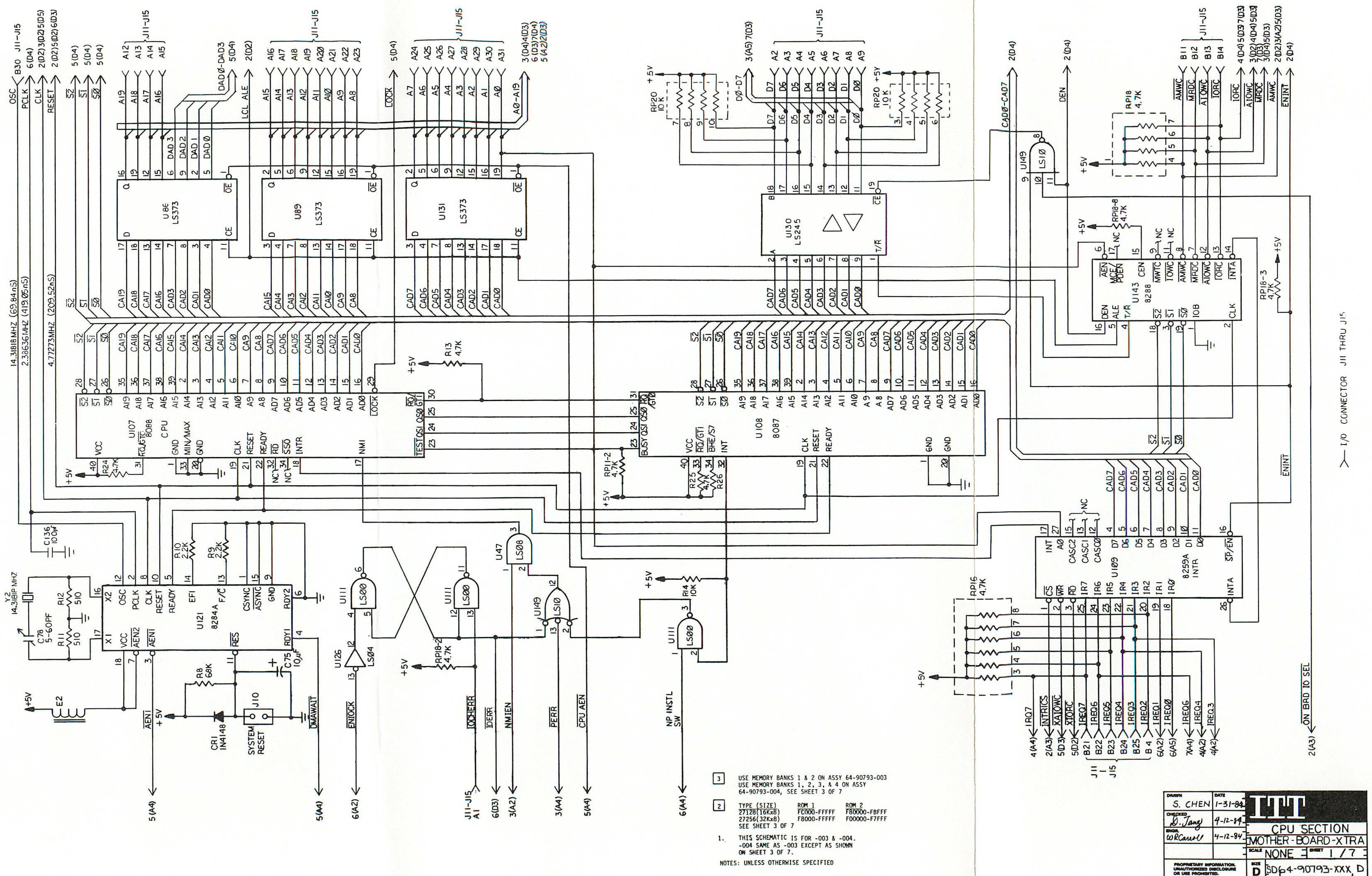
Up to 15 KV at any point except keyboard
No discharge below 15 KV on keyboard

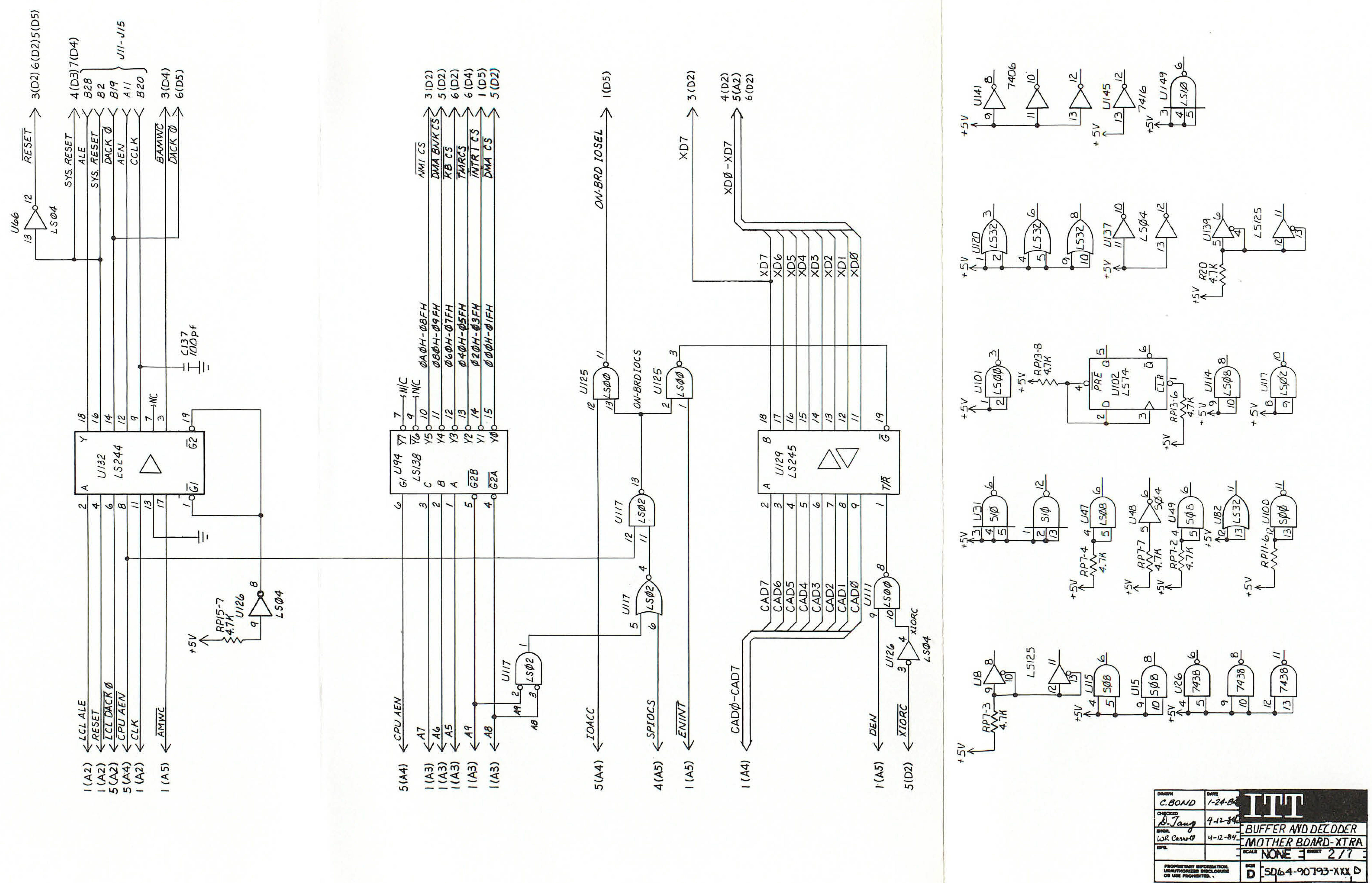
Power Supply Line Transients

Dropouts 1/2 cycle with no effect
Transients 6 KV peak, .5 Msec
Brownout 75 VAC for 6 hours without damage

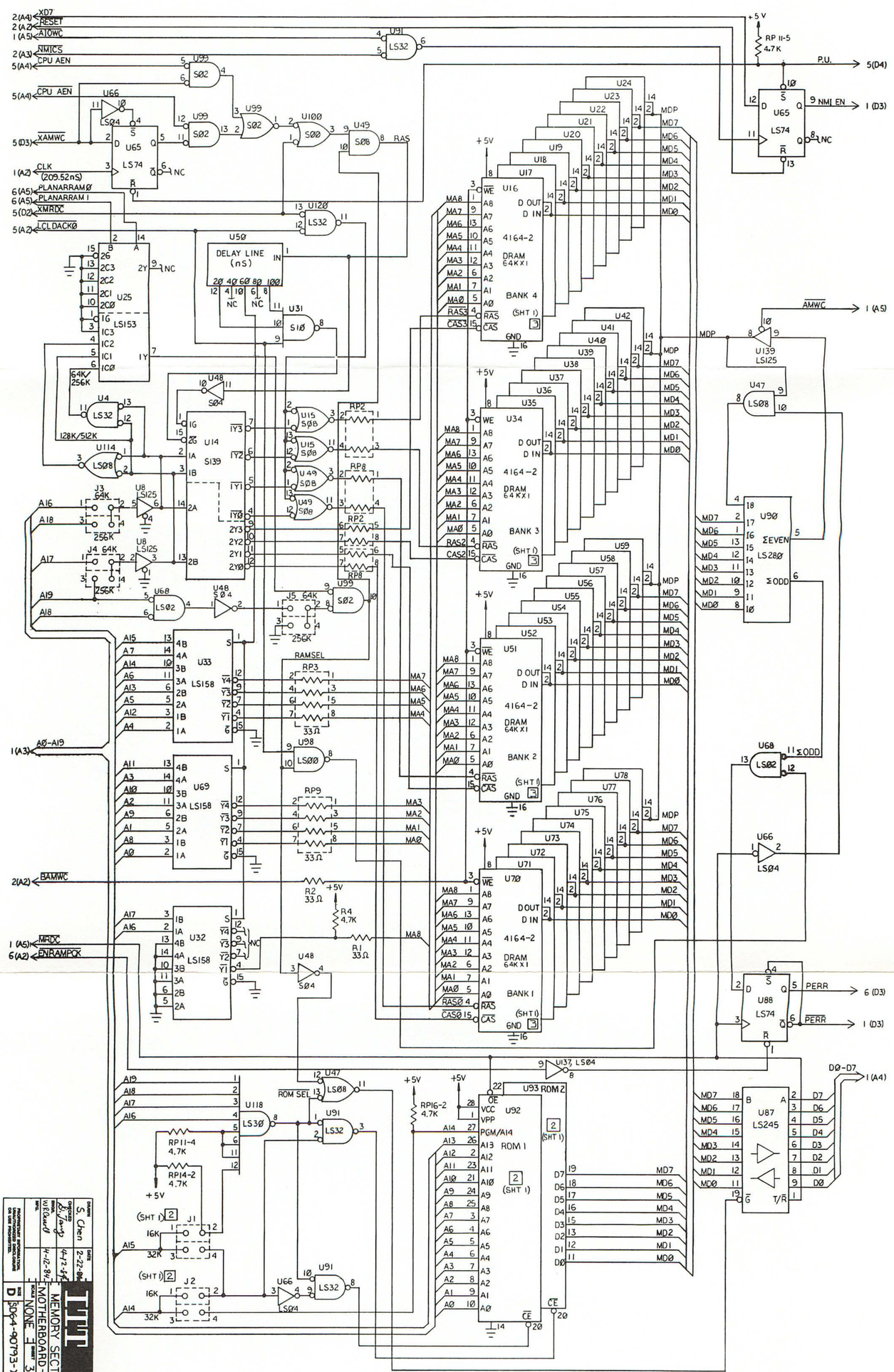
13 — Schematics

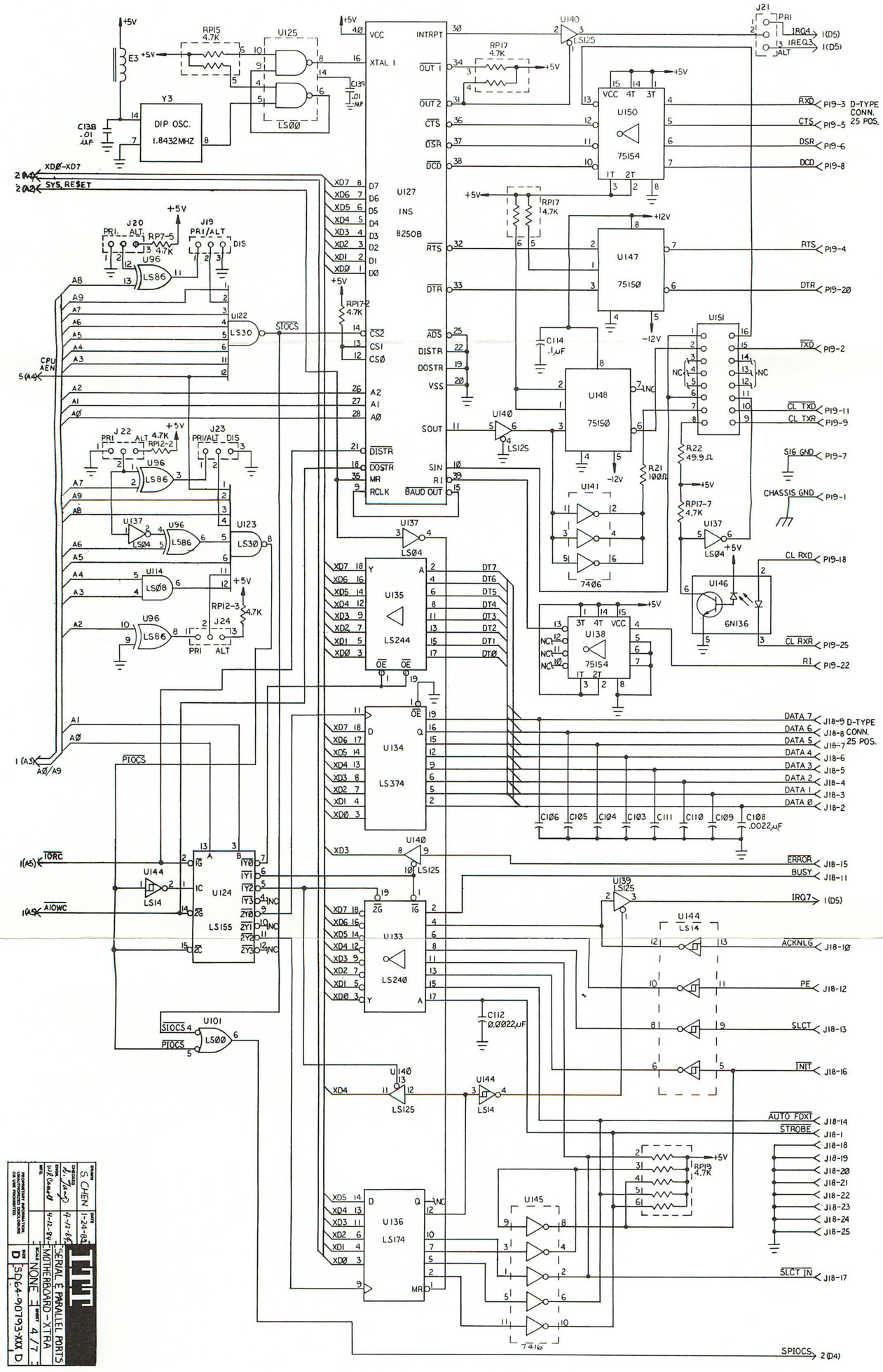
MOTHERBOARD
COMBO BOARD
COLOR/GRAPHICS BOARD
MEMORY ADD-ON BOARD
MONOCHROME BOARD
POWER SUPPLY

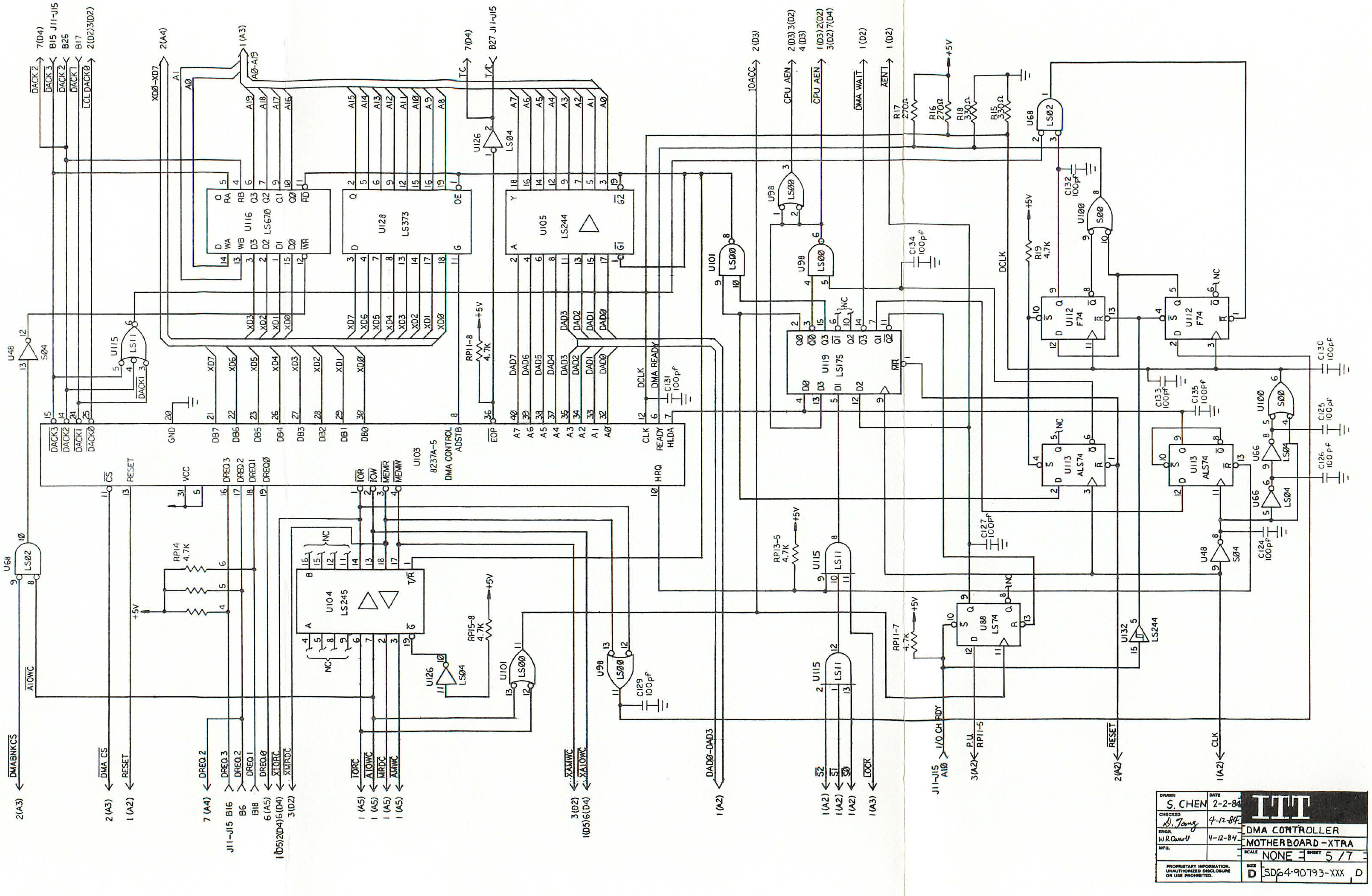

3 USE MEMORY BANKS 1 & 2 ON ASSY 64-90793-003
USE MEMORY BANKS 1, 2, 3, & 4 ON ASSY 64-90793-004, SEE SHEET 3 OF 7
2 TYPE (SIZE) ROM 1 ROM 2
27128(16Kx8) FC000-FFFFF F80000-FBFFF
27256(32Kx8) F8000-FFFFF F00000-F7FFF
SEE SHEET 3 OF 7
1. THIS SCHEMATIC IS FOR -003 & -004. -004 SAME AS -003 EXCEPT AS SHOWN ON SHEET 3 OF 7.
NOTES: UNLESS OTHERWISE SPECIFIED
DRAWN S. CHEN DATE 1-31-84
CHECKED D. Tang 4-12-84
ENGR. WRCarroll 4-12-84
ITT
CPU SECTION
MOTHER-BOARD-XTRA
SCALE NONE SHEET 1 / 7
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
SIZE D SD64-90793-XXX D

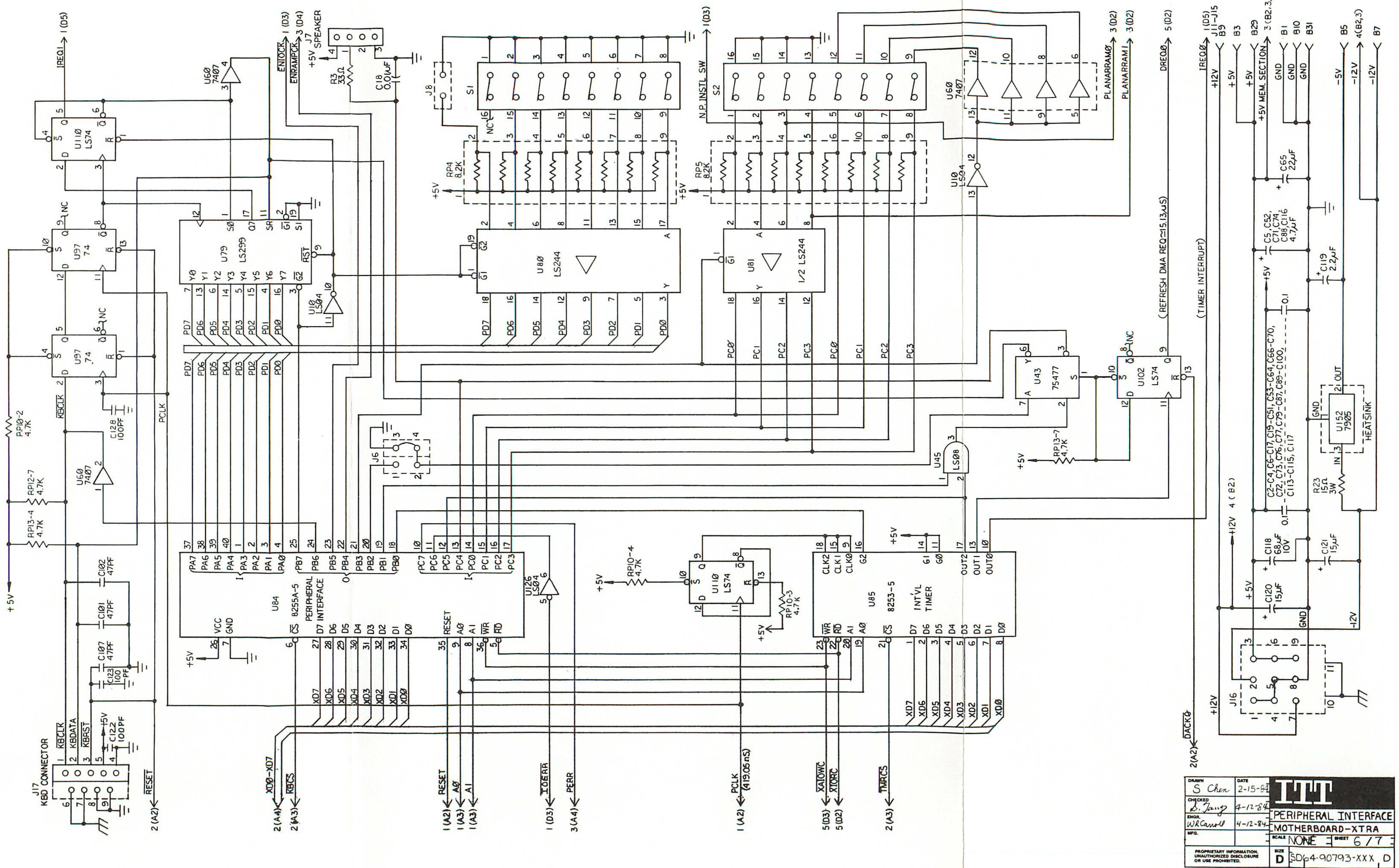


C.BOND
ITT
BUFFER AND DECODER
MOTHER BOARD-XTRA
NONE
2/7
D
SD64-90793-XXX

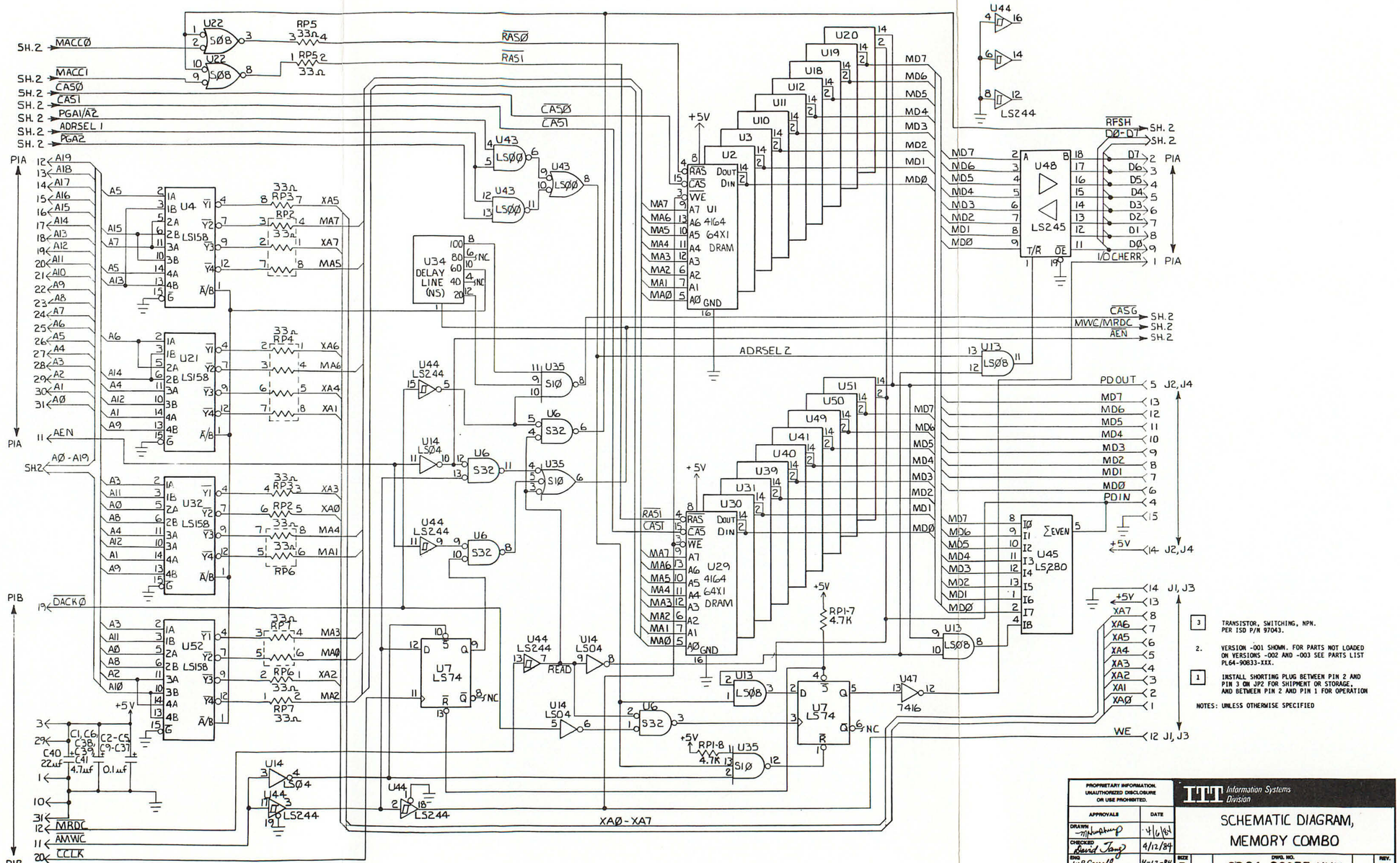

MEMORY SECTION
MOTHERBOARD-XTRA
S. Chen
2-22-84
4-12-84
NONE
3/7
D
S964-90793-XXX D
DELAY LINE (nS)
4164-2 DRAM 64KX1
BANK 4
BANK 3
BANK 2
BANK 1
ROM 1
ROM 2
RAMSEL
ROM SEL
PERR
MDP
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
DØ-D7
P.U.
NMI EN
AMWC
BAMWC
MRDC
ENRAMPOX
PLANARRAMØ
PLANARRAM 1
XMRDC
LCLDACKØ
CPU AEN
XAMWC
RESET
AIOWC
NMICS
RAS
CLK (209.52nS)
128K/512K
64K/256K
AØ-A19
ΣEVEN
ΣODD


+5V
RP15 4.7K
U125
LS00
E3
Y3
DIP OSC.
1.8432MHZ
C138 .01 µF
C139 .01 µF
U127
INS 8250B
INTRPT
XTAL 1
OUT 1
OUT 2
CTS
DSR
DCD
RTS
DTR
ADS
DISTR
DOSTR
VSS
SOUT
SIN
RI
BAUD OUT
MR
RCLK
D7
D6
D5
D4
D3
D2
D1
D0
CS2
CS1
CS0
A2
A1
A0
RP17 4.7K
U140
LS125
U150
75154
U147
75150
U148
U151
C114 .1µF
R22 49.9Ω
R21 100Ω
U141
7406
U146
6N136
U138
U137
LS04
U135
LS244
U134
LS374
U133
LS240
U136
LS174
U124
LS155
U144
LS14
U145
7416
U123
LS30
U122
U96
LS86
U114
LS08
U101
RP17-2 4.7K
RP12-2 4.7K
RP12-3 4.7K
RP17-7 4.7K
RP19 4.7K
J19 PRI/ALT DIS
J20 PRI ALT
J21 PRI ALT
J22 PRI ALT
J23 PRI/ALT DIS
J24 PRI ALT
XD0–XD7
SYS RESET
CPU AEN
STOCS
PIOCS
TORC
AIOWC
IRQ4
IRQ3
RXD
TXD
RTS
DTR
DCD
DSR
CTS
CL TXD
CL TXR
CL RXD
CL RXR
RI
SIG GND
CHASSIS GND
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA 0
C106 C105 C104 C103 C111 C110 C109 C108 .0022µF
ERROR
BUSY
IRQ7
ACKNLG
PE
SLCT
INIT
AUTO FDXT
STROBE
SLCT IN
SPIOCS
P19-3 D-TYPE CONN. 25 POS.
P19-5
P19-6
P19-8
P19-4
P19-20
P19-2
P19-11
P19-9
P19-7
P19-1
P19-18
P19-25
P19-22
J18-9 D-TYPE CONN. 25 POS.
J18-8
J18-7
J18-6
J18-5
J18-4
J18-3
J18-2
J18-15
J18-11
J18-10
J18-12
J18-13
J18-16
J18-14
J18-1
J18-18
J18-19
J18-20
J18-21
J18-22
J18-23
J18-24
J18-25
J18-17
S. CHEN
1-24-83
4-12-84
4-12-84
SERIAL & PARALLEL PORTS
MOTHERBOARD-XTRA
NONE
4 / 7
D
SD64-00193-XXX D


S. CHEN 2-2-84
D. Tang 4-12-84
W R Carroll 4-12-84
ITT
DMA CONTROLLER
MOTHERBOARD-XTRA
SCALE NONE SHEET 5/7
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
D SD64-90793-XXX D


ITT
PERIPHERAL INTERFACE
MOTHERBOARD-XTRA
SCALE NONE
SHEET 6/7
SIZE D
SD64-90793-XXX D
DRAWN S Chen 2-15-84
CHECKED 4-12-84
ENGR. 4-12-84
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
U84 8255A-5 PERIPHERAL INTERFACE
U85 8253-5 INT'VL TIMER
U79 LS299
U80 LS244
U81 1/2 LS244
U43 75477
U102 LS74
U110 LS74
U97 74
U60 7407
U45 LS08
U126 LS04
U152 7905
J17 KBD CONNECTOR
J7 SPEAKER
S1
S2
N.P. INSTL SW
RP4 8.2K
RP5 8.2K
(REFRESH DMA REQ=15.13μS)
(TIMER INTERRUPT)
PLANARRAMØ
PLANARRAM1
DRQØ
IRQØ
IRQ1
DACKØ
PCLK (419.05nS)
XD0-XD7
RESET
IOERR
PERR
XIOWC
XIORC
TMRCS
KBCS
ENIOCK
ENRAMPCK
+5V MEM SECTION
HEATSINK

DRAWN S. Chen	DATE 1-27-84	ITT
CHECKED S. Jang	4-12-84	FLOPPY DISK CONTROLLER
ENGR. W.R. Caudle	4-12-84	MOTHERBOARD XTRA
MFG.		SCALE NONE SHEET 7/7
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE D SD64-90793-XXX D



3 TRANSISTOR, SWITCHING, NPN. PER ISD P/N 97043.

2. VERSION -001 SHOWN. FOR PARTS NOT LOADED ON VERSIONS -002 AND -003 SEE PARTS LIST PL64-90833-XXX.

1 INSTALL SHORTING PLUG BETWEEN PIN 2 AND PIN 3 ON JP2 FOR SHIPMENT OR STORAGE, AND BETWEEN PIN 2 AND PIN 1 FOR OPERATION

NOTES: UNLESS OTHERWISE SPECIFIED

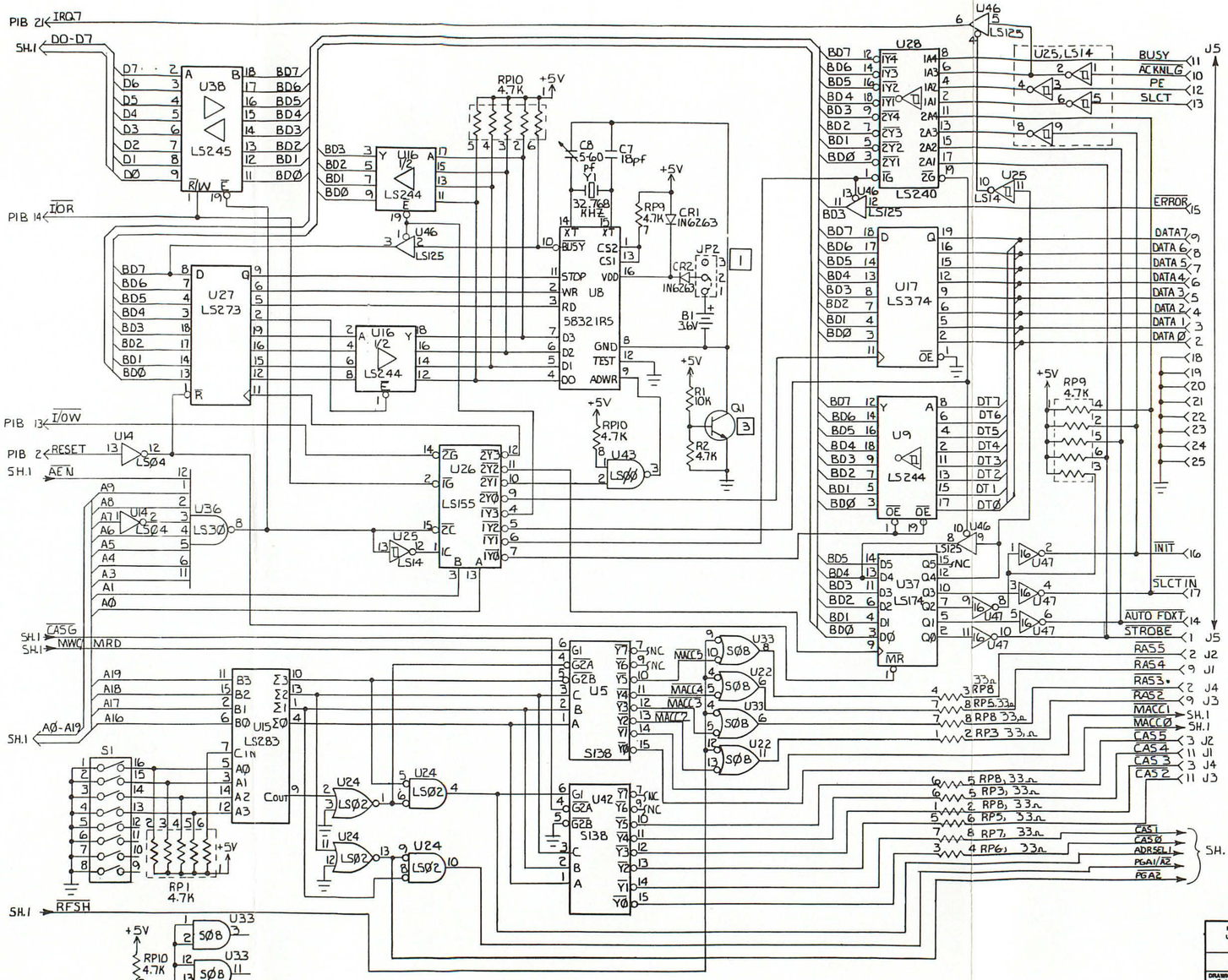
APPROVALS	DATE
DRAWN [illegible]	4/6/84
CHECKED David Jang	4/12/84
ENG W.R. Carroll	4-12-84
MFG	

ITT Information Systems Division

SCHEMATIC DIAGRAM, MEMORY COMBO

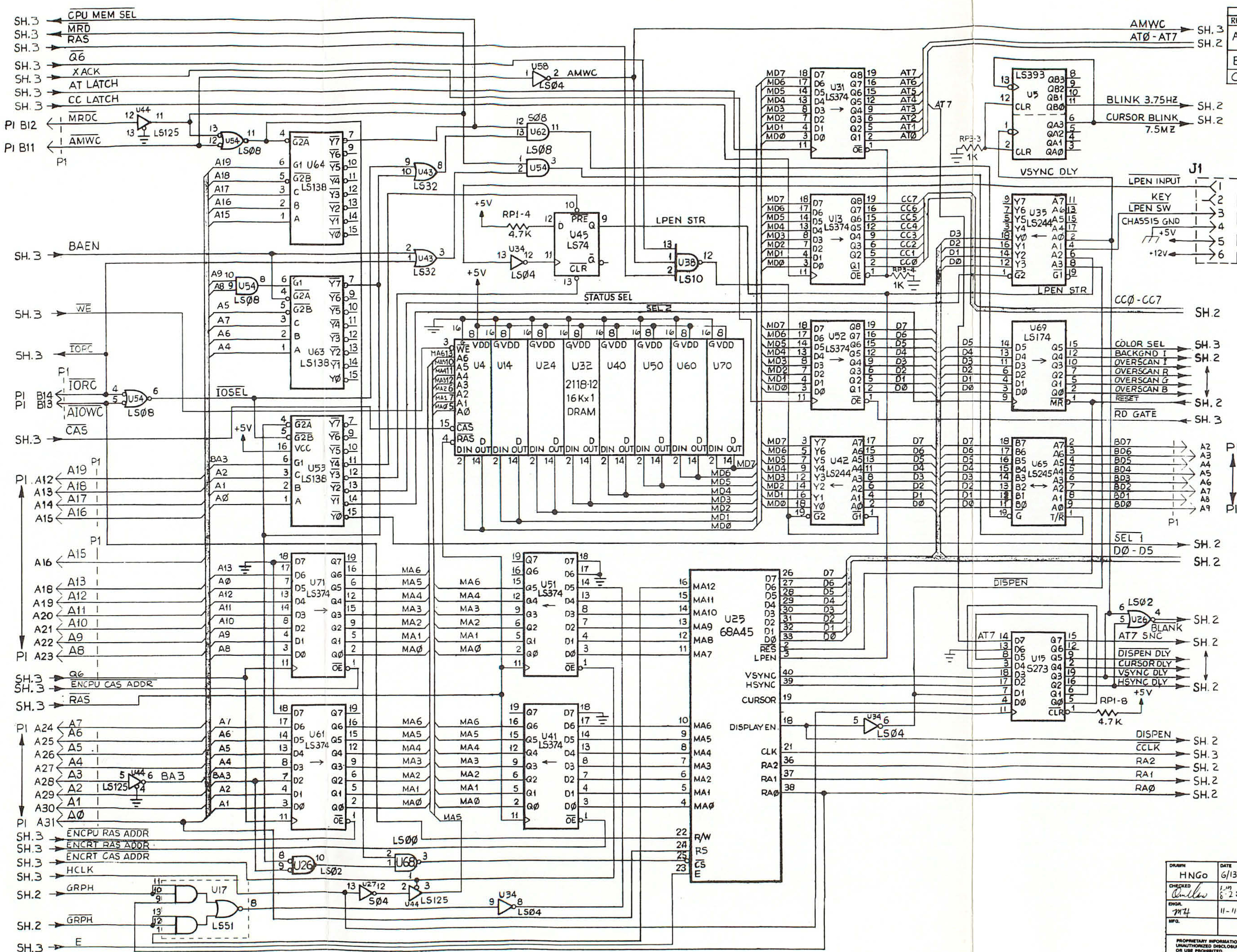
SIZE D | DWG. NO. SD64-90833-XXX | REV. B

SCALE — | DO NOT SCALE DRAWING | SHEET 1 OF 2

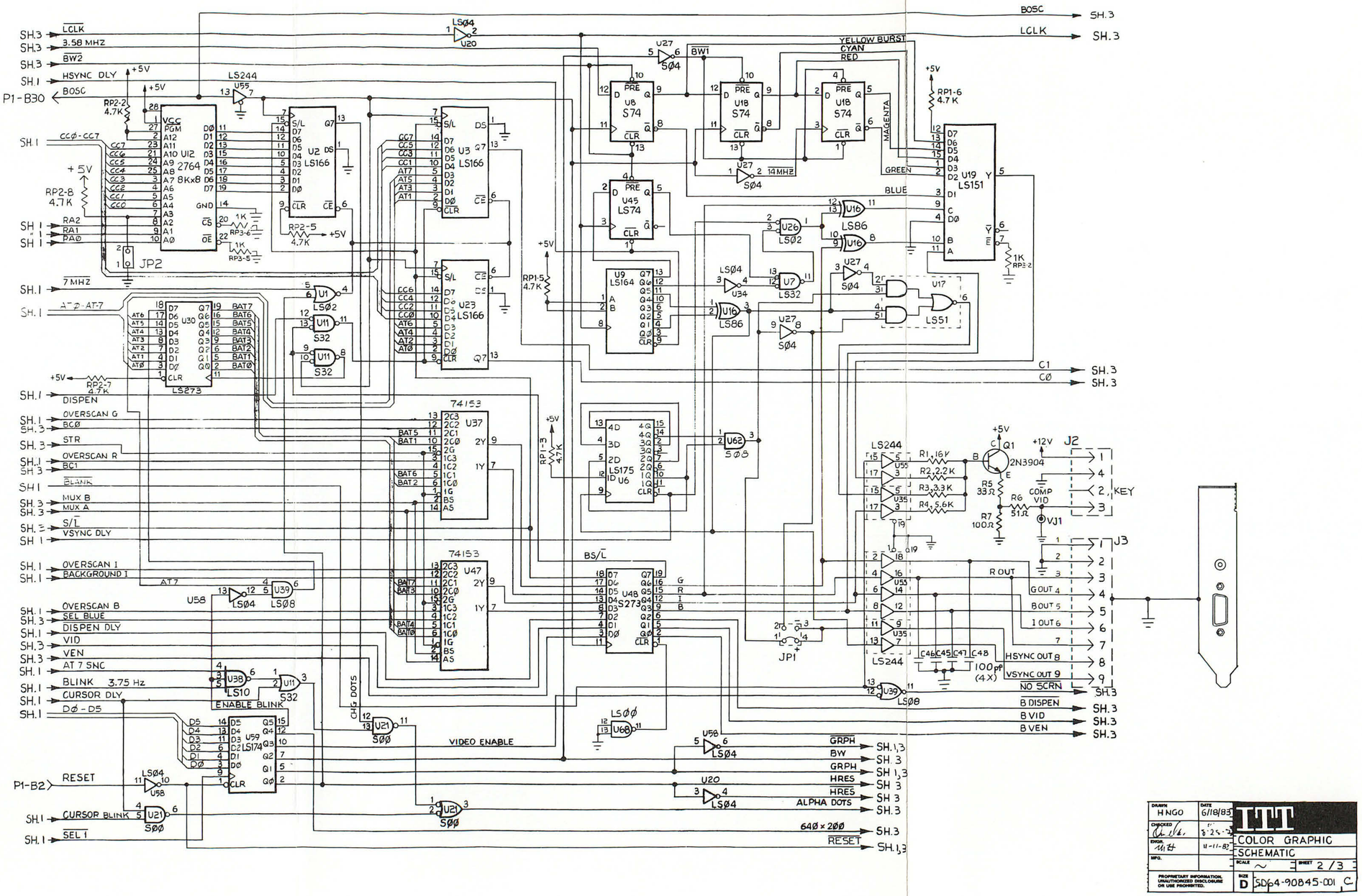


PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		ITH Information Systems Division	
APPROVALS	DATE	SCHEMATIC DIAGRAM, MEMORY COMBO	
DRAWN Monica Hampton	4/16/84		
CHECKED David Jang	4/12/84		
ENG W.R Carroll	4-12-84	SIZE D	DWG. NO. SD64-90833-XXX REV. B
MFG		SCALE ~	DO NOT SCALE DRAWING SHEET 2 OF 2

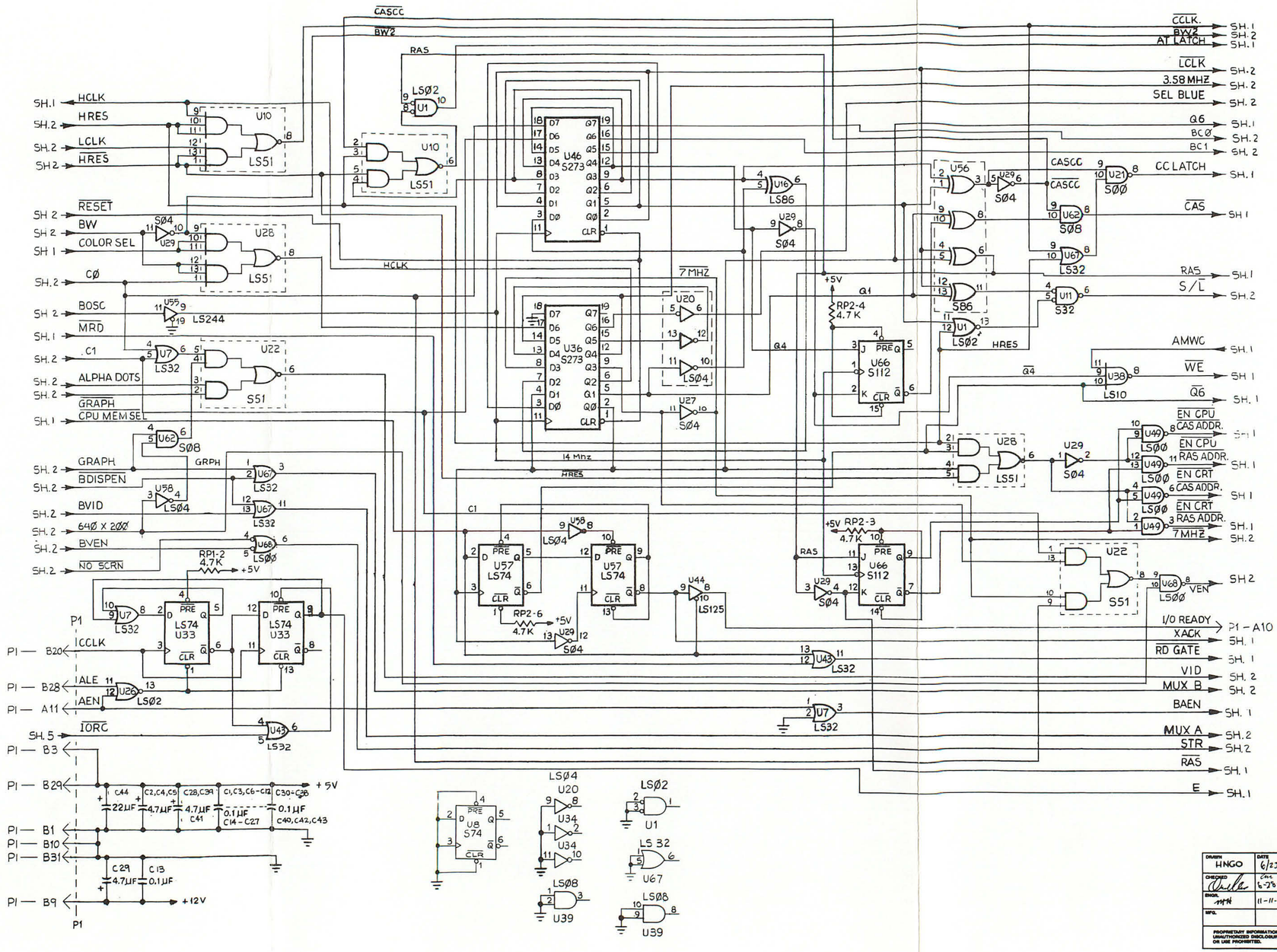
REVISIONS				
REV	ECO#	DESCRIPTION	DATE	APPR.
A	00028	WAS 10A (IEC 00011) NEW RELEASE	4/19/84	
B	00094	NO CHANGE SEE PARTS LIST		
C	00304	REMOVE P2	9/24/84	



DRAWN	DATE	ITT
HNGo	6/13/83	COLOR GRAPHIC SCHEMATIC
CHECKED		SCALE ~ SHEET 1/3
ENGR.	11-11-83	
MFG.		
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE D SD64-90845-001 C

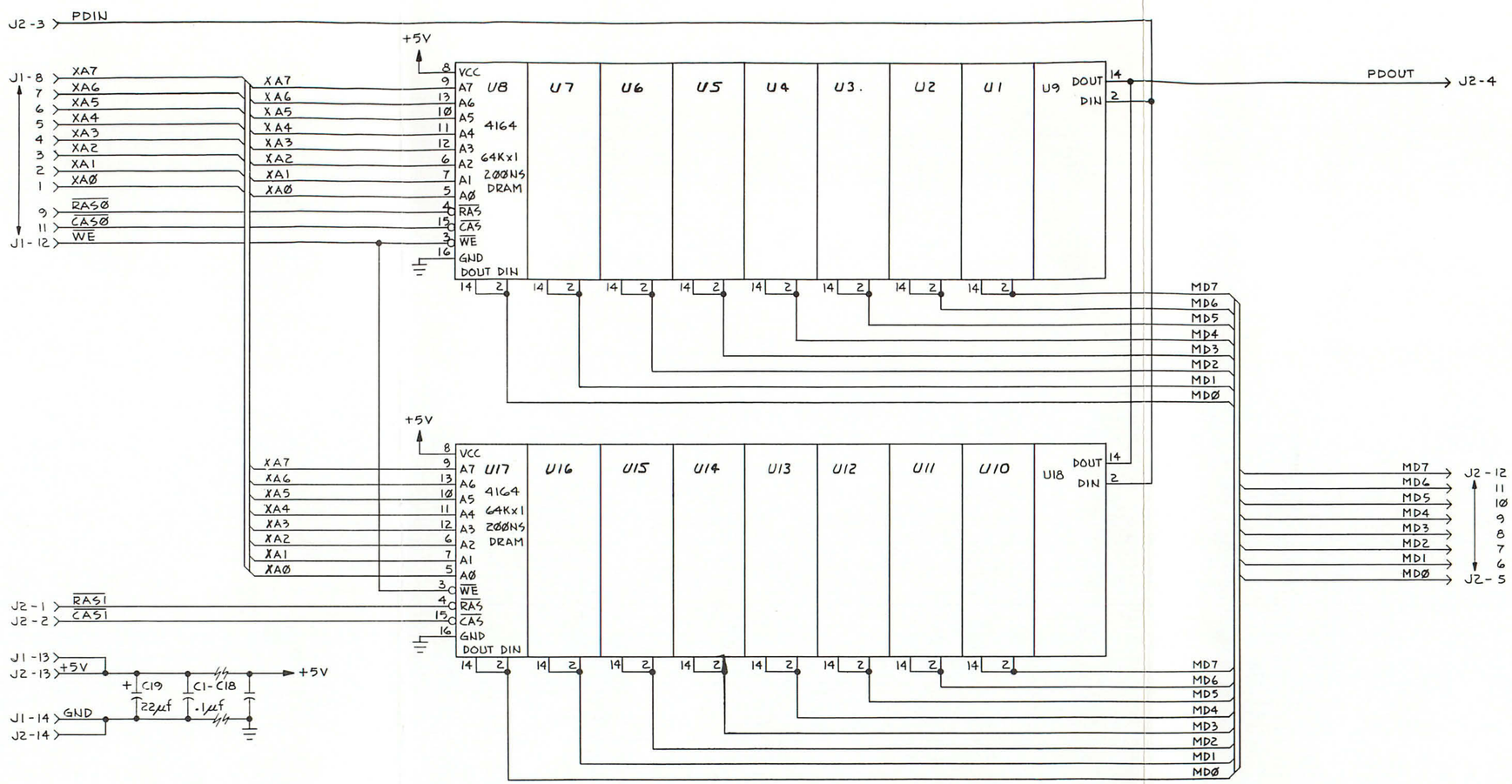


DRAWN HNGO	DATE 6/18/83	ITT
CHECKED	8-25-83	COLOR GRAPHIC
ENGR.	11-11-83	SCHEMATIC
MFG.		SCALE ~ SHEET 2 / 3
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE D SD64-90845-001 C



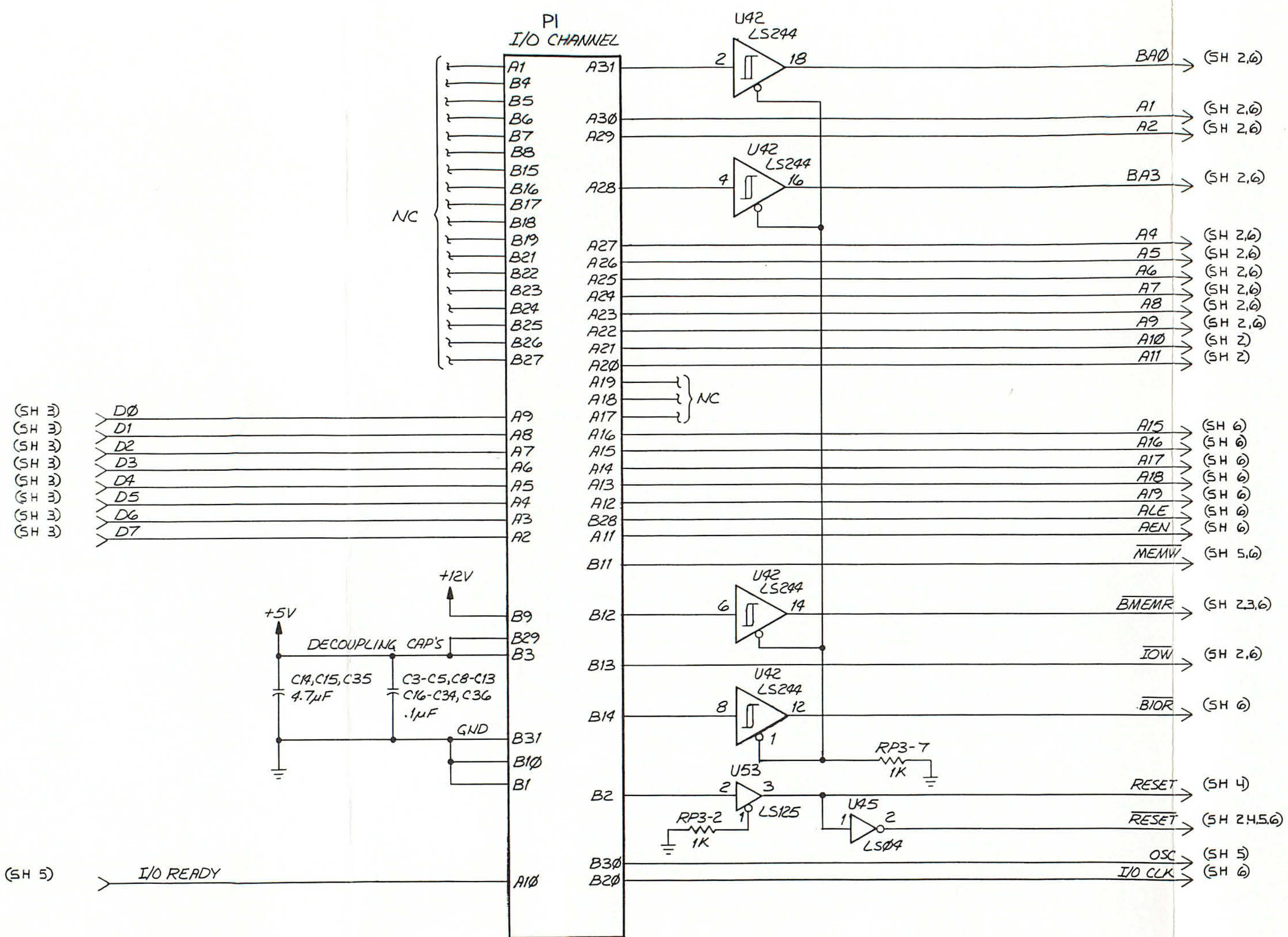
DRAWN HNGO	DATE 6/23/81	ITT
CHECKED	ENG 6-28-82	COLOR GRAPHIC
ENGR. MH	11-11-82	SCHEMATIC
MFG.		SCALE ~ SHEET 3/3
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE D SD64-90845-001 C

13-23/13-24



DRAWN FALKAR	DATE 9-7-83	ITT
CHECKED KM	9-14-83	SCHEMATIC COMBO
ENGR W.R. Carroll	4-26-84	BABY BOARD
APPD.		SCALE — SHEET 1/1
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE D 5D6A-90811-001 A

ZONE	REV	E.C.O.#	REVISIONS	DATE	APPROVED
	A	00020	WAS 7A (IEC 0000B)	4/6/84	D. Tang
	B	00089	NO CHG. ON THIS DOC.	6/26/84	D. Bo
	C	00094	SHT. 5, U33, CHG. FROM 16.88148MHZ TO 16.257 MHZ		

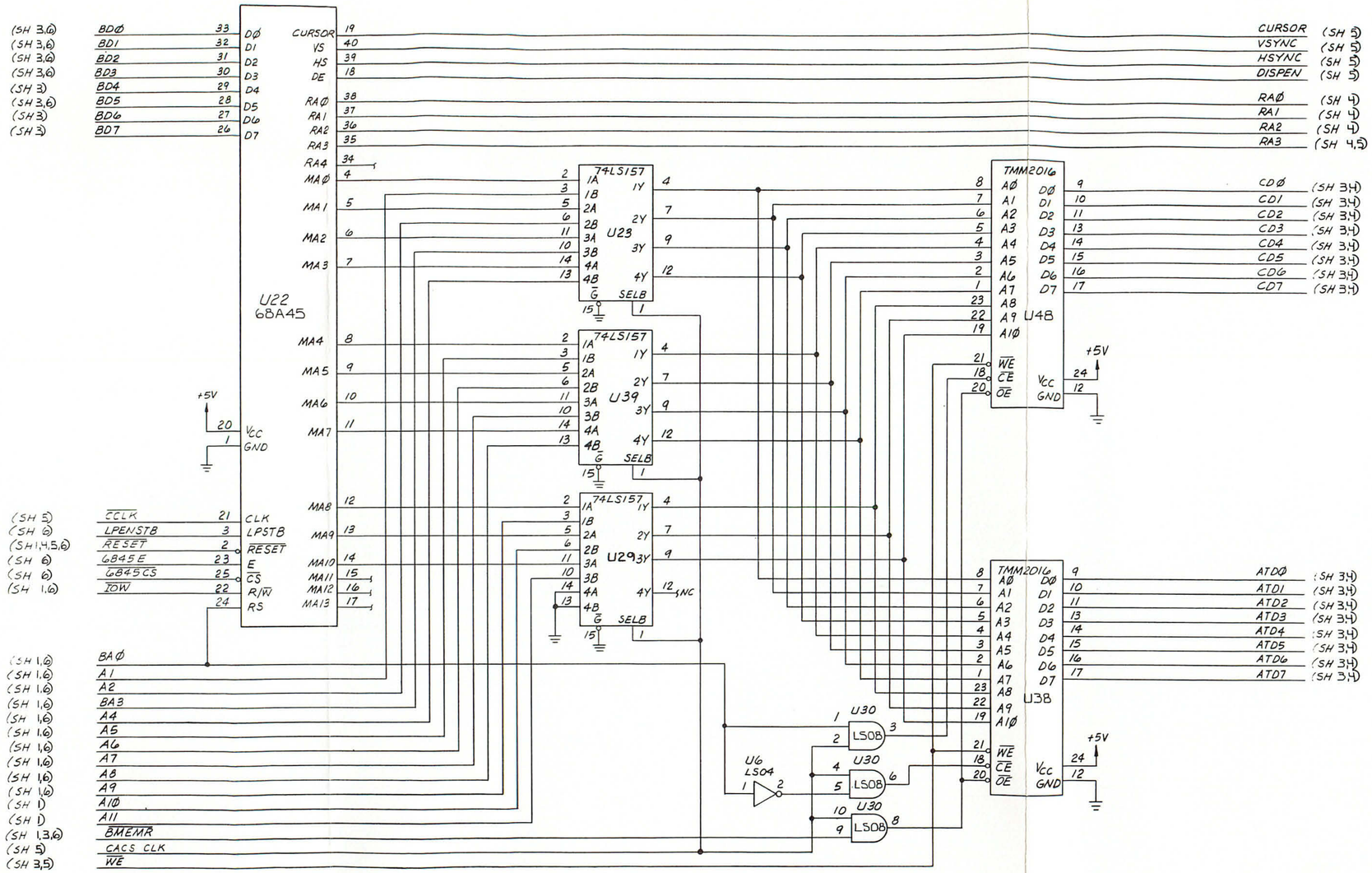


5. ALL I.C.'S ARE SN74XX FAMILY.
4. ALL CAPACITANCE IS IN MICROFARADS.
3. ALL RESISTORS ARE 1/4 WATT 5%
2. ALL RESISTANCE ARE IN OHMS.
1. SCHEMATIC SD64-90857-001 REVISION 7A IS GOOD FOR ASSY SD64-90857-001, REVISION 7A.

NOTES: UNLESS OTHERWISE SPECIFIED

DRAWN KAREN TRUJILLO	DATE 2-23-84
CHECKED	4-3-84
ENGR. David Tang	4-4-84
MFG.	

ITT
XTRA 6845
MONOCHROME CARD
SHEET 1/6
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
SIZE D SD64-90857-001 C



DRAWN	KARENTRAUB	DATE 2-23-84
CHECKED		4-3-84
ENGR	David Jang	4-4-84
MFG		

PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

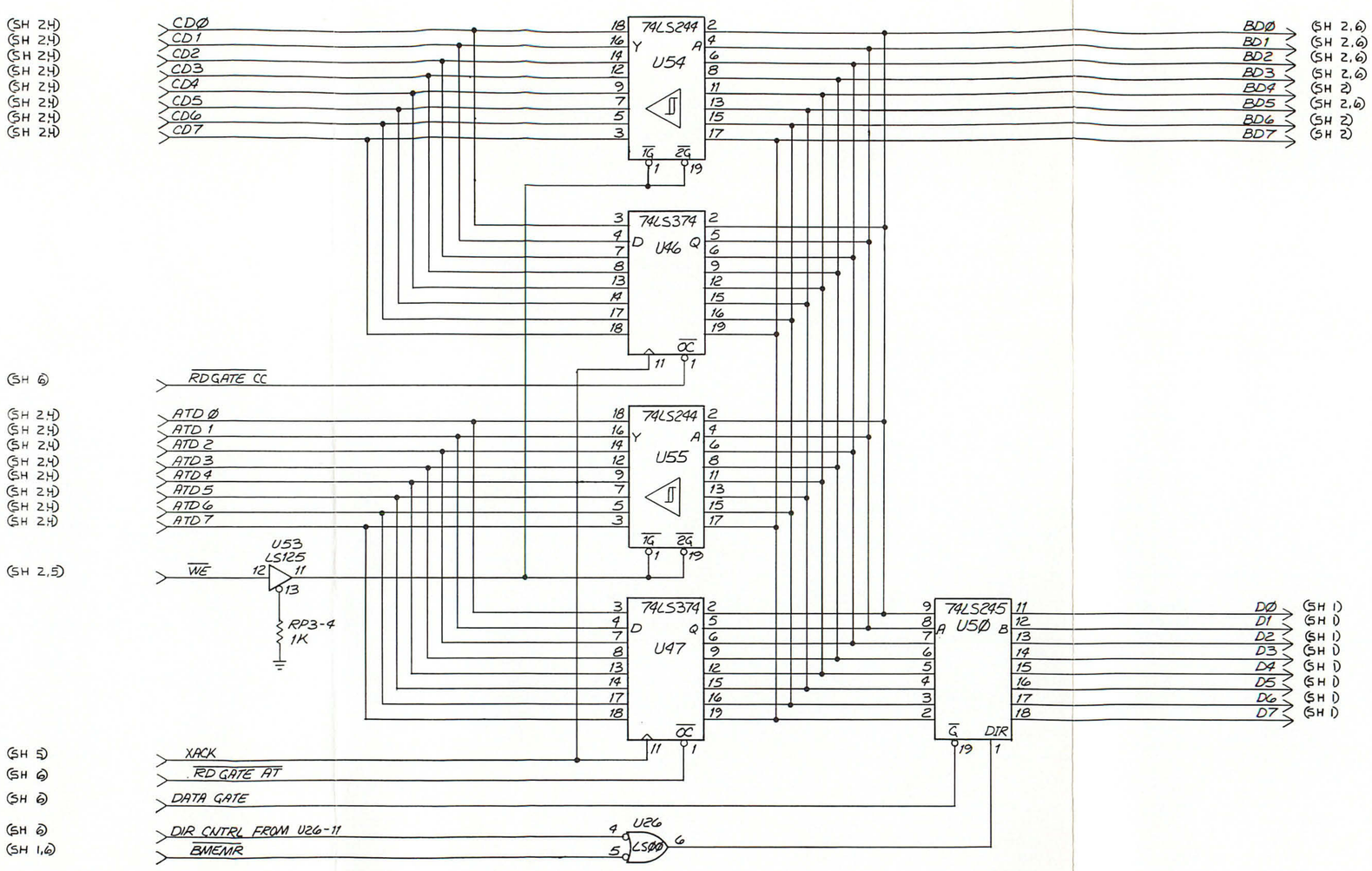
ITT

XTRA 6845

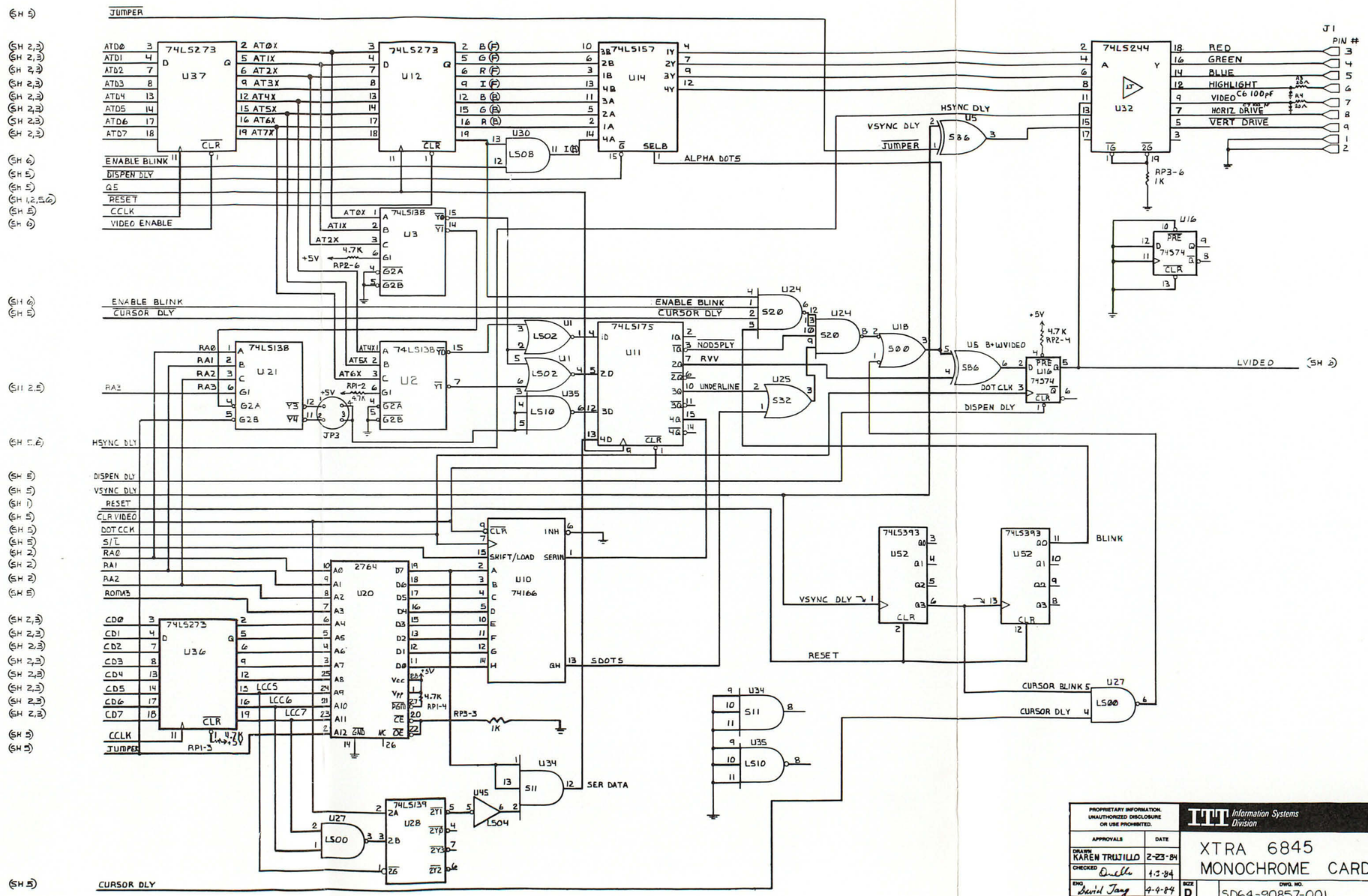
MONOCHROME CARD

SCALE — SHEET 2/6

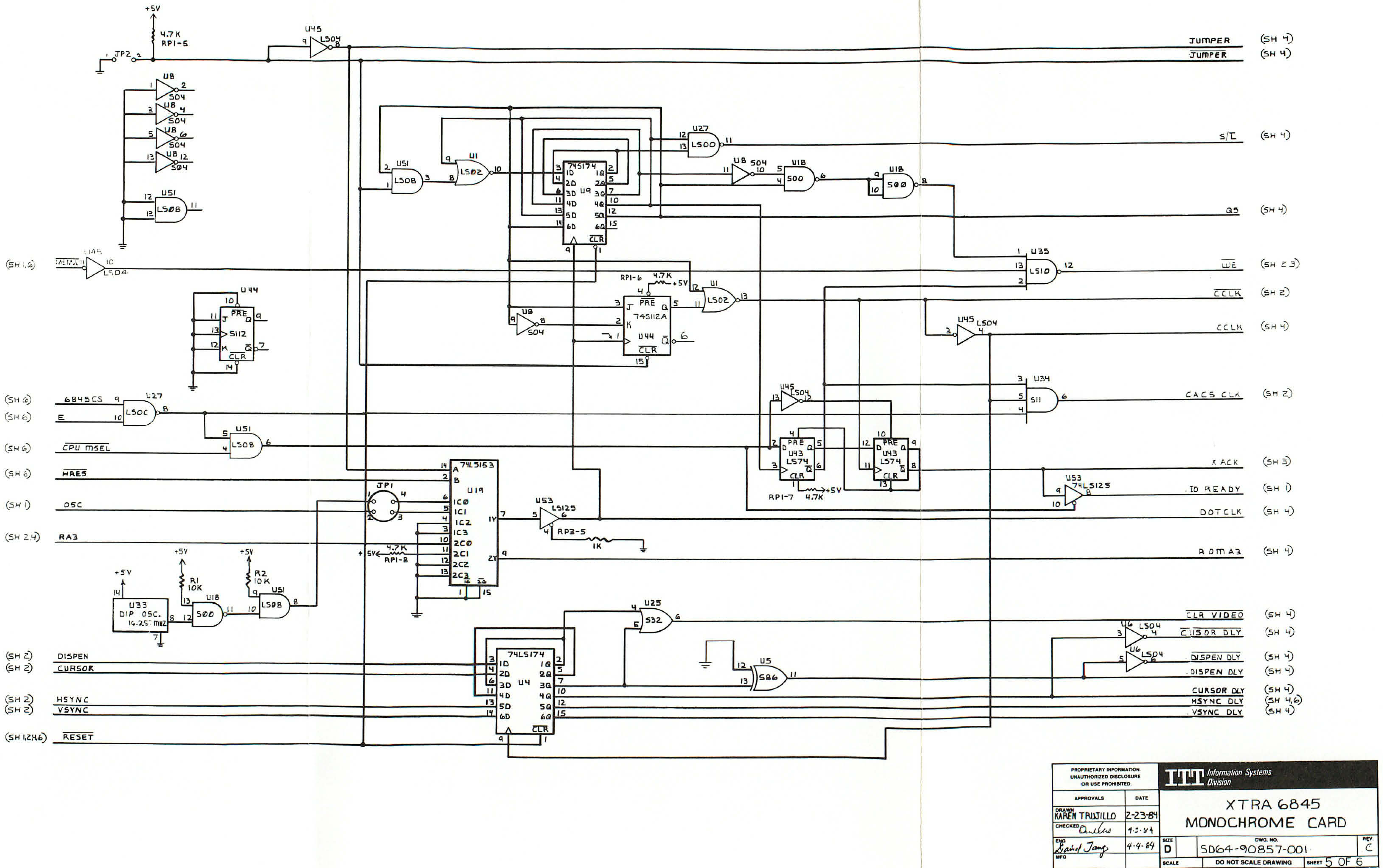
SIZE D — SD64-90857-001 C

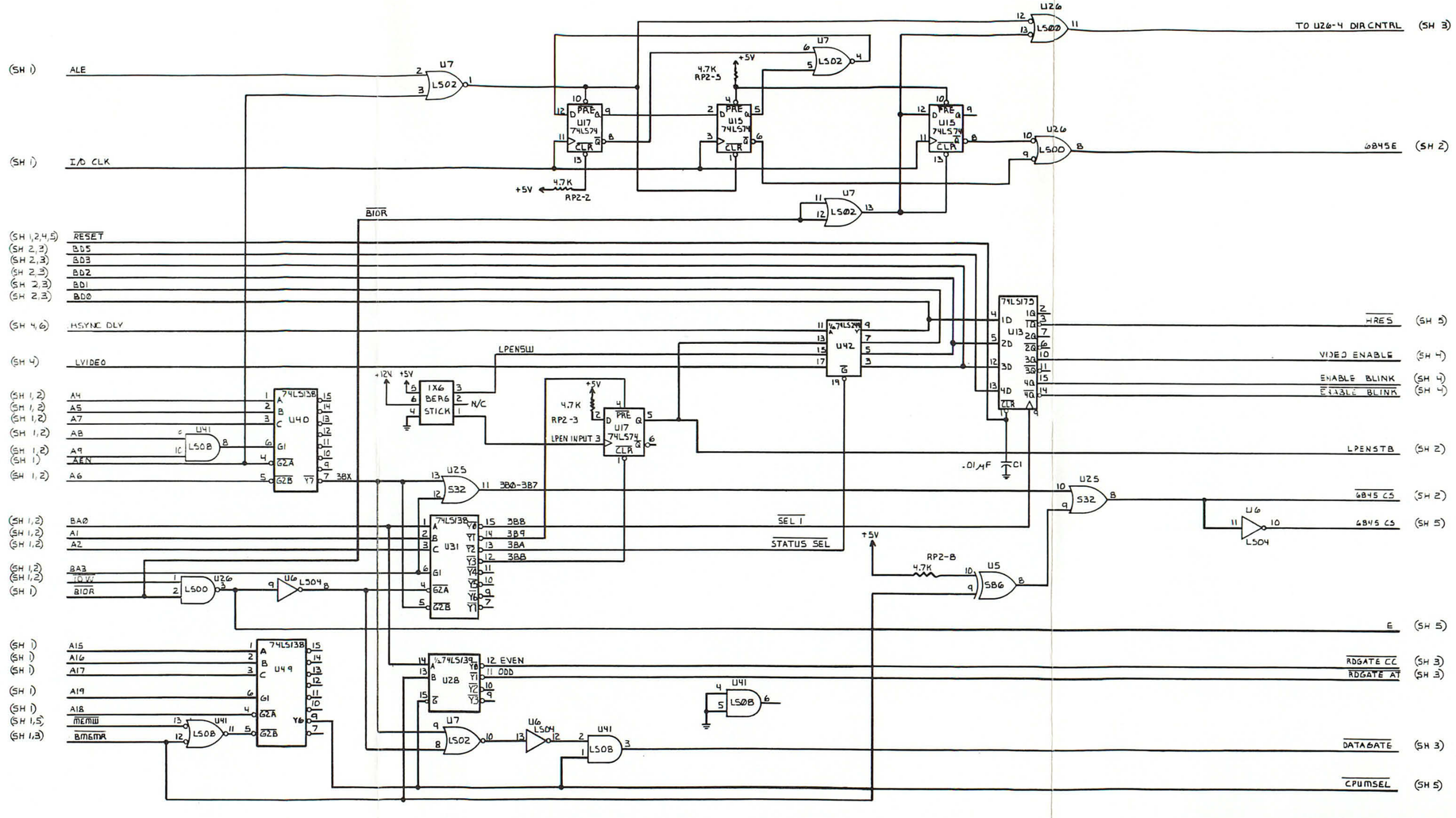


DRAWN KAREN TRUJILLO	DATE 2-23-84	ITT
CHECKED	4-2-84	EXTRA 6845
ENGR. David Jang	4-4-84	MONOCHROME CARD
MFG.		SCALE SHEET 3/6
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE D 50604-90857-001 C

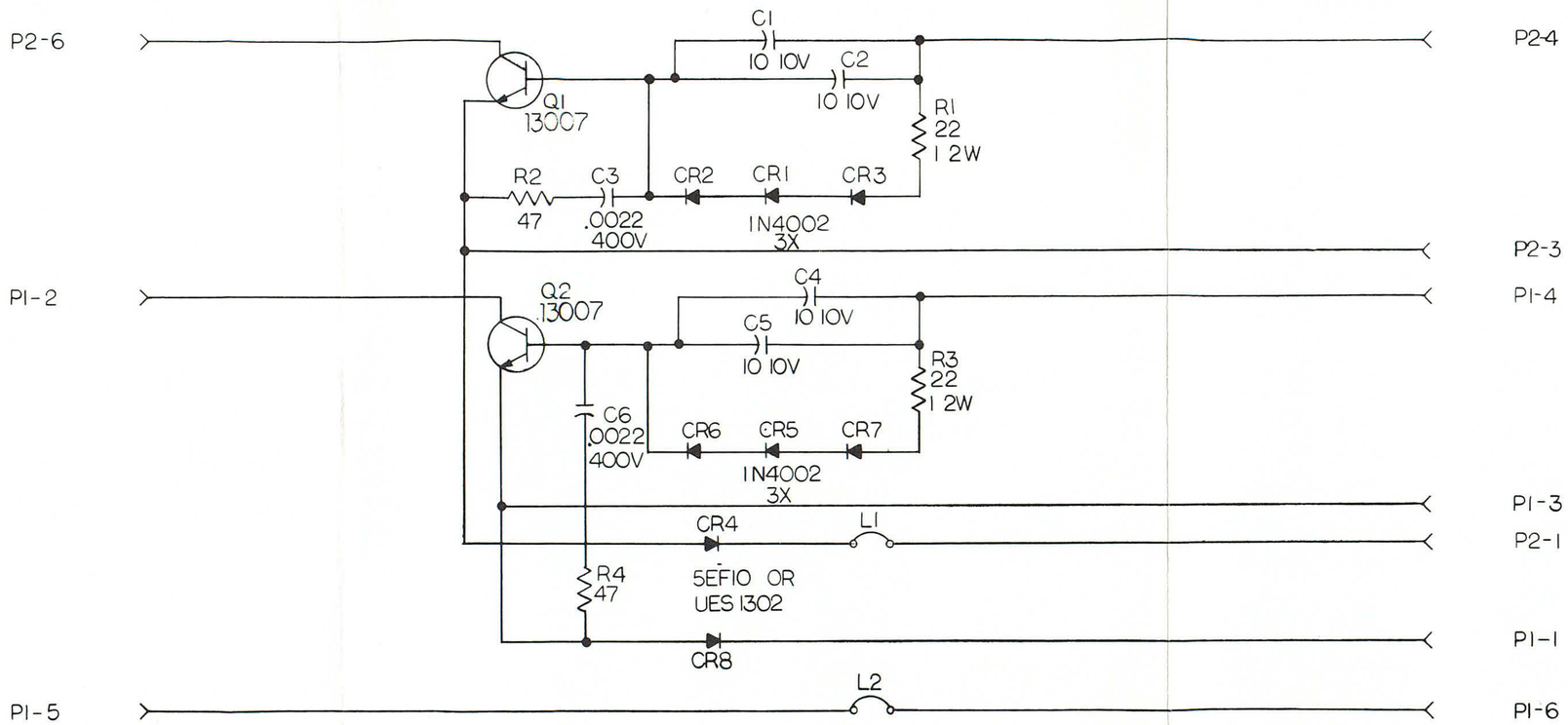


PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		ITT Information Systems Division	
APPROVALS	DATE	XTRA 6845 MONOCHROME CARD	
DRAWN KAREN TRUJILLO	2-23-84		
CHECKED	4-3-84		
ENG David Jang	4-9-84	SIZE D	DWG. NO. SD64-90857-001 REV. C
MFG		SCALE ~ DO NOT SCALE DRAWING	SHEET 4 OF 6

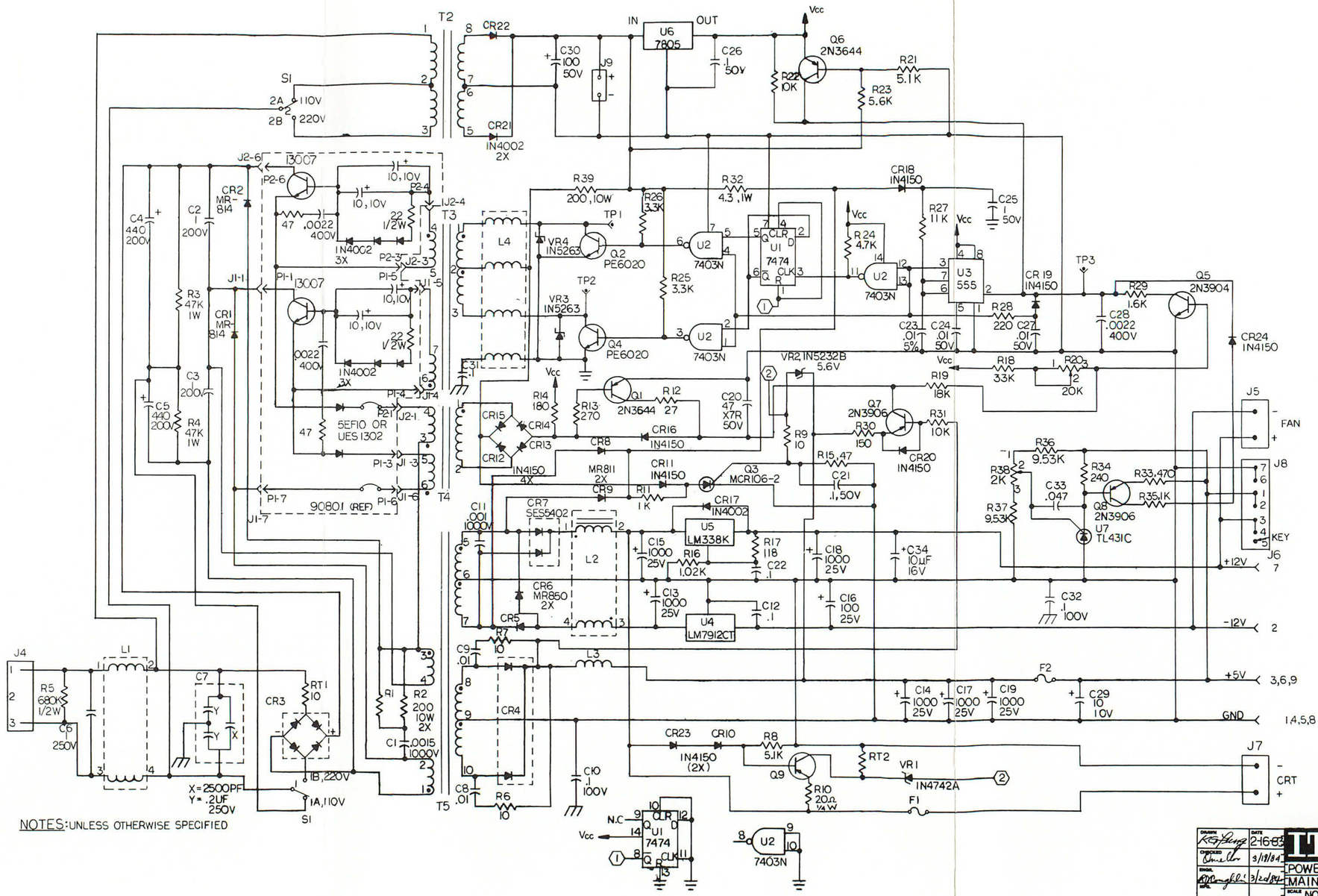

+5V
4.7K
RP1-5
JP2
U45
LS04
U8
S04
U51
LS08
JUMPER (SH 4)
JUMPER (SH 4)
U27
LS00
S/T (SH 4)
U1
LS02
74S174
U9
U18
S00
Q5 (SH 4)
(SH 1,6) MEMW
U35
LS10
WE (SH 2,3)
CCLK (SH 2)
CCLK (SH 4)
U44
S112
RP1-6
74S112A
U34
S11
CACS CLK (SH 2)
(SH 6) 6845CS
(SH 6) E
(SH 6) CPU MSEL
(SH 6) HRES
(SH 1) OSC
(SH 2,4) RA3
U43
LS74
RP1-7
XACK (SH 3)
U53
74LS125
IO READY (SH 1)
74LS153
U19
JP1
LS125
RP3-5
1K
DOTCLK (SH 4)
RP1-8
ROMA3 (SH 4)
U33
DIP OSC.
16.257 MHZ
R1
10K
R2
10K
U25
S32
CLR VIDEO (SH 4)
U6
CURSOR DLY (SH 4)
(SH 2) DISPEN
(SH 2) CURSOR
74LS174
U4
U5
S86
DISPEN DLY (SH 4)
DISPEN DLY (SH 4)
CURSOR DLY (SH 4)
(SH 2) HSYNC
HSYNC DLY (SH 4,6)
(SH 2) VSYNC
VSYNC DLY (SH 4)
(SH 1,2,4,6) RESET
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
ITT Information Systems Division
APPROVALS
DATE
DRAWN KAREN TRUJILLO 2-23-84
CHECKED 4-3-84
ENG David Tang 4-4-84
MFG
XTRA 6845
MONOCHROME CARD
SIZE D
DWG. NO. SD64-90857-001
REV. C
SCALE
DO NOT SCALE DRAWING
SHEET 5 OF 6



PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		ITT Information Systems Division	
APPROVALS	DATE	XTRA 6845 MONOCHROME CARD	
DRAWN KAREN TRUJILLO	2-23-84		
CHECKED	4-4-84		
ENG David Tang	4-4-84	SIZE D	DWG. NO. SD64-90857-001 REV. C
MFG		SCALE ~ DO NOT SCALE DRAWING	SHEET 6 OF 6



DRAWN G HSING	DATE 102482	ITT
CHECKED	3/19/84	SYS POWER SWITCHER - INV BOARD - SCHEMATIC.
ENGR MFG	3/20/84	SCALE NONE SHEET 1 / 1
PROPRIETARY INFORMATION. UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.		SIZE C 5D64-90801-001 A



NOTES: UNLESS OTHERWISE SPECIFIED

DRAWN	DATE	ITT
CHECKED	3/19/84	POWER SUPPLY
ENGR.	3/20/84	MAIN BOARD
MFG.	SCALE NONE	SHEET 1 / 1
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.	SIZE D	35D64-90805-002 C

A—ASCII Chart

ASCII	HEX	Control	CHAR	ASCII	HEX	CHAR
000	00H	NUL	(null)	032	20H	(space)
001	01H	SOH	☺	033	21H	!
002	02H	STX	☻	034	22H	”
003	03H	ETX	♥	035	23H	#
004	04H	EOT	♦	036	24H	$
005	05H	ENQ	♣	037	25H	%
006	06H	ACK	♠	038	26H	&
007	07H	BEL	(beep)	039	27H	´
008	08H	BS	◘	040	28H	(
009	09H	HT	(tab)	041	29H	)
010	0AH	LF	(line feed)	042	2AH	*
011	0BH	VT	(home)	043	2BH	+
012	0CH	FF	(form feed)	044	2CH	,
013	0DH	CR	(carriage return)	045	2DH	-
014	0EH	SO	♫	046	2EH	.
015	0FH	SI	☼	047	2FH	/
016	10H	DLE	►	048	30H	0
017	11H	DC1	◄	049	31H	1
018	12H	DC2	↕	050	32H	2
019	13H	DC3	!!	051	33H	3
020	14H	DC4	¶	052	34H	4
021	15H	NAK	§	053	35H	5
022	16H	SYN	▬	054	36H	6
023	17H	ETB	↨	055	37H	7
024	18H	CAN	↑	056	38H	8
025	19H	EM	↓	057	39H	9
026	1AH	SUB	→	058	3AH	:
027	1BH	ESC	←	059	3BH	;
028	1CH	FS	(cursor right)	060	3CH	<
029	1DH	GS	(cursor left)	061	3DH	=
030	1EH	RS	(cursor up)	062	2EH	>
031	1FH	US	(cursor down)	063	3FH	?

ASCII	HEX	CHAR	ASCII	HEX	CHAR
064	40H	@	096	60H	‘
065	41H	A	097	61H	a
066	42H	B	098	62H	b
067	43H	C	099	63H	c
068	44H	D	100	64H	d
069	45H	E	101	65H	e
070	46H	F	102	66H	f
071	47H	G	103	67H	g
072	48H	H	104	68H	h
073	49H	I	105	69H	i
074	4AH	J	106	6AH	j
075	4BH	K	107	6BH	k
076	4CH	L	108	6CH	l
077	4DH	M	109	6DH	m
078	4EH	N	110	6EH	n
079	4FH	O	111	6FH	o
080	50H	P	112	70H	p
081	51H	Q	113	71H	q
082	52H	R	114	72H	r
083	53H	S	115	73H	s
084	54H	T	116	74H	t
085	55H	U	117	75H	u
086	56H	V	118	76H	v
087	57H	W	119	77H	w
088	58H	X	120	78H	x
089	59H	Y	121	79H	y
090	5AH	Z	122	7AH	z
091	5BH	[	123	7BH	{
092	5CH	\	124	7CH	¦
093	5DH	]	125	7DH	}
094	5EH	^	126	7EH	~
095	5FH	—			

ASCII	HEX	CHAR	ASCII	HEX	CHAR
127	7FH	△	158	9EH	Pt
128	80H	Ç	159	9FH	*f*
129	81H	ü	160	A0H	*á*
130	82H	é	161	A1H	*í*
131	83H	â	162	A2H	*ó*
132	84H	ä	163	A3H	*ú*
133	85H	à	164	A4H	*ñ*
134	86H	å	165	A5H	*Ñ*
135	87H	ç	166	A6H	*a*
136	88H	ê	167	A7H	*o*
137	89H	ë	168	A8H	¿
138	8AH	è	169	A9H	⌐
139	8BH	ï	170	AAH	¬
140	8CH	î	171	ABH	½
141	8DH	ì	172	ACH	¼
142	8EH	Ä	173	ADH	¡
143	8FH	Å	174	AEH	«
144	90H	Ë	175	AFH	»
145	91H	æ	176	B0H	▒
146	92H	Æ	177	B1H	▒
147	93H	ô	178	B2H	▓
148	94H	ö	179	B3H	│
149	95H	ò	180	B4H	┤
150	96H	û	181	B5H	╡
151	97H	ù	182	B6H	╢
152	98H	ÿ	183	B7H	╖
153	99H	Ö	184	B8H	╕
154	9AH	Ü	185	B9H	╣
155	9BH	¢	186	BAH	║
156	9CH	£	187	BBH	╗
157	9DH	¥	188	BCH	╝

ASCII	HEX	CHAR	ASCII	HEX	CHAR
189	BDH	╜	220	DCH	▄
190	BEH	╛	221	DDH	▌
191	BFH	┐	222	DEH	▐
192	C0H	└	223	DFH	▀
193	C1H	┴	224	E0H	α
194	C2H	┬	225	E1H	β
195	C3H	├	226	E2H	γ
196	C4H	─	227	E3H	π
197	C5H	┼	228	E4H	Σ
198	C6H	╞	229	E5H	σ
199	C7H	╟	230	E6H	μ
200	C8H	╚	231	E7H	τ
201	C9H	╔	232	E8H	Φ
202	CAH	╩	233	E9H	Θ
203	CBH	╦	234	EAH	Ω
204	CCH	╠	235	EBH	δ
205	CDH	═	236	ECH	∞
206	CEH	╬	237	EDH	Ø
207	CFH	╧	238	EEH	ϵ
208	D0H	╨	239	EFH	∩
209	D1H	╤	240	F0H	≡
210	D2H	╥	241	F1H	±
211	D3H	╙	242	F2H	≥
212	D4H	╘	243	F3H	≤
213	D5H	╒	244	F4H	⌠
214	D6H	╓	245	F5H	⌡
215	D7H	╫	246	F6H	÷
216	D8H	╪	247	F7H	≈
217	D9H	┘	248	F8H	°
218	DAH	┌	249	F9H	∙
219	DBH	■	250	FAH	·

ASCII	HEX	CHAR
251	FBH	√
252	FCH	n
253	FDH	2
254	FEH	■
255	FFH	(blank 'FF')

DECIMAL VALUE	▶	0	16	32	48	64	80	96	112
▼	HEXA DECIMAL VALUE	0	1	2	3	4	5	6	7
0	0	BLANK (NULL)	▶	BLANK (SPACE)	0	@	P	‘	p
1	1	☺	◀	!	1	A	Q	a	q
2	2	☻	↕	″	2	B	R	b	r
3	3	♥	!!	#	3	C	S	c	s
4	4	♦	¶	$	4	D	T	d	t
5	5	♣	§	%	5	E	U	e	u
6	6	♠	▬	&	6	F	V	f	v
7	7	•	↨	’	7	G	W	g	w
8	8	◘	↑	(	8	H	X	h	x
9	9	○	↓	)	9	I	Y	i	y
10	A	◙	→	*	:	J	Z	j	z
11	B	♂	ESC ←	+	;	K	[	k	¦
12	C	♀	∟	,	<	L	\	l	¦
13	D	♪	↔	—	=	M	]	m	¦
14	E	♫	▲	.	>	N	^	n	~
15	F	☼	▼	/	?	O	_	o	△

DECIMAL VALUE	➡	128	144	160	176	192	208	224	240
⬇	HEXA DECIMAL VALUE	8	9	A	B	C	D	E	F
0	0	Ç	É	á	▒	└	╨	∝	≡
1	1	ü	æ	í	▒	┴	╤	β	±
2	2	é	Æ	ó	▓	┬	╥	Γ	≥
3	3	â	ô	ú	|	├	╙	π	≤
4	4	ä	ö	ñ	┤	─	╘	Σ	⌠
5	5	à	ò	Ñ	╡	+	╒	σ	⌡
6	6	å	û	a	╢	╞	╓	μ	÷
7	7	ç	ù	o	╖	╟	╫	τ	≈
8	8	ê	ÿ	¿	╕	╚	╪	Φ	○
9	9	ë	Ö	⌐	╣	╔	┘	θ	●
10	A	è	Ü	¬	║	╩	┌	Ω	•
11	B	ï	¢	½	╗	╦	■	δ	√
12	C	î	£	¼	╝	╠	▬	∞	n
13	D	ì	Y	¡	╜	═	▮	ϕ	2
14	E	Ä	Pt	≪	╛	╬	▮	∈	▮
15	F	Å	ƒ	≫	┐	╧	▬	∩	BLANK 'FF'

B—8088 Instruction Set Summary

8088 INSTRUCTION SET SUMMARY

DATA TRANSFER

MOV = Move	76543210	76543210	76543210	76543210
Register/memory to/from register	100010dw	mod reg r/m	Not Used	Not Used
Immediate to register memory	1100011w	mod 000 r/m	data	data if w 1
Immediate to register	1011w reg	data	data if w 1	Not Used
Memory to Accumulator	1010000w	addr low	addr high	Not Used
Accumulator to Memory	1010001w	addr low	addr high	Not Used
Register/memory to segment register	10001110	mod 0 reg r/m	Not Used	Not Used
Segment register to register/memory	10001100	mod 0 reg r/m	Not Used	Not Used

	76543210	76543210	76543210	76543210
PUSH = Push				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m	Not Used	Not Used
Register	0 1 0 1 0 reg	Not Used	Not Used	Not Used
Segment register	0 0 0 reg 1 1 0	Not Used	Not Used	Not Used
POP = Pop				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m	Not Used	Not Used
Register	0 1 0 1 1 reg	Not Used	Not Used	Not Used
Segment register	0 0 0 reg 1 1 1	Not Used	Not Used	Not Used
XCHG = Exchange				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m	Not Used	Not Used
Register with accumulator	1 0 0 1 0 reg	Not Used	Not Used	Not Used
IN = Input from				
Fixed port	1 1 1 0 0 1 0 w	port	Not Used	Not Used
Variable port	1 1 1 0 1 1 0 w	Not Used	Not Used	Not Used

OUT = Output to	**76543210**	**76543210**	**76543210**	**76543210**
Fixed port	1 1 1 0 0 1 1 w	port	Not Used	Not Used
Variable port	1 1 1 0 1 1 1 w	Not Used	Not Used	Not Used
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1	Not Used	Not Used	Not Used
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m	Not Used	Not Used
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m	Not Used	Not Used
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m	Not Used	Not Used
LAHF = Load AH with flags	1 0 0 1 1 1 1 1	Not Used	Not Used	Not Used
SAHF = Store AH into flags	1 0 0 1 1 1 1 0	Not Used	Not Used	Not Used
PUSHF = Push flags	1 0 0 1 1 1 0 0	Not Used	Not Used	Not Used
POPF = Pop flags	1 0 0 1 1 1 0 1	Not Used	Not Used	Not Used

ARITHMETIC

ADD = Add	76543210	76543210	76543210	76543210
Reg/memory with register to either	0 0 0 0 0 0 d w	mod reg r/m	Not Used	Not Used
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s w 01
Immediate to accumlator	0 0 0 0 0 1 0 w	data	data if w 1	Not Used
ADC = Add with carry				
Reg/memory with register to enter	0 0 0 1 0 0 d w	mod reg r/m	Not Used	Not Used
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w 1	Not Used
INC = Increment				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m	Not Used	Not Used
Register	0 1 0 0 0 reg	Not Used	Not Used	Not Used

	76543210	76543210	76543210	76543210
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	Not Used	Not Used	Not Used
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	Not Used	Not Used	Not Used
SUB = **Subtract**				
Reg/memory and register to either	0 0 1 0 1 0 d w	mod reg r/m	Not Used	Not Used
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w 1	Not Used
SBB = **Subtract with borrow**				
Reg/memory and register to either	0 0 0 1 1 0 d w	mod reg r/m	Not Used	Not Used
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/ m	data	data if s w 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w 1	Not Used

	76543210	76543210	76543210	76543210
DEC = Decrement				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m	Not Used	Not Used
Register	0 1 0 0 1 reg	Not Used	Not Used	Not Used
NEG = Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m	Not Used	Not Used
CMP = Compare				
Reg/memory and register to either	0 0 1 1 1 0 d w	mod reg r/m	Not Used	Not Used
Immediate with register/mernory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s w 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w 1	Not Used
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	Not Used	Not Used	Not Used
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1	Not Used	Not Used	Not Used
MUL = Multipy (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m	Not Used	Not Used
IMUL = Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m	Not Used	Not Used
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0	Not Used	Not Used

	76543210	76543210	76543210	76543210
DIV = Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m	Not Used	Not Used
IDIV = Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m	Not Used	Not Used
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0	Not Used	Not Used
CBW = Convert byte to word	1 0 0 1 1 0 0 0	Not Used	Not Used	Not Used
CWD = Convert word to double word	1 0 0 1 1 0 0 1	Not Used	Not Used	Not Used

LOGIC

NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m	Not Used	Not Used
SHL/SAL = Shift logical arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m	Not Used	Not Used
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m	Not Used	Not Used
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m	Not Used	Not Used
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m	Not Used	Not Used
ROR = Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m	Not Used	Not Used

	76543210	76543210	76543210	76543210
RCL = Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m	Not Used	Not Used
RCR = Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m	Not Used	Not Used
AND = And				
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m	Not Used	Not Used
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 1 r/m	data	data if w 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w 1	Not Used
TEST = And function to flags, no result				
Reg/memory and register	1 0 0 0 0 1 0 w	mod reg r/m	Not Used	Not Used
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/ m	data	data if w 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w 1	Not Used

OR = Or	**76543210**	**76543210**	**76543210**	**76543210**
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m	Not Used	Not Used
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/ m	data	data if w 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w 1	Not Used
XOR = Exclusive or				
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m	Not Used	Not Used
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/ m	data	data if w 1
Immediate to accumulator	0 0 1 1 0 1 0 0	data	data if w 1	Not Used

STRING MANIPULATION

REP = Repeat	1 1 1 1 0 0 1 z	Not Used	Not Used	Not Used
MOVS = Move byte/word	1 0 1 0 0 1 0 w	Not Used	Not Used	Not Used
CMPS = Compare byte/word	1 0 1 0 0 1 1 w	Not Used	Not Used	Not Used
SCAS = Scan byte/word	1 0 1 0 1 1 1 w	Not Used	Not Used	Not Used

	76543210	76543210	76543210	76543210
LODS = Load byte/word to AL/AX	1 0 1 0 1 1 0 w	Not Used	Not Used	Not Used
STOS = Store byte/word from AL/AX	1 0 1 0 1 0 1 w	Not Used	Not Used	Not Used

CONTROL TRANSFER

CALL = Call

Direct within segment	Not Used	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	Not Used	1 1 1 1 1 1 1 1	mod 0 1 0 r/m	Not Used
Direct intersegment	Not Used	1 0 0 1 1 0 1 0	offset- low	offset-high
	Not Used	Not Used	seg-low	seg-high
Indirect intersegment	Not Used	1 1 1 1 1 1 1 1	mod 0 1 0 r/ m	Not Used

JMP = Unconditional Jump

Direct within segment	Not Used	1 1 1 0 1 0 0 1	disp-low	disp -high
Direct within segment short	Not Used	1 1 1 0 1 0 1 1	disp	Not Used

	76543210	76543210	76543210	76543210
Indirect within segment	Not Used	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	Not Used
Direct intersegment	Not Used	1 1 1 0 1 0 1 0	offset- low	offset-high
	Not Used	Not Used	seg-low	seg-high
Indirect intersegment	Not Used	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	Not Used

RET = Return from Call

Within segment	Not Used	1 1 0 0 0 0 1 1	Not Used	Not Used
Within segment adding immediate to SP	Not Used	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	Not Used	1 1 0 0 1 0 1 1	Not Used	Not Used
Intersegment adding immediate to SP	Not Used	1 1 0 0 1 0 1 0	data-low	data-high

JE/JZ = Jump on equal/zero	Not Used	0 1 1 1 0 1 0 0	disp	Not Used
JL/JNGE = Jump on less/not greater or equal	Not Used	0 1 1 1 1 1 0 0	disp	Not Used
JLE/JNG = Jump on less or equal/not greater	Not Used	0 1 1 1 1 1 1 0	disp	Not Used

	76543210	76543210	76543210	76543210
JB/JNAE = Jump on below/not above or equal	Not Used	0 1 1 1 0 0 1 0	disp	Not Used
JBE/JNA = Jump on below or equal/not above	Not Used	0 1 1 1 0 1 1 0	disp	Not Used
JP/JPE = Jump on parity/parity even	Not Used	0 1 1 1 1 0 1 0	disp	Not Used
JO = Jump on overflow	Not Used	0 1 1 1 0 0 0 0	disp	Not Used
JS = Jump on sign	Not Used	0 1 1 1 1 0 0 0	disp	Not Used
JNE/JNZ = Jump on not equal/not zero	Not Used	0 1 1 1 0 1 0 1	disp	Not Used
JNL/JGE = Jump on not less/greater or equal	Not Used	0 1 1 1 1 1 0 1	disp	Not Used
JNLE/JG = Jump on not less or equal/greater	Not Used	0 1 1 1 1 1 1 1	disp	Not Used
JNB/JAE = Jump on not below/above or equal	Not Used	0 1 1 1 0 0 1 1	disp	Not Used
JNBE/JA = Jump on not below or equal/above	Not Used	0 1 1 1 0 1 1 1	disp	Not Used
JNP/JPO = Jump on not parity/parity odd	Not Used	0 1 1 1 1 0 1 1	disp	Not Used
JNO = Jump on not overflow	Not Used	0 1 1 1 0 0 0 1	disp	Not Used

	76543210	76543210	76543210	76543210
JNS = Jump on not sign	Not Used	0 1 1 1 1 0 0 1	disp	Not Used
LOOP = Loop CX times	Not Used	1 1 1 0 0 0 1 0	disp	Not Used
LOOPZ/LOOPE = Loop while zero equal	Not Used	1 1 1 0 0 0 0 1	disp	Not Used
LOOPNZ/LOOPNE = Loop while not zero/equal	Not Used	1 1 1 0 0 0 0 0	disp	Not Used
JCXZ = Jump on CX zero	Not Used	1 1 1 0 0 0 1 1	disp	Not Used

INT = Interrupt

Type specified	Not Used	1 1 0 0 1 1 0 1	type	Not Used
Type 3	Not Used	1 1 0 0 1 1 0 0	Not Used	Not Used
INTO = Interrupt on overflow	Not Used	1 1 0 0 1 1 0 1	Not Used	Not Used
IRET = Interrupt return	Not Used	1 1 0 0 1 1 1 1	Not Used	Not Used

PROCESSOR CONTROL

CLC = Clear carry	Not Used	1 1 1 1 1 0 0 0	Not Used	Not Used

	76543210	76543210	76543210	76543210
CMC = Complement Carry	Not Used	11110101	Not Used	Not Used
STC = Set carry	Not Used	11111001	Not Used	Not Used
CLD = Clear direction	Not Used	11111100	Not Used	Not Used
STD = Set direction	Not Used	11111101	Not Used	Not Used
CLI = Clear interrupt	Not Used	11111010	Not Used	Not Used
STI = **Set Interrupt**	Not Used	11111011	Not Used	Not Used
HLT = Halt	Not Used	11110100	Not Used	Not Used
WAIT = Wait	Not Used	10011011	Not Used	Not Used
ESC = Escape (to external device)	Not Used	11011xxx	mod	Not Used
CLI = Clear interrupt	Not Used	11111010	Not Used	Not Used
STI = Set interrupt	Not Used	11111011	Not Used	Not Used

	76543210	76543210	76543210	76543210
HLT = Halt	Not Used	11110100	Not Used	Not Used
WAIT = Wait	Not Used	10011011	Not Used	Not Used
ESC = Escape (to external device)	Not Used	11011xxx	mod x x x r/m	Not Used
LOCK = Bus lock prefix	Not Used	11110000	Not Used	Not Used

Footnotes:
AL = 8 bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg

if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high; disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 r/m = 110 then EA = disp-high; disp-low.

if s:w = 01 then 16 bits of immediate data form the operand
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

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