UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.
Before the Honorable Paul J. Luckern
Administrative Law Judge

DOCKET

In the Matter of CERTAIN INTEGRATED CIRCUITS AND PRODUCTS CONTAINING SAME	Re. Motion 402-17 Investigation No. 337-TA-402

MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT OF MOTION TO AMEND IDENTIFICATION OF PRIOR ART

I.
INTRODUCTION

Although it is far from clear that such motion is required, out of an abundance of caution and to avoid a potential issue at the prehearing conference Samsung hereby seeks leave to amend its identification of prior art.[1] (G.R. 10.) Samsung seeks to add the following:

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[1] Copies of Samsung's proposed amended identifications of prior art for the '724 and '166 patents are attached hereto as exhibits 1-2, respectively. The new material is found at No. 57 on p. 6 of exhibit 1 and on the last two pages of exhibit 2. The original identifications are attached as exhibits 3-4.

(1) the undisclosed Fujitsu June 18, 1980 Japanese patent application related to the '724 patent[2] ("Fujitsu application");

(2) reports analyzing recently obtained 16K and 64K DRAM chips manufactured by National Semiconductor ("National chip reports"); and

(3) documents regarding the development of the National Chips such as the Yang invention disclosure and the U.S. and U.K patent applications. ("National documents").

None of this evidence comes as a surprise to Fujitsu. Samsung listed the National 16K, 64K and 256K parts in its original prior art identification on March 6, 1998. After locating sample 16K and 64K chips Samsung expedited the analysis of those chips. All evidence relating to the chips and to National's work has been produced as it has become available--before it was requested and before the date for the exchange of exhibits. Accordingly, Samsung should be permitted to rely upon the above evidence at the hearing.

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[2] The Japanese original and a certified translation are attached as exhibits 13-14 to the March 27, 1998 Supplemental Memorandum of Points and Authorities in Support of Motion to Compel Production of Documents Under the Crime/Fraud Exception to Attorney-Client Privilege ("Supplemental Memorandum").

II.
THERE IS NO PREJUDICE TO FUJITSU

Although Fujitsu's adamant opposition speaks volumes to the devastating impact of this evidence on its case, none of this evidence prejudices Fujitsu. National's chips that Samsung listed on its prior art identification invalidate the '166 patent. The reports analyzing the chips confirm this. The National documents establish that National was first to combine stacked capacitors with folded bit lines. Understandably, Fujitsu does not want the court to consider this evidence.

Fujitsu cannot reasonably claim to be surprised by it own patent application that is directly relevant to the '724 patent. Indeed, Fujitsu has only its own mendacity to blame for why the Fujitsu application was not listed on Samsung's '724 prior art disclosure. (See Supplemental Memorandum, pp. 1-5.) With Takada swearing to the PTO that no other application besides the November 28, 1979 application existed, Fujitsu can hardly fault Samsung for not exposing the fraud sooner.

Similarly, there can be no surprise with respect to the National chip reports since Samsung listed the National 16K and 64K chips on its prior art list. (See exhibit 4, p. 7). Since the features on these chips are microscopic, it goes without saying that Samsung would have to present professional analyses, such as SEMs, for the chips to have any significance. Samsung, of course, would like the court to understand the structure of the National chips, which is difficult to discern without proper technical analysis. Fujitsu apparently does not want the court to read the analysis of the National chips precisely because the chips invalidate the '166 patent. These reports have been produced as soon as they have been received--without being specifically requested and well in advance of the April 13, 1998 date for the exchange of exhibits. Fujitsu has not been prejudiced.

With respect to the National documents, their recent discovery owes not to any lack of diligence on Samsung's behalf but rather to the inherent complications of conducting third-party discovery for archived records. The National documents were uncovered only after Samsung: (1) informally discussed the issue with National to determine whether formal discovery would be appropriate; (2) obtained and served a subpoena on National; (3) had National search for nearly 20-year-old records (a task it was understandably disinclined to undertake); (4) was told that the relevant documents were transferred to Fairchild Semiconductor after National sold its memory business to Fairchild; (5) had to repeat the entire process of investigating and of obtaining and serving an appropriate subpoena anew with Fairchild after which time Samsung ultimately located the National documents in a Utah warehouse. Just as with the National chip reports, Samsung has produced the National documents as soon as they have become available and well in advance of the April 13, 1998 deadline for the exchange of exhibits.

III.
CONCLUSION

Fujitsu is not surprised, much less prejudiced by Samsung's reliance on the evidence discussed above. Accordingly, to the extent a motion is required to amend Samsung's prior art identifications, Samsung respectfully submits that good cause exists and that Samsung should be permitted to file and serve the amended prior art identifications attached as exhibits 1 and 2.

Dated: April 7, 1998

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EXHIBIT 1

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.
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DRAFT

In the Matter of

CERTAIN INTEGRATED CIRCUITS AND PRODUCTS CONTAINING SAME

Investigation No.
337-TA-402

RESPONDENTS SAMSUNG ELECTRONICS CO., LTD AND SAMSUNG SEMICONDUCTOR, INC.'S AMENDED IDENTIFICATION OF PRIOR ART FOR U.S. PATENT 4,352,724 ("'724 PATENT")

1. All prior art identified during the prosecution of the '724 Patent including re-examination proceedings.

2. W.W. Koste, et al., "Via Profiling By Plasma Etching With Varying Ion Energy," IBM Technical Disclosure Bulletin, Vol. 22, No. 7, Dec. 1978, pp. 2737-2738.

3. Work completed by IBM by Messrs. Koste, Mathad, and Patnaik corresponding to IBM Technical Disclosure Bulletin, Vol. 22, No. 7, Dec. 1978, pp. 2737-2738.

4. G.S. Mathad and B. Patnaik, "Characteristics of Diode, Anode, and Triode Etching," Extended Abstracts from the Fall Meeting of the ElectroChemical Society in Los Angeles, California, Abstract 603, at 1510 (October 14-19, 1979).

5. T.A. Bartush, et al., "Sidewall Tailoring Using Two Different Reactive Ion Etchants In Succession," IBM Technical Disclosure Bulletin, 1977, p. 1388.

6. H.M. Gartner, J.E. Hitchner, A. Hoeg, Jr. and H.G. Sarkary, "Isotropic and Anisotropic Etching in a Diode System," IBM Technical Disclosure Bulletin, Vol. 20, No. 5, October 1977, pp. 1744-1745.

7. John L. Reynolds, et al., "Simulation of Dry Etched Line Edge Profiles," Journal of Vacuum Science Technology, Vol. 16, No. 6, December 1979, pp. 1772-1775.

8. James Dale Shy, "A Study of the Etching Characteristics of Semiconductor Materials in RF Plasmas," Master's Thesis, Air Force Institute of Technology, Air University, June 1974.

9. H.A. Clark, "Reactive Ion-Etch Process for Etched Sitewall Tailoring," IBM Technical Disclosure Bulletin, Vol. 19, No. 11, April 1977.

10. H.A. Clark, "Plasma Etching of SiO_2/Polysilicon Composite Film," Vol. 20, No. 4, September 1997.

11. Ernest Bassous, "Fabrication of Novel Three-Dimensional Microstructures By the Anisotropic Etching of (100) and (110) Silicon," IEEE Transactions On Electron Devices, Vol. ED-25, No. 10, October 1978, pp. 1178-1185.

12. Richard L. Bersin, "Chemically Selective, Anisotrophic Plasma Etching," Solid State Technology, April 1978, pp. 117-121.

13. Richard L. Bersin, "A Survey of Plasma-Etching Processes," Solid State Technology, May 1976, pp. 31-36.

14. J.A. Bondur, et al., "Step Coverage Process With Projection Printing and Reactive Ion Etching," IBM Technical Disclosure Bulletin, Vol. 19, No. 9, February 1977, pp. 3415-3416.

15. James A Bondur, "Dry Process Technology (Reactive Ion Etching)," Journal of Vacuum Science and Technology, Vol. 12, pp. 1023-29 (Sept/Oct 1976).

16. E.C.D. Darwall, "The Control of Plasma Etched Edge Profiles," 1046a Extended Abstracts, Vol. 77-2, (1977-10), pp. 40-401, The Plessey Company Ltd., Northamptonshire, England.

17. R.A. Gdula, "SF_6rei of Polysilicon," Extended Abstracts of the Journal of Electrochemical Society, Vol. 79-2, 14-19th October 1979, Abstract No. 608, pp. 1524-1526.

18. Gdula, Hollis & Pliskin, "Method of Controlling RIE Mesa Edge Profiles to Eliminate Mouseholing," IBM Technical Disclosure Bulletin, Vol. 21, No. 6, Nov. 1978.

19. W.R. Harshbarger, "Plasma Assisted Etching For VLIS," 1046B Extended Abstracts (1978) October, No. 2, Pennington, New Jersey, pp. 509-511.

20. H. Kalter, et al., "Plasmaätzen In Der IC-Technologie," Philips techn. Rdsch. 38, 203-214, 1979, pp. 203-214.

21. Werner Kern and C. Deckert, "Chemical Etching," Chapter V-1, pp. 401-496 in Thin Film Processes, J.L. Vossen and W. Kern, Eds., Academic Press, New York (1978).

22. C.J. Mogab and W.R. Harshbarger, "Plasma Process Set to Etch Finer Lines with Less Undercutting," Electronics, August 31, 1978, pp. 117-121.

23. Hiroshi Ono, et al., "A New Technology For Tapered Windows in Insulating Films," Journal of the Electrochemical Society, March 1979, pp. 504-506.

24. P.D. Parry and A.F. Rhodde, "Anisotropic Plasma Etching of Semiconductor Materials," Solid State Technology, April 1979, pp. 125-132.

25. R.A. Porter, et al., "Plasma Etching of Phisphosilicate Glass," 1046B Extended Abstracts (1978) October, No. 2, Pennington, New Jersey, pp. 515-516.

26. G.C. Schwartz and P.M. Schaible, "Reactive Ion Etching of Silicon," Journal of Vacuum Science Technology, 16(2), March/April 1979, p. 410.

27. R.C. Turnbull, "Tapering Metallurgy Edges," IBM Technical Disclosure Bulletin, Vol. 15, No. 5, October 1972, p. 1620.

28. Brandes and R.H. Dudles, "Wall Profiles Produced During Photoresist Masked Isotropic Etching," Journal of Electrochem. Society, Vol. 120 (January 1973).

29. "A New Technology for Tapered Windows in Insulating Films," Journal of the Electrochemical Society, Vol. 126, No. 3 (March 1979).

30. Parisi, Haszko & Rozgonyi, "Tapered Windows in SiO_2 . . .", Journal of the Electrochemical Society, Vol. 124, No. 6, June 1977.

31. Japanese Patent Application Kokai No. 53-13372, Fujitsu k.k., published February 6, 1978 ("Fujitsu Reference").

32. Electronics, June 5, 1972 at p. 43.

33. U.S. Patent No. 3,880,684.

34. U.S. Patent No. 3,986,912.

35. U.S. Patent No. 4,149,904.

36. U.S. Patent No. 4,214,946.

37. U.S. Patent No. 4,293,375.

38. U.S. Patent No. 4,436,583.

39. German Patent No. DT 23 40 442 (Counterpart of UK 1 398 019).

40. UK Patent No. 1 398 019.

41. German Patent No. DT 26 32 093 (Counterpart of US 3,986,912).

42. Japanese Patent No. 52-40978.

43. Japanese Patent No. 52-141443.

44. German Patent No. DE 27 27 788 (Counterpart of US 4,293,375).

45. German Patent No. DE 27 30 156 (Counterpart of Can. 1059882).

46. Canadian Patent No. 1059882.

47. German Patent No. De 28 45 460 (Counterpart of US 4,149,904).

48. Japanese Patent No. 54-61457.

49. Japanese Patent No. 54-87172.

50. EPO Patent No. 0 015 403 (Counterpart of US 4,214,946).

51. Japanese Patent No. 58-108229 (Counterpart of US 4,436,583).

52. Japanese Patent Application Kokai No. 53-116090, Oki Electric Industries K.K., published October 11, 1978 ("Kokai Reference").

53. Japanese Laid-Open Application, Kokai 54-87172 (J-2).

54. Japanese Patent Publication (Kokoku) No. 3-13744.

55. Japanese Laid-Open Application, Kokai 52-141443.

56. Japanese Patent Application 54-154003.

57. Japanese Patent Application 55-82388.

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EXHIBIT 2

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RESPONDENTS SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC.'S AMENDED IDENTIFICATION OF PRIOR ART FOR '166 PATENT

LIST OF '166 PRIOR ART

Author	Title	Source	Page(s)	Date of Publication
Arakawa	Semiconductor Memory Device	U.S. Pat. No. 4,355,375		10/19/82
Asai	Trends in Megabit DRAMS	1984 International Electron Device Meeting, Digest of Technical Papers	6-12	December 1984
Baglee	Stacked Capacitors for VLSI Semiconductor Devices	U.S. Pat. No. 5,049,958		09/17/91, filed 09/07/82
Barnes et al.	A High Performance Sense Amplifier for a 5 V Dynamic RAM	IEEE Journal of Solid State Circuits. Vol. SC-15, No. 5.	831-839	October 1980
Bohr et al.	CMOS Process for Fabricating Integrated Circuits, Particularly Dynamic Memory Cells with Storage Capacitors	U.S. Patent No. 4,536,947		8/27/85
Bohr et al.	CMOS Process for Fabricating Integrated Circuits, Paticularly Dynamic Memory Cells	U.S. Patent No. 4,505,026		3/19/85
Chan et al.	A 5 V-Only 64K Dynamic RAM Based on High S/N Design	IEEE Journal of Solid State Circuits. Vol. SC-15, No. 5.	846-853	October 1980
Chan et al.	A 100 ns 5 V 64K x 1 MOS Dynamic RAM	IEEE Journal of Solid State Circuits. Vol. SC-15, No. 5.	839-845	October 1980
Chatterjee et al.	A Survey of High-Density Dynamic RAM Cell Concepts	IEEE Transactions on Electron Devices. Vol. ED-26, No. 6	827 - 839	June 1979
Chatterjee et al.	Buried Storage Punch Through Dynamic RAM Cell	U.S. Pat. No. 4,203,125		05/13/80
Dan	Semiconductor Memory	JP 58-003270(A)		1/10/83
Dan	Semiconductor Memory	JP 58-003271(A)		1/10/83
Dennard	Field_Effect Transistor Memory	U.S. Patent No. 3,387,286		6/4/68
S.S. Eaton et al.	A 100 ns 64K Dynamic RAM Using Redundancy Techniques	ISSCC 1981	84-85	February 1981
Endo et al.	High Performance 64 kbit Dynamic RAM	Hitachi Review, Vol. 31, No. 5	237-240	1982
Engeler et al.	Semiconductor Imaging Detector Device	U.S. Pat. No. 3,906,544		9/16/75
Fortino et al.	Double-Polysilicon, Double Diffused, Charge-Coupled Device Dynamic Memory Cell	IBM Technical Disclosure Bulletin, Vol. 21, No. 9	3581	February 1979
Furman et al.	Self-Aligned Integrated Circuits	U.S. Patent No. 4,021,789		5/3/77
Furuyama	Semiconductor Memory Storage Device	JP 56-83060		7/7/81
Furuyama	Dynamic Memory Device	JP 58-199557		11/19/83
Geffken et al.	Process for High-Capacitance Single-Device Memory Cell	IBM Technical Disclosure Bulletin, Vol. 21, No. 6		November 1978
Grossman	Dynamic RAM Trends in the 80s	Southcon/81 Conference Record	8-1/1-7	1981

Author	Title	Source	Page(s)	Date of Publication
Harari	Highly Scalable Dynamic RAM Cell with Self-Signal Amplification	U.S. Pat. No. 4,612,629		09/16/86
Hida	Semiconductor Memory Cell	JP 58-95858		6/7/83
Higa	Semiconductor Memory	JP No. 58-564530(A)		04/04/83
Ishihara et al.	A 256K Dynamic MOS RAM with Alpha Immune and Redundancy	ISSCC 1982	74-75	February 1982
Ishihara et al.	Semiconductor Memory Device and Method for Manufacture	UK Patent No. GB 2 113 466		08/03/83, filed 01/05/83
Itoh	Semiconductor Memory	U.S. Pat. No. 4,044,340		08/23/77
Itoh	Memory System	U.S. Pat. No. 4,138,740		02/26/79
Itoh et al.	High Density One-Device Dynamic MOS Memory Cells	IEE Proceedings, Vol. 130, Pt. I, No. 3	127-135	June 1983
Itoh et al.	High Density Memory Cell Structure	1981 IEEE Symposium on VLSI Technology, Digest of Technical Papers.	48-49	December 1981
Itoh et al.	A Single 5V 64K Dynamic RAM	ISSCC 1980	228-229	February 1980
Itou	Memory Unit	JP 56-164570(A)		12/17/81
Jones	64K Dynamic RAM - The Challenge	Electro/81 Conference Record	1-6	
Joshi et al.	Integrated Circuit Process Utilizing Lift-Off Techniques	U.S. Pat. No. 4,123,300		10/31/78
Katto et al.	A 64kbit Dynamic Memory	Hitachi Review, Vol. 29, No. 3	119-122	1980
Kinoshita	Semiconductor Memory Device	U.S. Pat. No. 4,604,639		
Klein et al.	Dynamic MOS RAM with Storage Cells having Mainly Insulated First Plate	U.S. Pat. No. 4,475,118		10/02/84, filed 12/15/80
Klein et al.	Method for Making a Semiconductor Capacitor	U.S Pat. No. 4,413,401		11/8/83
Klein et al.	Method of Making Integrated Semiconductor Structure Having and MOS and a Capacitor Device	U.S. Pat. No. 4,290,186		09/22/81
Kohara et al.	Semiconductor Memory Device Having a MOS Transistor and Superposed Capacitor	U.S. Pat. No. 4,799,093		1/17/89
Kosa et al.	Semiconductor Integrated Circuit Device and Method of Manufacturing the Same	U.S. Pat. No. 4,764,479		8/16/88
Koyanagi et al.	Kokai Patent No. SHO 53[1978]-108392			09/21/78, filed 03/04/77
Koyanagi et al.	Novel High Density, Stacked Capacitor MOS RAM	Proceedings of the 10th Conference on Solid State Devices, 1978, Japanese Journal of Applied Physics, Vol. 18, 1979 Suppl.	35-42	1979
Koyanagi et al.	Semiconductor Memory Device	U.S. Pat. No. 4,151,607		04/24/79

Author	Title	Source	Page(s)	Date of Publication
Koyanagi et al.	16KBit Stacked Capacitor MOS RAM	Electronic Communication Association Technical Research Report, SSD80-30	25-32	02/22/80
Koyanagi et al.	A 5-V Only 16kbit Stacked Capacitor MOS RAM	IEEE Transactions on Electron Devices, Vol. ED-27, No. 8	1596-1601	August 1980
Koyanagi et al.	A 5-V Only 16kbit Stacked Capacitor MOS RAM	IEEE Journal of Solid State Circuits, Vol. SC-15, No. 4	661-666	August 1980
Koyanagi et al.	Novel High Density, Stacked Capacitor MOS RAM	International Electron Devices Meeting, Digest of Technical Papers 1978	348-351	December 1978
Landler et al.	Recessed Gate One-Device Cell Memory Array	IBM Technical Disclosure Bulletin, Vol. 18, No. 12	3951-3952	May 1976
Lee et al.	A 64Kb MOS Dynamic RAM	1979 ISSCC	146-147	February 1979
Lu	High-Capacitance Dynamic RAM Cell Using Buried Polysilicon Electrodes and Buried Oxide MOS Transistors	IBM Technical Disclosure Bulletin, Vol. 26, No. 3B	1318-1322	August 1983
G. Madland	Covering the Semiconductor Industry	Issue 3-1		1983
Maeda	Semiconductor Memory Device	U.S. Pat. No. 4,403,307		09/06/83
Mao	RAM Utilizing Offset Contact Regions for Increased Storage Capacitance	U.S. Pat. No. 4,493,056		01/08/85, filed 06/30/82
Masuda et al.	Single 5-V, 64K RAM with Scaled-Down MOS Structure	IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 4		August 1980
Masuda et al.	A Semiconductor Memory	GB 2 098 396		11/17/82
Masuda et al.	Single 5-V, 64K RAM with Scaled-Down MOS Structure	IEEE Transactions on Electron Devices, Vol. ED-27, No. 8	1607-1611	August 1980
Masuda et al.	A 5 V-Only 64K Dynamic RAM Based on High S/N Design	IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 5	846-854	October 1980
Masuoka et al.	Semiconductor Memory Device	U.S. Pat. No. 4,115,795		9/19/78
Masuoka	Dynamic Memory Device	JP 56-150857(A)		11/21/81
Miyasaka	Semiconductor Memory Unit	JP 57-111061(A)		07/10/82
Miyasaka	DRAM with Interleaved Folded Bit Lines	U.S. Pat. No. 4,476,547		10/9/84
Moeschwitzer	Semiconductor Memory Element with Two Field Effect Transistors	U.S. Pat. No. 4,507,758		3/26/85, filed 6/3/82
Nakano et al.	A Sub 100ns 356 kb DRAM	ISSCC 1983	224-225	February 1983
Nakano et al.	A Sub-100 ns 356K DRAM with Open Bit Line Scheme	IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 5	452-456	October 1983
Nakano	Semiconductor Memory Device	JP No. 55-162259(A)		12/17/80
Nakano	Dynamic Semiconductor Memory Device with Balanced Sensing	U.S. Pat. No. 4,545,037		10/1/85

Author	Title	Source	Page(s)	Date of Publication
	Arrangement			
Nakano	Semiconductor Memory Device	U.S. Pat. No. 4,384,347		05/17/83
Nakano et al.	Dynamic Random Access Memory Device	U.S. Pat. No. 4,484,312		11/20/84
Natori et al.	Semiconductor Memory Device	U.S. Pat. No. 4,199,772		4/22/80
Nishizawa et al.	Semiconductor Memory	U.S. Pat. No. 4,408,304		10/4/83
Ogura et al.	High Density Double Poly-Metal Bit Line Dynamic RAM Cell	IBM Technical Disclosure Bulletin, Vo. 24, No. 7B	3865-3867	December 1981
Ogura	Combined MOS/Memory Transistor Structure	U.S. Pat. No. 4,564,854		1/14/86
Ohta et al.	A Stacked High Capacitor RAM	ISSCC 1980		February 1980
Ohta et al.	Quadruply Self-Aligned Stacked High Capacitance Using Ta_2O_5 High-Density VLSI Dynamic Memory	IEEE Journal on Electron Devices, Vol. ED-29, No. 3	368-376	March 1982
Onishi	Dummy Cell Structure for MIS Dynamic Memories	U.S. Pat. No. 4,264,965		04/28/81
John G. Posa	Dynamic RAMS: Whate to Expect Next: A Special Report	Electronics	119-129	May 22, 1980
John G. Posa	NSC Forges Ahead with Triple-Poly RAMs	Electronics	42-43	June 30, 1981
John G. Posa	Late Entrants Star at Solid-State Parley	Electronics	41	January 17, 1980
John G. Posa	RAMs hit 512K production not in sight	Electronics	42, 44	March 13, 1980
V. Leo Rideout	One-Device Cells for Dynamic Random-Access Memories: A Tutorial	IEEE Transactions on Electron Devices, Vol. Ed-26, No. 6	839-852	June 1979
Rideout	MOS RAM with Implant Forming Peripheral Depletion MOSFET Channels and Capacitor Bottom Electrodes	U.S. Pat. No. 4,183,040		1/8/80
C.T. Sah	Evolution of the MOS Transistor - From Conception to VLSI	Proceedings of the IEEE, Vol. 76, No. 10	1280-1327	October 1988
Sakai et al.	Semiconductor Memory Device	U.S Pat. No. 4,355,374		10/19/82
Sakurai et al.	MOS Random Access Memory with Buried Storage Capacitor	U.S. Pat. No. 4,329,704		05/11/82
Salters	Semiconductor Device with Multiple Plate Vertically Aligned Capacitor Storage Memory	U.S. Pat. No. 4,460,911		7/17/84
Schroeder	Prospects for the 64K RAM - an outline of the problem	14th IEEE Computer Society International Conference	114-115	1977
Semiconductor Insights, Inc.	An Analysis of the NECuPD4164B 64Kx1 Dynamic RAM			October 1983
Shields et al.	Use of Polysilicon for Smoothing of Liquid Crystal MOS Displays	U.S. Pat. No. 4,382,658		05/10/83

Author	Title	Source	Page(s)	Date of Publication
Shimizu et al.	Semiconductor Memory Device	U.S. Pat. No. 4,612,565		09/16/86
Shimotori et al.	DRAM with PolySi Bit Lines and Added Junction Capacitance	U.S. Pat. No. 4,551,741		11/5/85
Shum	Electrically Erasable Read Only Memory	U.S. Pat. No. 4,257,056		3/17/81
F.J. Smith et al.	A 64 kbit MOS Dynamic RAM with Novel Memory Capacitor	IEEE Journal of Solid State Circuits, Vol. SC-15, No. 2	184-189	April 1980
W.H. Smith, Jr.	Vertical One-Device Memory Cell	IBM Technical Disclosure Bulletin, Vol. 15, No. 12	3585-3596	May 1973
Suguira	Insulated Gate Type Semiconductor Memory Device for Read Only Use	JP 58-16562		01/31/83, filed 07/22/81
Tanimura et al.	Method of Making Semiconductor Memory Device	U.S. Pat. No. 4,554,729		11/26/85
M. Taguchi and T. Nakamura	Double Layer Polysilicon Cells for Higher Density RAMs	FUJITSU Scientific and Technical Journal	129-146	December 1981
Taguchi et al.	A Capacitance-Coupled Bit-Line Cell for Mb Level DRAMs	ISSCC 1984	100-101	February 1984
Taguchi	Semiconductor Memory Device	U.S. Pat. No. 4,419,743		12/6/83
Taguchi et al.	A Capacitance-Coupled Bit Line Cell	IEEE Transactions on Electron Devices, Vol. ED-32, No. 2	290-295	February 1985
Taguchi	Semiconductor Memory Device	U.S. Pat. No. 4,635,085		1/6/87
Takemae	Semiconductor Memory Device and Process for Producing the Same	U.S. Pat. No. 4,513,304		04/23/85
Takemae	Semiconductor Memory Device and Fabricating Method Therefore	PCT Pub. No. WO 80/02624		11/27/80
Takemae	Semiconductor Memory Device	U.S. Patent No. 4,443,868		4/17/84
Takemae	A 1 Mb DRAM with 3-Dimensional Stacked Capacitor Cells	ISSCC 1985	250-251	February 1985
Takemae	Semiconductor Memory Device Having Stacked-Capacitor type Memory Cells	U.S. Pat. No. 4,754,313		1/28/88
Takeuchi	Manufacture of Semiconductor Device	JP 58-63158		04/14/83
Tashch, Jr.	High Capacity Dynamic RAM Cell	U.S. Patent No. 4,164,751		08/14/79
Thomas	Non-Destructive Read Out Field Effect Transistor Memory Cell System	U.S. Pat. No. 4,335,450		06/15/82
Tominaga et al.	High Performance 3 m MOS Memories	Hitachi Review, Vol. 30, No. 4	177-182	1981
Tsuchiya et al.	Semiconductor Memory Device	U.S. Patent No. 4,449,142		5/15/84
Wada	Integrated Circuit Memory	JP 58-155754		9/16/83
Wada	Integrated Circuit Memory	JP 58-155755		9/16/83

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EXHIBIT 3

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.
Before the Honorable Paul J. Luckern
Administrative Law Judge

In the Matter of CERTAIN INTEGRATED CIRCUITS AND PRODUCTS CONTAINING SAME	Investigation No. 337-TA-402

RESPONDENTS SAMSUNG ELECTRONICS CO., LTD AND SAMSUNG SEMICONDUCTOR, INC.'S IDENTIFICATION OF PRIOR ART FOR U.S. PATENT 4,352,724 ("'724 PATENT")

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EXHIBIT 4

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.
Before the Honorable Paul J. Luckern
Administrative Law Judge

In the Matter of CERTAIN INTEGRATED CIRCUITS AND PRODUCTS CONTAINING SAME	Investigation No. 337-TA-402

RESPONDENTS SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC.'S IDENTIFICATION OF PRIOR ART FOR '166 PATENT

LIST OF '166 PRIOR ART

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CERTIFICATE OF SERVICE

I hereby certify that copies of **MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT OF MOTION TO AMEND IDENTIFICATION OF PRIOR ART** was served this 7th day of April, 1998 as follows:

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