HYUNDAI SEMICONDUCTOR

HY5164

65,536 x 1-Bit Dynamic RAM

OCTOBER 1986

DESCRIPTION

The HY5164 is a high speed 65,536 bit dynamic Random Access Memory. Fast page mode has the features of fast usable speed, low power, and a typical soft error rate of less than 10 Failures In Time (FITs). The HY5164 is ideally suited for applications such as graphic display terminals, and any application where high performance is required.

FEATURING FAST PAGE MODE OPERATION

Fast page mode operation allows access of up to 256 bits at a 80 ns/bit rate with random or sequential addresses within a single row. Thus, a continuous data rate of over 12 million bits per second can be achieved. The HY5164 offers high performance with relaxed system timing requirements for fast usable speed. In addition, the fast $\overline{RAS}$ and $\overline{CAS}$ access times are compatible with high performance microprocessors without using WAIT state operation.

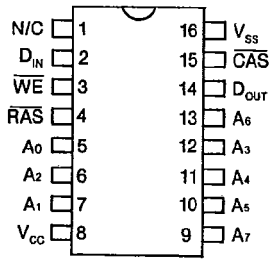
The HY5164 comes in either a 16-pin plastic or ceramic dual in-line package. All inputs, outputs and control signals are TTL compatible.

FEATURES

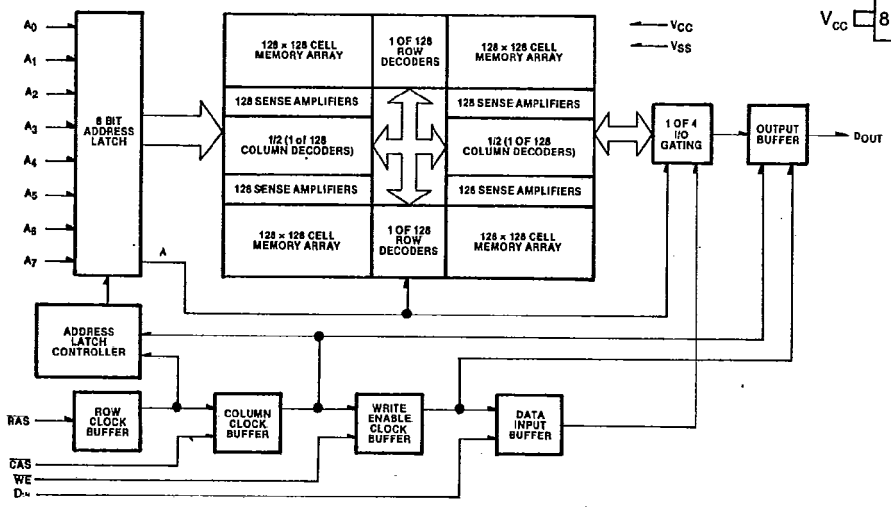
- ▲ CMOS Technology
- ▲ Power dissipation for the HY5164-12
  - — operating power 220 mW (max.)
  - — standby power, TTL 8.3 mW (max.)
- ▲ Refresh period 4ms/256 cycles.
- ▲ Typical soft error rate less than 10 FITs (0.001%/1000 hours)
- ▲ Fast page mode operation for a sustained data rate up to 12.4 MHz for HY5164-10

	HY5164-10	HY5164-12	HY5164-15
Maximum Access Time (ns)	100	120	150
Minimum Cycle Time (ns)	190	220	260
Maximum Column Address Access Time (ns)	65	80	95

PIN CONNECTIONS



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{CC}	POWER (+5V)
V_{SS}	GROUND

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ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	−10° to +80°C
Storage Temperature	Plastic −55°C to +125°C
Voltage on Any Pin except V_{CC} Relative to V_{SS}	−1.0V to 7.0V
Voltage on V_{CC} Relative to V_{SS}	−1.0V to 7.0V
Data Out Current	50mA
Power Dissipation	1.0W

NOTICE:
Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	SPEED	HY5164 Min.	HY5164 Typ.[2]	HY5164 Max.	UNIT	TEST CONDITIONS	NOTES
$\|I_{LI}\|$	Input Leakage Current (any input)				10	μA	$V_{IN} = V_{SS}$ to V_{CC}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State				10	μA	$\overline{RAS}$ at V_{IH}. $\overline{CAS}$ at V_{IH}. $D_{OUT} = V_{SS}$ to V_{CC}.	
I_{CC1}	V_{CC} Supply Current, Operating	−10		30	40	mA	$t_{RC} = t_{RC}$(min)	3,4
		−12		25	37			
		−15		20	32			
I_{CC2}	V_{CC} Supply Current, TTL Standby			1	3	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}, all other inputs ≥ −0.5V	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Cycle	−10		30	40	mA	$t_{RC} = t_{RC}$(min)	4
		−12		25	37			
		−15		20	32			
I_{CC4}	V_{CC} Supply Current, Fast page mode	−10		30	40	mA	$t_{PC} = t_{PC}$(min)	3,4
		−12		25	37			
		−15		20	32			
V_{IL}	Input Low Voltage (all inputs)		−1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)		2.4		$V_{CC}+1$	V		
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 4.2 mA	6
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −5mA	6

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and nominal supply voltages.
3. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max) is measured with the output open.
4. I_{CC} (max) is dependent upon the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{CC} (max) is measured within a maximum of two transitions per address input per random cycle, one transition per access cycle for Fast page mode.
5. Specified V_{IL} (min) is steady state operation. During transitions, the inputs may overshoot to − 2.0V for periods not to exceed 20 ns.
6. Test conditions apply only for D.C. characteristics. A.C. parameters specified with a load equivalent to two TTL loads and 100 pF.

CAPACITANCE[1]

$T_A = 25°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data In	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	7	pF
C_{OUT}	Data Out	—	7	pF

NOTES:

1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V}$$

with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

(See waveforms A to G)

SYMBOL	PARAMETER	HY5164-10		HY5164-12		HY5164-15		UNIT	NOTES
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RAC}	Access Time From $\overline{RAS}$		100		120		150	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		50		60		70	ns	5,6,7
t_{CAA}	Access Time From Column Address		65		80		95	ns	
t_{REF}	Time Between Refresh		4		4		4	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	80		90		100		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20		20		20		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	30	60	35	80	ns	8
t_{CSH}	$\overline{CAS}$ Hold Time	100		120		150		ns	
t_{ASR}	Row Address Set-up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	15		20		25		ns	
t_{ASC}	Column Address Set-up Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		20		25		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{OFF}	Output Buffer Turn Off Delay	0	25	0	30	0	35	ns	

NOTES:

1. All Voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms for the HY5164).
3. A.C. characteristics assume $t_T = 5$ ns.
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If $t_{RCD} > t_{RCD}$ (max) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
5. Load = 2 TTL loads and 100 pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max).
7. If $t_{ASC} < [t_{CAA}(max) - t_T]$, then access time is defined by t_{CAA} rather than by t_{CAC}.
8. t_{RCD} (max) is specified for reference only.
9. t_T is measured between V_{IH}(min) and V_{IL}(max).

A.C. CHARACTERISTICS (CONT'D.)

READ AND REFRESH CYCLES

(See Waveforms A,C,D,E and G)

SYMBOL	PARAMETER	HY5164-10		HY5164-12		HY5164-15		UNIT	NOTES
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read Cycle Time	190		220		260		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	150	75000	ns	
$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width (Read Cycle)	50	75000	60	75000	70	75000	ns	
$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	50		60		70		ns	
t_{RCS}	Read Command Set-up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	20		20		20		ns	10
t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	65		80		100		ns	

WRITE CYCLE

(See Waveforms B,C,F and G)

SYMBOL	PARAMETER	HY5164-10		HY5164-12		HY5164-15		UNIT	NOTES
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Write Cycle Time	190		220		260		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	150	75000	ns	
$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width (Write Cycle)	50	75000	60	75000	70	75000	ns	
$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	50		60		70		ns	
t_{WCS}	Write Command Set-up Time	0		−10		−10		ns	11
t_{WCH}	Write Command Hold Time	30		35		40		ns	
t_{WP}	Write Command Pulse Width	30		35		40		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		40		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		40		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	
t_{DH}	Data-In Hold Time	30		35		40		ns	

NOTES:

10. Either t_{RCH} or t_{RRH} must be satisfied.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the date out will contain the data read from the selected address. If none of the above conditions is satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (CONT'D.)

READ-MODIFY-WRITE CYCLE

(See Waveforms C and G)

SYMBOL	PARAMETER	HY5164-10		HY5164-12		HY5164-15		UNIT	NOTES
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	225		260		305		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	135	75000	160	75000	195	75000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	65	75000	70	75000	75	75000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		150		ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	30		30		30		ns	11
t_{AWD}	Column Address to $\overline{WE}$ Delay	35		45		55		ns	11

FAST PAGE MODE* CYCLE[12]

(See Waveforms E,F and G)

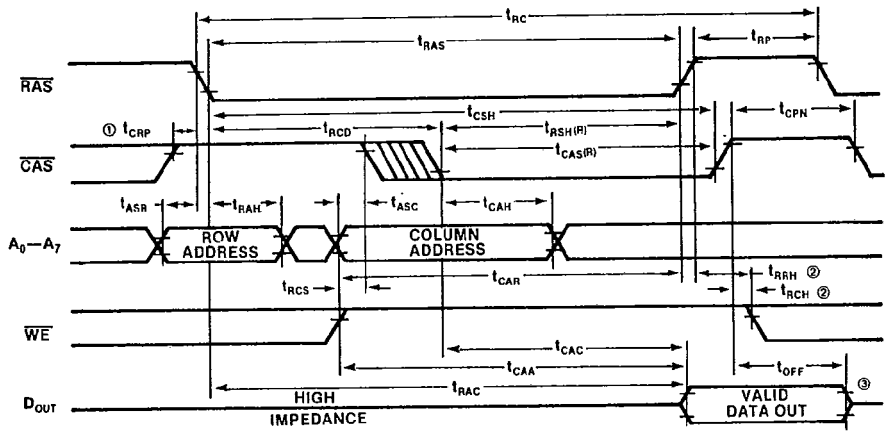
SYMBOL	PARAMETER	HY5164-10		HY5164-12		HY5164-15		UNIT	NOTES
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CAP}	Access Time From Column Precharge		75		90		105	ns	
t_{PC}	Fast page mode Read or Write Cycle Time	80		95		110		ns	
t_{CP}	Fast page mode $\overline{CAS}$ Precharge Time	20		25		30		ns	
t_{RPM}	Fast page mode $\overline{RAS}$ Pulse Width		75000		75000		75000	ns	
t_{PCM}	Fast page mode Read-Modify-Write Cycle Time	100		115		130		ns	

NOTES:

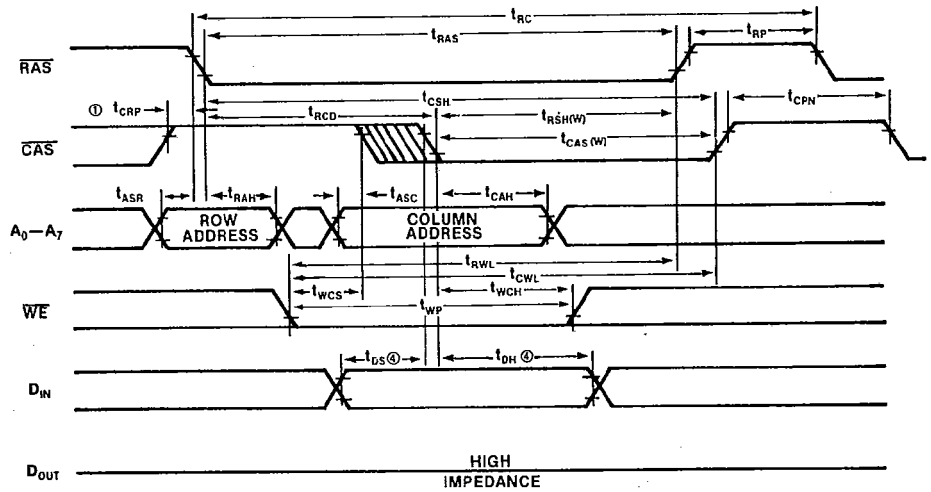
11. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain high impedance throughot the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If none of the above conditions is satisfied, the condition of the data out is indeterminate.
12. All previously specified A.C. characteristics are applicable.

WAVEFORMS

A. READ CYCLE



B. WRITE CYCLE

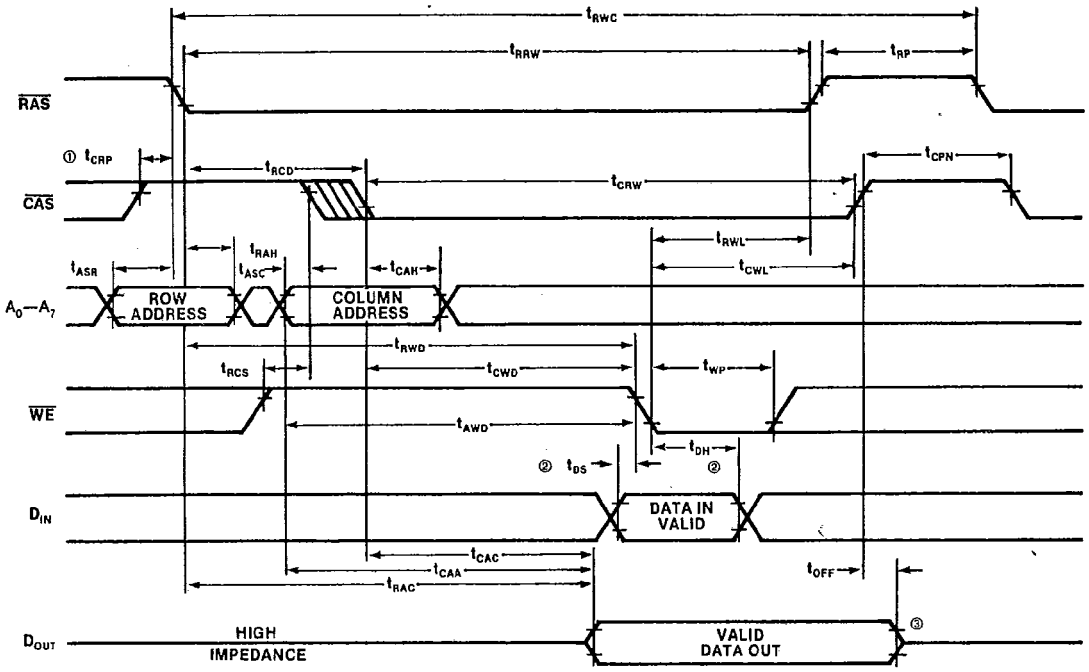


NOTES:

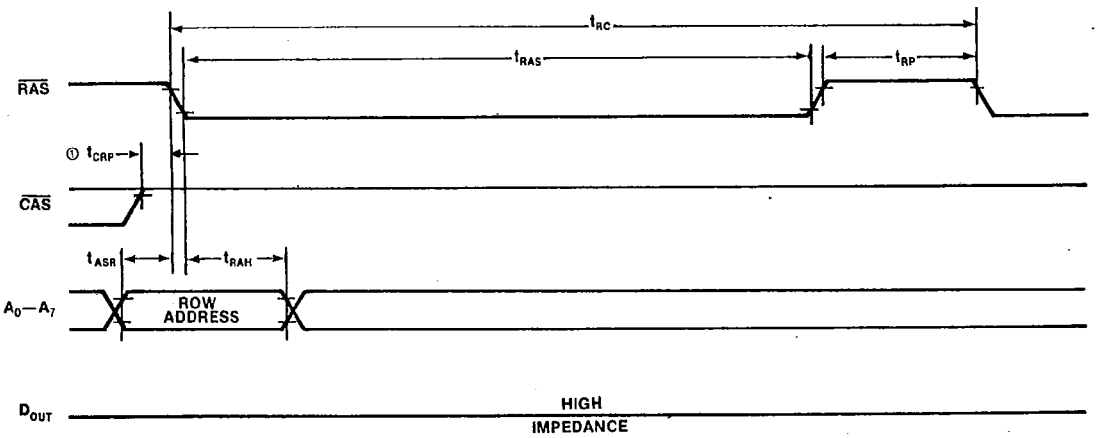
1. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
2. Either t_{RCH} or t_{RRH} must be satisfied
3. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
4. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

WAVEFORMS (CONT'D.)

C. READ-MODIFY-WRITE CYCLE



D. $\overline{RAS}$-ONLY REFRESH CYCLE

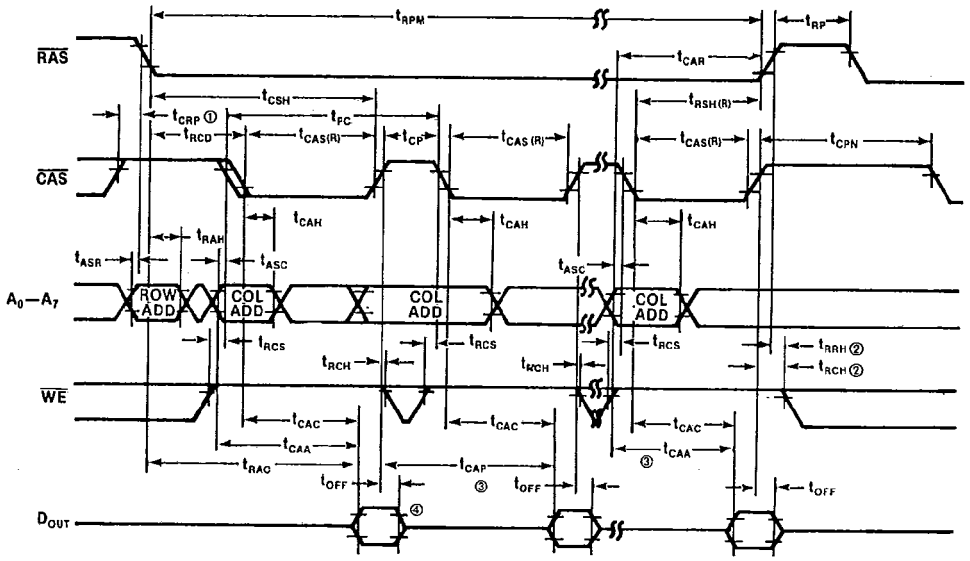


NOTES:

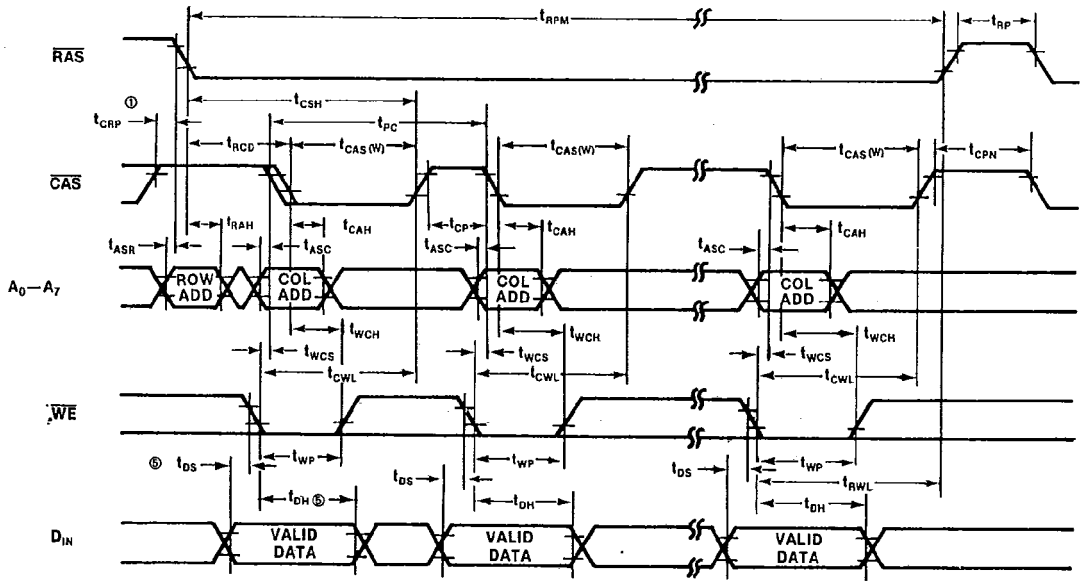
1. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
2. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
3. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (CONT'D.)

E. FAST PAGE MODE READ CYCLE



F. FAST PAGE MODE WRITE CYCLE

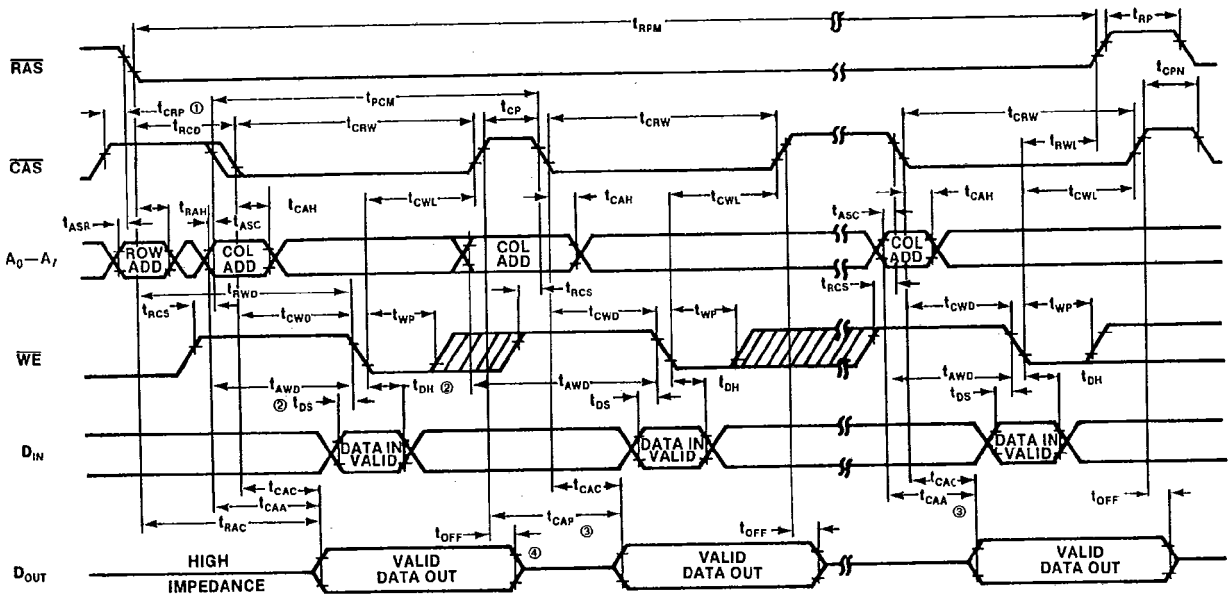


NOTES:

1. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
2. Either t_{RCH} or t_{RRH} must be satisfied.
3. Access time is t_{CAP} or t_{CAA} dependent, see Fast page mode discussion on pages 10 and 11.
4. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
5. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

WAVEFORMS (CONT'D.)

G. FAST PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES:

1. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
2. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
3. Access time is t_{CAP} or t_{CAA} dependent, see Fast page mode discussion on pages 10 and 11.
4. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

RAS/CAS TIMING

RAS and CAS have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by brining RAS and/or CAS low, must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle cannot begin until the minimum precharge time, t_{RP}, has been met.

READ CYCLE

A Read cycle is performed by maintaining Write Enable (WE) high during a RAS/CAS operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

WRITE CYCLE

A Write cycle is performed by taking WE low during a RAS/CAS operation. Data Input (D_{IN}) must be valid relative to the falling edge of WE or CAS, whichever transition occurs last.

REFRESH CYCLE

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A0 through A7) with RAS at least every 4 milliseconds. CAS can remain high (inactive) for this sequence. Any cycle, Read, Write, Read-Modify-Write, or RAS-only, will refresh the memory.

FAST PAGE MODE

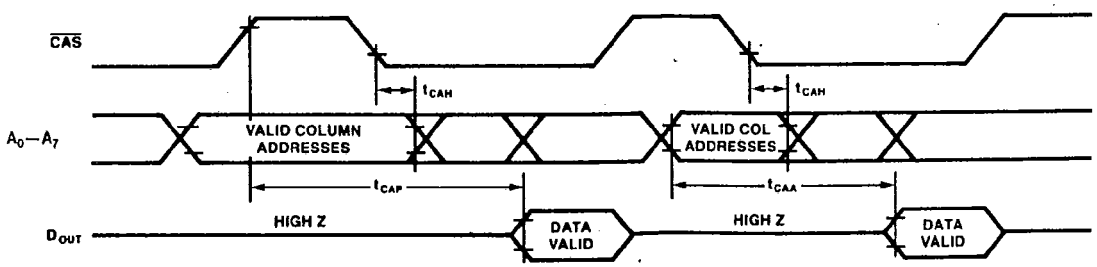
Fast page mode operation permits all 256 columns within the selected row of the selected device to be accessed at a high data rate. Maintaining RAS low while successive CAS cycles are performed, retains the row address internally, eliminating the need to reapply it. The column addres buffer acts as a transparent latch while CAS is high. Access begins from valid column addresses rather than from CAS, eliminating t_{ASC} and t_T from the critical timing path. CAS latches the addresses into the column address buffer and serves as an output enable.

During this operation Read, Write, or Read-Modify-Write cycles are possible at random or sequential addresses within the row. Following the entry cycle into Fast page mode operation, access time is t_{CAA} or t_{CAP} dependent. If the column addresses are valid prior to or coincident with the rising edge of CAS, then the access time is determined by the rising edge of CAS specified by t_{CAP} (see Figure 1.) If the column and addresses are valid after the rising edge of CAS, then the access time is determined by the valid column addresses specified by t_{CAA}. For both cases, the falling edge of CAS latches the addresses and enables the output.

Fast page mode operation provides a sustained data rate beyond 12MHz for applications that require high data bandwidth, such as bit mapped graphics. The following formula can be used to calculate the data rate:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255\, t_{PC}}$$

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

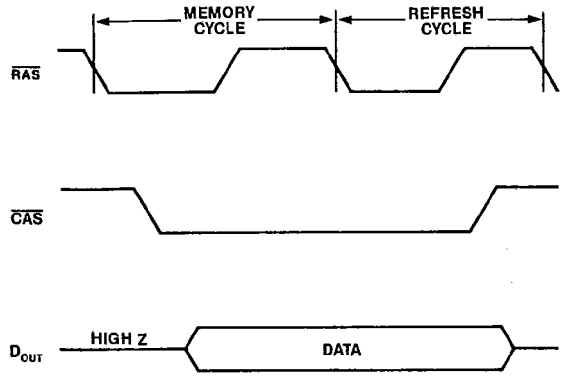


HIDDEN REFRESH

A standard feature of the HY5164 is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and, after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure 2).

This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability. The part will be internally refreshed at the row addressed at the time of the second $\overline{RAS}$.

FIGURE 2. HIDDEN REFRESH CYCLE



DATA OUT OPERATION

The HY5164 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

HY5164 DATA OUTPUT OPERATION FOR VARIOUS TYPES OF CYCLES

TYPE OF CYCLE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
Early Write Cycle	Hi-Z
$\overline{RAS}$-Only Refresh Cycle	Hi-Z
$\overline{CAS}$-Only Cycle	Hi-Z
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Delayed Write Cycle	Indeterminate

POWER ON

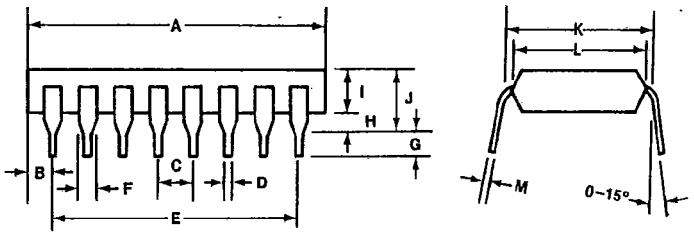
An initial pause of 100 μs is required after the application of the V_{CC} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock,such as $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms for the HY5164).

If $\overline{RAS}$=V_{SS} during power on, the device will go into an active cycle and I_{CC} would show current transients similar to those shown for the $\overline{RAS}$/$\overline{CAS}$ timings. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during power on.

PACKAGE OUTLINE

16 PIN PLASTIC

ITEM	MILLIMETERS	INCHES
A	19.05	0.750
B	0.635	0.025
C	2.54	0.100
D	0.457	0.018
E	17.78	0.700
F	1.524	0.060
G	3.302	0.130
H	0.508	0.020
I	3.302	0.130
J	3.81	0.150
K	7.62	0.300
L	6.35	0.250
M	0.254	0.010



ORDERING INFORMATION

HY5164 X XX

- XX: 10=100ns, 12=120ns, 15=150ns
- X: S=Plastic DIP 300MIL

HYUNDAI SEMICONDUCTOR

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