Intel740™ Graphics Accelerator P854 Hardware

Specification Update

Release Date:, July 1998

Notice: The Intel740™ graphics accelerator may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Order Number: 290622-002

Contents

Revision History

Date of Revision	Version	Description
April, 1998	-001	Initial Release.
July, 1998	-002	Added Component Marking Information for A-2. Added Errata 8 and 9; Specification Change 6; Specification Clarification 7.

Preface

This document is an update to the specifications contained in the *Intel740™ Graphics Accelerator Datasheet* (order number 290618), *Intel740™ Graphics Accelerator Software Developer's Manual* (order number 290617) and the *Intel740™ Design Guide* (Order Number 290619), and contains issues affecting all designs using the Intel740 graphics accelerator.

This document is intended for hardware system manufacturers and software developers of applications and tools. It contains Hardware and Software Errata, Specification Changes, Specification Clarifications, and Documentation Changes of the Intel740 graphics accelerator.

Identification Information

Component Marking Information

Intel740™ graphics accelerator device version:

Stepping	S-Spec	Top Marking	RAMDAC Free.	Notes
A-1	N/A	FW82740 Q622ES	203[1] MHz	Engineering Sample, FM Test
A-2	N/A	Intel740 FW82740SL292 Intel (M) (C) '97 Q631ES or Q632ES	203[1] MHz	Engineering Sample
A-2	SL292	Intel740™ or Intel740 FW82740 Intel (M) © '97	203[1] MHz	Production Material

NOTE:
1. 203MHz guaranteed by design

Component Identification via Programming Interface

The Intel740 graphics accelerator device stepping can be identified by the following register contents:

Intel740 Graphics Accelerator Device Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
P854 A-1	8086h	7800h	01h
P854 A-2	8086h	7800h	21h

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Summary Table Of Changes

The following table indicates the issues for Hardware and Software Errata, Specification Changes, Specification Clarifications, Temporary Restrictions, or Documentation Changes which apply to all currently available steppings and planned steppings. Intel intends to account for the outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Nomenclature

Errata are design defects or errors. Errata may cause the Intel740™ graphics accelerator device's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Builds determine the current version number of the Intel740™ Graphics Accelerator Software Driver Release (SDR) kit.

Specification Changes are modifications to the current published specifications. These modifications will be incorporated in future releases of the affected specifications.

Specification Clarifications describes a specification in greater detail or highlights complex design situations that may require implementation changes. These clarifications will be incorporated in future releases of the affected specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These clarifications will be incorporated in future releases of the affected specifications.

S-Specs are temporary exceptions to the published specifications and apply only to the units assembled under that s-spec.

Codes Used in Summary Table

X:	Errata, Specification Change, Specification Clarification, or Documentation Change applies to the given stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change or clarification does not apply to listed stepping.
Shaded:	This material is either new or modified from the previous version of this document.

ERRATA

NO.	P854 A-1	FUTURE PLANS	A-1 S/W Fix	A-2 Fix	ERRATA
1	X	NoFix			Deviations from Legacy VGA Configurations
2	X	NoFix			Perspective Divide of Textures
3	X	NoFix			Z Precision
4	X	NoFix	Driver v.2.5		Video Capture Color Correction
5	X	Fixed in B0	Driver v.2.6		Indication of Flip Completion
6	X	NoFix	Driver v.2.6		Monochrome Source BLT with Immediate Data
7	X	Fixed in B0		Driver v. 3.1, H/W workaround	Writes to A.G.P. in 2X Mode
8	X	NoFix	N/A	N/A	Vertical Scaling Implementation for Interlaced Formats
9	X	NoFix	N/A	Driver v.3.1	Horizontal Scaling Implementation

NOTE:
1. This S/W release and following releases contain the specified S/W fix.

Specification Changes

NO.	Document	PLANS	SPECIFICATION CHANGES
1	Intel740 Graphics Accelerator Design Guide	Doc	Reference Schematics: crystal oscillator value, IREFSET value
2	Intel740 Graphics Accelerator Datasheet, Intel740 Graphics Accelerator Software Developer's Manua	Doc	Textures in local memory, 3D Rendering to AGP memory
3	Intel740 Graphics Accelerator Datasheet, Intel740 Graphics Accelerator Software Developer's Manua	Doc	Wireframe Mode
4	Intel740 Graphics Accelerator Datasheet, Intel740 Graphics Accelerator Software Developer's Manua	Doc	Interlaced Monitor Support
5	Intel740 Graphics Accelerator Datasheet	Doc	4bpp in Extended Modes
6	Intel740 Graphics Accelerator Datasheet, Intel740 Graphics Accelerator Software Developer's Manual	Doc	Y Decrement Mode for Monochrome Blits

Specification Clarifications

NO.	Document/Build	PLANS	SPECIFICATION CLARIFICATIONS
1	Intel740 Graphics Accelerator Software Developer's Manual	Doc	Anti-aliasing artifacts using the Microsoft Direct3D* API
2	Intel740 Graphics Accelerator Software Developer's Manual	Doc	Supported Texture Formats
3	Intel740 Graphics Accelerator Datasheet	Doc	Panning of the Display Window
4	Intel740 Graphics Accelerator Datasheet	Doc	Overlay Implementation of Stride, Filtering while Scaling
5	Intel740 Graphics Accelerator Software Developer's Manual, Intel740 Graphics Accelerator Datasheet	Doc	Supported Scaling Modes
6	Intel740 Graphics Accelerator Datasheet	Doc	Setting of Coherency Bits
7	Intel740 Graphics Accelerator Datasheet, Intel740 Graphics Accelerator Design Guide	Doc	Hook-up for 1Mx16 SDRAM

Documentation Changes

NO.	Document Revision	Chapter	Page(s)	Documentation Changes
1	Intel740 Graphics Accelerator Datasheet	1	1-3	Architectural Overview: Figures 1-4 and 1-5
2	Intel740 Graphics Accelerator Datasheet	2	2-5	Signal Description: VMI Video Port and VMI Host Port, Table 2-5,
3	Intel740 Graphics Accelerator Datasheet	2	2-6	REFSET value, Table 2-6
4	Intel740 Graphics Accelerator Datasheet	2	2-7	GPIO4 Implementation, Table 2-8
5	Intel740 Graphics Accelerator Datasheet	2	2-8	Clock Frequency, Table 2-9
6	Intel740 Graphics Accelerator Datasheet	3	3-10	Register Description

ERRATA

1. Deviations from Legacy VGA Configurations

Problem: There are VGA deviations present in the Intel740 graphics accelerator which prevent total compatibility with the IBM VGA device standard. There are four VGA compatibility tests that do not pass on the Intel740 graphics accelerator, the tests are defined as follows:

1. A test to ensure the internal shifters are operating as expected. This test sets VLOAD/2 and VLOAD/4 and views the results.
2. A test that verifies that the full font glyph can be shown using large characters. This test displays a large character set (32 x 16) and sets various underline positions and cursor sizes.
3. A test that verifies the page select bit functions. This test places values into memory in different page bit configurations and verifies that those values ended up where they were expected.
4. A test that verifies that mode 0 and 1 are working. This test verifies memory is read/writable and tests each mode 0, 0+ and 0*.

Implication: Legacy DOS applications may potentially be affected.

Workaround: None.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

2. Perspective Divide of Textures

Problem: When calculating texture addresses for texture mapping of texels, the Intel740 graphics accelerator device performs perspective division on certain pixels within the polygon. All other pixel values use an approximation technique for the given polygon to calculate the texture address of the remaining pixels. As a result, the textures addresses generated by the approximation technique can deviate from the theoretical value.

Implication: This errata may cause those addresses calculated without perspective divide to have the pixel mapped to an incorrect texture value. This may result in visual anomalies.

Workaround: In order to remove most visual anomalies, applications can use Mip-mapped textures, as the error in the texture calculation will be so small that little real visual difference will be seen.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

3. Z Precision

Problem: There is a precision issue within the Intel740 graphics accelerator device for determining Z-values. This results in some objects having incorrect Z-values.

Implication: In certain instances, pixels behind another object can be seen in front of the object. This would occur if objects are located very close together in the z direction.

Workaround: There is no workaround in the Intel740 graphics accelerator software driver.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

4. Video Capture Color Correction

Problem: Video capture from CCIR601 format yields a luminance range of 16-235, while the 422-to-RGB conversion engine expects a range of 0-255.

Implication: Without the workaround, contrast is incorrect when video capture is displayed. Because the gamma correction table is used as part of the workaround, gamma correction is not available for video capture.

Workaround: The Intel740 graphics accelerator software driver corrects the contrast using the gamma correction table for display of video capture applications.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

5. Indication of Flip Completion

Problem: For flip operations between the front buffer and the render buffer, the Intel740 graphics accelerator device does not correctly indicate that the flip has been completed.

Implication: Flip completion must be detected using polling.

Workaround: The Intel740 graphics accelerator software driver version 2.6 uses the Front Buffer Info Packet command to poll the CR40 BIT 7 (EXTENDED START ADDRESS ENABLE) REGISTER.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section. Monochrome Source BLT with Immediate Data

6. Monochrome Source BLT with Immediate Data

Problem: When performing a monochrome source Blit with an Immediate Data command the Intel740 graphics accelerator will lock-up under the following conditions; when the last bit of the last QWORD of the monochrome source is used in the blit and the last pixel of the destination crosses a QWORD boundary at the destination. This condition occurs only when in 24 bpp (destination pixels will not cross QWORD boundaries for 8 bpp and 16 bpp). As a result, the H/W generates an erroneous request for an additional QWORD. The H/W then waits for an additional QWORD that does not exist causing the H/W to lock-up.

Implication: The Intel740 graphics accelerator will lock-up.

Workaround: The S/W workaround checks if the monochrome source size is a QWORD multiple (this indicates that the last bit of a QWORD may be used in the Blit) and that the destination is 24 bpp. If this condition is true, then an extra QWORD of data is sent with the real data, preventing the lock-up or any visual anomaly.

7. Vertical Scaling Implementation for Interlaced Formats

The steppings affected, see the Summary Table of Changes at the beginning of this section.

Problem: Vertical Scaling using the Intel740 device is limited to powers of 2 when capturing interlaced formats.

Implication: Interlaced formats requiring the Intel740 graphics accelerator scalar can only be scaled by a power of 2, e.g., 1/2, /1/4, 1/8.

Workaround: For interlaced formats such as TV in, the TV in decoder can be used for vertical scaling. Intel740 graphics accelerator production device drivers restrict vertical scaling for interlaced formats to powers of 2.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

8. Horizontal Scaling Implementation

Problem: The Intel740 graphics accelerator performs horizontal scaling in 16-pixel increments.

Implication: Per-pixel scaling is not available.

Workaround: The Intel740 graphics accelerator drivers ensure that horizontal scaling is performed in 16-pixel increments.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

9. Writes to A.G.P. in 2x Mode

Problem: During 2X mode writes from the Intel740 graphics accelerator device to A.G.P. memory, some glitches may occur on the AD strobe lines to the 440LX chipset.

Implication: If the glitches are high enough, corrupt data gets latched into memory and corruption appears on the screen, staying until overwritten. 440BX systems are unaffected due to better layout requirements on motherboards and better noise rejection on the input buffers. The software workaround causes the following: 1) Win9X* 2D benchmarks reduced approximately 20% on 2M local memory solutions, no effect on 4M/8M solutions, and 2) WinNT* 2D benchmarks will be similarly affected.

Workaround: Both hardware and software workarounds exist. The hardware workaround must be tested for robustness on individual designs.

HARDWARE WORKAROUND:

1. Quadruple spacing (20 mils for 5 mil traces, 24 mils for 6 mil traces) around strobes ADSTB_A, ADSTB_B.
2. on card include a 43 ohm resistor on ADSTB_A, ADSTB_B and SBSTB.
3. Run strobes over ground layer in board layout if possible.
4. Use pass/fail criteria testing provided by Intel to test robustness of the hardware workaround.

Software workaround:

1. Driver rev. 3.1 and beyond will prevent writes to A.G.P. from the Intel740 graphics accelerator device.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section. S/W workaround using Dynamic Texturing is being investigated.

Specification Changes

1. Reference Schematics

A 3.3V 66.666mhz crystal oscillator (50ppm) should be used for the Intel740 graphics accelerator device instead of 14.3MHz.

Pin 30 of the BIOS device should be pulled directly to Vcc (3.3V or 5V), not left as a NC.

IREFSET resistor value should be 511 ohms instead of 560 ohms

A 43 OHM series resistor should be added to the ADSTB_A, ADSTB_B and SBSTB lines.

Spacing around ADSTB_A, ADSTB_B and SBSTB should be four times the trace width (20 MILS for 5 MIL traces, 24 MILS for 6 MIL traces)

A 0 OHM series resistor should be added to the SBSTB line.

2. Textures in Local Memory, 3D Rendering to A.G.P. Memory

The Intel740 graphics accelerator device does not support placing textures in Local Memory or the rendering buffer in A.G.P. memory. The Intel740 graphics accelerator device only supports placement of textures in A.G.P. memory and of rendering buffers in Local Memory.

This limits screen resolution to 640x480 for 3D applications when using 2M of local memory, eliminating support for 800x600 resolution in 3D for 2M implementations. 2D applications are unaffected.

When using version 3.0 or 5.0 of the Microsoft DirectX API, the Intel740 graphics accelerator Direct3D driver will automatically place textures in A.G.P. memory and the render buffer in Local Memory, so long as memory locations are unspecified. In DirectX 5.0, if developers choose to explicitly specify A.G.P./Local Memory allocation, then textures must be located in A.G.P. memory with the render buffer in Local Memory.

This change will be reflected in the Intel740 Graphics Accelerator Datasheet and the Intel740 Graphics Accelerator Software Developer’s Manual.

3. Wireframe Mode

Wireframe mode on the Intel740 graphics accelerator does not implement Bresenham-type lines. Instead, the Intel740 graphics accelerator software driver uses line primitives to draw wireframes. As a result, wireframe objects may contain some extra pixels and may demonstrate a “whisker” effect, where the line extends slightly beyond the designated length. This change will be reflected in the Intel740 Graphics Accelerator Software Developer’s Manual and the Intel740 Graphics Accelerator Datasheet.

4. Interlaced Monitor Support

The Intel740 graphics accelerator device does not support interlaced monitors. This change will be reflected in the Intel740 Graphics Accelerator Datasheet and the Intel740 Graphics Accelerator Software Developer’s Manual.

5. 4bpp in Extended Modes

The Intel740 graphics accelerator device does not support 4bpp color in extended modes (800x600 and above). This change will be reflected in the Intel740 Graphics Accelerator Datasheet.

6. Y Decrement Mode for Monochrome Source Blit

The Intel740 graphics accelerator device does not support Y Decrement Mode for monochrome source blit. This change will be reflected in the Intel740 Graphics Accelerator Software Developer's Manual and the Intel740 Graphics Accelerator Datasheet.

Specification Clarifications

1. Anti-Aliasing Artifacts using the Microsoft Direct3D* API

The Intel740 graphics accelerator device implements antialiasing on polygon edges with wide alpha blended lines. Sharp corners of a rendered object may cause the lines to extend significantly beyond the bounding box extents calculated by the Direct3D API. These extents determine the area to be Blted from the render buffer to the display buffer, as well as the area of the buffer needing to be cleared before rendering the next frame. Therefore, since the Intel740 graphics accelerator device may render pixels outside of the extents due to its wide, alpha blended lines, Blts with the normal calculated extents will either not display all of the anti-aliased pixels, or the buffer area cleared will not remove all the rendered pixels. The artifact may be eliminated if the application enlarges the extents of the anti-aliased region before using them for Blts.

2. Supported Texture Formats

The current stepping and drivers for the Intel740 graphics accelerator device do not support palletized 1 or 2-bit formats, as well as the YUV texture formats.

3. Panning of the Display Window

The Intel740 graphics accelerator per pixel horizontal panning supports panning using the following granularities: 8 pixels for 8bpp, 4 pixels for 16bpp, and 6 pixels for 24 bpp.

4. Overlay Implementation of Stride, Filtering while Scaling

The Intel740 graphics accelerator supports filtering during scaling if stride (defined as the length of the data stream stored in a single line of memory) is less than or equal to 720 pixels. If stride is greater than 720 pixels, filtering is automatically turned off in the Intel740 graphics accelerator device drivers. As a result, intercast format will not be filtered by the Intel740 graphics accelerator device. The TV decoder should be used for filtering intercast format if needed.

5. Supported Scaling Modes

The Intel740 graphics accelerator device supports only Normal scaling mode. Overwrite scaling mode is not supported. Normal scaling mode is selected by setting bits 7:6 of the MR03 register to 0 0.

6. Setting of Coherency Bits

Some versions of system BIOS do not set the A.G.P. coherency bits correctly. These are bit 13, offset B0 in the 440LX chipset and bits 5 and 13, offset B0:B1, offset B1 in the Intel®440BX AGPset. This results in a system hang when running 3D applications. The Intel740 graphics accelerator device driver version 2.7 and beyond configures these bits correctly.

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Documentation Changes

1. Architectural Overview Chapter (Intel740 Graphics Accelerator Changes)

Issue: For Figures 1-4 and 1-5 (page 1-3), the bus from the 440LX AGPset to System Memory is labeled “2X AGP”. This should be ”Memory Interface Bus”.

Affected Docs: Intel740™ Graphics Accelerator Datasheet (order number 290618)

2. Signal Description Chapter (Intel740 Graphics Accelerator Datasheet Changes)

Issue: Changes to Table 2-5, Video Interface Signals (page 2-5).

VMI Video Port section of the table:
The “Type” column in the row for the Video Capture Data Port (VP[7:0]/VMIHD[7:0]) indicates that the signal is bidirectional (I/O). The signal type should be input only (I).

VMI Host Port section of the table:
The first sentence in the “Description” column for the VMI Host Data (VP[7:0]/VMIHD[7:0]) begins with “VP[15:8]”. This should be “VMIHD[7:0]”.
Also, the Type column indicates input only (I). This should be bidirectional (I/O).

Affected Docs: Intel740™ Graphics Accelerator Datasheet (order number 290618)

Issue: Table 2-6, Display Interface Signals (page 2-6): The resistor value for REFSET is indicated as 560 ohms 1%. The value should be 511 ohms 1%.

Issue: Table 2-8, General Purpose Input/Output Signals (page 2-7): “Description” column for GPIO4. The second sentence indicates that the interrupt functionality is triggered by a high-to-low transition. This should be a low-to-high transition.

Affected Docs: Intel740™ Graphics Accelerator Datasheet (order number 290618)

Issue: Table 2-9, Clock and Reset Signals (page 2-8): XTAL1 clock frequency is indicated as 66.667 MHz. This should be 66.6667 MHz.

Affected Docs: Intel740™ Graphics Accelerator Datasheet (order number 290618)

3. Register Description Chapter (Intel740 Graphics Accelerator Datasheet Changes)

Issue: Section 3.1.14, SID-Subsystem Identification Register (page 3-10): There is s a typographical error in the signal name. The description indicates that the strapping options are on VIP[15:0]. This should be VP[15:0].

Affected Docs: Intel740™ Graphics Accelerator Datasheet (order number 290618)

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