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CONTENTS

C.P.U. Board.....p 1

Memory Board.....p 4

PIO Disk Controller.....p 6

Video Board.....p 9

Video Serial Board.....p 12

Multi Port Board II & III.....p 13

Communications C.P.U.....p 14

Keyboard I.....p 16

Keyboard II.....p 17

CRT Monitor I.....p 18

CRT Monitor II.....p 19

Power Supply.....p 20

Appendix.....p 21

C.P.U. Board

Introduction

The C.P.U. board contains the main system processor, a startup monitor in EPROM, two serial ports and two parallel ports, 1K bytes of scratch ram and the interface circuits required to operate an S-100 Bus sytem.

sheet 1

Clock Generation

U1 and X1 form a crystal controlled oscillator with a basic 16MHz or 12MHz output on 4MHz and 6MHz boards respectivly.In a 4MHz system the 16Mhz output is divided by four through U2 to produce the 01 clock on pin 6 for the Z80A. In a 6MHz system the clock is dived by two only. This 6MHz clock is buffered further by U44 and a 220 ohm resistor before being applied to pin 6 on the Z80B. A phase generating circuit made up of a section of U3 and U1 combines clock output signals from U2 (4MHz) or U2 and U1 (6MHz) to produce the S-100 bus 01 clock pin-25. Additional inverters in U1 serve to buffer the 02 clock to the S100 bus pin 24.

C.P.U. Support Circuits

U6 is the Z80 C.P.U. The S-100 system control signals from the C.P.U. are generated by gates and flip-flops to produce the signals SINP, SMEMR, SOUT, SINTA, SM1, SHLTA, PWRT*, PMREQ*, RFC*, PSYNC, PWAIT, PDBIN, and PHLDA etc. (Refer to the appendix for signal definitions). The bus address lines are buffered and controlled as follows:

U7 buffers the upper address byte , U8 buffers the lower address byte.

The data bus is split into an input and output bus via U12 (input) and U13 (output). When RD* on the Z80 is true (pin 21 low) U12 will be enabled at pins 1 & 19 to input data to the C.P.U.

U4 combined with U46 produces the signals which synchronize the Z80 with any wait states detected by PRDY or XRDY. A detected wait state is clocked through U46-5&6 to hold the Z80 and produce PWAIT on the S-100 bus pin-27. The second half of U46 produces the PSYNC signal for bus cycle start identification.

The incoming control signals ADDDSB*, STDSB*, SSDSB*, CCDSB*, DODSB* and PHOLD* are generated by external devices to gain control of the system bus and perform Direct Memory Access or Multi-Processing etc. In addition PINT* and NMI* allow for maskable and non-maskable interrupts to be detected.

ROM, RAM and Board Initialization

When power is applied to the system, C31 charges up and thus the one-shot U22 is triggered. The output at pin 6 is used to reset the board UARTS (page 2). The output from pin 6 clocks Flip-Flop U23-3 which produces a low out of pin 6. This low propagates through U26-5 and U32-3 to bus pin 53 where it is used to disable the input buffer U12 via U5-5 from reading data on the system bus.In addition the low propagates through U5-13 so when the C.P.U. MEMR signal goes true on the first op-code fetch the output of U5-8 selects the System Monitor ROM U28. The C.P.U. reads the contents of the data bus which will be the first location in the selected ROM and executes the instruction decoded there. The instruction is a jump to the next instruction in the ROM itself, thus the C.P.U. will be directed to the system monitor on power-up. One of the first few instructions in the monitor is an output to port 0EH, which clears the output of flip-flop U23. By this action the Monitor ROM is shaddowed out of the first 1K of system address space. From now on all on-board ROM and RAM decoding is via the U24 and U25 chip decoders. U30 & U31 provide 1K bytes of RAM used for stack space and scratch area for the system monitor.

ROM/RAM Shadow Circuit

In order to allow a complete 64K RAM board to be used after booting in the system the on-board ROM and RAM must be switched out(shadowed). This is accomplished by holding U25-12 high. Initially on power up U23-9 is low to enable the on-board memory because it is cleared via POC* gated through U4-6. This output from U23-9 enables NOR GATE U15-8 so that any memory referance signal at U15-9 is gated through, then inverted by U32-2 to enable decoder U25. When the system boots it sends a WRITE PORT 0A signal to U23-11 which clocks a high to pin 9 and thus turns off the NOR GATE to the Memory Decoder. If it is desired to turn the decoder back on, a WRITE PORT 0B signal can be sent to U4-5, which propagates through to clear U23.

sheet 2

Port Control

Sixteen on-board ports are decoded via port decoders U18 (port reads) and U19 (port writes). U17 is used to select which one of 16 port groups is decoded. The output of U17 is selected such that it enables U18 & U19 for the first 16 ports. Thus ports 00 to 0F can be decoded.

UART Section

U33 takes the basic UART Clock and divides it further for input to U34 such that the baud rates from 19.2K down to 150 are generated for board use.

The UARTS U35 & U36 receive and transmit serial data via U40 & U41 from RS-232 sources. UART pins 26 to 33 accept output data from the C.P.U. for transmission while pins 5 to 12 provide received data for C.P.U. input. A section of U32, U4 and U27 combine to provide serial printer busy testing for U36 when it is used as a printer port.

Parallel Printer Ports

U39 latches data from the C.P.U. for a printer when the correct port number has triggered the latching AND GATE U4-11. This data is presented to the parallel printer cable along with a delayed strobe pulse via U38-9 (port 7) or U39-9 (port 6). The status of the printer(s) is read by enabling27 and reading the condition of the printer status line (BUSY in Centronics terms).

Memory Board

Introduction

The memory board consists of 64K to 256K bytes of dynamic RAM into which is loaded the Operating System and user programs for execution of various applications

Power On Initialization Circuit

When power is applied to the RAM board the initialization circuit made up of U18-3 to 6 applies the system POC* reset pulse to U13-1 to select BANK 0 and U17-11 & U6-13 to clear the Wait State Counter U73 & internal refresh pulse flip-flop U6. The memory board is now ready to accept CPU "reads" and "writes".

Address and Data I/O

A MEMR or MEMW signal at U3-2 or 13 will produce a high output to clock the Memory Cycle Flip-Flop U6. The Q output will switch high and enable the RAS decoder gates in U1. The address to the RAMS is available first via Address Buffer U23 which supplies the lower eight address bits required by the RAM address registers. U23 is enabled at first via a low in U17-3 . This address byte is strobed into the selected bank as determined via the decoded bank on U60 and this strobes in the RAS* data on RAM pin 4. 15 nanoseconds later this signal switches U10-8 low , thus enabling the upper Address Buffer U24 to apply address bits to the RAMS. After another 30 nanoseconds the CAS* signal propagates through to U10-2 & 3 to pin 15 on the RAMS. The address is now set up and data can be read or written to the selected location. If a read operation is in progress the valid data is presented to the Read Latch U19 for Bank 0 or U20 for Banks 1-3 and the data is latched in place . The latching occurs when the 250 (150) nanosecond delay line output drives U10-5 high which then clears U6 so that 50 (30) nanoseconds later the low on U10-10 propagates to U11-4 as a high , and then to U19 & U20-11 as a latched low. This latched data is read by the CPU when MEMR* and inverted PDBIN signals on U7-5 & 6 combine with the valid block selected signal on U4-8 to produce an enable output on U19 or U20-1. If the memory cycle is a Write then the input data from the Data Buffer U25 is written into the RAMS via the delayed MEMW signal propagating through U12-13 & 12 , U18-1 & 2 and U3-3,4,5, & 6 or U74 3,4,5 & 6 to pin 3 on the RAM chips.

Refresh Cycle

In the normal system state the RAMS are refreshed when a RFSH* pulse is detected on U12-5 & 6. This pulse switches U7-10 low which in turn sets up the RAS gates in U5 .It also activates the Memory Cycle Flip-Flop U6 via U3-1 & 12 , selects the refresh counter output by enabling U14-1 & 19 ,holds CAS* inactive via U10-1 & 3 and disables the address bus buffers via U10-9 & 8 and U17-1 & 3 . The Q output of U5 propagates through the common input on U1 to generate the RAS* refresh pulse on the RAMS. When RFSH* goes high the Refresh Counter is advanced via U18-8 & 9 and the cycle ends. In the case of a system wait state the Wait State Counter U73 is enabled via the wait state propagating through U22-1 & 2 , & U17-12 & 11. System clock pulses buffered via U22-11,10,5 & 6 drive the counter until the terminal count at pin 15 switches U17-8 low which in turn presets U6-9 high thus producing a RFSH* pulse in U7-8 . This pulse will last until the next clock count, and refreshing will appear the same as with a standard refresh cycle. When the wait state ends the counter will be cleared and the refresh stopped.

Board Control Options

Switch S2 and Decoder U60 allow the Memory Board to be configured as one of two boards in a system. It also allows individual 64K banks of memory to be enabled or disabled as required in some system configurations. In operation the board may be selected or de-selected by sending a board select code to port FFH. This port address is detected by U11 & U21 and combined with SOUT & A0 via U67-1,2,13 & 12 through U17 4,5 & 6 to latch a bank select code into U13 which in turn is decoded via U60. When the code is set, the memory bank will be enabled and it will occupy the system programmable memory space. For operating systems such as MP/M additional circuits function as follows. U58 & U59 decode the common-base memory address on a page decode basis. Any memory address at or above the selected page always switches in bank 0. This is accomplished via sections of U8, U12, U74 & U75 which detect the decoded page address and enable bank 0 output buffer U19 for memory reads. Switch SW5 is used to set the bank commonbase page.

PIO Disk Controller

Introduction

The floppy disk controller interfaces the system processor with flexible magnetic media. This media is used to maintain the a copy of O.S., application programs and user data and allow random access to any record on its' surfaces.

CPU Interface

The disk controller occupies port addresses 60H to 67H. The addresses are decoded using address bits A3 to A7 via U16-1,2,4,5 & 6 combined with U15-9 & 8 and U23-8,9 &10 . These integrated circuits provide the basic port decode for any address from 60H to 67H. This signal is combined with U27-17 & 13 and U17-5 & 6 , through U23-11 & 13 for ports 60H to 63H. When combined with U27-17 & 3 at U21-9 & 10 ports 64H to 67H are decoded. U27-8 & 12 and U27-6 & 14 buffer the addresses to U10-6 & 5 for accessing the registers in the FDCC . The output of U21-8 activates U10-3 to select the FDCC for the range of 64H to 67H . U24-9,10,11 & 8 provides flip-flop U25-2 with a logic high for 64H to 66H . All of these gates combine with other CPU signals to produce properly decoded read and write signals on the controller board. For reads the bus signals SINP and PDBIN are used , while for writes SOUT and PWR* are used. During a disk data transfere to or from the system PRDY is used to allow the controller to shift each byte from/to the disk. POC* resets the controller and system clock 02 is used to time PRDY states . Direct control of disk and side select functions , wait state enabling , density select and 5" or 8" selection is via Control Latch U31 . The state of this latch may be read via buffer U30 .

Disk Interface

Output signals to the disk drives are via gates U32 for drive and side select and gates U8 for write data and functional control. Data from the disks is via gates in U7, U9 , and U15 for read data , index pulses and drive status. The write data circuit consistes of gates in U23, U8 and pre-settable counter U2 and buffer U8 which process signals WD , LATE , EARLY and GT43 to produce proper precompensated write data . Data read back from the disk is shaped by single-shot U7 for presentation to the Disk Controller. To compensate for bit-shift in the read data stream a V.F.O. is used to generate the data clock window. U7 provides pulses to the V.F.O. whose width is dependent upon the disk size and density selected . This pulse width is set from latched conditions on the input of gates in U14 which provide a range of resistance values for the single-shot timing .

The output of the single-shot then controls U6 which also is controlled along with part of U34 by U5-7 . This circuit processes the data stream and V.F.O. output to produce the pump up/down signals for the operational amplifier U3 which forms an active low-pass filter.

The output from U3 controls the frequency of U13 , a V.C.O. circuit . U13's output is divided by U4 and selected by each half of U5 according to the disk size and density selected . U5-9 provides the final read clock for the FDCC .

Disk Controller Port Summary

63H controls U31 for direct drive select , side & size select ,density select & wait state enabling
64H FDCC command & status port
65H FDCC current track port
66H FDCC sector port
67H FDCC data I/O port and new track address register

Disk Controller Chip

The FDCC integrated circuit U10 is a dedicated microprocessor which handles the following functions:

disk head positioning
disk head load/unload
disk status checks
sector read and write with verification
single/double density operation with 5" or 8" disks
automatic write current reduction
track formatting

All of these functions are carried out under program control with minimum system software overhead .

Disk Read and Write Operations

A disk READ operation proceeds in the following manner. The controller is first accessed for selection of the proper disk , disk size , disk side , and density via port 63H . The desired track and sector are then entered into the FDCC and the command is issued to seek the track . The Disk Controller checks its current position , compares it with the desired track and steps in or out as needed to reach the track . When the system finds the controller ready, it enables the wait state generator via U16 and issues a read command . The WAIT EN signal on U16-9 & 10 removes the preset on U25-4 so that U25-2 provides clockable data . The FDCC begins its search for the correct sector and the system outputs a port 67H read command to accept the data .

The read signal SINP switches U23-4 via 5 and in turn it is inverted by U17-9 & 8 to clock a high out of U25-6 . This becomes data for U34-2 and this is clocked through to U32-11 & 10 on the next rising edge of system clock 02 . The low signal produced on U32-10 puts the CPU in a wait state so that input data is not read until the controller signals that it is valid . Once the controller has found the desired data field it shifts it in to produce a byte of data and then sets its DRQ signal high. This signal is inverted by U14-3 & 4 thus bringing the output of U16 low and presetting U25-4 so that the Q output goes high. This HI combined with a HI on U26-4 & 5 produces a RE* pulse on U10-4 . The zero on U34-2 is clocked throug to disable the wait state and the CPU is then able to input the data . This continues until the sector has been read at which time the CPU then checks the status register for any errors that may have occured during the operation . A disk WRITE operation uses the same circuits but with U26-1,2,13 & 12 used for write pulse generation .

Video Board

Introduction

The video board provides the system with a means of visual communication to the outside world.

Board Initialization

The Z80 executes the program stored in the Video PROM U16 (a 1K byte EPROM) which provides the instructions for a) initializing the CRT controller and the system bus and keyboard interface , b) interpreting commands sent to the board and c) controlling the type and location of screen attribute fields . When the system powers up the Z80 is reset by the power-on circuit consisting of U32-3 & 4 , U36-2 & 3 ,C13 , R8, and CR2 which applies a reset pulse to the Z80 U17-26 . This pulse also resets the Character Field Control Latch U25 The Z80 then begins execution of the program in U16 which directs it to clear the Interrupt and Keyboard Ready Flip-Flops (U37-6 & 8), then it initializes the CRT controller by setting the scan frequency , the number of scan lines per field , the number of characters per line ,the number of rows per screen , the type of scanning to be used , the starting position of the first character row , and the type of scrolling used. From this point the Z80 next clears the screen sets interrupt mode 1 ,sets the carry flag , enables interrupts and goes to a halt until further processing is needed.

I/O and Command Processing

A keyboard character enters via connector U13 and is latched into the Data Latch U35 when the keyboard strobe switches to a one thus clocking a high out of U37-9 which in turn clocks the Data Latch The character ready status on U37-8 is inverted and buffered to the bus via tristate gate U36-14 & 13 . The CPU may poll the state of this Keyboard Ready Buffer by reading port 0H . When this is done, the port decoder made up of U33 and U32-8 & 9 puts a high on U31-3 , while address A0 puts a low on U31-13 . At the same time SINP inverted through U32-13 & 12 enables U31 and PDBIN inverted through U32-11 & 10 provides the data to be decoded on U31-11. The data is routed through as a low on U36-15 , thus enabling the outputs to be read for a status check . When the Keyboard Ready Buffer is high the system is signaled that a character is available for inputing from the keyboard. This input routine does not require any response from the Z80 on the Video Board . When the system checks status to output a character to the video board it reads the state of U36-11 . A high on this gate indicates that the Z80 is ready to service interrupts so that a character may be sent to the video board.

The CPU then writes a character to the video port 1H . The PWR* signal buffered and inverted by U32-1 & 2 places a high on U31-1 , while the SOUT signal inverted by U32-5 & 6 puts a low on U31-2. This combines with U31-3 & 13 switched to a high to route a low to U31-4 which via U27-3 & 4 allows the data into U34 . When the write cycle ends U31-4 switches high thus holding the data in U-34 and setting the Keyboard Ready Flip-Flop U37-6 to a low which interrupts the Z80. Upon receiving the interrupt the Z80 jumps to location 38H and begins executing the processing program . It checks for a completed service routine then inputs the latched character from U34 while clearing the Interrupt Flip-Flop . The character is checked to see if it is a control character. If not is is put in the next screen location ,the cursor position is updated and any necessary scrolling is done before returning to a halt . If the character is a control type it is checked against a table and the appropriate control function is executed before returning to a halt condition .

The CRT controller , U18, is accessed by the Z80 for I/O functions at the following ports :

80H horizontal line count
81H interlace mode , horizontal sync width and delay
82H scans/data row , characters/data row
83H skew bits , data rows/frame
84H scan lines/frame
85H vertical data start
86H last displayed data row
88H read cursor line address
89H read cursor character address
8AH reset
8BH upward scroll
8CH load cursor character address
8DH load cursor line address
8EH start timing chain

Once the controller has been initialized it carries out the functions of providing video scan signals , and character data for the screen by controlling the display of characters from the video RAM . To do this the controller shares the internal data bus with the Z80 by using the BUSRQ* and BUSAK* lines on the Z80. U19-1,2 & 3 control the manner in which the Z80 gives or takes control of the bus. On power up the power-on circuit clears all port 10H outputs low so that U19-2 gives the Z80 control of the bus. This allows the Z80 to initialize the CRT controller and enter the main program sequence . When a clear screen command is given this gate is again used to allow a rapid clear sequence and in addition U25-9 is set high to blank the screen during this operation to keep clutter off the screen.

After initialization U25-16 sets U19-2 high so that the CRT controller takes command of the bus via BUSRQ*. If the Z80 needs the bus to process an interrupt it may only have it during screen blanking pulses so that no interferance is noted on the screen. The BUSAK* signal also selects the address source of the RAM via U7, U8 & U9-1. When these pins are low the CRT controller has the RAM.

Attribute Field Control

U25 and bit 7 in the RAM determine the modifications to the display such as reverse field , underlining , half intensity etc. The control character is checked for attribute type and the appropriate bit is set on the U25 latch. The characters associated with that field are flagged by bit 7 (high) so that during character shift-out from in U24 the flag bit sets U30-5 high , thus enabling the gates to pass the field . Blinking fields receive an on/off signal from U12 which divides the V SYNC signal from U23-6 to a slower rate.

Charcter Generation

As the CRT controller scans the screen it accesses the character for each location from video RAMS U3, U4, U5, and U6. The character is put on the bus and clocked through U15 to address lines on the Character Generator U14. Each character dot row pattern is accessed by the controller with its R0 to R2 outputs. This selects the output data which is loaded into the shift register U24 and then serially shifted out to the mixing circuits. These circuits combine the characters with attribute functions , screen blanking and a composite output to provide final data for the CRT screen.

Clock Generation

Gates U2-10 & 12 with components C3,C4 ,R3,R4 and the 14.4 MHz crystaL Y1 make up the basic clock circuit. This signal is buffered through U2-1 & 2 for the character dot clock on U24-2. Divider U1 next divides this clock to produce the character load clock fron pin 11 and the Z80 clock from pin 13.

Video Serial Board

Introduction

The serial board enables the standard system video controller board to operate as an ascii terminal. It may also drive a slave printer from an optional connector.

Basic communications is via EIA receiver U2-3 into the board and EIA driver U1-3 out of the board. This I/O traffic flows through UART U3. Keyboard data may enter from one of two socket types (SKT 2A & 2B) into pins 26 to 33 of the UART. The keyboard strobe toggles U3-23 so that keyboard data is written into the UART transmit register. This data is converted to a serial stream and sent to the system via U1-3. Incomming data is converted to parallel form and shiffted into the 64 byte FIFO U5 & U6 via U3-19 being clocked by U8-5. U8-8 next resets U3-9 via a low to U3-18. Data quickly propagates to the end of the FIFO where the signals OR from U5-14, SCRN RDY from J1-41, and U15-8 indicate that the C.R.T. board is ready to accept data. This condition sets a logic zero at U7-12. The next clock on U7-11 sets U7-8 hi and thus address A0 is set to a one. The next clock pulse at U7-3 sets SOUT hi and PWR* low. This writes the data into the C.R.T. data register, so that it may be processed and written to the screen. In the case of a 'bell' charcater being received, the C.R.T. board strobes J1-21 so that single-shot output U16-6 provides about 4 volts input to the bell transducer for .5 seconds.

Baud rates for the UART are selected via a BCD encodeing thumb wheel switch connected to SK4. The BCD value at U13-9,10 & 11 gates one of eight clock rates out pin 5 to the UART clock pins 17 & 40. A 3MHz clock from the C.R.T. board enters at J1-25 to provide board control clocks and a basic timing reference fo the baud rate divider circuits. U9A & U9B provide clock outputs of 19.2K baud and 9600 baud. U10 further divides the 9600 baud clock for rates from 4800 baud down to 300 baud. U11 and U12 are used to generate a 110 baud clock.

Data for a parallel printer is buffered through U14. The data into the printer is controlled by enabling or disabling the strobe circuit U16. U16-11 is controlled by the C.R.T. board at J1-64. When this bit is hi the printer receives a strobe signal. For serial operation J1-64 is inverted by U15-6. This enables the tri-state buffer U17 so that all received data from U2-3 is switched through EIA level generator U1-6.

Multi Port Board II and III

Introduction

The MPB consists of seven serial communications ICs to enable operation of remote consoles and printers.

The MPB interfaces to the system at the processor level. It does this via a 40 pin male header that plugs into the C.P.U. 40 pin expansion socket. This socket has all signals wired in parallel with the Z80. In addition J3 is connected to the C.P.U. board in order to draw +5, +12 & -12 volts d.c., and provide a signal EXT*. EXT* simply indicates to the C.P.U. board that a UART on the MPB has been selected for a read or write operation, and therefore data buffers on the system bus are disabled.

U24 is used to decode two groups of sixteen ports for addressing the MPB circuits. U13 & U14 are used to read/write one group and U15 & U16 are used to read/write the second group. U8 provides buffering for the lower four address bits to the port decoders U13 to U16. U11-1,2 & 3 provide port read strobes, and U11-4,5 & 6 provide port write strobes. U12-1,2 & 3 combines port read/write pulses with U11-9 & 13 group decoder pulses so that U33-1,2,3,4 & 6 generate a valid EXT* signal for all possible ports decoded on the MPB. U35-12,13,11,1,2 & 3 and Spare-4,5,& 6 enable U34 for reading the status port of any UART. U12-12,13 & 11 and U35-9,10 & 8 and U29-13,12 & Spare-9,10 & 8 enable U1 for reading the data from any UART. Each UART has three port address strobes assigned to it. The even strobe (eg: 12RD) is used to access the status register of the selected UART and determine if it is ready to transmit data or if it has received data. The two odd strobes (eg: 13W & 13R) are used to write data to the UART or to read received data from the UART. Serial I/O data is sent/received via an EIA driver or receiver at pins 25 and 20 on each UART. In addition MPB IIIs have a BUST* handshake line which is ANDED with the TBE (Transmit Buffer Empty) status so that a slave printer may be connected to the remote console without loss of data during form-feeds etc.

U30, U31 & U32 provide baud rate clock generation for rates from 150 baud to 19.2K baud. The desired rate is selected by a jumper wire from the UART clock inputs to the clock source. In addition U9-5 & 6 provide a selected baud rate and/or 300 baud to U23 by gating clocks from U10-3 or 6.

Connections to remote consoles are via a 50 conductor cable connected to J1. This cable usually connects to an I/O board containing up to 10 DB25 pin connectors. Provision for two parallel printer connections are found on the standard I/O board as well (P5 & P10).

Communications C.P.U.

Introduction

The communications C.P.U. board consists of a standard C.P.U. card with two input and two output 8-bit latches on the system bus. Internally the board may operate in a polled of interrupt mode.

Buss Interface

U1 is used to buffer one byte of data to be read by the system processor (data received from a remote site). U3-13 & 11 and U4 provide 8 bits of status information for the system processor. U5 holds data written by the system processor (data to be sent to a remote site). U7 holds commands written to the Com. Board for subsequent execution. U8 provides 4 decoded ports (2 read & 2 write ports) for the system processor to send/receive data as well as status & commands to the Com. Board. U9 decodes 8 ports for internal use on the Com. Board. U3-5,7 & 9 buffer the state of flip-flops U2 & U6 so that the Com. Board can determine when a bus I/O request is pending or completed.

C.P.U. Mods

U35 along with U40 & U41 provide the serial link to a local modem. U39-18 is used to latch a Request to Send bit out to the modem interface via U32-10 and RS 232 driver U41-8. Data for transmission is flagged valid when TBE on U35 is true along with Clear to Send and Data Set Ready from the modem. This state is buffered by U27-6 and may be tested by reading port 4. A block of data buffered by the Com. Board may then be strobed into U35 by writing to port 5. The data is converted to serial form and sent out via U35-25 to U41-3. Data received from the modem is input to U40-1 and converted to TTL levels at U40-3 for serial input to U35-20. U25 and U24 provide the memory address decoding required to access the Com. Board PROM and Read/Write memory.

Operation

The control program in prom runs in a loop checking for a command sent from the system processor. When a command is written into the command register it clocks U6-3 and sets output 6. This is read by the control program when it reads U3-5. The control program then checks the command list to determine the action requested by the system. If data is to be sent to the modem the control program next loops to read data bytes written into U5 as indicated by U3-7 each time a write to that latch sets U2-8. Each byte read is placed in a buffer in the Com. Board RAM until an End Of Block byte is read in. At that point the control program sets Request To Send true and waits for the modem to respond. When the modem is ready the entire block of data is transmitted out. If data is to be read from the modem the control program loops on the modem data received port and reads in each byte as it is received.

The modem data is placed in a separate input buffer until an EOB character is received. The control program then sets the Message Received bit true in U4 and goes back to the command check loop. When the system requests the data be sent to the system bus the control program writes it into U1 a byte at a time until the EOB character has been sent out. The control program then goes back to the command test loop. During all phases of data I/O the control program checks for an unconditional abort command from the system. This enables the system to gain control of the Com. Board at any time and bring to a stop any operation that may otherwise hang the board in a loop.

Keyboard I

Introduction

The keyboard employs a highly developed capacitive contact encoding system which reduces to a minimum the chance of errors or downtime for the part of the system which receives the direct "human-entered" instruction.

Operation

The heart of the keyboard is a keyboard controller chip U7. This circuit transmits key scanning codes on outputs X0 to X14. These pulses apply a voltage to the keyboard column pads located on the circuit board under each key. Outputs YA to YC select the keyboard row sensors connected to U12 . When a key is depressed it will be detected when the proper scan code and select code produces an output on U12-3. U11 shapes the detected pulse and delays the sensing of the next one in order to provide keyboard debouncing. The output of U11-2 informs the controller that a key has been detected so that the controller may construct the proper ASCII code on output D1 to D8 and generate a strobe pulse on the STB/AKD pin. U6 which clocks bit six out of its Q output is used to generate the control character codes when STB/AKD clocks pin 3 at the control character-set time. Two special keys produce modifications to the keyboard controller ASCII code. TTY LOCK (indicated by the controller output ALI which turns on a LED) when activated will suppress lower case output from the keyboard. The shift lock key (indicated by SLI for turning on its LED) will hold the keyboard output in shifted character mode while it is active. The ASCII output and strobe pulses are buffered and also duplicated again but in inverted form by gates in U1, U2, and U3. This provides both active high and active low data to suit varios interface needs. The actual strobe pulse is shaped by one half of U10. If the key is held depressed U7-39 will stay low and this will enable U8 once the Half-Second single-shot U10 times out. After time out CR3 will be held high by U9-2 , thus enabling the timing elements in U8. When enabled U8 will send out a stream of pulses which activates the Strobe One-Shot every tenth of a second. The translate ROM U14 and special key circuit U5 are not used in the standard system.

Keyboard II

Introduction

This keyboard consists of a single chip MPU, a control program in EPROM and a few interface chips for decoding a spring switch keyboard.

Operation

U5 receives a clock from the crystal controlled oscillator U1 which is divided and made two-phase by flip-flop U9. U7 buffers and latches the program address for EPROM U8. The program instructs the MPU to activate and scan the keyboard matrix. U2 and U3 each provide matrix drive for 8 keyboard lines. P11 to p17 on U5 read the 16 lines driven by U2 and U3. When a depressed key is detected the MPU will use the scanned matrix value and fetch the corresponding ASCII code from control prom U8. This acsii code is then written into U6. P24 on U5 generates a keyboard strobe bit so that external logic can aquire the keyboard data.

CRT Monitor I

Introduction

The Cathode Ray Tube Monitor (CRT) includes the circuits that provide the display tube raster and the video tube itself. In the System a composite signal is used to provide the deflection and video information on one signal line.

Operation

A single +12 volt input provides all the power for the Monitor P.C. Board. Composite video is input on J1-8 and fed to the input of U2-17. This integrated circuit separates the horizontal, vertical and video pulses and sends them to other circuits for further processing. The horizontal pulse goes to U4-2 where it is used to lock the free-running horizontal oscillator inside this package. U3 acts as a feedback amplifier in this circuit to maintain frequency locking. The horizontal output on pin 16 is fed to Q4 where it is amplified and fed to the flyback circuit via T2 and Q3.

The flyback transformer generates the high voltage needed by the CRT anode for electron beam deflection and also other voltages used for the accelerator and focus grids in the neck of the tube. The output at point 11 goes to the horizontal deflection coil in order to control the sweep of the beam across the face of the screen.

The vertical signal is fed to U1-8 where it is amplified for driving the vertical deflection coil connected to points 8 and 9. This circuit also includes potentiometers R18 and R22 for making adjustments to the vertical size and linearity. The video data, that is the characters to be displayed on the screen, is buffered and amplified by Q2 and fed to the CRT modulation grid. It comes from the Video P.C. Board via points 3 and 4.

C.R.T. Monitor II

Introduction

This video monitor is driven by TTL signals to produce a raster display from the C.R.T. controller.

Operation

Operation is very similar to the first unit. Vertical drive at P100-9 is processed by U201. This one circuit controlls vertical size, linearity and hold as well as providing amplification of the signal in order to drive the vertical yoke. Horizontal drive at P100-1 is shaped by Q103 and applied to U301 which determines the horizontal position of the scan field on the screen. U302 buffers the horizontal pulse and drives the high voltage drive transistor Q302. This driver activates the flyback transformer T301 and provides horizontal deflection for the Horizontal yoke. The high-voltage side of the flyback provides the 11.4K volts needed for anode potential. Also voltages are generated to control the focus and video level on the phosphor. Video at P100-8 is shapped by by Q101 & Q102 and sent to the C.R.T. gun.

Power Supply

Introduction

The linear power supply is a compact unit with the electronics built on one printed circuit board. It uses a combination of fixed and adjustable integrated circuit voltage regulators to control the current and voltage supplies for the system logic boards and disc drives.

Operation

Power Transformer T1 has a dual primary which allows operation from 115 or 230 VAC supply lines. The outputs from T1 supply the necessary AC voltage levels required by the various rectifiers and regulators to produce the following DC output voltages:

+5V	to all logic boards and floppy disc drives
-5V	to floppy disc drives
+12V	to all logic boards
-12V	to all logic boards
+24V	to the floppy disc stepper circuits
+18V UR	to the CRT +12V regulator circuit

BR1, BR2, and D13 & D14 provide rectification for each of the secondary windings with the associated capacitor network for BR1 and C8, C10, C11, C12 and C14 providing the initial filtering for input to the regulators. U1 regulates the +24V output with Q1 acting as a current amplifier. R1 provides current output information for U1-3 so that the maximum current level set by R11, and R14 will not be exceeded. C1 and Q4 provide frequency compensation which along with D16 provides protection from the typical inductive load of a stepper motor. U2 and U3 are arranged in similar circuit configurations to that of U1 for control of the +12 and +5 volt supplies. U4 and U5 are three- terminal regulator circuits which provide -12 and -5 volts for system use.

Overvoltage protection is provided by D6 and Q5 for the +5V and D4 and Q6 for the +12V. If the output voltage exceedes the sensing zener voltage in each circuit a voltage drop appears across the associated resistor and this in turn triggers the SCR which shunts the output to ground.

APPENDIX

System Bus Signals

pin #	name	function
1	+5v	ttl logic supply
2	+12v	logic supply
3	XRDY	wait state # 1
4	NMI*	z80 non-maskable interrupt
12	NMI*	alternate connection for pin 4
13	PWR FL*	optional power fail
18	STAT DSB*	disable 8 status signals
19	CCDSB*	disable 5 command/control
22	ADD DSB*	disable 16 address
23	DO DSB*	disable 8 data out
24	02	cpu clock 2
25	01	cpu clock 1
26	PHLDA	cpu transfers bus control
29	A5	address bit 5
30	A4	address bit 4
31	A3	address bit 3
32	A15	address bit 15
33	A12	address bit 12
34	A9	address bit 9
35	DO1	data out bit 1
36	DO0	data out bit 0
37	a10	address bit 10
38	DO4	data out bit 4
39	DO5	data out bit 5
40	DO6	data out bit 6
41	DI2	data in bit 2
42	DI3	data in bit 3
43	DI7	data in bit 7
44	SM1	op-code fetch
45	SOUT	data to output device
46	SINP	data from an input device
47	SMEMR	data from memory
48	SHLTA	show a halt condition
49	CLOCK*	optional 2mhz clock
50	GND	bus power return
51	+5	ttl logic supply
52	-12v	logic supply
66	RFC*	z80 refresh signal
67	PHAN*	phantom control
68	MWRITE	data to memory
72	RDY	wait state " 2
73	PINT*	primary interrupt request line
74	HOLD*	bus command control signal
75	RESET*	reset system signal
76	PSYNC	new cpu cycle start
77	PWR*	valid write data

System Bus Signals (cont)

pin #	name	function
78	PDBIN	data input request
79	A0	address 0
80	A1	address bit 1
81	A2	address bit 2
82	A6	address bit 6
83	A7	address bit 7
84	A8	address bit 8
85	A13	address bit 13
86	A14	address bit 14
87	A11	address bit 11
88	DO2	data out bit 2
89	DO3	data out bit 3
90	DO7	data out bit 7
91	DI4	data in bit 4
92	DI5	data in bit 5
93	DI6	data in bit 6
94	DI1	data in bit 1
95	DI0	data in bit 0
96	SINTA	strobe interrupt device
99	POC*	power on clear (reset system)
100	GND	bus power return