REVISIONS				
REV		DESCRIPTION	INC BY	APPROVAL & DATE
A		ENG REL	GB	Hannan 12-5-75
B		12 μ SEC WAS 8 μSEC, A18-8 WAS A18-9, REVISED PULSE	D.T. 2-24-76	Hannan 2.25.76

DWG. NO. 19025-001

MODEL NO. FIRST USE 142	NEXT ASSY FIRST USE —	

DRAWN	HANNAN	
CHECK		
APPD		
APPD		

CALCOMP
CALIFORNIA COMPUTER PRODUCTS, INC.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .XX .XXX
ANGLES ±

Read Decoder and PLL Theory of Operation
(Ref. Schematic Dwg. #15967-001)

SCALE	SIZE	DWG NO.	REV.
	A	19025-001	B

DO NOT SCALE DRAWING

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28-55

1.0 GENERAL

This memo presents one approach to the recovery of information from a rotating magnetic medium.

Commonly used techniques for recording high density information are Frequency Modulation (FM) and, Modified Frequency - Modulation (MFM).

FM Writes:
1. Transition at the end of every bit cell.
2. Transition in the middle of every "one".

MFM Writes:
1. Transition in the middle of every "one".
2. Transition at the end of a zero if the following bit is a zero.

The advantages of these methods are numerous but the most important is the high data rate for a given bandwidth.

During play back of raw data from a disc one observes distortion and frequency variation of the data. One form of frequency variation (slow) is attributed to changes in disc speed (RPM). This change in RPM can be as high as ±5% from drive to drive. Instantaneous frequency shift (fast) or "peak shift" caused by the head/disc interface is another problem to be reckoned with, when trying to recover data.

1.0 Continued

A Phase Locked Loop (PLL) is a scheme that compensates for slow frequency and phase variation and doesn't respond to fast changes, by following slow variations a PLL predicts (from a time average of a previous cell) the beginning and end of the data bit cell.

A block diagram of the PLL system is given in Fig. 1.2.1.

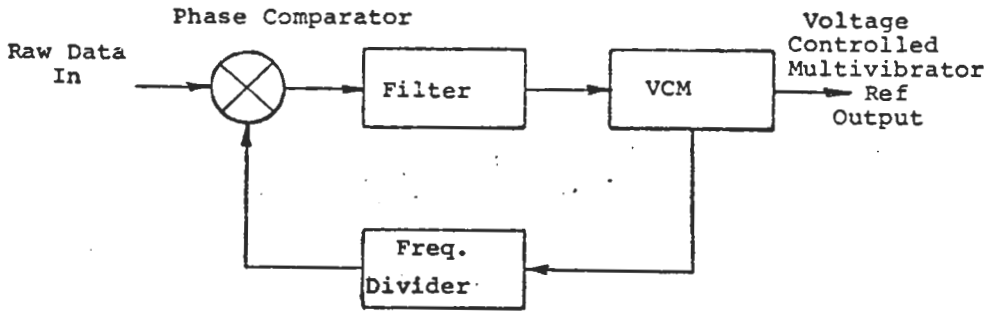

Fig. 1.2.1

PLL Block Diagram

2.0 PHASE LOCKED SYSTEM DESCRIPTION (REF. Schematic Dwg. #15967-001)

2.1 Phase Comparator (PC)

The PC generates an error signal proportional to the phase relationship of the incomming raw data and an internal Voltage Controlled Multivibrator (VCM). The average of the error signal (pulse train) depends upon the relative phase of the Raw Data and VCM (Fig. 2.1.1). A block diagram and timing diagram for PC are given in Figs. 2.1.2 and 2.1.3.

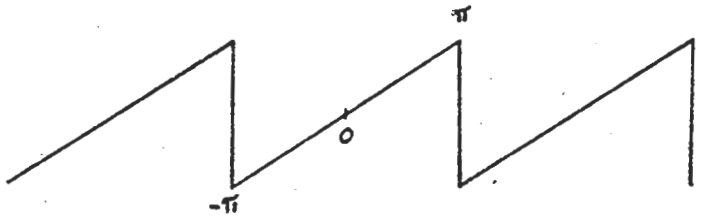

Fig. 2.1.1 PC Characteristics

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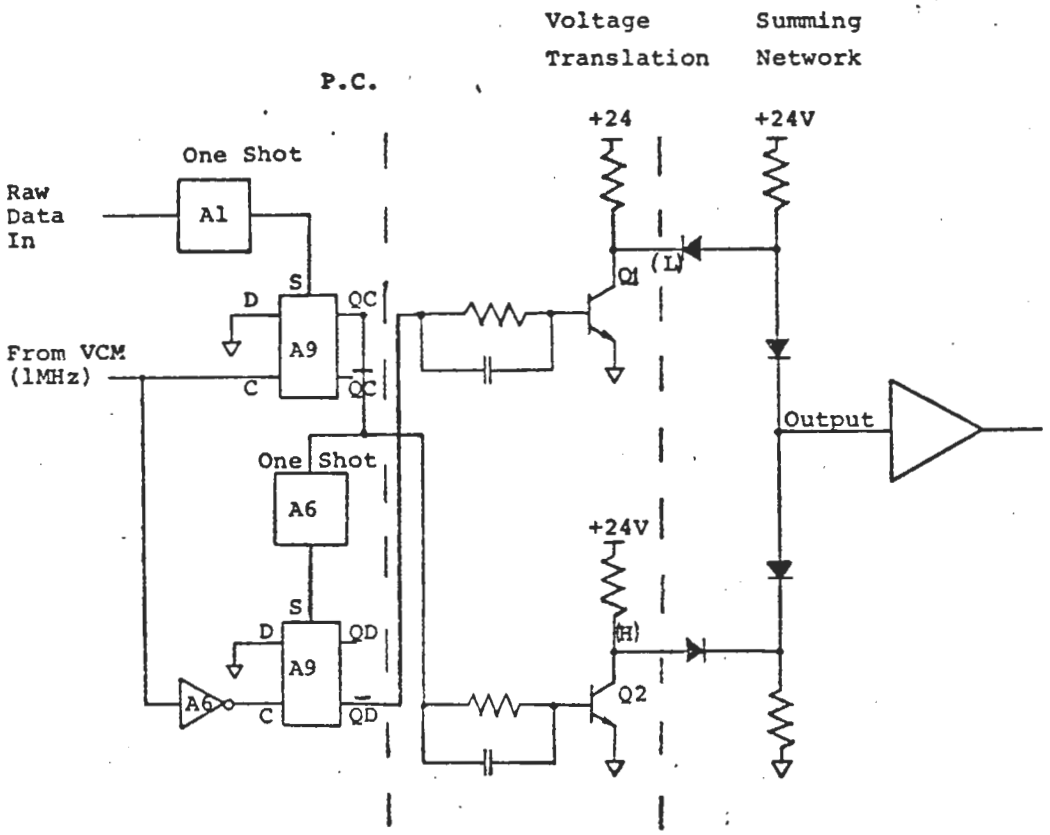

Fig. 2.1.2
P.C. Diagram

2.1 Continued

As shown in Fig. 2.1.2 both "D" flip-flops set lines derive their inputs from one shots in order to minimize the effects of pulse widths. A voltage translator shifts the level of signals from 0V, +5V to 0V, +24V, and a summing network provides a path for the error voltage into an active filter.

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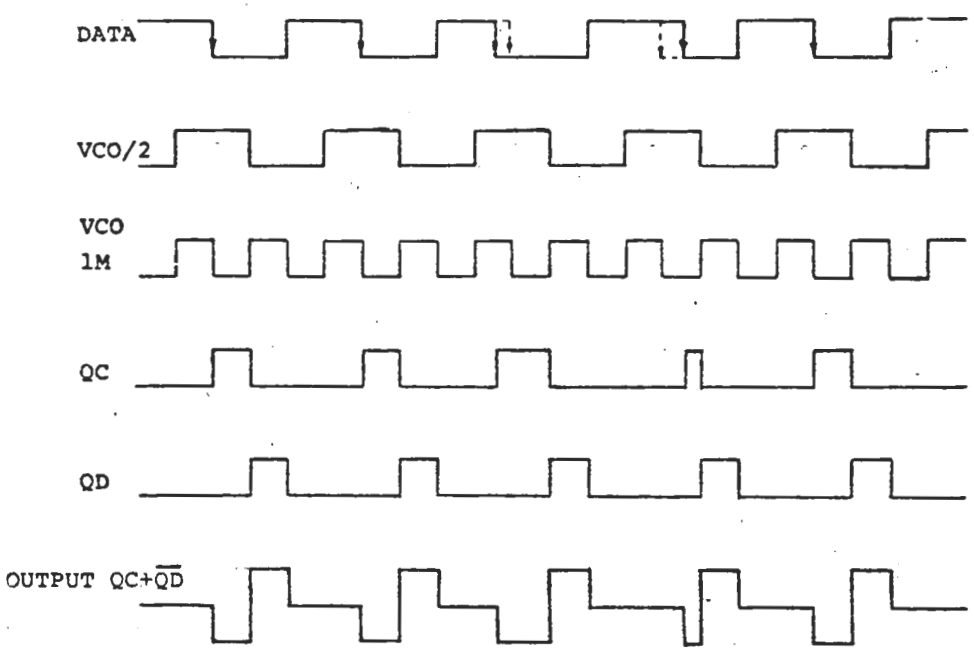

FIG. 2.1.3

Phase comparator timing diagram

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2.2 Active Filter

The active filter operates between +24 to 0V (A15) the DC output of the OP-AMP is nominally set at +15V which brings VCM to center frequency. The output is limited by CR5 and VR1 (to eliminate condition in which A15 chokes VCM). R17 shifts the output of A15 and adjusts the free running frequency of VCM. R21 sets the DC gain of A15 where C8, C9, R21, and R22 determine the filter characteristics.

2.3 VCM and Divider

The VCM is a controlled coupled multivibrator (Q3 and Q6), whose frequency is controlled by two current sources (Q4 and Q5). The center frequency is a function of R26, R33 C11, C14 and the output voltage of A15. The center frequency for the VCM is 2.0 MHz (for MFM) or 1.0 MHz (for FM*). VR5 is the reference for the current sources. CR6 and CR7 are clamping diodes, they help to shape the waveform on collectors of Q6 and Q3. The output is coupled to the frequency divider. The frequency divider (A12) is a "D" flip-flop. Input to the frequency divider is from the V.C.M. Output of the frequency divider is applied to the P.C.

* For MFM C11=C14=100pf
For FM C11=C14=200pf

3.0 DATA DECODER DESCRIPTIONS (REF. Schematic Dwg. #15967-001)

3.1 The Data Decoder Consists of the following Segments:

1. Decoder
2. Missing clocks detector
3. Read sync.

Two timing diagrams are presented; one for FM (Fig. 3.1.1) and, one for MFM (Fig. 3.1.2). The timing diagram is separated for the above three segments. It should be noted that since the decoder is used for FM or MFM not all circuitry is being used for either decoding scheme selected.

It also should be noted that the read sync is extermly instrumental in steering the deocder to its correct phase relationship. The single shot multivibrator (A8) sets the data in the center of the "window" (A10-5). A8 is also used to determine the margin of the decoder.

FIG. 3.1.1

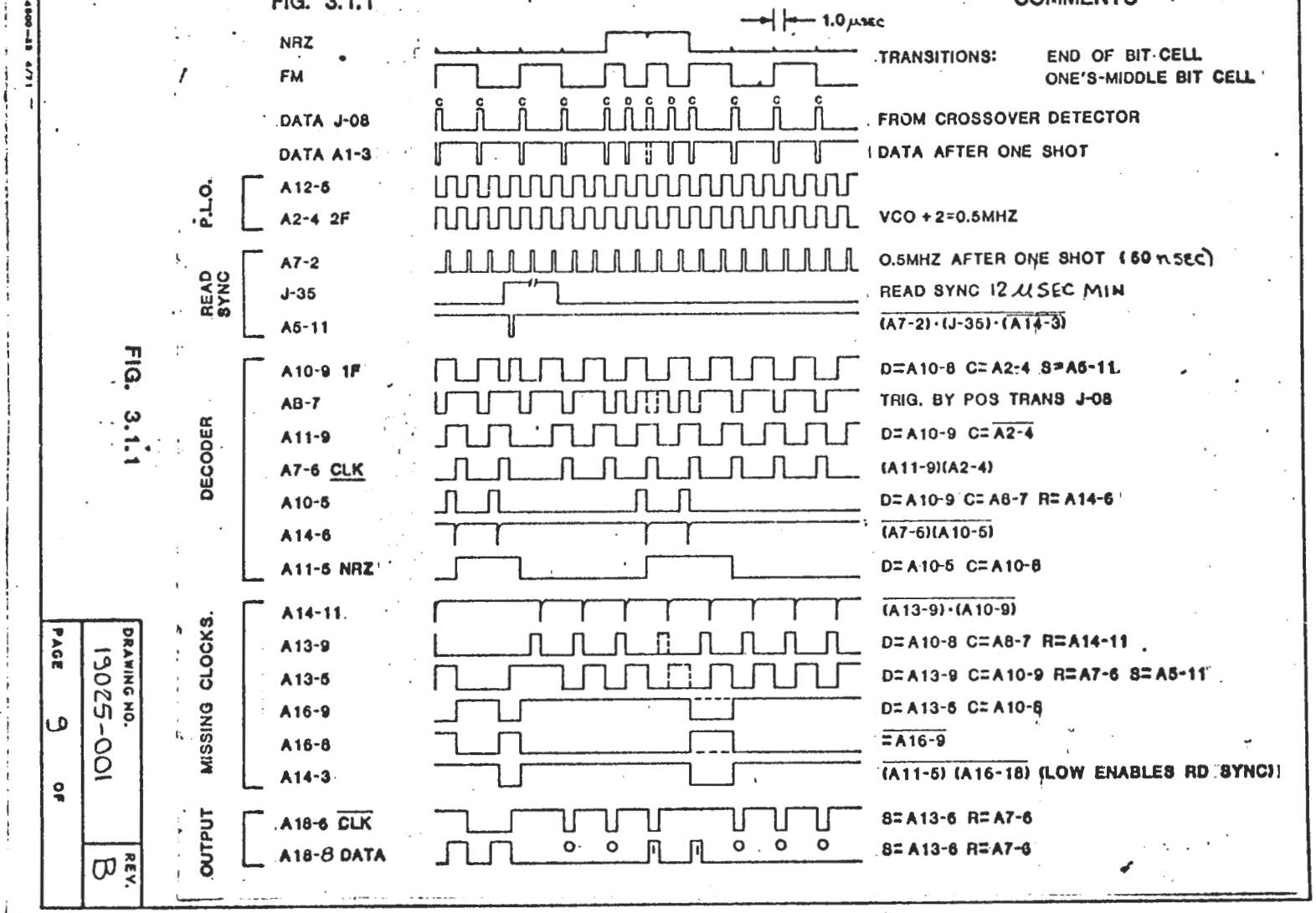

FIG. 3.1.1

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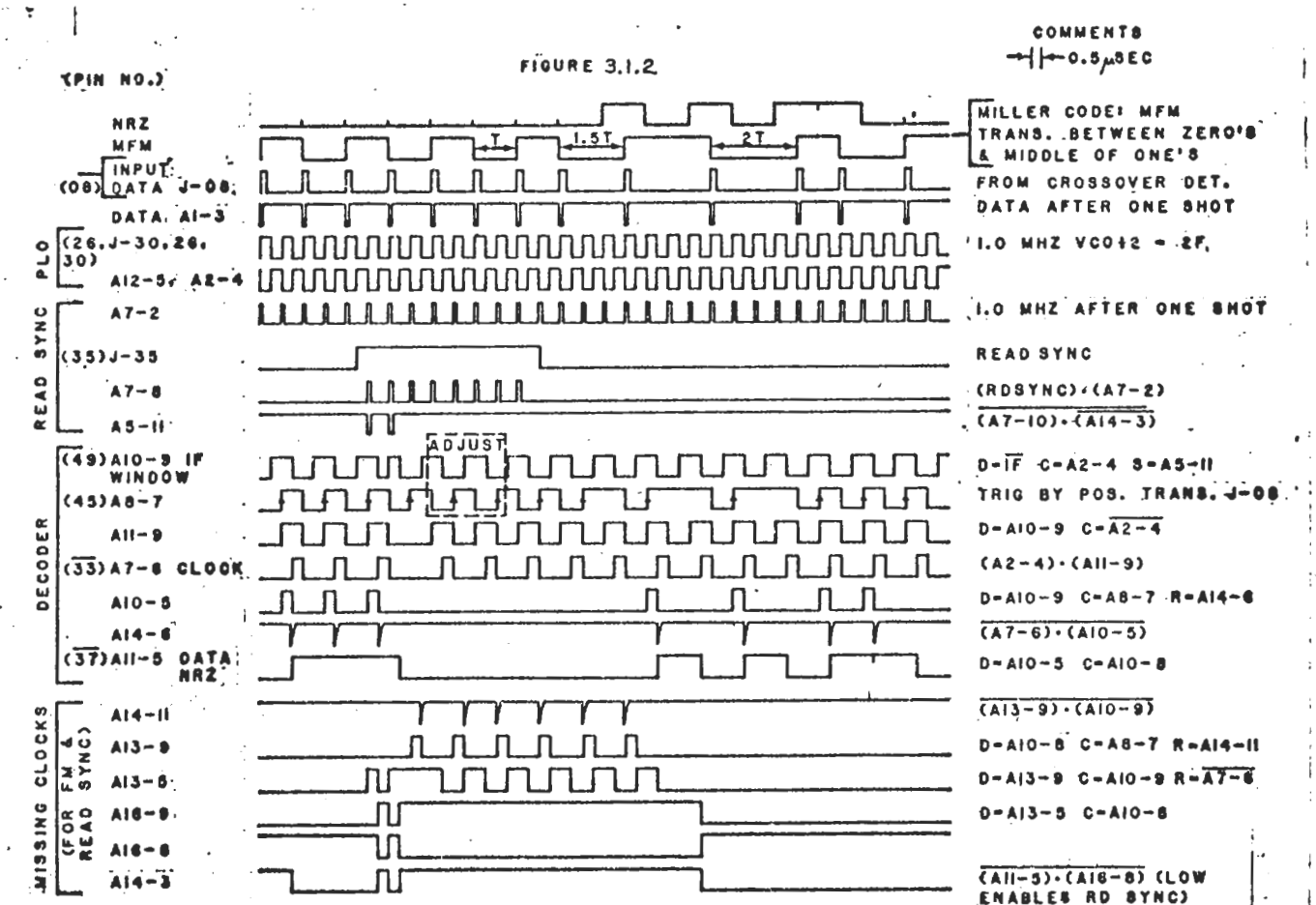
FIG 3.1.2

FIGURE 3.1.2



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4.0 INTERFACE - DATA DECODER W/PLO (Ref. Schematic Dwg. #15967-001)

4.1 CONNECTOR JJX, 60 CONTACTS

Connector PN #90547-001, or connector PN 18918-001.

4.2 INTEPFACE LINE DESCRIPTION

4.2.1 Power Requirements	Signal Pair
+ 24V ± 5% (APPROX 120 mA)*	56
+ 5V DC ± 5% (APPROX 500 mA)	59, 60
GROUND	03, 57

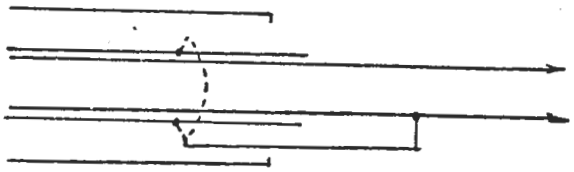
*Unless otherwise specified all wires are #24

4.2.2 INPUTS:

WRTCLK;	*TTL LEVEL (SOURCE 7 mA)	23
RDGT;	TTL LEVEL (SOURCE 7 mA)	02
DATA IN;	TTL LEVEL (SOURCE 14 mA) **	08
READ SYNC;	TTL LEVEL (SOURCE 7 mA)	

* 0.0 to .8V LOW, 2.0 to 5.5V HIGH

** DATA IN; USE #22 AWG TWISTED WIRES SHIELDED & JACKETED PN 90962-001



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4.2.3 OUTPUT		SIGNAL PIN
PLO OUTPUT (For MFM) SHORT BETWEEN		26 to 30
PLO OUTPUT (For FM) SHORT BETWEEN		28 to 30
$\overline{\text{DATA}}$; TTL LEVEL	(max SINK 50 mA)	37
$\overline{\text{CLOCK}}$; TTL LEVEL	(max SINK 50 mA)	33

4.3 ADJUSTMENTS

R17 PLO CENTER FREQ

R5 WINDOW MARGIN

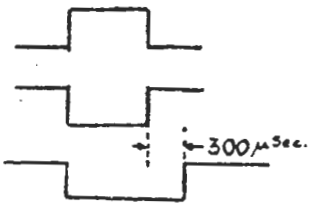
4.4 SIGNAL DESCRIPTION (For MFM)

4.4.1 Input Signals

READ SYNC: A high level pulse (for min. 8 used) will cause data separator to sync. to preamble of 0's for data tracking.

DATA IN: Preamble of all 0's is 500 KHz ± 2.5% for min. of 160 usec, after RDGT becomes high.

RDGT: WRTGT



WRTGT (Read Gate applied to Fd 142)

RDGT (Applied to Data Decoder w/PLO

WRTCK: 500 KHz ± .1%

4.4.2 Output Signals

$\overline{\text{CLOCK}}$: Pulses 500 nsec wide (Freq 500 KHz ± 3.0%)

$\overline{\text{DATA}}$: This line is low if one bit is present and high if zero bit is present. (NRZ Form)

4.5 SIGNAL DESCRIPTION (For FM)

4.5.1 INPUT SIGNALS

READ SYNC: A high level pulse (for min 12 usec) will cause data separator to sync. To preamble of 0's for data tracking.

DATA IN: Preamble of all 0's is 250 KHz ± 2.5% for min of 500 usec after RDGT becomes high.

RDGT: See 4.4.1 RDGT

WRTCK: 500 KHz ±.1%

4.5.2 OUTPUT SIGNALS

$\overline{\text{CLOCK}}$. Pulses 1usec wide(Freq 250 KHz ± 3%) this pulse occurs simultaneously with pulses occuring on the $\overline{\text{DATA}}$ LINE

DATA: This line is low for 1 usec if one bit is present and high if zero bit is present. $\overline{\text{CLOCK}}$ is used to strobe data into the controller..

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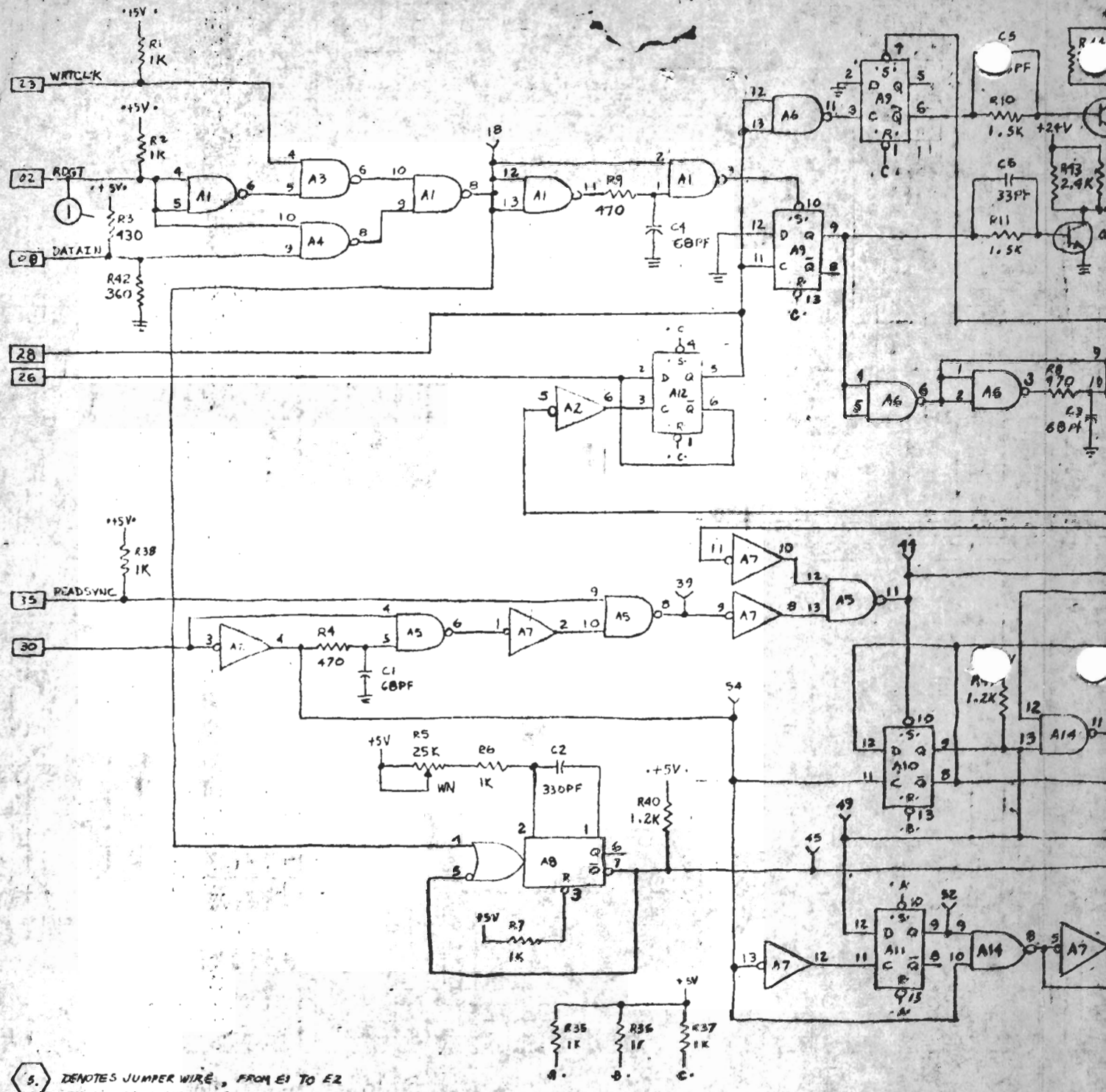


VOLTAGE	INTEGRATED CIRCUIT PIN NO.
+5V	14
	16
GND	7
	8

(5.) DENOTES JUMPER WIRE, FROM E1 TO E2

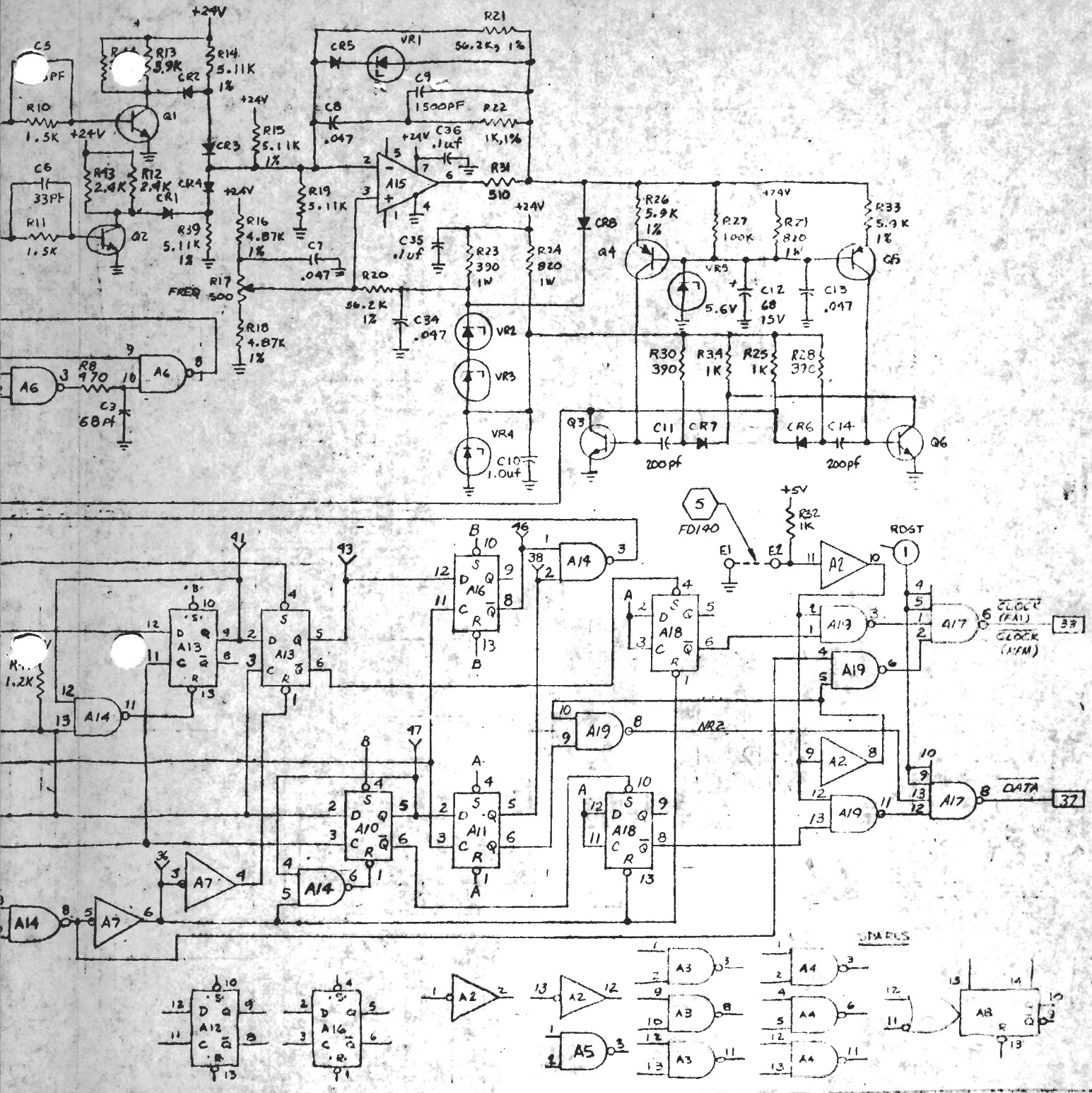
4. ALL 1% AND 0.1% RESISTORS AND 1/8W

3. Y INDICATES TEST POINTS LOCATED ON EDGE OF BOARD OPPOSITE CONNECTOR EDGE.

2. CAPACITANCE VALUES ARE IN MICROFARADS.

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.



INTEGRATED CIRCUIT VOLTAGE CHART		
VOLTAGE	PIN NO.	I.C. REF DESIGNATOR
+5V	14	A1-A7, A9-A14, A16, A17, A18, A19
	16	A8
GND	7	A1-A7, A9-A14, A16, A11, A18, A19
	8	A8

REF DES LAST USED	REF DES NOT USED
R44	C21
C36	
CR7	
VR5	
Q6	
A19	

CENTURY DATA SYSTEMS, INC.
ANAHEIM CALIFORNIA

READ DECODER W/P L.D.

VR71

DRAWN			SIZE		REV
CHECK			D	15967-001	E2
APPD					
SCALE			SHEET 6 OF 6		