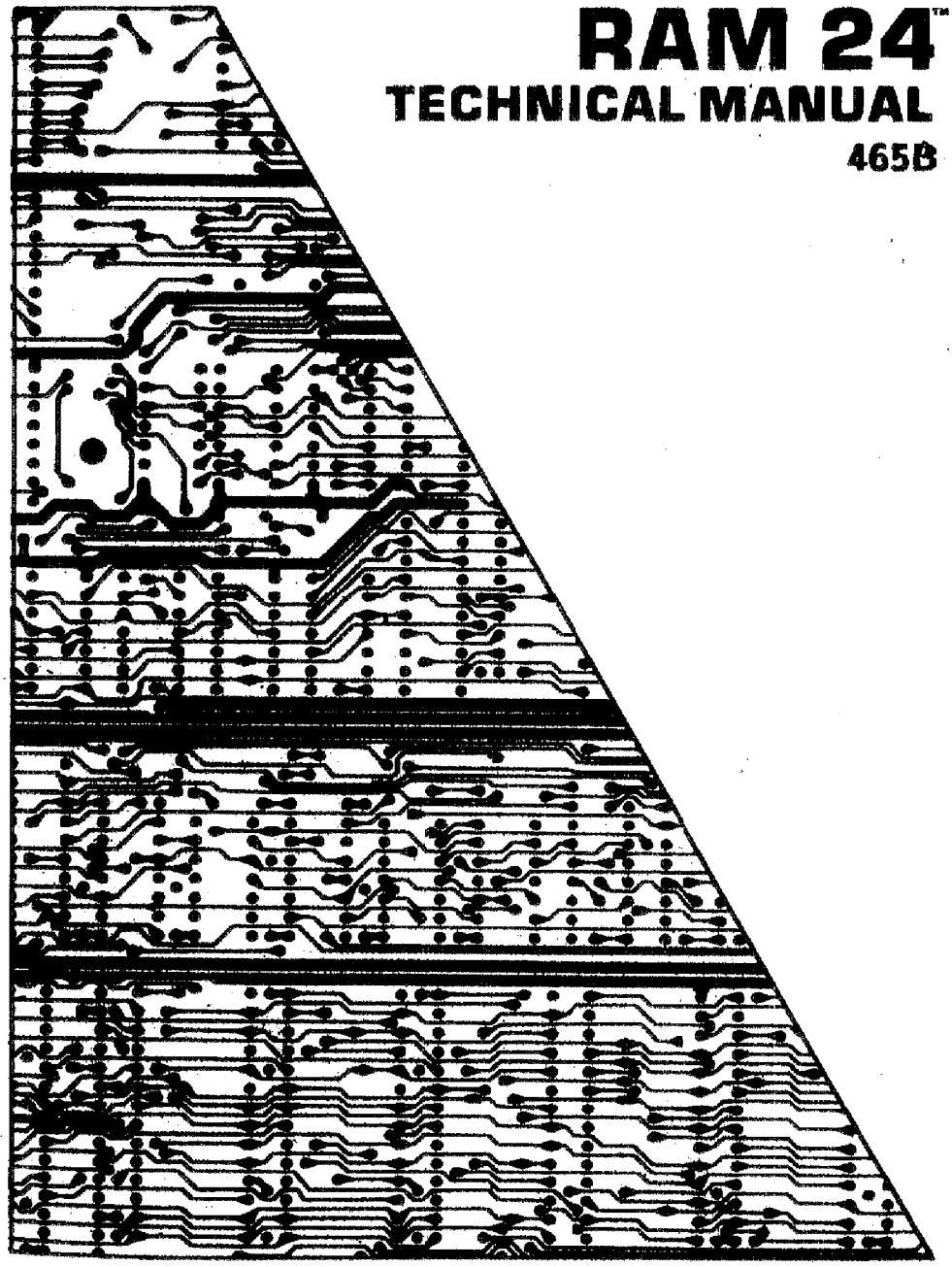
CompuPro™

RAM 24™
TECHNICAL MANUAL
465B



8261-0465B

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RAM 24 Technical Manual 465B

Hayward, CA 94545

Part No: 8261-0465B
Filename: RAM24.MAN

Contents

Specifications

Timing	Meets all IEEE 696/S-100 specifications
Speed	RAM chip access time 100 ns.
Address Bits	24-bits; meets IEEE 696/S-100 extended address specifications
Address	DIP switch selectable on any 1 megabyte boundary for 768K and 1 megabyte versions and on any 512K byte boundary for 512K byte versions
Data Transfer	8-bit or 16-bit; conforms with IEEE 696/S-100 timing requirements for sXTRQ* and SIXTN*
Power Consumption	Less than 4 watts typical at nominal +8V

About the RAM 24

The RAM 24 from **CompuPro** represents one of the most advanced RAM boards ever produced for the IEEE 696/S-100 Bus. By combining state-of-the-art static CMOS RAM technology with **CompuPro's** design excellence, the RAM 24 offers the most versatile, efficient and reliable performance available today. The board works as "word-wide" memory for today's 16-bit systems and automatically switches to "byte-wide" mode in 8-bit systems.

The RAM 24 uses 32 high performance 32K X 8 CMOS RAM chips to provide a total of 1 megabyte or 512 Kwords of storage. The RAM 24 is addressable on any 1 megabyte boundary in the 16 megabyte address space specified by the IEEE 696 standard. The basic RAM 24 board can be configured by CompuPro to accept 512 Kbytes, 768 Kbytes or 1 megabyte of RAM. In addition, it can be configured by CompuPro to have the lower 256K of its memory as global memory, that is, the lower 256K appears in all sixteen 1 Mbyte spaces of the 16 Mbyte S-100 address space.

CompuPro's RAM 24 has plenty of speed to run with our CPU 286^{tm}, CPU 68K^{tm}, CPU 8085/88^{tm}, and CPU-Z^{tm} boards at their highest speeds. The RAM 24 is designed to work with higher speed CompuPro CPUs when they become available. It also handles high-speed DMA flawlessly, a feature few memory boards can boast.

CompuPro also uses a high-quality double-sided circuit board design that has a full solder-mask and legend. Sockets are provided for all ICs for ease of maintenance. All edge connector contacts are gold on a nickel substrate to ensure long and reliable operation.

Configurations

The RAM 24 can be built at CompuPro to a variety of different configurations based on the following two variables:

- There may be 512 Kbytes, 768 Kbytes, or 1 Mbyte of total memory.

- Memory on the board may appear only within the address space selected by Switch 1 (S1), or it may be global.

  Global memory appears in the same relative memory space in all of the sixteen 1 Mbyte pages of the 16 Mbyte S-100 address space. Global memory is used by memory banking schemes to allow a processor that could normally access only 1 Mbyte to access a memory access space approaching 16 Mbytes.

  Refer to **Switch Settings** for sample switch settings for banked memory.

To identify the quantity of RAM on a board, count the large 28 pin packages in U14 - U45.

62256 SRAM Chips	Total Memory
16	512 Kbytes
24	768 Kbytes
32 (all)	1 Mbyte

To further identify the board, find the number on top of the PAL (Programmable Array Logic) at location U4. The table below identifies the board from the PAL.

PAL U4	Total Memory/Organization
430	1 Mbyte/no global memory
442	768 Kbytes/responds in upper 768K of 1 Mbyte region
443	512 Kbytes/no global memory
444	1 Mbyte/lower 256 Kbyte global

NOTE: The number on the PAL U4 and the settings of switch S1 (as described under **Switch Settings**) must match the number of RAM chips present.

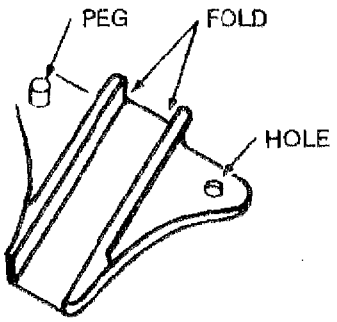
Installing the RAM 24

Basic Installation

Step 1. Unpack the RAM 24 Board.

Along with the board, you will find two card extractors in the plastic bag.

CARD EXTRACTOR



Step 2. Install Card Extractors.

1. Hold the board so the component side is toward you.

2. Insert the peg on the card extractor into the hole in the right corner of the board. Fold the extractor over the board's edge until the extractor's hole snaps over the peg.

   NOTE: Make sure the long edge of the extractor is along the top edge of the board.

3. Repeat for the left extractor.

Step 3. Check Switch Settings

For standard switch settings for use with a CompuPro operating system, check the operating system Installation Guide. Switch jumper settings are described in detail under the **Switch Settings** section.

Step 4. Insert the RAM 24 into the S-100 Bus.

The power to the system must be off. Place the board into a slot towards the front of the enclosure. The edge connector is offset, so the RAM 24 will fit only one way. **Push down GENTLY until the board is firmly installed.**

Switch Summary

The following table summarizes the function and logic of the paddles of Switch 1.

Paddle No.	Function
1	No Connection (leave OFF)
2	ON for 512K boards OFF for 768K or 1M boards
3	OFF for 512K boards ON for 768K or 1M boards
4	OFF for 512K boards ON for 768K or 1M boards
5	ON for 512K boards OFF for 768K or 1M boards
6	A19 for 512K boards OFF for 768K or 1M boards
7	Address line A20
8	Address line A21
9	Address line A22
10	Address line A23

Switch Settings

S1-1 (Switch 1, Paddle 1) Not Connected

S1-2 through S1-5 Board Size Select

The settings of paddles 2 through 5 determine whether the board is recognized as a 512 Kbyte, 768 Kbyte or 1 Mbyte board. Set paddles 2 and 5 ON for a 512 Kbyte board, OFF for a 768 Kbyte or 1 Mbyte board. Set paddles 3 and 4 OFF for a 512 Kbyte board, ON for a 768 Kbyte or 1 Mbyte board.

CAUTION: Never power up the board with both paddles S1-2 and S1-3 ON or with S1-4 and S1-5 ON. This could result in permanent damage to the board.

S1-6 through S1-10 Address Select

The starting address of the board is selected by setting paddles 6 through 10 for a RAM 24 with 512 Kbytes and paddles 7 through 10 for a board with 768 Kbytes or 1 Mbyte. The address is set in a binary fashion with each paddle of S1 representing an address bit. An ON paddle represents a binary "zero" and an OFF paddle represents a binary "one."

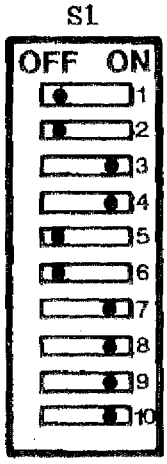
Paddle 6 has no effect on boards set for 1 Megabyte operation. Set it OFF.

NOTE: The IEEE 696/S-100 Bus with 24 address lines can accommodate 16 Megabytes and thus 16 RAM 24 1 Megabyte boards. Before installing more memory make sure both your CPU and your software can utilize it. Also some CompuPro CPUs map functions such I/O, Memory Management, On-board Memory, etc. into the upper end of the last (0F00000h) Megabyte of memory.

Sample Switch Settings

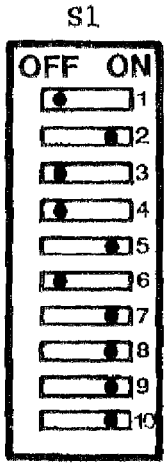
Example 1:

A 1 Megabyte RAM board with starting address 000000h.



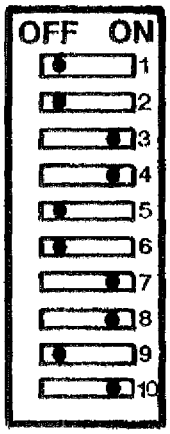
Example 2:

A 512K RAM board addressed at 080000h. This puts the board at the highest 512K address which an 8086 or an 8088 can directly address.



Example 3:

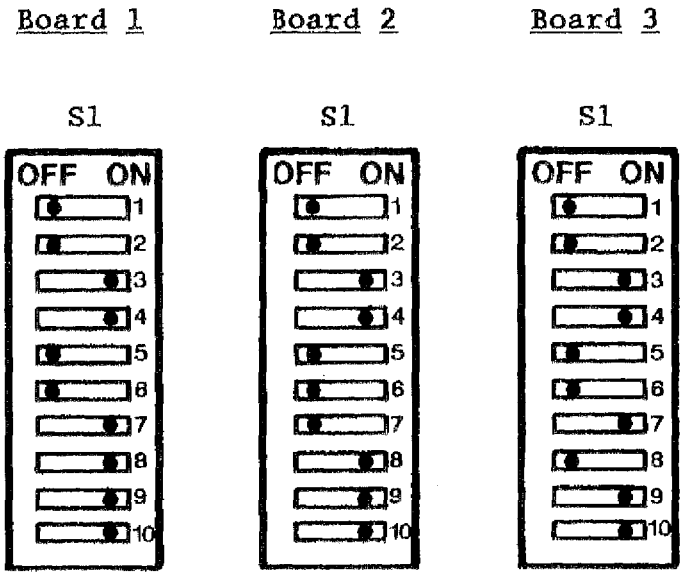
A 1 Megabyte RAM board addressed at 400000h.



Example 4: Banked Memory

The standard implementation of memory banking is to use one 1 Mbyte RAM 24 with PAL 444 installed at U4 and up to fifteen 768 Kbyte RAM 24 boards with PAL 442 installed at U4. This allows the processor to access up to 12 Mbytes of memory.

In this example, Board 1 is the 1 Mbyte board addressed at the first 1 Mbyte page of memory, and Boards 2 and 3 are 768 Kbyte boards addressed at the second and third 1 Mbyte page of memory. The processor can thus address 2.5 Mbytes of memory.



Theory of Operation

The RAM 24 requires only that the starting address of the board be set using switch S1. All other features, such as PHANTOM and byte (8-bit) / word (16-bit) transfers, are handled automatically by onboard logic. This board responds to the upper eight address lines (A16 - 24) as provided for by the IEEE 696/S-100 standard.

Board Addressing

When the address present on bus lines A19 through A23 matches that set with S1-6 through S1-10, U3 (25LS2521) generates signal ASEL* (Address Select). When the board is set for 1 Mbyte operation (S1-4 ON and S1-5 OFF), A19 (S1-6) has no effect on the comparator. Resistors R1-3, R5, and R6 pull the switched comparator inputs high when the paddles are off.

Memory Addressing

The RAM ICs for 1 Mbyte and 768 Kbyte boards are configured as dual arrays decoded by U1 and U2 (74F138s). A single array is present on 512 Kbyte boards, decoded by U2. U1 is enabled when A19 is high and U2 is enabled when it is low.

The selected decoder activates one of the sixteen chip select signals (CS0* - CS15*), which enable only two chips at any one time. This, coupled with the fact that the RAM chips power down when not selected, makes the RAM 24 consume less power than most dynamic RAM designs while featuring the simplicity of operation that only static RAM delivers. Since the proper chips are selected as soon as address lines A16 - A18 are valid, access time is minimized.

Data Transfer

The RAM 24 dynamically switches between "byte-wide" or "word-wide" modes depending on the state of the sXTRQ* signal on the S-100 bus per the protocol established by the IEEE 696/S-100 standard. The DATA IN and DATA OUT buses operate as a bidirectional 16-bit data path when word transfers are performed. The two buses remain unidirectional during byte operations.

The RAM 24 handles the multiplexing of the data buses with two bidirectional bus buffers U9 and U11, and one intermediate buffer U10 (all 74F245s). The direction of U9 and U11 is controlled by sMEMR which indicates whether the bus is expecting a Read or a Write. The direction of U10 is permanently set to go from the even byte array to the odd byte array.

PAL U4 (16L8) controls the enables for U9 through U11. The PAL supervises the control and data bus interface between the S-100 bus and the board. PAL U4 enables its outputs when ASEL* is active and both PHANT (PHANTOM* inverted from the bus by U7) and sOUT are not asserted. sMEMR active indicates a read operation and sWO* a write.

ENDO* (enable data out) is low on any write to the board or on a word read (sXTRQ* and pDBIN asserted). ENDI* (enable data in) is low on any read (pDBIN high) from the board or word write (again sXTRQ* low). ENX* (enable transfer) is low to write the odd byte (A0 and sXTRQ* high) where data flows from the S-100 Data Out bus through U11 through U10 to the odd array data bus (MD8-MD15). ENX* is also asserted when reading the even byte (A0 low, sXTRQ* and pDBIN high) so data travels from the even array data bus (MD0*-MD7*) through U10 through U9 to the S-100 Data In bus.

OEA* (output enable even array) and OEB* (output enable odd array) assert the output enables of the RAM chips during read cycles.

WEA* (write enable even array) and WEB* (write enable odd array) gate pWR* from the bus at U6 (74F32). The respective even and odd write array signals WA* and WB* then actually enable writing the data into the chip(s).

ESX* (enable SXTN acknowlege) and PHANT gate sXTRQ* at U7 (74AS27). The output SXT when high turns on switching transistor Q1 through current limiting resistor R4 and accelerating capacitor C1. Q1 then pulls down S-100 open collector line SXTN* indicating to the bus master it is ready to make a sixteen bit data transfer.

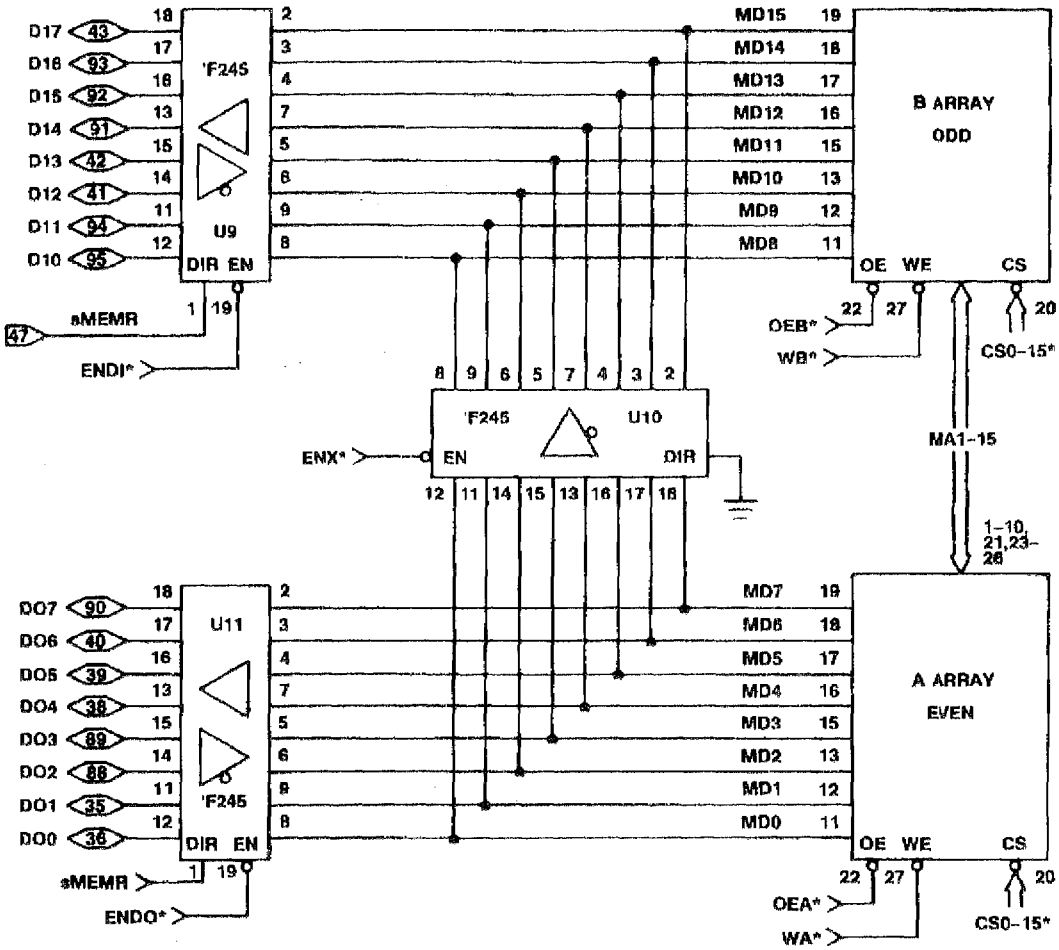
Address lines A1 through A15 are buffered by U6, U7, U5 and U4 (the latter two are 74LS04s).

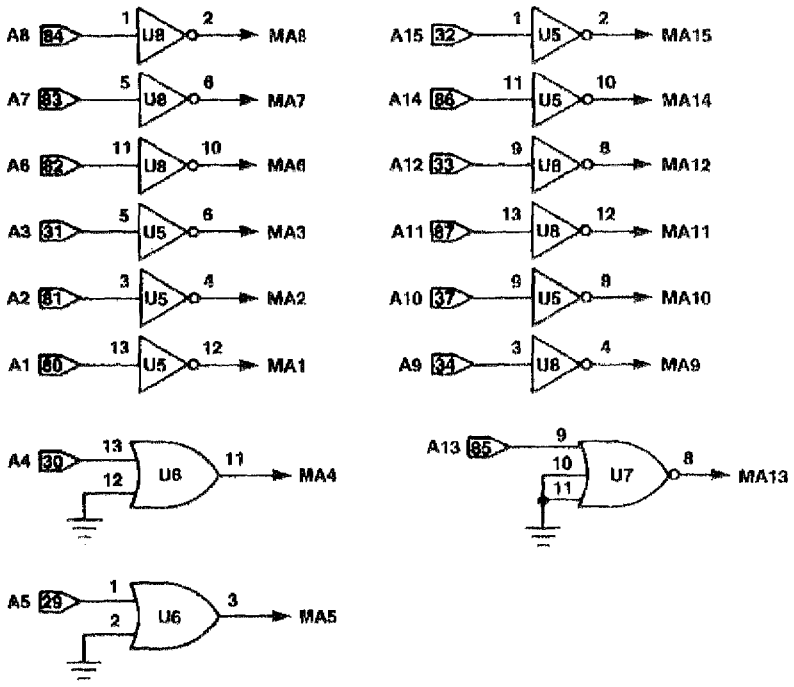
Locating RAM ICs by Address and Byte

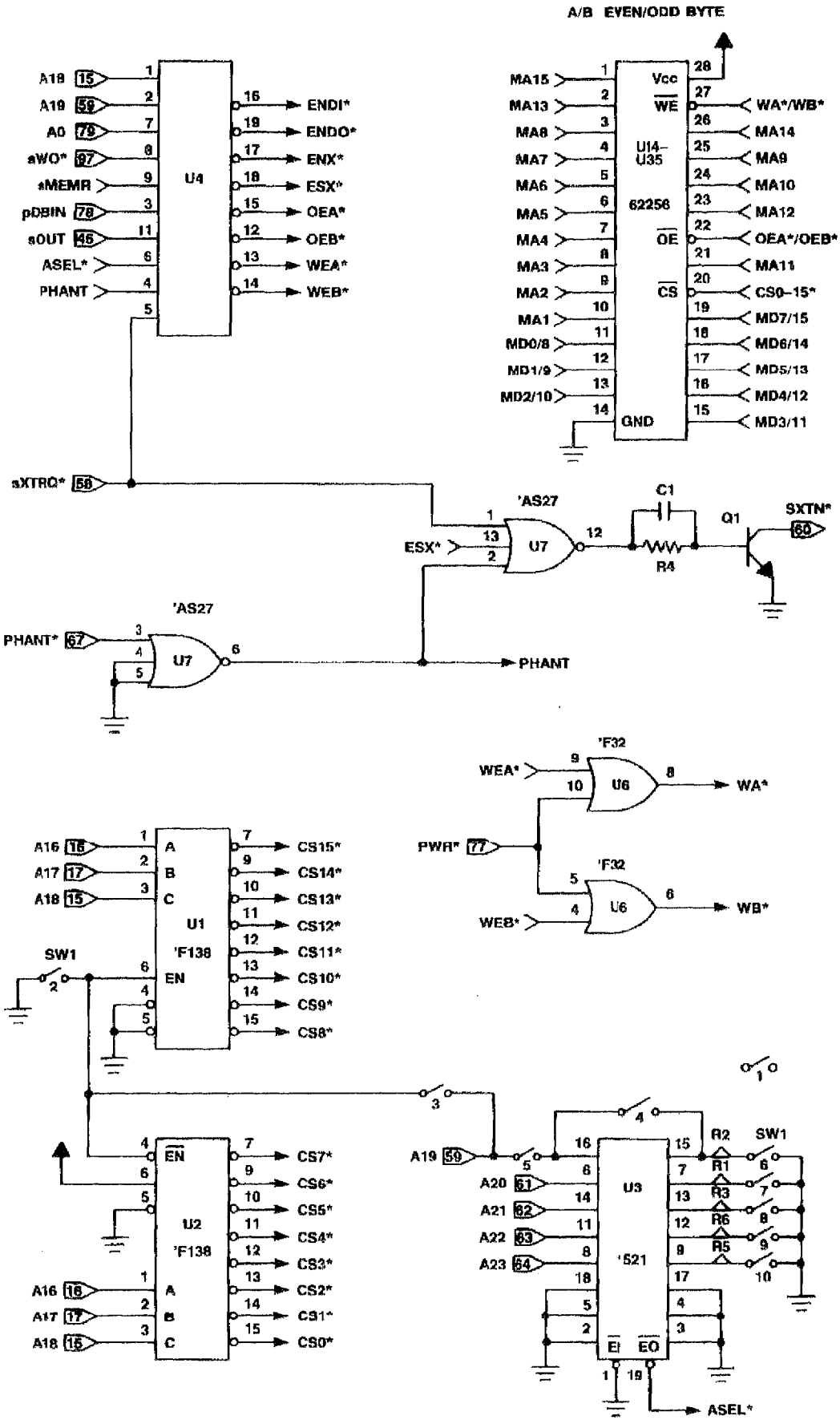
The Component Layout at the end of this manual can be used as a map to locate specific RAM ICs by address and byte array. The following table lists the address within the board and what RAM chip corresponds to that address.

Address	Even Byte	Odd Byte
00000h-0FFFFh	0A	0B
10000h-1FFFFh	1A	1B
20000h-2FFFFh	2A	2B
30000h-3FFFFh	3A	3B
40000h-4FFFFh	4A	4B
50000h-5FFFFh	5A	5B
60000h-6FFFFh	6A	6B
70000h-7FFFFh	7A	7B
80000h-8FFFFh	8A	8B
90000h-9FFFFh	9A	9B
A0000h-AFFFFh	10A	10B
B0000h-BFFFFh	11A	11B
C0000h-CFFFFh	12A	12B
D0000h-DFFFFh	13A	13B
E0000h-EFFFFh	14A	14B
F0000h-FFFFFh	15A	15B

For a 512K RAM 24, chips are located at 0A-7A and 0B-7B. For a 768K RAM 24, chips are located at 4A-15A and 4B-15B.


'F245
U9
DIR EN
sMEMR
ENDI*
D17 43
D16 93
D15 92
D14 91
D13 42
D12 41
D11 94
D10 95
MD15 19
MD14 18
MD13 17
MD12 16
MD11 15
MD10 13
MD9 12
MD8 11
B ARRAY
ODD
OE WE CS
OEB*
WB*
CS0-15*
'F245
U10
ENX*
EN
DIR
MA1-15
1-10,
21,23-
26
U11
'F245
DIR EN
sMEMR
ENDO*
DO7 90
DO6 40
DO5 39
DO4 38
DO3 89
DO2 88
DO1 35
DO0 36
MD7 19
MD6 18
MD5 17
MD4 16
MD3 15
MD2 13
MD1 12
MD0 11
A ARRAY
EVEN
OE WE CS
OEA*
WA*
CS0-15*


A8 84 U8 MA8
A7 83 U8 MA7
A6 82 U8 MA6
A3 31 U5 MA3
A2 81 U5 MA2
A1 80 U5 MA1
A15 32 U5 MA15
A14 86 U5 MA14
A12 33 U8 MA12
A11 87 U8 MA11
A10 37 U5 MA10
A9 34 U8 MA9
A4 30 U6 MA4
A13 85 U7 MA13
A5 29 U6 MA5



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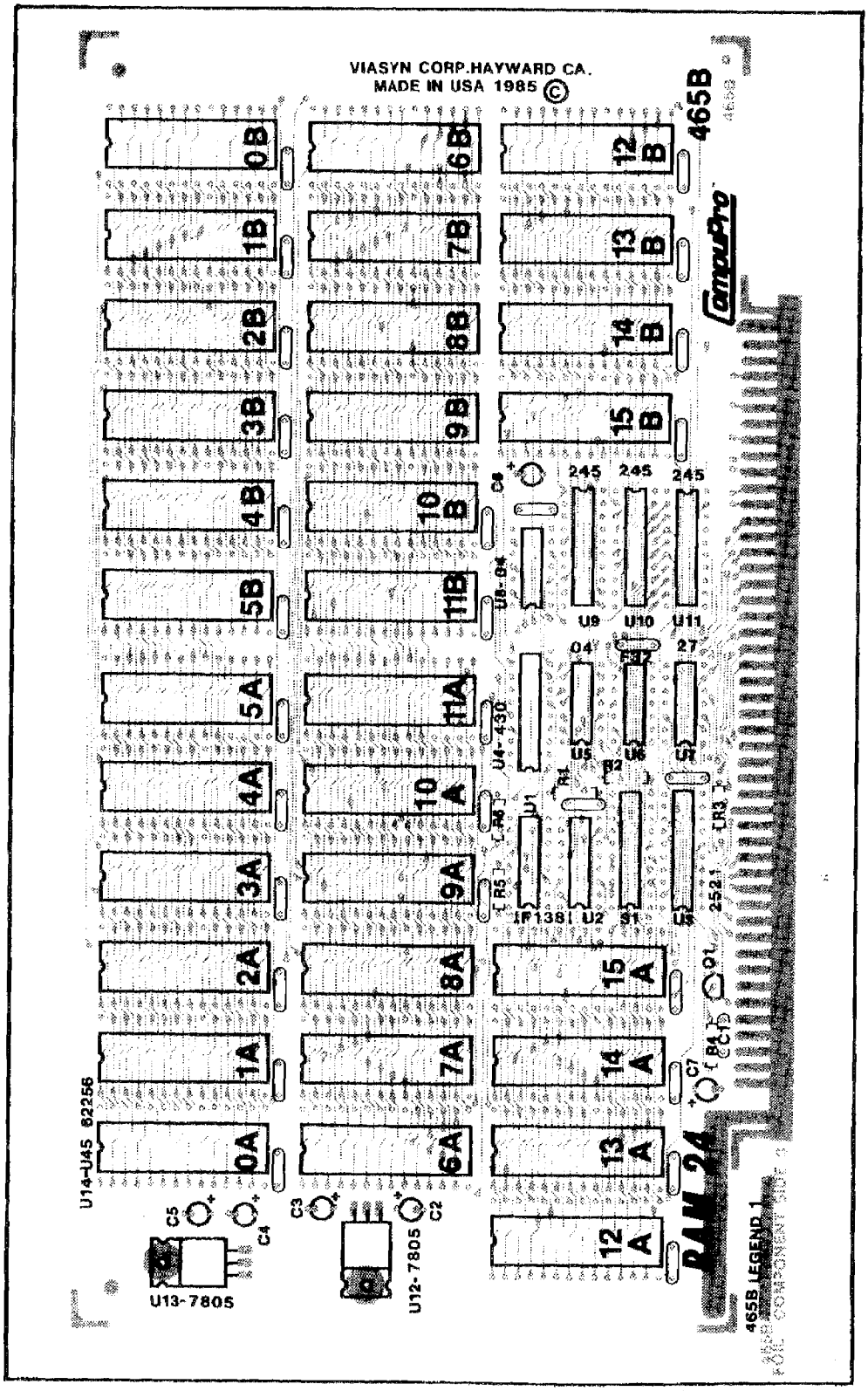

Component Layout

LIMITED WARRANTY

Viasyn Corporation warrants this computer product to be in good working order for a period of ninety days from the date of purchase by the original end user. Should this product fail to be in good working order at any time during this warranty period, VIASYN will, at its option, repair or replace the item at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of VIASYN. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse or unauthorized modification of the product.

If you need assistance, or suspect an equipment failure, always contact your System Center or dealer first. System Center technicians are trained to provide prompt diagnosis and repair of equipment failures. If you are not satisfied by the actions taken by your System Center or dealer, please call VIASYN at (415) 786-0909 to obtain a **Return Material Authorization (RMA)** number, or write to VIASYN at 26538 Danti Court, Hayward, CA, 94545-3999, Att: RMA. Be sure to include a copy of the original bill of sale to establish a purchase date. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location and to use the original shipping container or equivalent. Be sure to mark the RMA number on the outside of the shipping container or delivery may be refused. Contact your System Center/dealer or write to VIASYN at the above address for further information.

All expressed and implied warranties for this product, including the warranties of merchantability and fitness for a particular purpose, are limited in duration to the above listed periods from the date of purchase and no warranties, either expressed or implied will apply after this period.

If this product is not in good working order as warranted above, your sole remedy shall be repair or replacement as provided above. In no event shall VIASYN be liable to you for any damages, including any lost profits, lost savings or other incidental or consequential damages arising out of the use of or inability to use such product, even if VIASYN or a System Center/dealer has been advised of the possibility of such damages, or for any claim by any other party.

If this product is out of warranty, please call or write the VIASYN RMA department to obtain a quotation for factory service. If this product was sold as a system by VIASYN, it may eligible and you may elect to purchase on site/depot maintenance from SPERRY. Contact your System Center/Dealer, your nearest SPERRY office or VIASYN for more details.

If you have purchased a SPERRY service and maintenance agreement, the following two paragraphs also apply:

If VIASYN or its service contractor fails after repeated attempts to perform any of its obligations set forth in this agreement, VIASYN's or its service contractor's entire liability and VIASYN's customer's sole and exclusive remedy for claims related to or arising out of this agreement for any cause and regardless of the form of action, whether in contract or tort, including negligence and strict liability, shall be Viasyn's customer's actual, direct damages such as would be provable in a court of law, but not to exceed the cost of the item of equipment involved.

In no event shall VIASYN or its service contractor be liable for any incidental, indirect, special or consequential damages, including but not limited to loss of use, revenue or profit, even if VIASYN or its service contractor has been advised, knew or should have known of the possibility of such damages; or damages caused by VIASYN's customer's failure to perform its obligations under this agreement; or claims, demands or actions against VIASYN's customer by any other party.

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EFFECTIVE 9/1/86. This warranty supersedes all previous warranties. All previous editions are obsolete.

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