Cromemco®

64KZ-II

Manual Addendum

CROMEMCO, Inc.
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Mountain View, CA. 94043

Part No. 023-2017

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This manual was produced using a Cromemco System Three computer with a Cromemco HDD-22 Hard Disk Storage System running under the Cromemco Cromix™ Operating System. The text was edited with the Cromemco Cromix Screen Editor. The edited text was proofread by the Cromemco SpellMaster™ Program and formatted by the Cromemco Word Processing System Formatter II. Camera-ready copy was printed on a Cromemco 3355A printer.

CROMEMCO 64KZ-II MANUAL ADDENDUM

Manual Changed: Cromemco 64KZ Random Access Memory
                 Instruction Manual
Part Number: 023-0008
Manual Date: May 1981

Make the changes shown below.

MANUAL CHANGES

Page 1, text:

Change: **Z80 and 8080 CPU compatibility**
To: **Z-80A CPU compatibility**

Delete: Powerful DMA Configuration options with DMA
         OVERRIDE.

Page 1, Technical Specifications table:

Change: **+8 VOLTS @ 1.8 A (MAXIMUM)**
To: **+8 VOLTS @ 0.9 AMPERES (MAXIMUM)**

Page 3, Figure 1:

Delete the last item in the last sentence of the second
paragraph as follows

; and a 64KZ used in a Direct Memory Access DAZZLER
system.

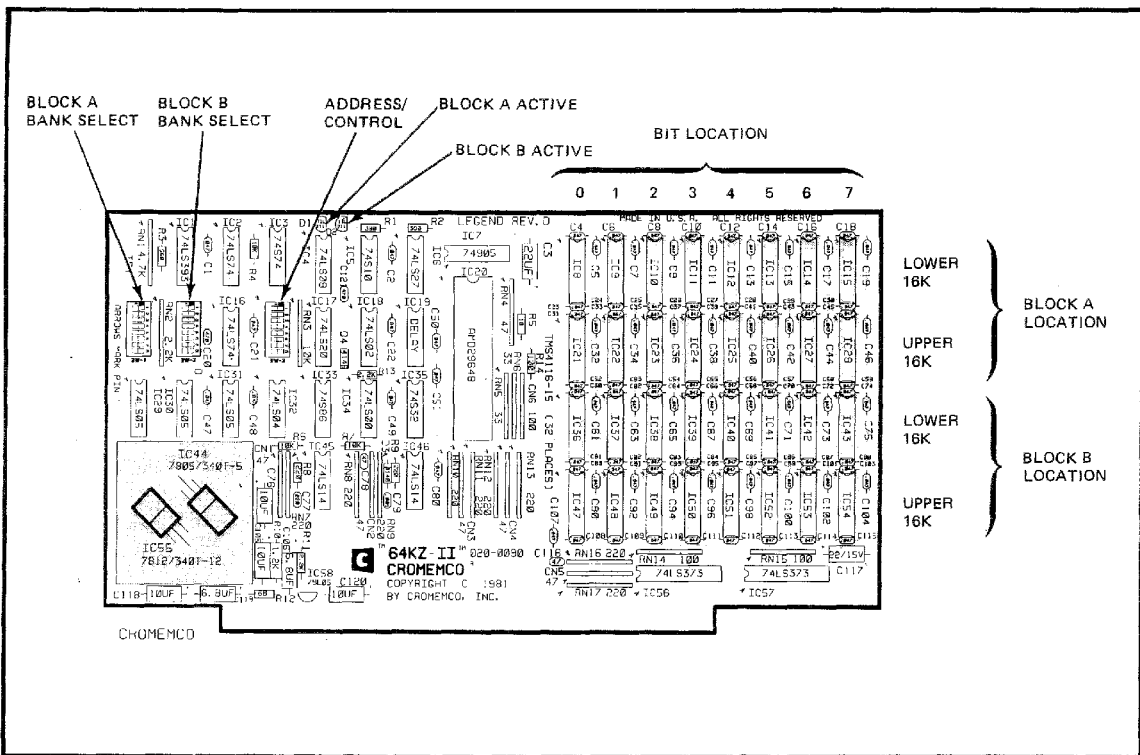Replace Figure 1 with the following figure.

Figure A: 64KZ SWITCH, BLOCK INDICATOR, AND
MEMORY CHIP LOCATIONS

Page 4, text:

Change the sentence between the figures to:

In the SW3 ADDR/CONTROL group, there are four switch functions for each memory block. These are 1) Upper 16K Array Disable, 2) Lower 16K Array Disable, 3) Reset, and 4) A15 Block Enable. Refer to Figure B.

Page 4, Figure 3:

Replace Figure 3 with the following figure.

BLOCK A LOWER 16K ENABLED
BLOCK A UPPER 16K ENABLED
RESET A ENABLED
BLOCK B LOWER 16K ENABLED
BLOCK B UPPER 16K ENABLED
RESET B ENABLED
SELECTS 8000h—FFFFh A15 B=1
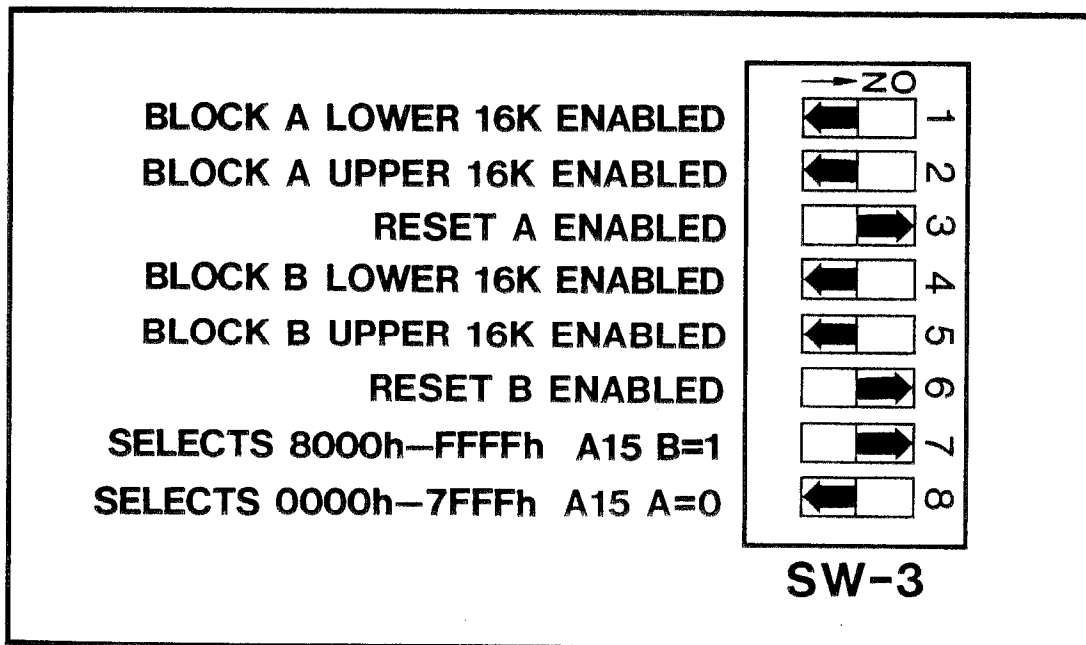SELECTS 0000h—7FFFh A15 A=0

SW-3

Figure B: ADDRESS/CONTROL SWITCH

Page 5, text:

Replace the three paragraphs entitled **The Override** and **DMA Switches** with the following:

The 16K Array Disable Switches

The 16K Array Disable Switches allow each 16Kbyte array to be disabled or enabled manually. Once the array has been manually disabled, it cannot be software enabled. Refer to Figure B.

Change **SW2** to **SW1**; **SW3** to **SW2**.

Page 6, Figure 4:

Change **SW2** to **SW1**; change **SW3** to **SW2**.

Page 6, Example 1:

Change the first sentence in the first paragraph as follows:

> **This example illustrates how one might configure the 64KZ-II board in a no options mode. This assumes no multiple memory banks.**

Change the last sentence in the first paragraph to:

> **The board automatically enables after a RESET or POC since RESET A = RESET B = IN. The board remains in the memory map for all software generated BANK SELECT control words (except 0) since BANK 0-7 = IN for both BLOCK A and B.**

Pages 7 and 8, Figures 5 and 6:

Change the switch positions, labeling and settings for the 64KZ-II board figures as shown in Figures A and B in this addendum.

Change **SW1** to **SW3**, **SW2** to **SW1**, and **SW3** to **SW2**.

Pages 9 through 12, text and figures:

Delete Example 3. Note that Section 2.2, at the bottom of page 12, is not deleted.

Page 13, text and figures:

Change the first sentence to the following:

> **There are two events which may change the active/inactive status of a 64KZ memory BLOCK:**

Power On Clear (POC) or RESET and executing an OUT
40h, A instruction which configures or reconfigures
the memory banks.

Delete the remainder of the page.

Page 14, text:

Delete the first two sentences.

Pages 16, 17, 18, and 21, Figures 12 through 15:

Change the switch labeling as shown in Figures A and B
in this addendum.

Change SW1 to SW3, SW2 to SW1, and SW3 to SW2.

Page 22, text:

Change the first paragraph to read:

The BANK SELECT port address is changed from its
factory wired 40h value by cutting the traces used
to jumper across location IC7 (as shown in Figure
1). Then, a properly programmed 74S288 PROM is
installed in their place. With the PROM inserted,
the 64KZ-II responds to 1 of 15 remaining
addresses, 41h through 4Fh. When ordering a PROM,
the desired I/O address must be stated.

Delete the second paragraph.

Page 23, text:

Delete everything after the numbered items near the top
of the page.

Page 24, figure and text:

Delete everything from the beginning of the page down to
and including the third paragraph.

Page 25-27, Sections 2.5 and 2.6, Figures 18 and 19.

Delete all.

Page 28:

Add the following examples of switch settings for High
Resolution Color Graphics Systems. Set the switches of
additional 64KZ-II boards as shown in the Cromix
Operating System manual for Banks 1, 2, and 3. Note
that SW-3 must be set like SW-1, SW-1 like SW-2, and
SW-2 like SW-3.

SWITCH SETTINGS FOR HIGH RESOLUTION COLOR GRAPHICS SYSTEM USING THE CDOS OPERATING SYSTEM

64KZ-II SWITCH SETTINGS

SW-1 (BLOCK A)

Switch	BANK
1	0 ON
2	1 OFF
3	2 OFF
4	3 OFF
5	4 OFF
6	5 ON
7	6 ON
8	7 OFF

SW-2 (BLOCK B)

Switch	BANK
1	0 ON
2	1 OFF
3	2 OFF
4	3 OFF
5	4 OFF
6	5 ON
7	6 ON
8	7 OFF

SW-3 (ADDRESS/CONTROL)

Switch	Function
1	BLOCK A LOWER 16K ENABLED
2	BLOCK A UPPER 16K ENABLED
3	BLOCK A RESET ENABLED
4	BLOCK B LOWER 16K ENABLED
5	BLOCK B UPPER 16K ENABLED
6	BLOCK B RESET DISABLED
7	BLOCK B 8000h--FFFFh
8	BLOCK A 0000h--7FFFh

FIRST 48KTP SWITCH SETTINGS

SW-1

1	2	3	4	5	6	7	8
ON	↑	↑	↑	↓	↑	↑	↑

SELECTS { A15=0, 4000h-FFFFh, A14=1 } DMA OFF, DMA IN, PRESET, MEMDSBL, SECOND PORT PAGING, PAGE 0

SW-2

Switch	BANK
1	7 OFF
2	6 OFF
3	5 ON
4	4 OFF
5	3 OFF
6	2 OFF
7	1 OFF
8	0 OFF

SECOND 48KTP SWITCH SETTINGS

SW-1

1	2	3	4	5	6	7	8
ON	↑	↑	↓	↓	↑	↑	↓

SELECTS { A15=0, 4000h-FFFFh, A14=1 } DMA OFF, DMA IN, PRESET, MEMDSBL, SECOND PORT PAGING, PAGE 1

SW-2

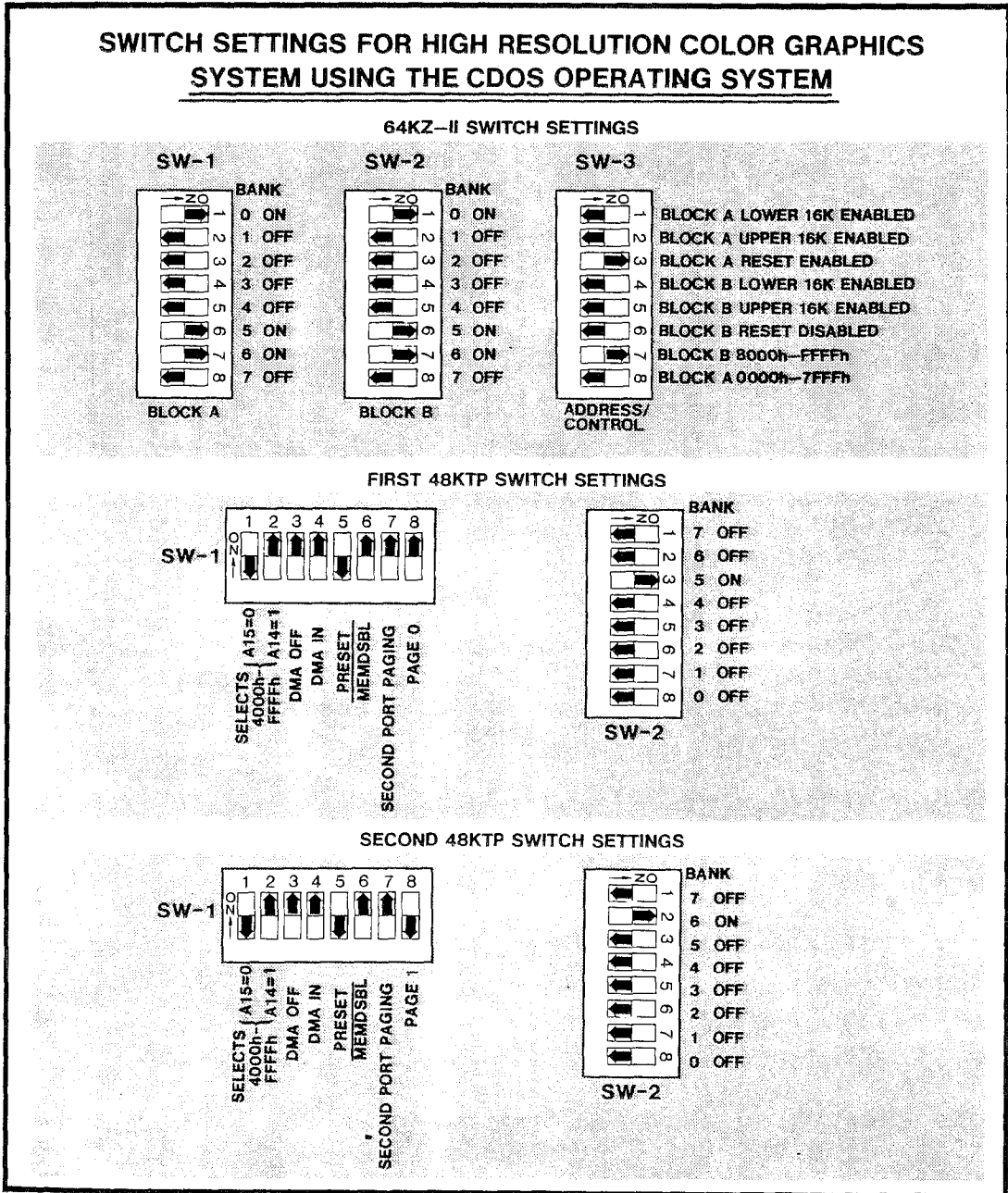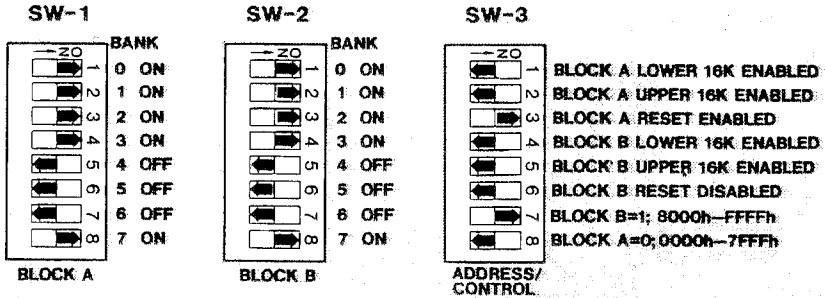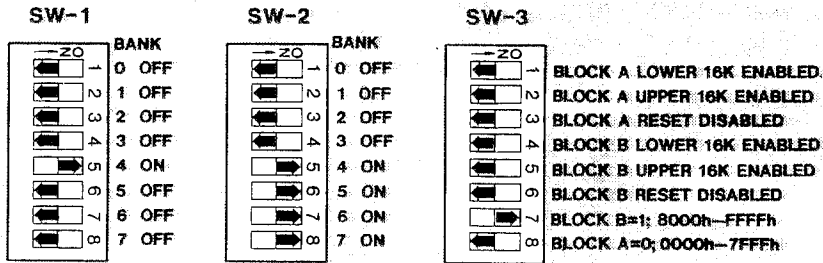| Switch	BANK
1	7 OFF
2	6 ON
3	5 OFF
4	4 OFF
5	3 OFF
6	2 OFF
7	1 OFF
8	0 OFF

Figure C: CDOS/COLOR GRAPHICS SYSTEM SWITCH SETTINGS

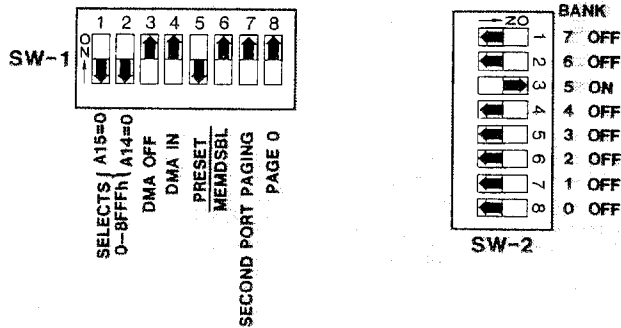# SWITCH SETTINGS FOR HIGH RESOLUTION COLOR GRAPHICS SYSTEM USING THE CROMIX OPERATING SYSTEM

BANK 0 (CROMIX) 64KZ-II SWITCH SETTINGS

SW-1

BANK	
0	ON
1	ON
2	ON
3	ON
4	OFF
5	OFF
6	OFF
7	ON

BLOCK A

SW-2

BANK	
0	ON
1	ON
2	ON
3	ON
4	OFF
5	OFF
6	OFF
7	ON

BLOCK B

SW-3

- BLOCK A LOWER 16K ENABLED
- BLOCK A UPPER 16K ENABLED
- BLOCK A RESET ENABLED
- BLOCK B LOWER 16K ENABLED
- BLOCK B UPPER 16K ENABLED
- BLOCK B RESET DISABLED
- BLOCK B=1; 8000h—FFFFh
- BLOCK A=0; 0000h—7FFFh

ADDRESS/CONTROL

BANK 4 (USR 1) 64KZ-II SWITCH SETTINGS

SW-1

BANK	
0	OFF
1	OFF
2	OFF
3	OFF
4	ON
5	OFF
6	OFF
7	OFF

SW-2

BANK	
0	OFF
1	OFF
2	OFF
3	OFF
4	ON
5	ON
6	ON
7	ON

SW-3

- BLOCK A LOWER 16K ENABLED
- BLOCK A UPPER 16K ENABLED
- BLOCK A RESET DISABLED
- BLOCK B LOWER 16K ENABLED
- BLOCK B UPPER 16K ENABLED
- BLOCK B RESET DISABLED
- BLOCK B=1; 8000h—FFFFh
- BLOCK A=0; 0000h—7FFFh

FIRST 48KTP SWITCH SETTINGS

SW-1

SELECTS { A15=0 0—8FFFh, A14=0 }, DMA OFF, DMA IN, PRESET, MEMDSBL, SECOND PORT PAGING, PAGE 0

SW-2

BANK	
7	OFF
6	OFF
5	ON
4	OFF
3	OFF
2	OFF
1	OFF
0	OFF

SECOND 48KTP SWITCH SETTINGS

SW-1

SELECTS { A15=0 0—8FFFh, A14=0 }, DMA OFF, DMA IN, PRESET, MEMDSBL, SECOND PORT PAGING, PAGE 1

SW-2

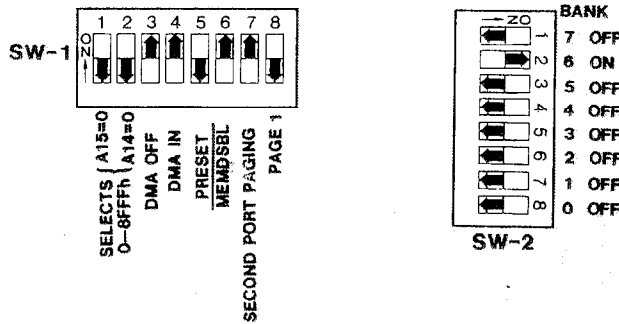| BANK	
7	OFF
6	ON
5	OFF
4	OFF
3	OFF
2	OFF
1	OFF
0	OFF

Figure D: CROMIX/COLOR GRAPHICS SYSTEM SWITCH SETTINGS

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Page 29, Figure 20:

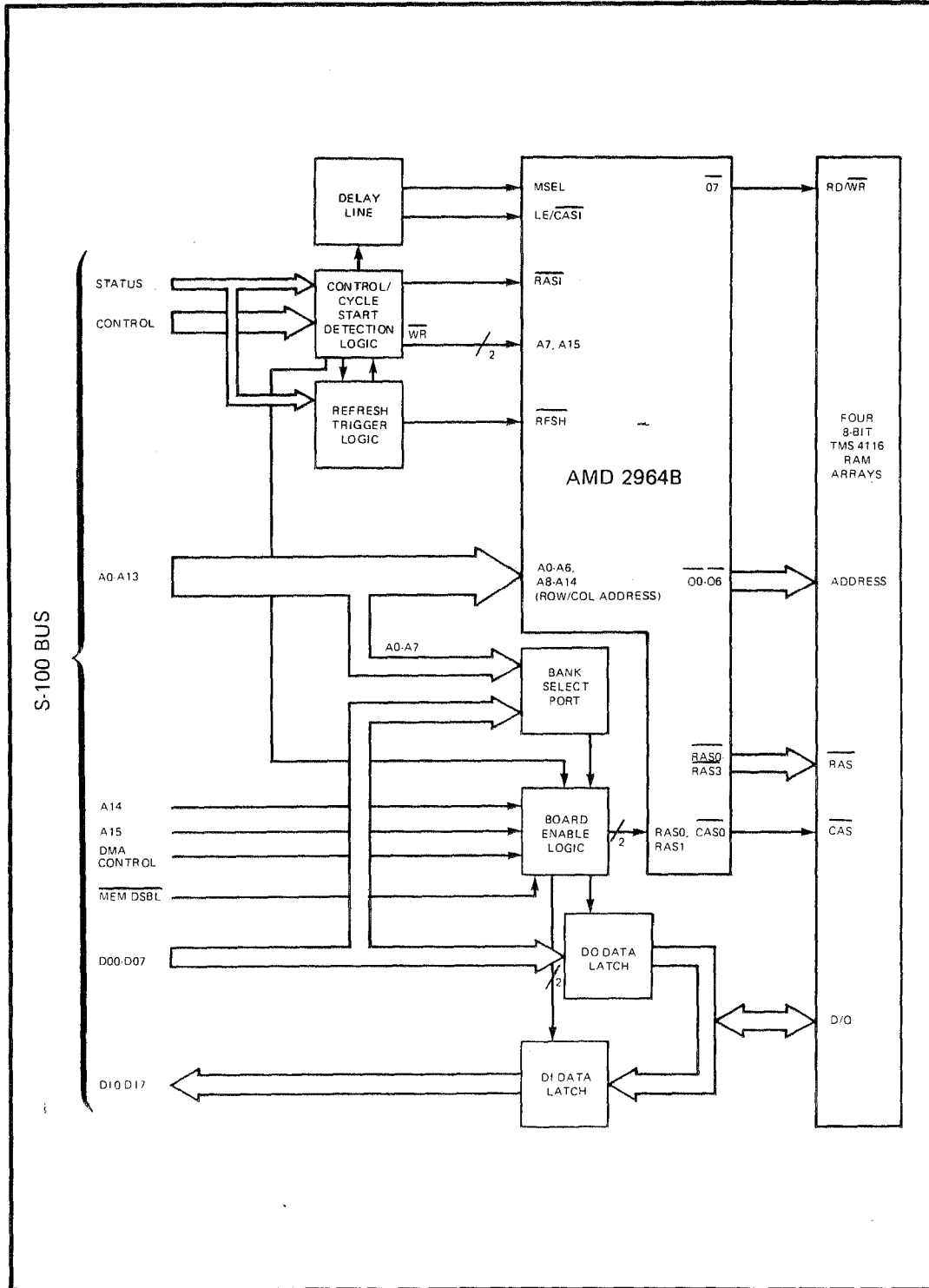Replace Figure 20 with the following figure:

Figure E: 64KZ-II BLOCK DIAGRAM

Page 30, text:

Add the following description of the 64KZ-II board at
the beginning of the page.

64KZ-II Memory Board

The 64KZ-II is a direct replacement for the 64KZ
board. The difference between the boards is the
way in which the functions are implemented by the
hardware circuits. DMA manipulation is no longer
used. Memory disable, along with the ability to
disable each 16K memory array manually, is
included. As shown on the new block diagram,
Figure C, the timing shift registers, refresh
counter, address latches, and RAS/CAS logic
functions are combined into one LSI microcircuit.
This reduces the power consumption while increasing
the reliability of the board. All memory data
passes through the data bus internal to the 64KZ-II
board. Incoming data from the system DO bus is
latched and held on the internal data bus. Then
the incoming data is stored at the addressed memory
location. Outgoing data from an addressed memory
location is placed on the internal data bus. Then
the outgoing data is latched onto the system DI
data bus.

Page 35 and 36, Parts List:

Replace the parts list with the new parts list that
follows.

PARTS LIST

Designation	Description	Cromemco Part No.
Integrated Circuits		
IC1	74LS393	010-0141
IC2	74LS74	010-0055
IC3	74S74	010-0142
IC4	74LS08	010-0064
IC5	74S10	010-0035
IC6	74LS27	010-0112
IC8-15	TMS 4116	011-0019
IC16	74LS74	010-0055
IC17	74LS20	010-0095
IC18	74LS02	010-0068
IC19	delay line	011-0080
IC20	AM2964B	010-0329
IC21-28	TMS 4116	011-0019
IC29-31	74LS05	010-0065
IC32	(non TI) 74LS04	010-0066
IC33	74S86	010-0125
IC34	74LS00	010-0069
IC35	74S32	010-0090
IC36-43	TMS 4116	011-0019
IC44	7805/340T-5	012-0001
IC45-46	74LS14	010-0061
IC47-54	TMS 4116	011-0019
IC55	7812/340T-12	012-0002
IC56-57	74LS373	010-0102
IC58	79L05	012-0053
Diodes		
D1-2	LED grn min til211	008-0020
D3-4	1N914/1N4148	008-0002

Designation	Description	Cromemco Part No.
Capacitors		
C1-2	.047 uf axial	004-0061
C3	22 uf tant	004-0028
C4-19	.047 uf axial	004-0061
C20	470 pf mono	004-0080
C21-75	.047 uf axial	004-0061
C76	10 uf tant	004-0032
C77	220 pf mono	004-0077
C78	47 pf mono	004-0000
C79	.001 uf mono	004-0043
C80-104	.047 uf axial	004-0061
C105	10 uf tant	004-0032
C106	6.8 uf tant	004-0034
C107-115	.047 uf axial	004-0061
C116	47 pf mono	004-0000
C117	22 uf tant	004-0028
C118	10 uf tant	004-0032
C119	6.8 uf tant	004-0034
C120	10 uf tant	004-0032
C121	470 pf mono	004-0080
Capacitor Networks		
CN1-5	47 pf, 8 pin	005-0000
CN6	100 pf, 8 pin	005-0001
Resistors		
R1-2	390	001-0013
R3	560	001-0015
R4	10 K	001-0182
R5	10	001-0000
R6-7	10 K	001-0182
R8-9	220	001-0010
R10	1/2 watt 1.2 K	001-0189
R11	2.2 K	001-0021
R12	68	001-0005
R13	2.2 K	001-0021

Designation	Description	Cromemco Part No.
Resistor Networks		
RN1	4.7 K, 8 pin	003-0009
RN2	2.2 K, 8 pin	003-0008
RN3	10 K, 8 pin	003-0025
RN4	47, 8 pin	003-0047
RN5-6	33, 8 pin	003-0000
RN7-13	220, 8 pin	003-0057
RN14-15	100, 8 pin	003-0001
RN16-17	220, 8 pin	003-0057
Miscellaneous		
	3 8 pos. dip switches	013-0002
	4 6-32 hex nuts	015-0013
	4 #6 lock washers	015-0020
	4 6-32x1/2 screws	015-0044
	1 large heat sink	021-0017

Page 37, 64KZ Part Location Diagram:

Replace the diagram with the following figure.

PART LOCATION DIAGRAM

C19 C46 C59 C74 C75 C88 C103 C104 C115
C18 IC15 IC28 IC43 IC54 22/15V C117
C17 C38 C45 C44 C58 C72 C73 C97 C101 C102 C114
ALL RIGHTS RESERVED C16 IC14 IC27 IC42 IC53 RN15 100 74LS373 IC57
C15 C29 C43 C42 C57 C70 C71 C86 C99 C100 C113
C14 IC13 IC26 IC41 IC52
C13 C28 C41 C40 C56 C68 C69 C85 C97 C98 C112
MADE IN U.S.A. C12 IC12 IC25 IC40 IC51
C11 C27 C39 C38 C55 C66 C67 C84 C95 C96 C111
C10 IC11 IC24 IC39 IC50 RN14 100 74LS373 IC56
C9 C26 C37 C36 C54 C64 C65 C83 C93 C94 C110
C8 IC10 IC23 IC38 IC49
C7 C25 C35 C34 C53 C62 C63 C82 C91 C92 C109
C6 IC9 IC22 IC37 IC48 RN16 220 RN17 220
C5 C24 C33 C32 C52 C60 C61 C81 C89 C90 C108
C4 IC8 IC21 IC36 IC47 C116 (47) CN5 47
C3 C23 C31 TMS4116-15 (32 PLACES) C107
22UF R5 10 R14 100 CN6 100 RN13 220 CN4 47
RN4 47 RN6 33 RN5 33
LEGEND REV.D IC7 74905 IC20 AMD2964B RN12 220 RN11 220 CN3 47
R2 IC6 RN10 220
R1 390 C50 C51 C80 64KZ-II™ 020-0090 CROMEMCO.® COPYRIGHT © 1981. BY CROMEMCO, INC.
74LS27 IC19 DELAY IC35 74S32 IC46 74LS14
C2 C22 C49 R9 220 C79 4148 RN9 220 CN2 47
74S10 IC18 74LS02 IC13 2.2K 74LS00 (47) C78
IC5 C12 (470) D4 4148 IC34 R7 10K RN8 220
74LS08 IC17 74LS20 IC33 74S86 IC45 74LS14 IC58 79L05 C120 10UF
D1 IC4 RN3 10K R6 R8 C77 220 RN7 220 R11 2.2K
IC3 74S74 SW3 IC32 74LS04 10K 220 C106 6.8UF R12
R4 10K C21 C48 C76 R10 1.2K C105 10UF R119 68
IC2 74LS74 IC16 74LS74 IC31 74LS05 CN1 47 10UF C118 10UF 6.8UF
C1 C20 (470) C47 IC44 7805/340T-5
IC1 74LS393 SW2 74LS05 IC55 7812/340T-12
R3 560 RN2 2.2K IC30 IC29
RN1 4.7K SW1 74LS05
TP1 ARROWS MARK PIN 1

Schematic Diagram:

Replace the schematic with the new diagram included in this addendum.