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8PIO
8 Port Input/Output Interface

Instruction Manual

Cromemco

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Introduction

The Cromemco 8PIO is an S-100 bus compatible, eight parallel input/output port board (see simplified block diagram, Figure 1). Each of the eight independent I/O ports consists of a separate input port and an output port with the same port address. Each input/output port pair share 8 bi-directional lines which are brought out to EIA connectors J1 thru J4 for I/O interfacing. Both the input and output ports are latched: output data is automatically latched into an OUT port when the system CPU executes an output instruction to the 8PIO, and input data is latched into an 8PIO IN port by a positive-going transition on the LATCH INPUT line which is controlled by the user. Handshake signals are provided on both the IN and OUT ports.

I/O port number 6 plays a special role on the 8PIO. It may be left in its factory-wired condition to software monitor and control the other seven 8PIO ports, or alternately, it may be re-configured as a standard eighth I/O port.

The 8PIO provides three on-board terminal I/O devices: an 8-bit switch register, a 3-bit switch

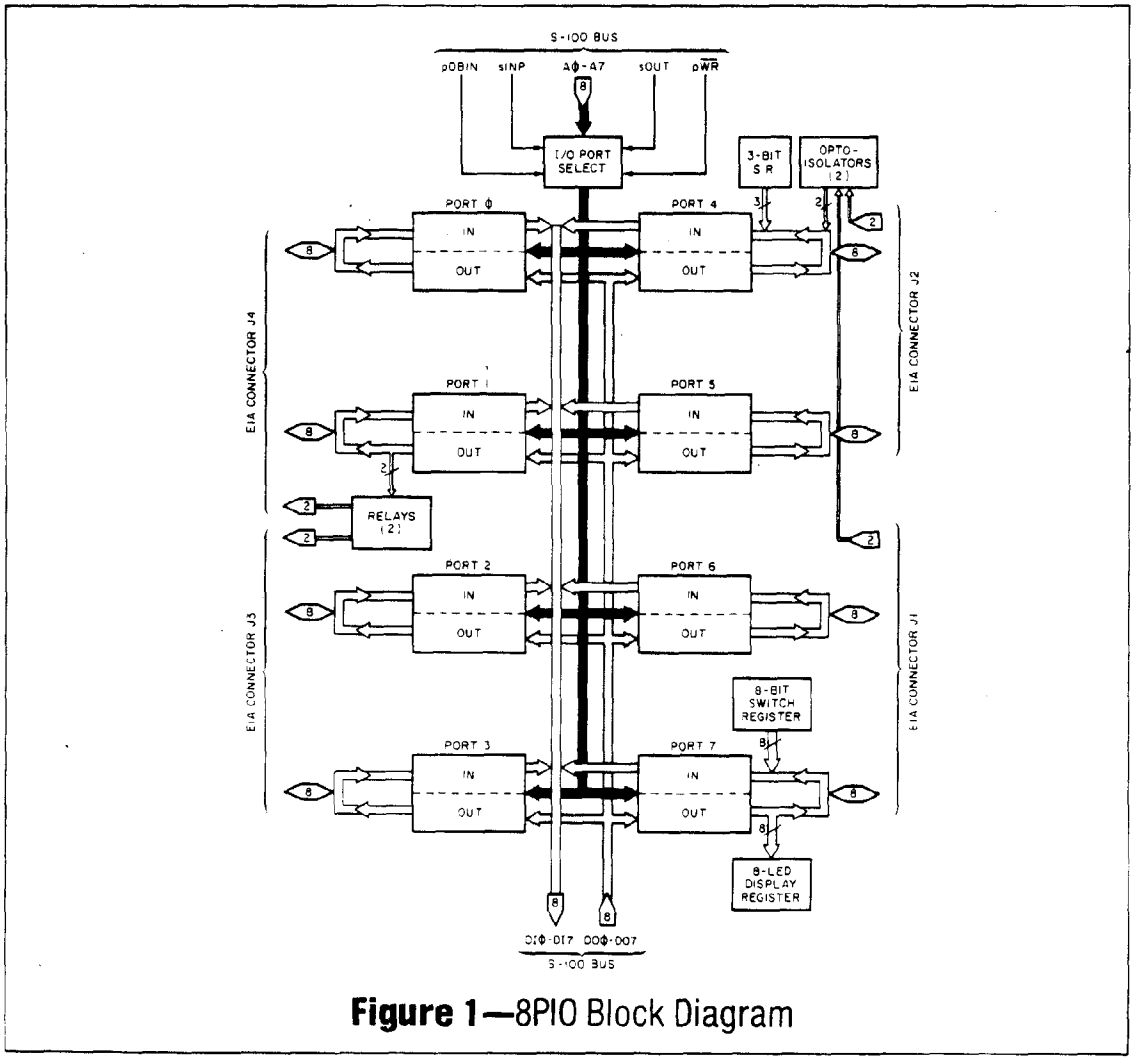


Figure 1—8PIO Block Diagram

register and an 8 LED display register. The 8PIO also features four versatile interfacing circuits: a pair of OUT port activated relays and a pair of optically isolated couplers connected to an IN port. All of these devices are connected to the 8PIO in a non-dedicated fashion: they may be either used or left unused in a way that leaves all ports available for I/O with other devices.

Technical Specifications

Number of I/O ports:	8
I/O port description:	Each I/O port 8-bit parallel, bi-directional, separate latched input and latched output with handshake.
Output port handshake:	Separate $\overline{\text{OUTPUT STROBE}}$ line for each OUT port. These clock derived lines go low 1.Ø-1.5 μsec after output instruction and remain low for 1.Ø μsec.
Input port handshake:	Each IN port status line connected to bits of port IN 6 for software polling.
Output port drive:	4 TTL unit loads.
Input port loading:	3.5 TTL unit loads.
Relay contact ratings:	2 amperes @ 28 volts.
Opto-isolator input:	Logic Ø = Ø volts @ Ø mA, Logic 1 = 5 volts @ 25 mA.
Switch registers:	One 3-bit S.R. connected to port IN 4; one 8-bit S.R. connected to port IN 7.
LED display register:	Eight LEDs connected to port OUT 7.
I/O connectors:	Four 8PIO 26-pin connector strips mate with 25-lead flat ribbon cable terminated with 25-pin female EIA connector.
Power:	+5 volts @ 1.5 amperes.
Bus compatibility:	S-1ØØ.
Environment:	Ø to 55 degrees Celsius.

Section 2
Operating Instructions

Operating Instructions

To operate the 8PIO in your S-100 bus system, you must assign the board a Base Address, install interface cabling between the 8PIO and your terminal I/O devices, then write and execute software to control the parallel data transfers between the CPU and the system terminal devices.

2.1 Assigning An 8PIO Base Address

There are eight parallel I/O ports on the 8PIO card. Each I/O port consists of a separate 8-bit IN port and an 8-bit OUT port which share the same eight bi-directional data lines. The eight sets of bi-directional lines are brought out to EIA connectors J1 thru J4 for I/O interfacing (see Figure 2).

The system CPU writes one byte of parallel data to an 8PIO OUT port by executing an OUT [port],A instruction, and inputs one byte of parallel data by executing an IN A,[port] instruction, where '[port]' is an assigned 8PIO port address. 8PIO I/O port addresses are assigned at the lower of two DIP switch packages mounted on the 8PIO board (see

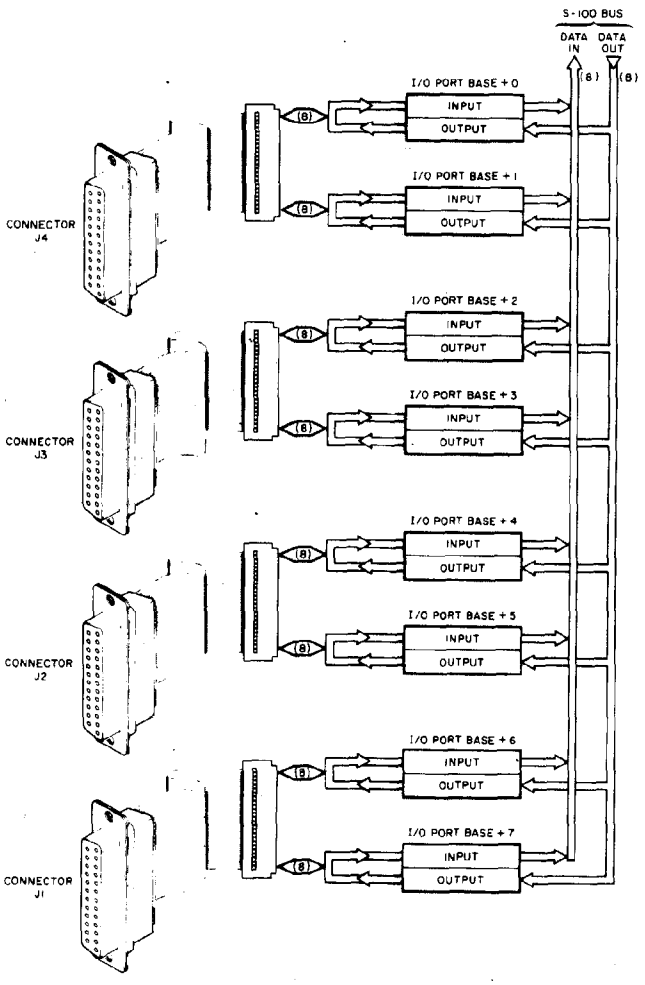


Figure 2—8PIO Parallel Data Paths

Figure 3). Five of the eight DIP switch positions are used to select the 8PIO **Base Address** (see Figure 4), while the remaining three switches form a 3-bit input switch register which is connected to port IN 4 (see Section 2.6).

The 8PIO **Base Address** defines the five most significant S-100 address bits A7, A6, A5, A4, A3 which select the 8PIO board, and the remaining three address bits A2, A1, A0 define the Base Address **Offset**. The three bit offset selects one-of-eight ports on an addressed 8PIO board. 8PIO port 0 is defined to have an offset of 0 from the Base Address, I/O port 1 is defined to have an offset of +1 from the Base Address, and so on.

Positioning a Base Address switch ON conditions the 8PIO to respond to a logic 1 level on its corresponding address line; an OFF switch responds to logic 0.

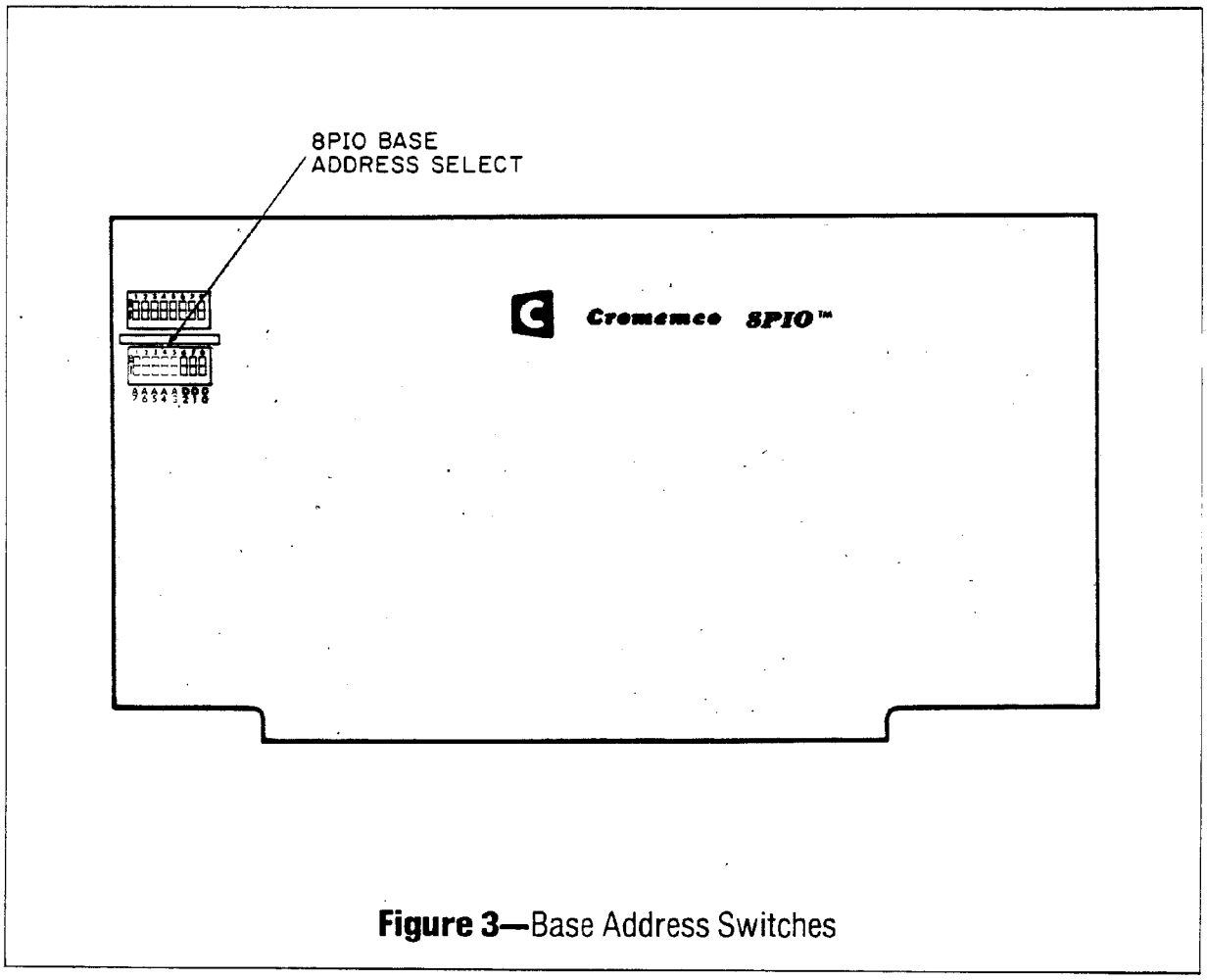


Figure 3—Base Address Switches

Example 1

—Setting Base Address switches A7 thru A3 OFF (logic Ø) maps the 8PIO into port addresses ØØH (port Ø) thru Ø7H (port 7).

—Setting Base Address switches A7 thru A3 ON (logic 1) maps the 8PIO into port addresses ØF8H (port Ø) thru ØFFH (port 7).

—Setting A3 thru A5 ON and A6 and A7 OFF (see Figure 4) maps the 8PIO into port addresses 38H (port Ø) thru 3FH (port 7). ■

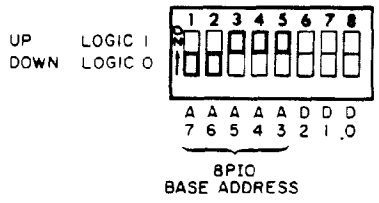


Figure 4
Example Base Address Switch Settings

In the example above and throughout the remainder of this manual, 'port Ø' will refer to the lowest assigned 8PIO port address (with Ø offset) and 'port 7' will refer to the highest assigned port address (with an offset of +7).

If two or more 8PIO boards are installed in the same S-1ØØ bus system, the boards should be assigned distinct and non-overlapping Base Addresses, otherwise a conflict will result when inputting I/O data to the CPU. NOTE: Base Addresses ØØH and 3ØH are already used by Cromemco's 4FDC floppy disc controller; 4ØH is used by Cromemco's memory boards with BANK SELECT; and 5ØH is used by Cromemco's PRI printer interface. Do not assign the 8PIO a conflicting Base Address if your system contains any of these Cromemco parts.

After a Base Address has been assigned, the 8PIO may be installed in any empty S-1ØØ bus slot. NOTE: Never insert or remove an 8PIO board or board parts with the system power ON. Interfacing cables may then be installed connecting 8PIO terminal strips J1 thru J4 to the system terminal I/O devices. After installing interface cabling, parallel data may be transferred between the CPU and your system terminal devices under software control (see Sections 2.3 and 2.4).

2.2 8PIO Interface Cabling

Cromemco provides two interface cables which are plug compatible with 8PIO connectors J1-J4; Part No. 519-ØØ17 (62 cm, $15) and Part No. 519-ØØ18 (11Ø cm, $15). Each of these cable assemblies consists of a 26-pin female connector which mates with one 8PIO terminal strip connector J1-J4, a 25-conductor flat ribbon cable of length 62 cm/11Ø cm, and a 25-pin female DB-25S EIA terminating connector. Your I/O terminal devices should be equipped with a mating 25-pin male DB-25P EIA connector when using either of these Cromemco supplied cables.

Carefully note that all J1, J2, J3 and J4 **pin numbers** referenced in this manual and in the 8PIO schematic refer to **DB-25S EIA pin numbers** (see Figure 5), and not to J1 thru J4 pin-outs on the 8PIO board itself. Cromemco supplied cables must be installed by aligning the arrow head near each connector strip on the printed circuit board with the ribbon **cable stripe** (the colored edge of the ribbon cable). With the cable stripe properly aligned, the pin-outs of EIA connectors J1 thru J4 are shown in Table 1.

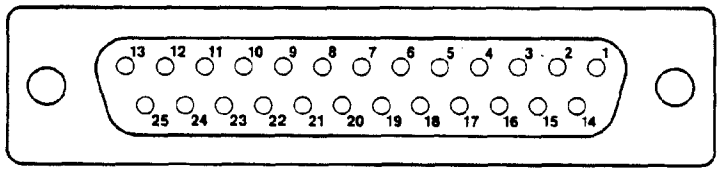


Figure 5—J1 Thru J4 Pin Numbers

Table 1—EIA Connector J1 Thru J4 PIN-OUTS

Pin	Connector J1	Connector J2	Connector J3	Connector J4
1	$\overline{\text{OUTPUT STROBE 6}}$	$\overline{\text{OUTPUT STROBE 4}}$	$\overline{\text{OUTPUT STROBE 2}}$	$\overline{\text{OUTPUT STROBE Ø}}$
2	$\overline{\text{OUTPUT ENABLE 6}}$	$\overline{\text{OUTPUT ENABLE 4}}$	$\overline{\text{OUTPUT ENABLE 2}}$	$\overline{\text{OUTPUT ENABLE Ø}}$
3	LATCH INPUT 6	LATCH INPUT 4	LATCH INPUT 2	LATCH INPUT Ø
4	BIT DØ PORT 6	BIT DØ PORT 4	BIT DØ PORT 2	BIT DØ PORT Ø
5	BIT D1 PORT 6	BIT D1 PORT 4	BIT D1 PORT 2	BIT D1 PORT Ø
6	BIT D2 PORT 6	BIT D2 PORT 4	BIT D2 PORT 2	BIT D2 PORT Ø
7	BIT D3 PORT 6	BIT D3 PORT 4	BIT D3 PORT 2	BIT D3 PORT Ø
8	BIT D4 PORT 6	BIT D4 PORT 4	BIT D4 PORT 2	BIT D4 PORT Ø
9	BIT D5 PORT 6	BIT D5 PORT 4	BIT D5 PORT 2	BIT D5 PORT Ø
1Ø	BIT D6 PORT 6	BIT D6 PORT 4	BIT D6 PORT 2	BIT D6 PORT Ø
11	BIT D7 PORT 6	BIT D7 PORT 4	BIT D7 PORT 2	BIT D7 PORT Ø
12	$\overline{\text{OUTPUT STROBE 7}}$	$\overline{\text{OUTPUT STROBE 5}}$	$\overline{\text{OUTPUT STROBE 3}}$	$\overline{\text{OUTPUT STROBE 1}}$
13	$\overline{\text{OUTPUT ENABLE 7}}$	$\overline{\text{OUTPUT ENABLE 5}}$	$\overline{\text{OUTPUT ENABLE 3}}$	$\overline{\text{OUTPUT ENABLE 1}}$
14	LATCH INPUT 7	LATCH INPUT 5	LATCH INPUT 3	LATCH INPUT 1
15	BIT DØ PORT 7	BIT DØ PORT 5	BIT DØ PORT 3	BIT DØ PORT 1
16	BIT D1 PORT 7	BIT D1 PORT 5	BIT D1 PORT 3	BIT D1 PORT 1
17	BIT D2 PORT 7	BIT D2 PORT 5	BIT D2 PORT 3	BIT D2 PORT 1
18	BIT D3 PORT 7	BIT D3 PORT 5	BIT D3 PORT 3	BIT D3 PORT 1
19	BIT D4 PORT 7	BIT D4 PORT 5	BIT D4 PORT 3	BIT D4 PORT 1
2Ø	BIT D5 PORT 7	BIT D5 PORT 5	BIT D5 PORT 3	BIT D5 PORT 1
21	BIT D6 PORT 7	BIT D6 PORT 5	BIT D6 PORT 3	BIT D6 PORT 1
22	BIT D7 PORT 7	BIT D7 PORT 5	BIT D7 PORT 3	BIT D7 PORT 1
23	+OPTO D3 PORT 4	+OPTO D4 PORT 4	RELAY DØ PORT 1	RELAY D1 PORT 1
24	-OPTO D3 PORT 4	-OPTO D4 PORT 4	RELAY DØ PORT 1	RELAY D1 PORT 1
25	GROUND RETURN	GROUND RETURN	GROUND RETURN	GROUND RETURN

$\overline{\text{OUTPUT STROBE}}$: Handshake signal which transitions low 1.Ø - 1.5 μsec after the CPU Outputs data to an OUT port (Section 2.3).

$\overline{\text{OUTPUT ENABLE}}$: Output port control line. A low level enables the OUT port; a high level tri-states the OUT port (Section 2.3).

LATCH INPUT: Level sensitive control line which latches input data into an IN port (Section 2.4).

BIT DX PORT Y: Bi-directional data line connected to bit X of I/O port Y.

+OPTO: Anode end of LED diode input to opto-isolator. Output of phototransistor connected to D3 and D4 of port IN 4 (Section 2.8).

-OPTO: Cathode end of LED diode input to opto-isolator. Output of phototransistor connected to D3 and D4 of port IN 4 (Section 2.8).

RELAY: Relay output contacts. Relay driven by output bit DØ or D1 from port OUT 1 (Section 2.9).

After the cables have connected the 8PIO and your I/O devices, you are ready to transfer TTL-level data over pins 1 thru 22, and non-TTL level data over pins 23 and 24.

2.3 Outputting Data

One byte of data is transferred from CPU Reg. A over S-1ØØ bus data-out lines DOØ-DO7 to an 8PIO output port by executing an OUT [port],A instruction, where '[port]' is a user-assigned 8PIO port address (see Section 2.1). Executing such an instruction causes the OUT port's handshake line $\overline{\text{OUTPUT STROBE}}$ (available on EIA connectors J1-J4 at pin 1 or 12) to pulse low. The timing of $\overline{\text{OUTPUT STROBE}}$ relative to the output instruction which initiates it is shown in Figure 6. Either the rising or falling edge of $\overline{\text{OUTPUT STROBE}}$, or its active-low level, may be used to latch or gate the data byte from the 8PIO output port to a terminal device connected to it.

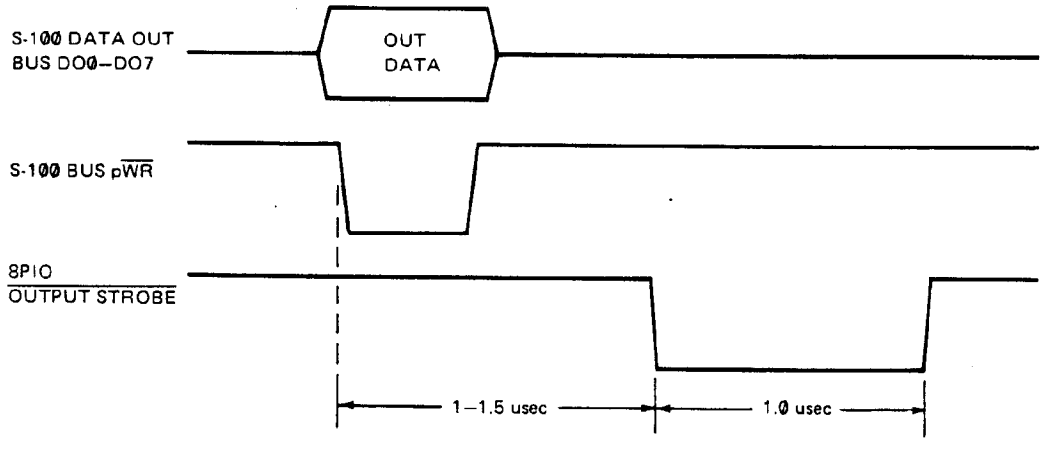


Figure 6—Handshake Signal $\overline{\text{Output Strobe}}$ Timing

Writing a data byte to an 8PIO OUT port does latch (or save) the data byte in an OUT port until a later data byte over-writes it, but it does **not** automatically make the parallel data available at EIA connectors J1-J4; each 8PIO OUT port must be individually **enabled** (brought out of its tri-state, or floating outputs condition) before the data byte actively drives J1-J4 bi-directional data pins DØ-D7.

8PIO ports OUT Ø-OUT 5 and OUT 7 may be enabled in two ways. The first method is driving the port's OUTPUT ENABLE line low (available at J1-J4 at pin 2 or 13); the second is by programmatically forcing the appropriate OUT 6 control bit to the logic 1 state (see Section 2.5 for full details). These two enabling sources, one hardware and the other software controlled, are "wire-ORed" together as shown in Figure 7. An enable from either source, or both, will enable the target 8PIO output port.

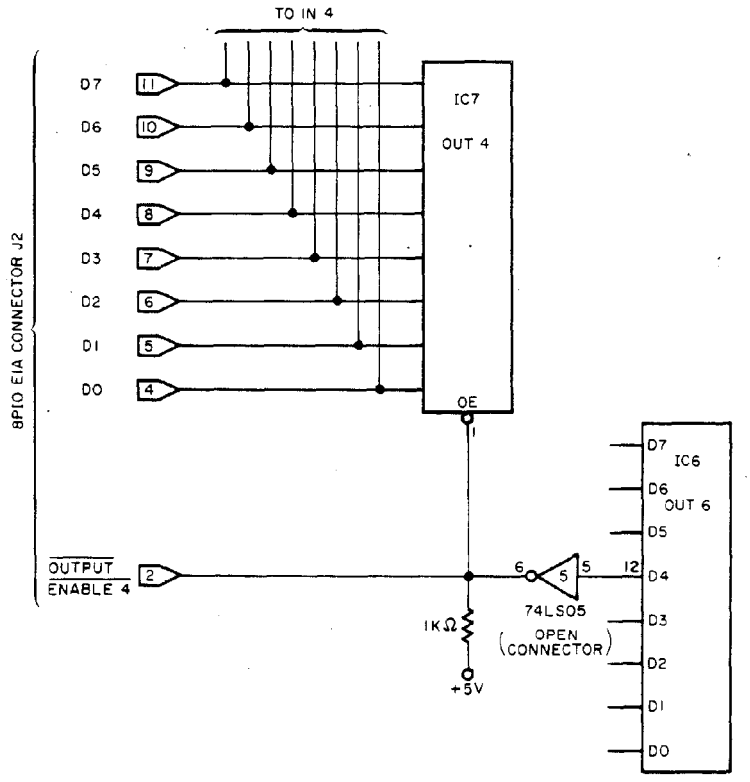


Figure 7—TRI-STATE Control of OUT 4

Example 2

Suppose you assign your system 8PIO board Base Address 80H. Further assume you assign 8PIO port OUT 4 the task of parallel loading a presettable 74196 BCD Decade Counter. The counter could be interfaced to the 8PIO as illustrated in Figure 8. Executing instruction OUT [84H],A then latches 8-bits of Reg. A data into OUT 4 and forces the OUTPUT STROBE 4 line to pulse low. This pulse enables OUT 4 gating the low-order nybble D0-D3 to the 74196 parallel load inputs A, B, C and D, and asserts the 74196 PARALLEL LOAD input pin active low, thereby presetting the counter. ■

Example software to accomplish this task is shown below:

```
                    ;
                    ; PRESET 74196 COUNTER EXAMPLE
                    ;
                    ; THIS SUBROUTINE PRESETS A 74196 BCD COUNTER
                    ; TO VALUE (COUNT) WHEN INTERFACED TO A
                    ; CROMEMCO 8PIO BOARD AS SHOWN IN FIGURE 8
                    ;
                    BASE:   EQU     80H             ;8PIO BASE ADDRESS
                    PRESET: ORG     8000H
8000    3A0680              LD      A,(COUNT)       ;COUNT TO REG. A
8003    D384                OUT     BASE+4,A        ;LOW NYBBLE TO 74196
8005    C9                  RET                     ;RETURN
8006    01          COUNT:  DB      1               ;PRESET TO COUNT=1
                            END     PRESET
```

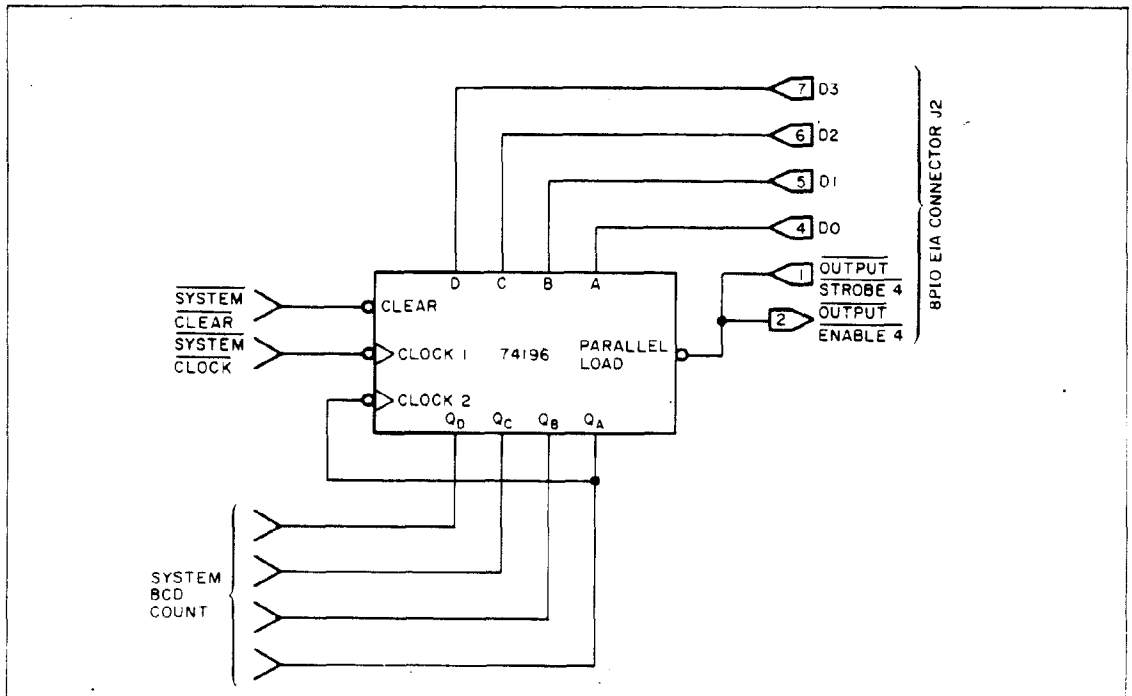


Figure 8—Example 2 Schematic

At this point, it's appropriate to reiterate that each 8PIO OUT port shares eight bi-directional data lines DØ-D7 with its correspondingly numbered IN port. The OUTPUT ENABLE control lines effectively define the direction of data flow over these bi-directional lines; when OUTPUT ENABLE is active low, parallel data flows from an 8PIO OUT port to its associated terminal device. When OUTPUT ENABLE is inactive high, the data lines are "turned around" to the input mode wherein external devices may actively drive the bi-directional lines (without conflict from floating 8PIO OUT ports) for the purpose of inputting parallel data to 8PIO IN ports.

2.4 Inputting Data

Transferring parallel data from an external input device to the system CPU is a two-step process. First, the data byte is loaded into an 8PIO IN port by asserting the port's LATCH INPUT control line. Then, the system CPU reads the IN port contents by executing an IN A,[port] instruction, where '[port]' is a user-assigned 8PIO port address.

Each 8PIO input port consists of a 74LS373 octal latch and supporting circuitry. Parallel TTL-level input data at EIA connectors J1-J4 drive the eight latch input lines. The LATCH INPUT control lines (also available at J1-J4) are used to load a byte into a latch. When LATCH INPUT is high, the latch contents follow (equal) the latch inputs. When the LATCH INPUT line is forced low, the data set up at the latch inputs are stored in the latch. Thus, applying a positive pulse (PW = 15 nsec [min]) to the LATCH INPUT line allows the user to sample input data at the time of the pulse, and tying the LATCH INPUT line high (or letting the line float since it is tied to +5 volts thru a pull-up resistor) allows the CPU to sample the input data in real time.

A high level on a LATCH INPUT line resets an RS flip flop provided with each IN port. The eight flip flop outputs, which then indicate IN port empty/full status, are connected to port IN 6 for input port software polling (see Section 2.5). Reading the contents of an 8PIO IN port by executing an IN A, [port] instruction sets the RS flip flop, but does not change the contents of the port.

When inputting parallel data from an external input device, one must be sure to turn the bi-directional data lines DØ-D7 around to the input mode (by forcing OUTPUT ENABLE high) to preclude a bus conflict between the external device and the OUT port on the same data lines (see Section 2.3). In implementations where an 8PIO OUT port only "talks" to its own IN port, no bus conflict is possible.

Example 3

Suppose a certain application requires the sampling of a real time BCD seconds clock. The sample implementation described here uses two cascaded 74LS90 decade counters driven by a 1.00 Hz clock. The BCD counter outputs are asynchronously read thru 8PIO port IN 2 (see Figure 9). Note that the LATCH INPUT line is tied high forcing the contents of IN 2 to follow the counter in real time. Also note that OUTPUT ENABLE is tied high which defines the bi-directional lines as input lines only. The counters are preset to count 00 by executing an OUT [BASE+2],A instruction. The contents of Reg. A is irrelevant to the preset operation; only the low pulse on the OUTPUT STROBE is used. ■

Sample software is shown ahead.

```
                        ;
                        ;  SAMPLE BCD SECONDS EXAMPLE PROGRAM
                        ;
                        ; THIS SUBROUTINE SAMPLES A REAL TIME
                        ; BCD SECONDS CLOCK WHEN A CROMEMCO
                        ; 8PIO BOARD IS INTERFACED AS SHOWN IN
                        ; FIGURE 9.  THE SAMPLED TIME IS PLACED
                        ; IN LOCATION 'TIME'.  THE SUBROUTINE
                        ; CHANGES THE CONTENTS OF REG. A
                        ;
                        BASE:   EQU     20H             ;8PIO BASE ADDRESS
                                ORG     8000H
8000    DB22            BCDSEC: IN      A,BASE+2        ;READ BCD SECONDS
8002    3A0680                  LD      (TIME),A        ;STORE IN LOC. TIME
8005    C9                      RET                     ;RETURN
8006    00              TIME:   DB      0               ;INITIALIZE TO 00
                                END     BCDSEC
                        ;
                        ; THIS SUBROUTINE PRESETS THE BCD
                        ; COUNTERS TO 00 SECONDS. THE CONTENTS
                        ; OF REG. A IS IRRELEVANT AND UN-
                        ; CHANGED BY THE SUBROUTINE
                        ;
8007    D322            PRESET: OUT     BASE+2,A        ;PRESET COUNTERS
8009    C9                      RET                     ;RETURN
                                END     PRESET
```

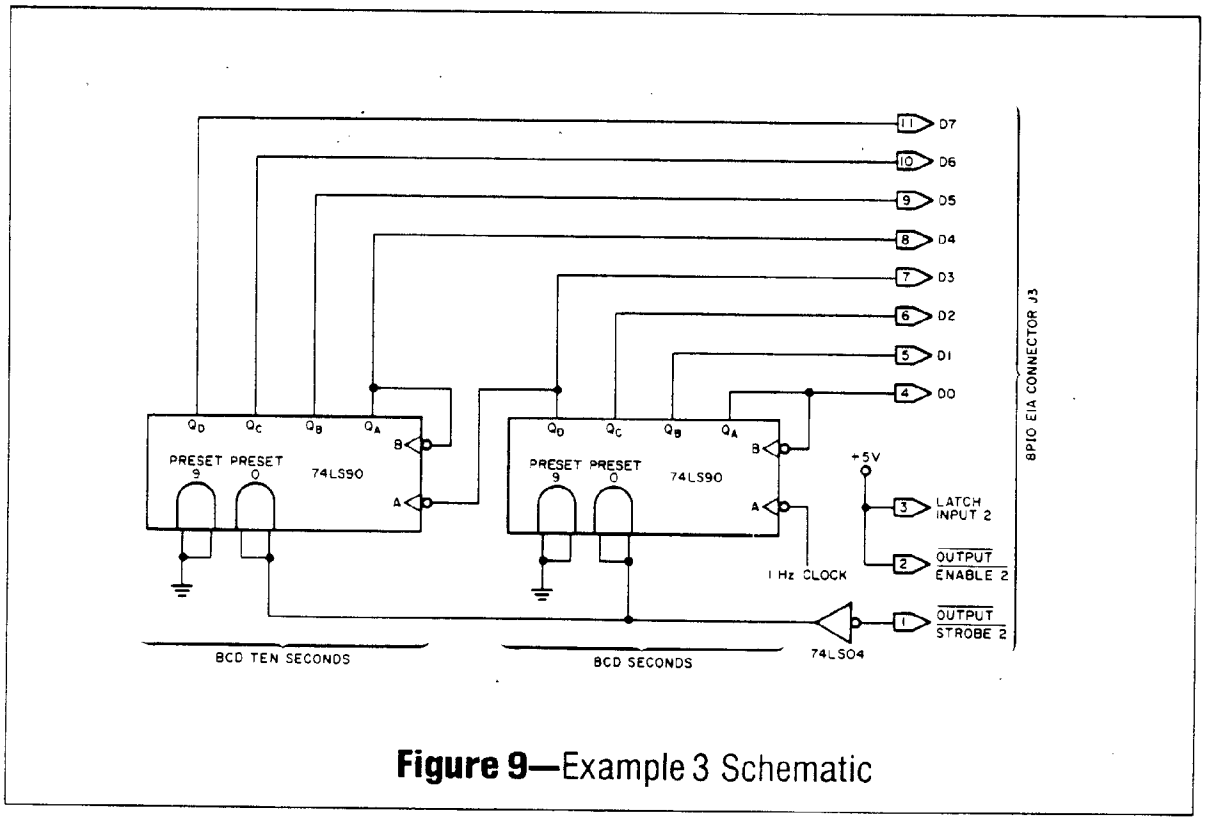


Figure 9—Example 3 Schematic

2.5 8PIO Port 6 Functions

I/O port 6 plays the special role on the 8PIO. In its factory wired condition, the empty/full status of all IN ports may be software polled by the CPU thru port IN 6. All OUT ports (with the exception of port OUT 6) may be enabled or tri-stated under CPU software control thru OUT 6. These software control features may be defeated and IN/OUT 6 wired as a standard eighth I/O port with the simple hardware fix described at the end of this section.

When an IN port's LATCH INPUT control line goes high, a flip flop connected to port IN 6 is reset to logic Ø. When the input port is read by the CPU (an IN A,[port] is executed), the flip flop is set to logic 1. The eight flip flop outputs may be polled at IN 6 with the following interpretation:

Table 2—Polling INPUT Port Status

IN 6 BIT	LOGIC 1	LOGIC Ø
DØ	IN Ø EMPTY	IN Ø FULL
D1	IN 1 EMPTY	IN 1 FULL
D2	IN 2 EMPTY	IN 2 FULL
D3	IN 3 EMPTY	IN 3 FULL
D4	IN 4 EMPTY	IN 4 FULL
D5	IN 5 EMPTY	IN 5 FULL
D6	IN 6 EMPTY	IN 6 FULL
D7	IN 7 EMPTY	IN 7 FULL

Example 4

Suppose your 8PIO is assigned Base Address 38H. Your software then executes instruction IN A,3EH to sample IN 6, since BASE+6 = 38H+6H. Suppose input byte 1ØØØ11Ø1B is read into Reg. A. This data then indicates that IN ports Ø, 2, 3 and 7 are "empty," and IN ports 1, 4, 5 and 6 are "full" of newly latched data. ■

Example 5

This example presents an IN port software polling program. The program makes the following assumptions:

1) The system CPU is a Z8Ø operating in Interrupt Mode 1 (IM1).

2) The system includes a Cromemco 8PIO board assigned Base Address = ØFØH, and additional external hardware such that a high level on any of the eight 8PIO LATCH INPUT lines interrupts the Z8Ø via its INT input.

3) The interrupt service routine (which begins at address ØØ38H for IM1) polls the 8PIO port INØ first, IN1 second, . . . ,IN7 last.

The program (shown on the next page) consists of a routine starting at Interrupt Mode 1 service address ØØ38H which tests individual bits of IN 6 by rotating them into the carry flag. Bit DØ is tested first, and if it is found to be a Ø (indicating IN Ø is full), a jump to service address 'INØ' is performed. If DØ is a 1 (indicating IN Ø is empty), then D1 is tested in the same fashion, and so on. The program assumes that at least one of the bits DØ-D7 is a Ø, otherwise an interrupt would not have been generated. The second example program segment illustrates a service routine for IN Ø. Note that there would be a service routine for each active IN port. ■

```
                        ;
                        ;  SOFTWARE POLLING EXAMPLE PROGRAM
                        ;
                BASE:   EQU     0F0H            ;8PIO BASE ADDRESS
                        ORG     0038H           ;IM1 SERVICE ADDRESS
0038  F5        POLL:   PUSH    AF              ;SAVE REG'S ON STACK
0039  C5                PUSH    BC              ;       "
003A  E5                PUSH    HL              ;       "
003B  214500            LD      HL,JPTBL-3      ;INITIALIZE HL
003E  010300            LD      BC,3            ;LOAD BC WITH OFFSET
0041  DBF6              IN      A,BASE+6        ;READ IN 6
0043  09        NXTBIT: ADD     HL,BC           ;HL POINTS TO JP ADDR.
0044  1F                RRA                     ;ROTATE LSB INTO CY
0045  38FC              JR      C,NXTBIT        ;1=EMPTY, 0=FULL
0047  E9                JP      (HL)            ;FULL--JUMP TO TABLE
0048  C34080    JPTBL:  JP      IN0             ;
004B  C35080            JP      IN1             ;JP (HL) INSTRUCTION
004E  C36080            JP      IN2             ;FORCES A JUMP TO ONE
0051  C37080            JP      IN3             ;OF THE JP INSTRUCTIONS
0054  C38080            JP      IN4             ;LISTED IN THIS TABLE
0057  C39080            JP      IN5             ;
005A  C3A080            JP      IN6             ;
005D  C3B080            JP      IN7             ;
                        ;
                        ;
                        ; IN 0 SAMPLE SERVICE ROUTINE
                        ; STORES IN 0 DATA IN LOCATION
                        ; 'DATA0'
                        ;
                        ORG     8040H           ;IN 0 SERVICE ADDRESS
8040  DBF0      IN0:    IN      A,BASE+0        ;INPUT PORT 0 DATA
8042  324A80            LD      (DATA0),A       ;STORE IN LOC. DATA0
8045  E1                POP     HL              ;RESTORE REG'S
8046  C1                POP     BC              ;      "
8047  F1                POP     AF              ;      "
8048  FB                EI                      ;ENABLE INTERRUPTS
8049  C9                RET                     ;RETURN
804A  00        DATA0:  DB      0               ;INITIALIZE TO 00H
8050  --        IN1:    --      --              ;IN 1 SERVICE ADDRESS
                        RET
8060  --        IN2:    --      --              ;IN 2 SERVICE ADDRESS
                        RET
  .                       .                                .
  .                       .                                .
  .                       .                                .
80B0  --        IN7:    --      --              ;IN 7 SERVICE ADDRESS
                        RET
                        END     POLL
```

In addition to providing 8PIO IN port software polling, 8PIO port 6 also provides a means of software controlling 8PIO OUT ports. The output lines of port OUT 6 are connected to the OUTPUT ENABLE control lines of each 8PIO OUT port, except OUT 6 itself. Outputting DØ=Ø at OUT 6 tri-states (or floats) the output lines of OUT Ø (unless an external device forces OUTPUT ENABLE Ø low); outputting DØ=1 at OUT 6 enables the output lines of OUT Ø. The other bits of OUT 6 control corresponding OUT ports in a similar fashion. Table 3 summarizes this behavior.

Port OUT 6 drives the tri-state control lines with open collector drivers (see Figure 7). Thus, an OUT port may be enabled either by a logic 1 bit from OUT 6 or by a low at its OUTPUT ENABLE line (available at J1-J4). Note that OUT 6 controls the other 8PIO OUT ports even when OUT 6 is in its tri-state, or floating condition.

Table 3—PORT OUT 6 TRI-STATE Control

PORT OUT 6 BIT	LOGIC 1	LOGIC Ø
DØ	ENABLE PORT Ø	TRI-STATE PORT Ø
D1	ENABLE PORT 1	TRI-STATE PORT 1
D2	ENABLE PORT 2	TRI-STATE PORT 2
D3	ENABLE PORT 3	TRI-STATE PORT 3
D4	ENABLE PORT 4	TRI-STATE PORT 4
D5	ENABLE PORT 5	TRI-STATE PORT 5
D6	USED AS I/O LINE ONLY	
D7	ENABLE PORT 7	TRI-STATE PORT 7

Example 6

Suppose you have a system with an 8PIO board assigned to Base Address ØFØH, and you execute the sample program below. This program would then enable OUT Ø, OUT 2, OUT 3 and OUT 7, and would tri-state OUT 1, OUT 4 and OUT 5. ■

You may defeat either one, or both, port 6 software control capabilities by performing the hardware fixes described below. With both fixes performed, I/O port 6 becomes a standard eighth 8PIO I/O port. In this mode, all output ports are tri-state controlled by their OUTPUT ENABLE lines at J1-J4 only, and no software polling capability exists.

1) Remove IC4 and IC19 to disable the IN 6 polling capability.

2) To disable the OUT 6 tri-state control capability and to configure OUT 6 as a standard output port, remove IC5, then lift IC14 pin 11 from its socket hole.

```
                        ;
                        ; PORT OUT 6 TRI-STATE
                        ; CONTROL PROGRAM EXAMPLE
                        ;
                BASE:   EQU     ØFØH            ;8PIO BASE ADDRESS
                        ORG     8ØØØH
8ØØØ    3EFD    OUTCTL: LD      A,1ØØØ11Ø1B     ;CONTROL BYTE
8ØØ2    D3F6            OUT     BASE+6,A        ;OUTPUT TO 8PIO PORTS
8ØØ4    C9              RET                     ;RETURN
                        END     OUTCTL
```

2.6 8PIO Switch Registers

The 8PIO provides two on-board switch registers; a 3-bit S.R. connected to port 4 data lines DØ-D3, and an 8-bit S.R. connected to port 7 data lines DØ-D7. The registers are located on the two DIP switch packages shown in Figure 1Ø.

Refer to the 8PIO schematic and notice that the S.R. switches hold bi-directional data lines at ground potential when closed (ON). Thus, when a switch register is being used as an input device, no other device should compete with it for data line use. Likewise, if a switch register is not in use, all switches should be left open (OFF) to free their associated data lines.

To input a logic 1 bit from a switch register, the switch should be positioned OFF (down). To input a logic Ø bit, the switch should be positioned ON (up). Do not use the numerals printed on the switch DIPs for bit numbering, but rather refer to the 8PIO silk screened legend or refer to Figure 11 below.

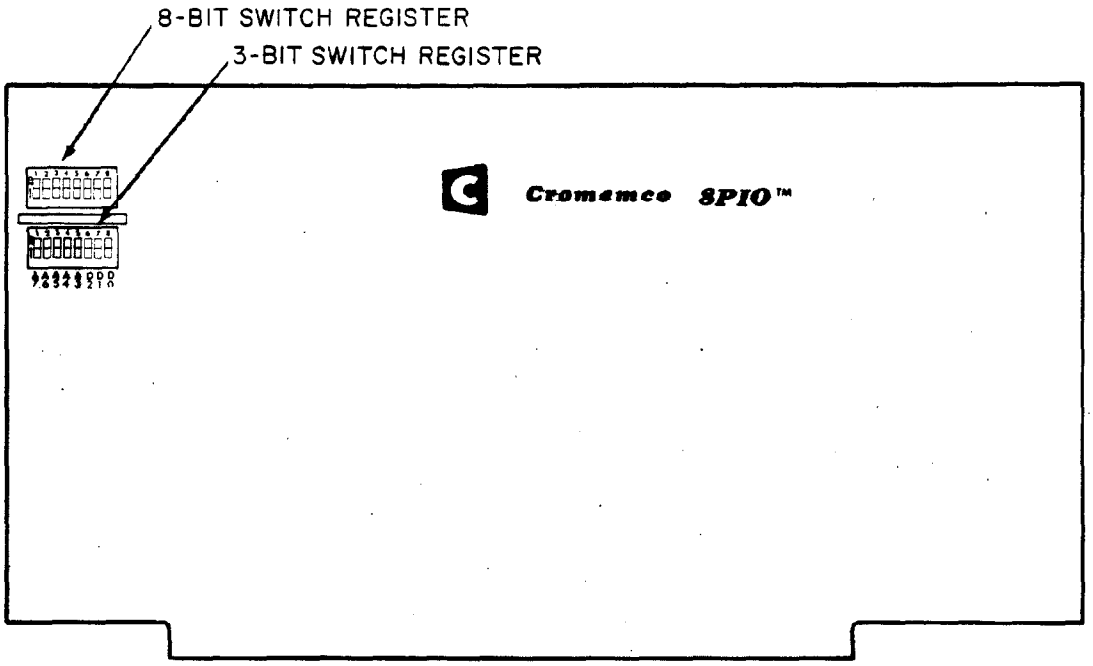


Figure 10—8PIO Switch Register Locations

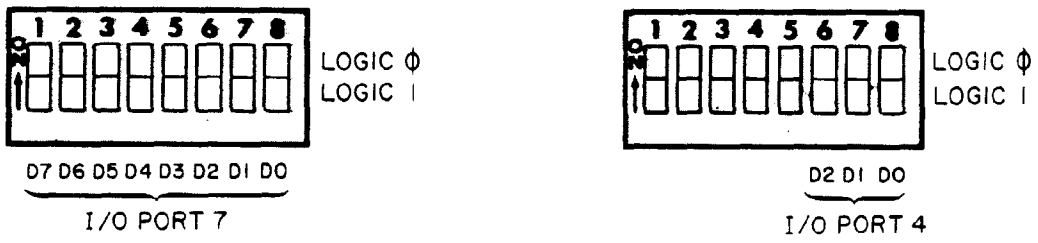


Figure 11—8PIO S.R. Bit Assignments

2.7 8PIO LED Display Register

The 8PIO provides an on-board 8-bit LED display register connected to OUT 7. Refer to the 8PIO schematic and notice that port OUT 7, implemented in two 74175s, is isolated from the bi-directional port 7 lines DØ-D7 by 74LS244 buffer/drivers. The LEDs, in turn, are driven by 74LS240s connected directly to port OUT 7. This arrangement results in the LEDs always indicating the contents of port OUT 7, even if the 8-bit switch register connected to I/O port 7 is simultaneously in use. The 8-bit switch register may ground I/O port 7 data lines as the 72LS244 buffer/drivers are short circuit protected.

Example 7

The example program below displays the 8PIO 8-bit switch register contents in the LED display register. ■

```
                    ;
                    ; LED DISPLAY (8-BIT S.R.)
                    ;
                    BASE:   EQU     50H             ;8PIO BASE ADDRESS
                            ORG     8000H
8000    DB57        DISPSR: IN      A,BASE+7        ;INPUT THE S.R.
8002    D357                OUT     BASE+7,A        ;OUTPUT TO LEDS
8004    C9                  RET                     ;RETURN
                            END     DISPSR
```

2.8 8PIO Dual OPTO-ISOLATORS

The 8PIO features an MCT66 dual phototransistor optoisolator interfacing circuit to provide complete electrical isolation between an I/O device and the S-100 bus. A useful application might be a TTY interface where isolation is desirable due to the large inductive voltage spikes often present on the TTY ground line.

The isolator inputs are at J1 pins 23 and 24, and at J2 pins 23 and 24. The isolator outputs are connected to bits D3 and D4 of port IN 4 (see Figure 12 below).

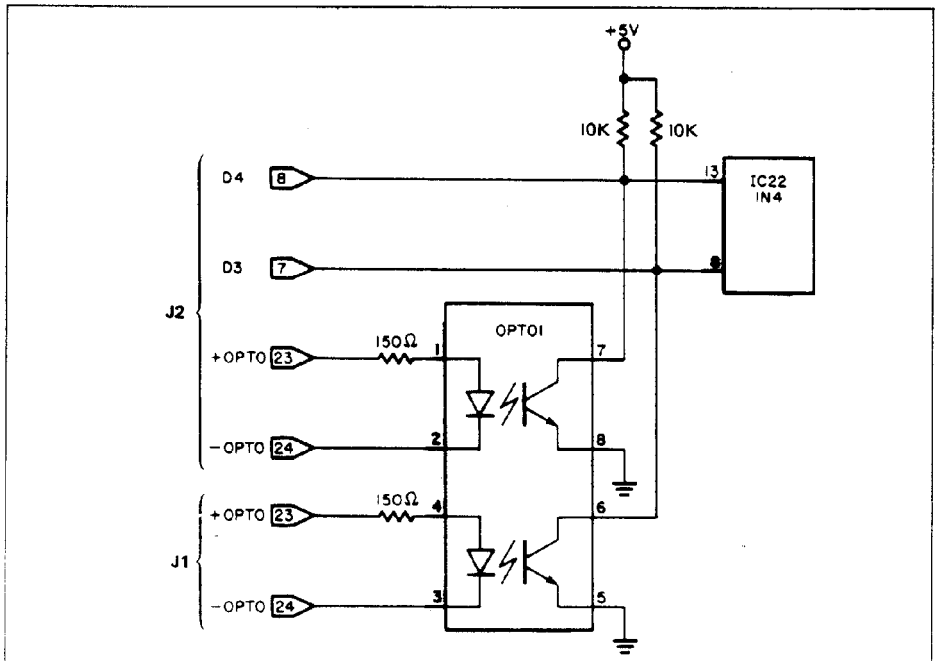


Figure 12—8PIO Dual OPTO-ISOLATORS

The phototransistor inputs are current limited with a 150 ohm resistor which anticipates digital drive voltages of 0v and 5v. Applying 5v with pin 23 more positive than pin 24 results in a forward current of approximately 25 mA. This forward current lights an internal input LED which brings the phototransistor into its conduction region resulting in a logic 0 input bit to IN 4 (an input voltage near 0v). Applying 0v to the input LED results in no emitted light which leaves the transistor OFF resulting in a logic 1 input bit to IN 4 (an input voltage near +5v due to the 1K pull-up resistor).

If higher applied voltages are used, a larger current limiting resistance value is needed. The input LED maximum rated forward current is 60 mA; its "knee" voltage is approximately 1.25 volts, and a typical operating forward current is 25 mA. An appropriate total series current limiting resistance is then approximated by:

$$R = [V(applied) - 1.25\ volts] / 25\ mA$$

Even though the MCT66's coupled isolation voltage is rated at 1500 volts, for safety reasons Cromemco recommends that no steady-state voltage higher than 45 volts with respect to S-100 bus system ground be applied between any pins of J1, J2, J3, or J4.

2.9 8PIO Relays

The 8PIO contains two on-board relays which are controlled by OUT 1 bits D0 and D1. Outputting a logic 0 energizes the relay electromagnet and moves the contact; outputting a logic 1 leaves the relay contact in its "normal," or un-energized position. 8PIO's are factory shipped with the relay contacts jumper wired in a normally closed (NC) condition, although they may easily be modified to a normally open (NO) condition. To do this, carefully cut the existing foil trace connecting 8PIO pads labeled "23" and "NC" (located to the left of each relay). Then, connect pads labeled "23" and "NO" with an insulated jumper wire.

The relay contacts are available at EIA connectors J3 and J4 at pins 23 and 24 (see Figure 13). The relay output contacts are rated at 2 amps at 28 VDC. Cromemco recommends you do **not** use the relay contacts to make and break 120 VAC circuits.

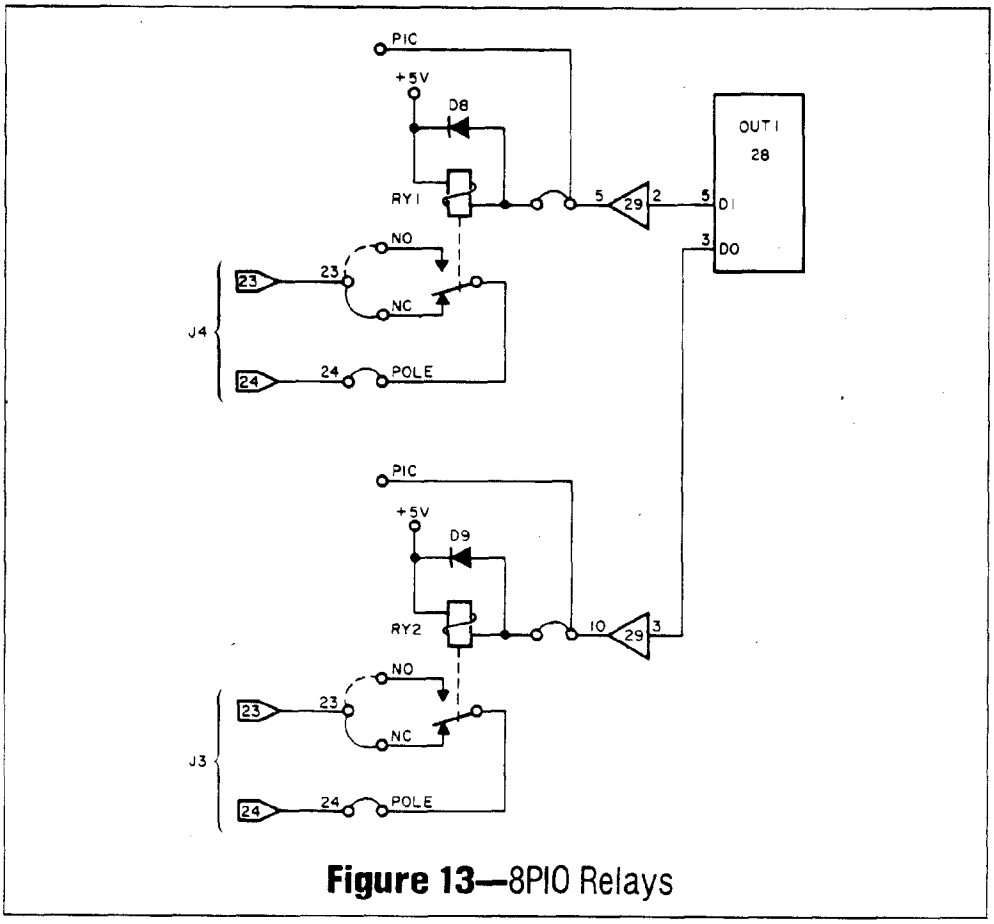


Figure 13—8PIO Relays

2.10 8PIO Initialization

If you leave 8PIO port 6 in its factory wired condition monitoring and controlling the other 8PIO ports, the board should then be initialized as described below after each system RESET. The initialization process consists of two parts: setting all polled IN port status flip flops to indicate "empty," and either enabling or tri-stating all OUT ports as required by your system configuration.

When a system RESET occurs, the S-100 bus line pRESET is momentarily forced low. This low level clears 8PIO ports OUT 7 and OUT 6, and clearing OUT 6 in turn tri-states ports OUT 0-OUT 5 and OUT 7. The OUT ports may then be selectively enabled or tri-stated by outputting a control byte to OUT 6 formatted as shown in Section 2.5, Table 3. Enabling an OUT port effectively defines its eight bi-directional I/O lines as **output lines only.** Tri-stating an OUT port implies the I/O lines may be used for both input and output, with the data direction hardware defined with the OUTPUT ENABLE lines at connectors J1-J4.

The polled IN status flip flops may be set (indicating "empty," or no new input data) by inputting data from each IN port after each system RESET (status flip flops are automatically set when the CPU reads data from an IN port). If all IN ports are software polled, then eight separate input instructions must be executed, one to each port.

Parts List

ICs		Part No.
IC1	74LS240	010-0038
IC2	74LS244	010-0100
IC3	74LS373	010-0102
IC4-5	74LS05	010-0065
IC6	74LS273	010-0107
IC7-10	74LS374	010-0133
IC11	74LS244	010-0100
IC12-13	74LS374	010-0133
IC14-15	74LS136	010-0050
IC16-17	74175	010-0006
IC18	74LS279	010-0039
IC19	74LS05	010-0065
IC20	74LS244	010-0100
IC21-27	74LS373	010-0102
IC28	754508	010-0103
IC29-30	7805	012-0001
IC31	74LS04	010-0066
IC32	74LS279	010-0039
IC33-34	74LS138	010-0096
IC35	74LS244	010-0100
IC36	74LS10	010-0063
IC37	74LS138	010-0096
IC38	74LS75	010-0054
IC39	74LS00	010-0069
IC40	74164	010-0043

Miscellaneous	Part No.
1 Heatsink	021-0017
2 DIP Switch, 8 Pole	013-0002
4 Screws, 6-32 x ½	015-0044
4 Hex Nuts, 6-32	015-0013
4 #6 Lock Washers	015-0020
OPT01 Dual Opto-Isol.	012-0010
RY1-2 Relays, SPDT 5V	013-0019
J1-4 Connector Strip	017-0030
L1-4 Inductor 22 μH	007-0000
PC Board	020-0022
10 Spring Sockets	017-0057
Silicon Pad	021-0109

Resistors		Part No.
R1-2	150	001-0008
R3-4	1K	001-0018
R5	4.7K	001-0024
R6	10K	001-0030
R7	1K	001-0018
R8	10K	001-0030
R9	4.7K	001-0024
R10-11	2.2K	001-0021

Resistor Networks		Part No.
RN1	180 SIP 10 PIN	003-0028
RN2-9	1K SIP 10 PIN	003-0011
RN10-11	1K SIP 8 PIN	003-0007

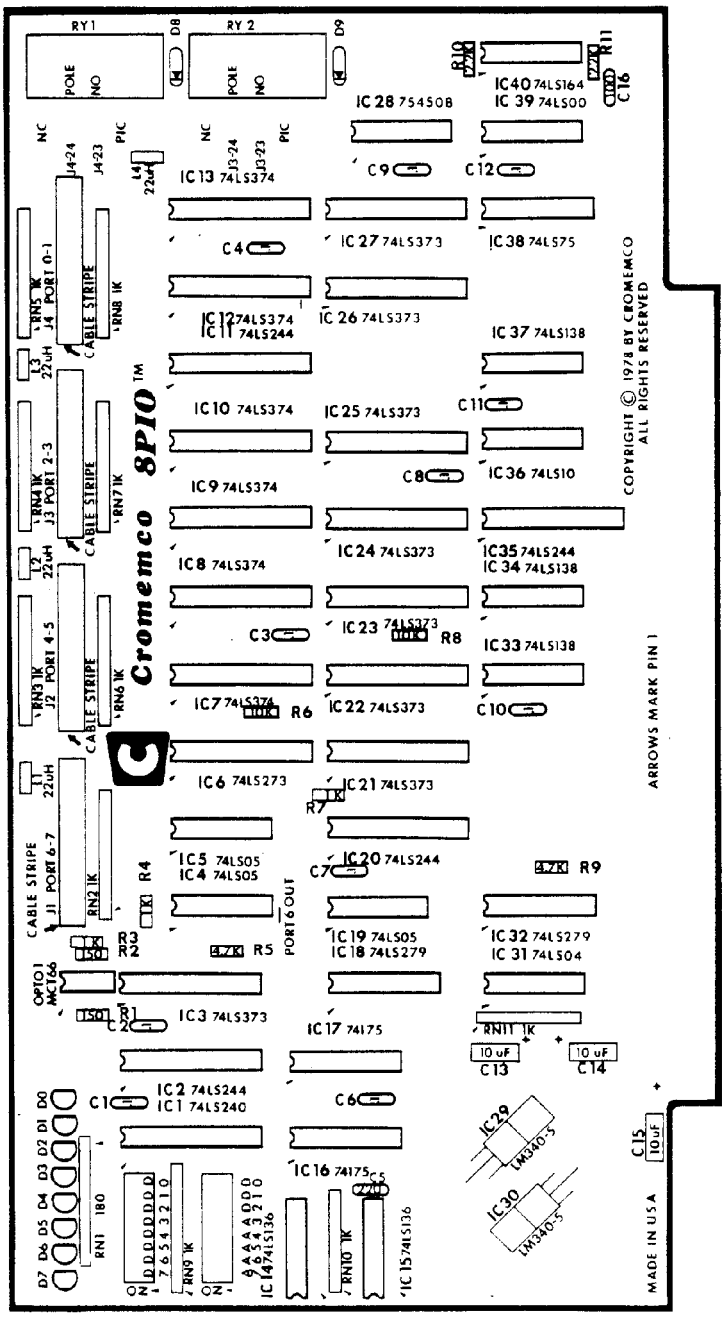
Capacitors		Part No.
C1-4	.047 μF	004-0061
C5	220 pF	004-0013
C6-12	.047 μF	004-0061
C13-15	10 μF	004-0032
C16	100 pF	004-0008

Diodes		Part No.
D0-7	TIL-211 LED	008-0020
D8-9	IN4148/IN914	008-0002

Sockets		Part No.
1	8 PIN	017-0000
10	14 PIN	017-0001
8	16 PIN	017-0002
20	20 PIN	017-0004

Documentation	Part No.
8PIO Instruction Manual	023-0047

Parts Location Diagram



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2. the return authorization number
3. a description of the problem, and
4. proof of the date of retail purchase

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