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XPU

Instruction Manual

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XPU

Instruction Manual

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CROMEMCO, Inc.
P.O. Box 7400
280 Bernardo Avenue
Mountain View, CA 94039

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Chapter 1

THE XPU EXTENDED DUAL PROCESSOR UNIT

INTRODUCTION

The Cromemco XPU extended dual processor unit incorporates two microprocessors on a single board. The MC68000/68010 provides the power and speed of a new generation of 32-bit microprocessor chips, while the Z80 guarantees compatibility with most existing hardware and software. One of the two microprocessors controls the bus at any given time, yielding control to the other as required by the software.

The MC68000/68010 microprocessor has 18 32-bit internal registers, a 16-bit external data bus, and a 24-bit external address bus. It can directly address 16 megabytes of memory and has 56 instruction types, 5 data types, and 14 address modes yielding an instruction set of over 1000 instructions. These features make the MC68000/68010 extremely fast and versatile. Unlike the MC68000, the MC68010 permits program execution to be suspended by a bus error and later restarted. This permits the development of Virtual Memory software when used in conjunction with the Cromemco XMM board.

Table 1-1 shows the operational specifications for the XPU board.

Table 1-1: XPU SPECIFICATIONS

Processors:	MC68000/68010 and Z80B
Clock Rate:	MC68000/68010 - 10MHz Z80B - 5MHz System - 4MHz
Instruction Set:	MC68000/68010 - over 1000 instructions in 56 main types Z80B - 158 instructions including the 78 instructions of the 8080 processor
Power-on Jump:	Jumper selectable to any 4K memory boundary within the first 64K page. Preselected for standard Cromemco systems.
Processor Control:	Software controlled switching between processors.
Bus:	S-100/IEEE-696
Power Requirements:	+8 volts @ 2.0 amps
Operating Environment:	0 to 55 degrees C

SETUP AND INSTALLATION

Switch Settings

There are no switches on the XPU.

Jumper Selectable Options

The XPU board is ready for use in your Cromemco system as it is shipped from the factory. Figure 1-1 shows the locations of three jumpers which may be used in special circumstances.

Wait State Jumper - If you have a revision K or higher MCU board and do not enable error correction, a jumper in this location will increase memory speed by reducing the MC68000/68010 memory cycle wait states from 3 to 2. **Do not use this jumper with an older MCU board or with error correction enabled.**

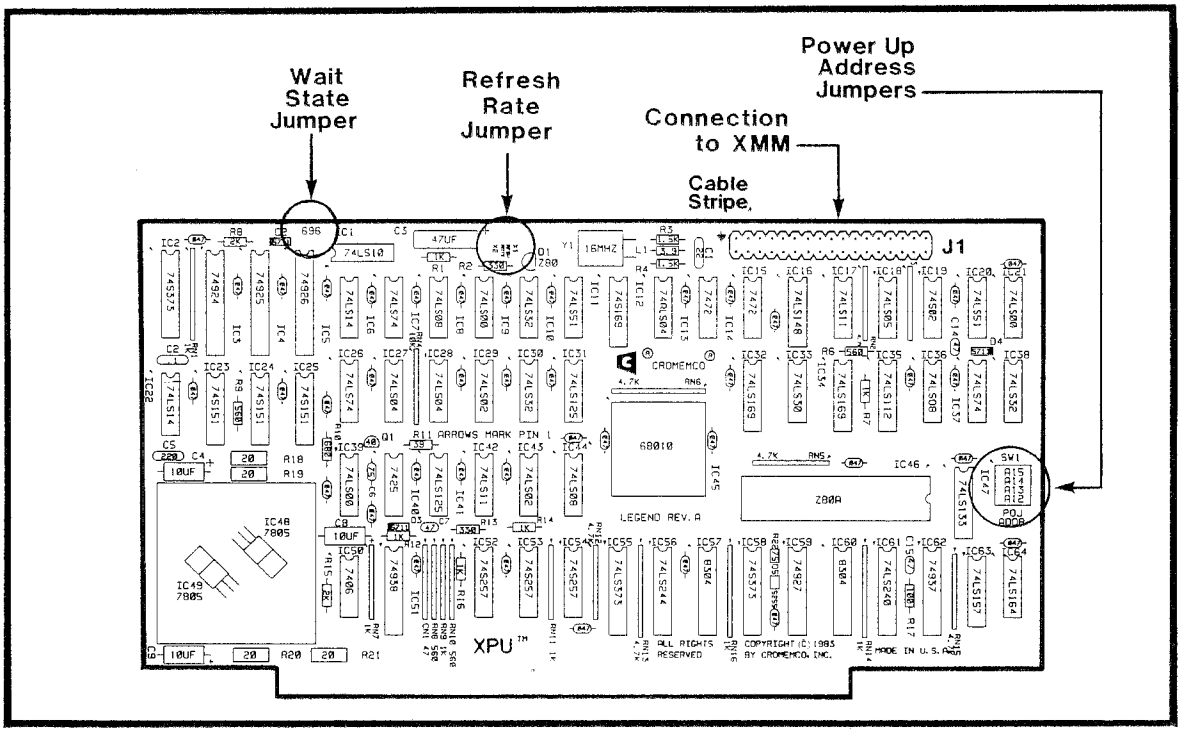

Figure 1-1: XPU JUMPER LOCATIONS

Memory Refresh Rate - As shipped, there is a trace between the common node and the X2 solder pad. During MC68000/68010 operation, this causes a refresh cycle to be inserted approximately every 16 microseconds. Cutting this trace and installing a jumper between the common node and the X1 solder pad will double the time between refresh cycles and increase processing speed by about 3%. This slower refresh rate is compatible with all versions of the MCU/MSU series boards, but it is not compatible with 256KZ boards.

Power Up Address - The power up address is factory set to C000h (jumpers at A15 and A14). These jumpers change the upper 4 bits of the address where execution begins.

Installation

Turn off all power to the system and unplug it before installing or removing any circuit board.

If you have an XMM board, connect it to the XPU with the 34-conductor cable (part number 519-0062), with the red cable stripe on the left.

MEMORY SUPPORT

The XPU supports both vertical and horizontal memory configurations.

Horizontal memory, arranged in banks, is used by CDOS and the Z80 Cromix Operating System. This memory configuration allows the operating system, contained in one 64K-byte bank, to select one of up to six banks of 64K bytes each. This provides a total of 448K bytes of addressable memory. Horizontal memory requires the use of Cromemco 64KZ, 64KZ-II, or 256KZ memory boards and does not support the 68000 Cromix Operating System.

Vertical memory is used by the 68000 Cromix Operating System. This configuration allows the operating system to directly address up to 16 megabytes of memory without using bank selection. Vertical memory requires Cromemco 256KZ board(s), or an MCU with MSU-series boards. CDOS is not supported by vertical memory configurations. All Cromemco I/O boards are compatible with an XPU configured with vertical memory, except the SDI/48KTP and the WDI-II.

Mapped memory requires the installation of the companion XMM board. The XPU provides address lines A23-A12 and some control signals on a 34-pin connector, J1. When connected to the Cromemco XMM (eXtended Memory Management board), addresses generated by the MC68000/68010 and Z80 programs may be relocated on 4K-byte boundaries. Memory protection implemented on the XMM can prevent unauthorized access to data residing in memory.

INPUT AND OUTPUT

In the Z80 mode of operation, the XPU performs input and output by executing Z80 **in** and **out** instructions that specify the desired values and ports.

In the MC68000/68010 mode, the XPU performs input and output by reading and writing from and to the top 64K bytes of memory (i.e., FF0000h - FFFFFFh). This area of memory is mapped by the XPU firmware to correspond to ports 0 - FFFFh.

In both modes of operation, port xxFFh is reserved for switching from one microprocessor to the other. Refer to the following section for an example of I/O using each microprocessor.

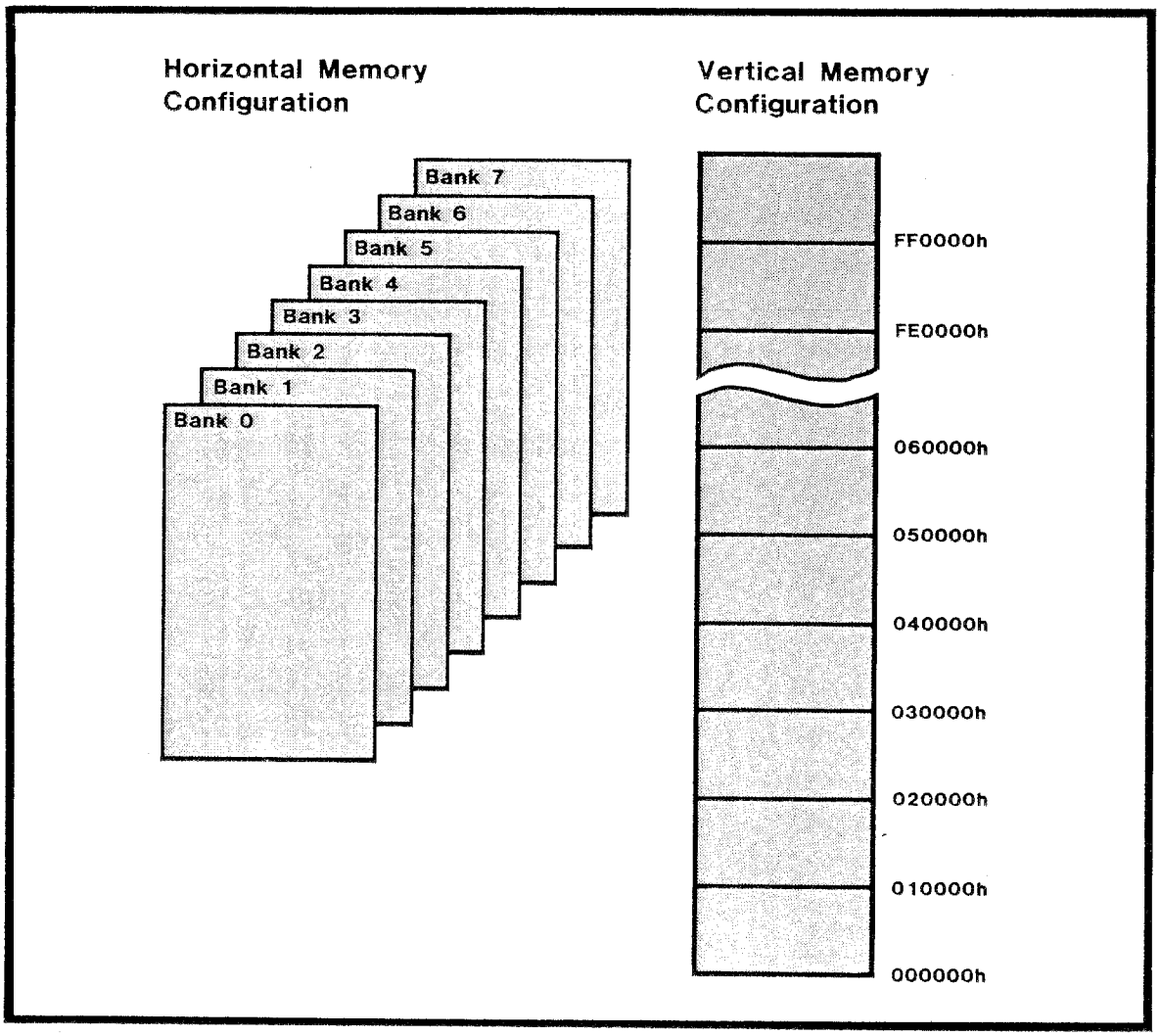

Figure 1-2: MEMORY CONFIGURATIONS

MICROPROCESSOR SELECTION

The XPU board automatically starts up in the Z80 mode of operation. When a **1** is output to port FFh, control switches to the MC68000/68010.

When the MC68000/68010 is first used, after power-up or system reset, it obtains its stack pointer (sp) from location 0 and its program counter (pc) from location 4. Subsequently, when control switches from the Z80 to the MC68000/68010, the program continues execution as though it had not been interrupted.

The following Z80 instructions initiate MC68000/68010 operation with the stack at 6000h and a starting address of 7000h. On subsequent calls to the MC68000/68010, only the two instructions with the comment **switch control to the MC68000/68010** are needed because the stack pointer and program counter have already been established.

```
        ld      hl,intdat       ; initialize sp & pc
        ld      de,0            ;    /
        ld      bc,8            ;   /
        ldir                    ;  /
        ;
        ld      a,1             ; switch control to
        out     0ffh,a          ; MC68000/68010
        ;
intdat: db      0, 0, 60h, 0    ; location of stack
        db      0, 0, 70h, 0    ; starting address
```

To switch from the MC68000/68010 to the Z80, output a **0** to port FFh. This may be done by writing to the top 64K of memory as follows.

```
    move.b      #0,0ffffffh
```

The 24-bit address to which the zero is moved may be thought of as consisting of three segments. The first **ff** indicates the top 64K of memory (the area reserved for memory mapped I/O). The second **ff** is mandatory. The last **ff** is the port address.

Chapter 2

BUS SIGNALS AND I/O PORT CHARACTERISTICS

S-100 BUS SIGNALS

The introduction of a new CPU usually causes some bus signals to be redefined, some to be deleted, and others to be added. The Z80, used in the new XPU central processor, was the heart of the Cromemco C-10 computers. Therefore, the Z80 has influenced signal redefinition very little. Major changes have occurred because the XPU uses two microprocessors, one of which is the new MC68000/68010. Most of the new signals concern either board-level switching between the two processors, the 16-bit data bus, the 24-bit address bus, or control differences.

The signals of Cromemco's S-100 bus, which are compatible with the IEEE-696 standard, can be grouped into seven functional categories as follows.

1. Address (A)
2. Control inputs (CI)
3. Control outputs (CO)
4. Data (D)
5. DMA data transfer control (DMA)
6. Status (S)
7. Utility (U)

Table 2-1 shows each S-100 bus connection, signal mnemonic, name, and function. A bus signal mnemonic indicates both the signal purpose and the active state. The active state reveals what logic, binary, and electrical states to expect on a given signal line. When the mnemonic is followed by an asterisk, the signal is active low. Without the asterisk, the signal is active high. For example, if the signal is **GAPK*** and the electrical state is low (a more negative voltage), the logic state is true and the binary state is 1. For an active high signal, such as **GAPK**, an electrical high (more positive voltage) is a logical true and a binary state of 1.

Pin Number	Mnemonic	Signal Name	Function	Pin Number	Mnemonic	Signal Name	Function
1	+8V		U	51	+8V		U
2	+18V		U	52	-18Vur		U
3	XRDY	External Ready	CI	53		undefined	
4		undefined		54	SLVCLR*	Slave Clear (bus slaves)	U
5		undefined		55		undefined	
6		undefined		56		undefined	
7		undefined		57		undefined	
8		undefined		58	sXTRQ*	Sixteen Request	S
9		undefined		59	A19	Extended Address Bit 19	A
10		undefined		60	SIXTN*	Sixteen Acknowledge	CI
11		undefined		61	A20	Extended Address Bit 20	A
12	NMI*	Non-maskable Interrupt	CI	62	A21	Extended Address Bit 21	A
13	PWRFAIL*	Power Fail	U	63	A22	Extended Address Bit 22	A
14		undefined		64	A23	Extended Address Bit 23	A
15	A18	Extended Address Bit 18	A	65	MREQ*	Memory Request	U
16	A16	Extended Address Bit 16	A	66	RFSH*	Refresh (Memory)	U
17	A17	Extended Address Bit 17	A	67	MEMDSB*	Memory Disable	U
18	SDSB*	Status Disable	DMA	68	MWRT	Memory Write	S
19	CDSB*	Control Output Disable	DMA	69		undefined	
20		Ground	U	70		Ground	U
21		undefined		71	Z80/68*	Z80/MC68000/68010 Processor Active	CO
22	ADSB*	Address Disable	DMA	72	pRDY	Ready	CI
23	DODSB*	Data Out Disable	DMA	73	pINT*	Interrupt Request	CI
24	ϕ2	System Clock	U	74	pHOLD*	Hold	CI
25	pSTVAL*	Status Valid Strobe	CO	75	RESET*	Reset (Bus Masters)	U
26	pHLDA	Hold Acknowledge	CO	76	pSYNC	Synchronize	CO
27	EXTAD*	Extended Address Enable	U	77	pWR*	Write	CO
28		undefined		78	pDBIN	Data Bus In	CO
29	A5	Address Bit 5	A	79	A0	Address Bit 0	A
30	A4	Address Bit 4	A	80	A1	Address Bit 1	A
31	A3	Address Bit 3	A	81	A2	Address Bit 2	A
32	A15	Address Bit 15	A	82	A6	Address Bit 6	A
33	A12	Address Bit 12	A	83	A7	Address Bit 7	A
34	A9	Address Bit 9	A	84	A8	Address Bit 8	A
35	DO1/D9	Data Out Bit 1/Data Bit 9	D	85	A13	Address Bit 13	A
36	DO0/D8	Data Out Bit 0/Data Bit 8	D	86	A14	Address Bit 14	A
37	A10	Address Bit 10	A	87	A11	Address Bit 11	A
38	DO4/D12	Data Out Bit 4/Data Bit 12	D	88	DO2/D10	Data Out Bit 2/Data Bit 10	D
39	DO5/D13	Data Out Bit 5/Data Bit 13	D	89	DO3/D11	Data Out Bit 3/Data Bit 11	D
40	DO6/D14	Data Out Bit 6/Data Bit 14	D	90	DO7/D15	Data Out Bit 7/Data Bit 15	D
41	DI2/D2	Data In Bit 2/Data Bit 2	D	91	DI4/D4	Data In Bit 4/Data Bit 4	D
42	DI3/D3	Data In Bit 3/Data Bit 3	D	92	DI5/D5	Data In Bit 5/Data Bit 5	D
43	DI7/D7	Data In Bit 7/Data Bit 7	D	93	DI6/D6	Data In Bit 6/Data Bit 6	D
44	sM1	Status Instruction Fetch	S	94	DI1/D1	Data In Bit 1/Data Bit 1	D
45	sOUT	Status Output	S	95	DI0/D0	Data In Bit 0/Data Bit 0	D
46	sINP	Status Input	S	96	sINTA	Status Interrupt Acknowledge	S
47	sMEMR	Status Memory Read	S	97	sWO	Status Write Out	S
48	sHLTA	Status Halt Acknowledge	S	98	ERROR*	Error	U
49	CLOCK	Clock, 2 MHz	U	99	POC*	Power On Clear	U
50		Ground	U	100		Ground	U

Signal Function Categories: A=address, CI=control inputs, CO=control outputs, D=data, DMA=control for DMA data transfers, S=status, and U=utility.

Pins 4-10 are defined by IEEE spec., but unused by Cromemco; Pin 71 is used by Cromemco, but undefined by IEEE spec.

Table 2-1: S-100 BUS/XPU SIGNALS

S-100 BUS/XPU SIGNAL DEFINITIONS

The following list provides detailed definitions of each S-100 bus signal. Additional information about signal interaction with other boards may be obtained by consulting the appropriate board reference manuals.

Address Bus Signals

The address bus, consisting of parallel signal paths of 24 bits, selects specific memory locations or I/O ports. The MC68000/68010 drives all 24 bits directly. During Z80 operation, the Z80 drives the lower 16 bits and an auxiliary latch drives the upper 8. On power up or reset, the auxiliary latch is reset.

Memory Addressing - Memory addressing uses 24 bits, **A0 through A23**, providing a 16-megabyte address range.

I/O Addressing - I/O addressing uses 16 bits, **A0 through A15**, allowing selection of 65,536 ports.

Control Input Signals

XPU control input signals are output by bus slaves such as peripheral interface boards and memory boards. These signals synchronize the operation of the XPU and the bus slaves.

External Ready - The **XRDY** signal synchronizes the response of a bus master to a bus slave. It can start and stop XPU operation.

Hold or Bus Request - The **pHOLD*** signal is a DMA bus request generated by the DMA controller of a bus slave. The CPU determines when the request is granted and, at the appropriate time, outputs the pHLDA signal.

Interrupt Request - The **pINT*** signal is initiated by a bus slave. Each board may output an interrupt request to the XPU on this signal line. The interrupts are serviced according to priorities established by the software and/or hardware.

Non-Maskable Interrupt Request - In a manner similar to pINT*, the **NMI*** signal is initiated by a bus slave. The difference between the signals is that NMI* cannot be masked by software and must be serviced by the XPU as soon as possible.

Ready - The **pRDY** signal is active during normal microprocessor operation. The negation of pRDY is the wait-state request which indicates that an addressed memory board or peripheral is not ready for data transfer.

Sixteen Acknowledge - The **SIXTN*** signal indicates that a request for 16-bit data transfer has been granted and that the transfer may begin. Refer also to the sXTRQ* status signal.

Bus Error - The **ERROR*** signal tells the XPU to suspend or abort an MC68000/68010 cycle. This may occur when the MCU detects a non-correctable memory error, the XMM detects an illegal address translation attempt, or a page fault occurs and the XMM command register indicates that page faults are to be handled by the MC68000/68010 processor.

Control Output Signals

The control output signals are output by the XPU to control data transfer and provide the required timing reference.

Data Bus Input Strobe - The **pDBIN** read signal strobes data from the addressed slave onto the data bus.

Hold Acknowledge - The **pHLDA** signal indicates to the board with the highest priority request that the XPU has relinquished control of the system bus for DMA-controlled data transfer. Refer to the DMA control signals and pHOLD*.

Processor Active - The **Z80/MC68000/68010*** signal indicates which microprocessor is controlling the bus. When high, the Z80 is in control; when low, the MC68000/68010 is in control.

Status Valid Strobe - The **pSTVAL*** signal indicates that the address and status signals present on the bus are stable and valid. Refer to pSYNC and the status signals.

Synchronization - The **pSYNC** signal indicates the start of a new bus cycle. Refer to pSTVAL* and the status signals.

Write - The **pWR*** write signal strobes data from the data bus to the addressed slave.

Data Bus Signals

The data bus consists of sixteen parallel data lines.

Under the control of the Z80, the bus is used as two unidirectional 8-line data buses. The data input lines, **DI0 through DI7**, bring data to the XPU. The data output lines, **DO0 through DO7**, transfer data from the XPU.

Under the control of the MC68000/68010, all 16 lines, **D0 through D15**, are used as a bidirectional data bus. Refer also to sXTRQ*, SIXTN*, and the control output signals.

DMA Control Signals

The **pHOLD*** signal is issued by a board when it requires control of the bus for DMA. The XPU acknowledges pHOLD* with a pHLDA signal when it is ready to relinquish control of the bus. At the same time, the following signals disable the CPU bus buffers, effectively isolating the CPU from the bus and allowing the DMA controller to become the bus master.

1. Address Disable **ADSB***
2. Control Output Disable **CDSB***
3. Data Output Disable **DODSB***
4. Status Disable **SDSB***

Status Signals

The following status signals identify the bus cycle in progress, and indicate the purpose of the address currently on the bus.

1. Memory read **sMEMR**
2. Operating Instruction Code Fetch **sM1**
3. Input **sINP**
4. Output **sOUT**
5 Memory Write **MWRT**
6. Write cycle **sWO***
7. Interrupt Acknowledge **sINTA**
8. Halt Acknowledge **sHLTA**
9. Sixteen bit data bus request **sXTRQ***

The status signals are best defined in terms of the bus cycle each represents. Table 2-2 shows the electrical state of the status signals for each bus cycle.

Table 2-2: STATUS SIGNAL STATES

Status Signal	Bus Cycle Tape						
	Memory Read	Op Code Fetch	Memory Write	Output	Input	Interrupt Acknowledge	Halt Acknowledge
sMEMR	H	H	L	L	L	L	X
SM1	L	H	L	L	L	X	X
sWO*	H	H	L	L	H	H	H
sOUT	L	L	L	H	L	L	L
MWRT	L	L	H	L	L	L	L
sINP	L	L	L	L	H	L	L
sINTA	L	L	L	L	L	H	L
sHLTA	L	L	L	L	L	L	H
sXTRQ*(8-bit)	H	H	H	H	H	H	X
sXTRQ*(16-bit)	L	L	L	L	L	L	X

Utility Signals

Utility signals are necessary to the overall operation of the system. They include power supply and power supply status signals, the system clock, and general reset and error signals.

+8 Volts Unregulated - This is the only supply voltage required for the XPU, MCU, and MSU boards. The +18 and -18 Volts Unregulated lines are available for other boards. Regulation of the supply voltage is performed on each board.

Grounds - Signal grounds are connected together on the S-100/IEEE-696 bus.

Phase 2 System Clock - The XPU generates the 4-MHz system clock signal.

Clock - The 2-MHz **CLOCK** signal is independent of all other bus timing signals. It may be used by circuits to generate time periods, or by other functions requiring a fixed input frequency.

Reset - The **RESET*** signal resets all bus masters and slaves, including the XPU.

Slave Clear - The **SLAVE CLR*** signal resets those bus slaves which monitor this signal.

Power-On Clear - The **POC*** signal is active only at the time that power is applied to the system. When active, POC* issues the RESET* and SLAVE CLR* signals.

Memory Disable - The **MEMDSB*** signal inhibits operation of those memory boards capable of responding to this signal. Cromemco 64KZ boards are inhibited by this signal, but MSU boards are not.

Memory Request - The **MREQ*** signal indicates that the address on the bus is valid for a memory read or write.

Refresh - The **RFSH*** signal indicates when the Z80A is performing a refresh cycle.

XPU/XMM SIGNAL DEFINITIONS

The XPU and XMM communicate over a 34-pin connector containing address and status information for memory mapping. The following list defines the XPU/XMM signals shown in Table 2-3.

Signals for Z80 Mapping

Memory Request - The **MREQ*** signal is generated by the Z80 processor to indicate the start of a Z80 memory cycle. This signal is used by the XMM board to adjust the timing of mapped Z80 cycles to correspond to the timing of unmapped cycles.

M1 - The Z80 **M1*** signal indicates the start of either an instruction fetch or an interrupt acknowledge cycle. This signal is used by the XMM to adjust the timing of mapped Z80 cycles to correspond to the timing of unmapped cycles.

Input/Output Request - The Z80 **IOREQ*** signal is true whenever an input/output or interrupt acknowledge cycle is performed. This signal is used by the XMM to adjust the timing of mapped Z80 cycles to correspond to unmapped cycles.

Z80 Ready - The **ZRDY** signal from the XMM indicates to the XPU that the Z80 cycle may proceed. When the Z80 processor is running in mapped mode, the start of each cycle on the bus is delayed to provide time for the translation of address bits A12 through A15 to S-100 address bits A12 through A23.

Table 2-3: XPU/XMM SIGNALS

Pin	Signal	Source	Definition
1	GND	BOTH	Ground
2	MREQ*	XPU	Z80 Memory Request Control Line
3	A15	XPU	MC68000/68010/Z80 Address Line 15
4	10MHZ	XPU	10MHz Master Clock
5	A14	XPU	MC68000/68010/Z80 Address Line 14
6	M1*	XPU	Z80 M1 Cycle Control Line
7	A13	XPU	MC68000/68010/Z80 Address Line 13
8	GND	BOTH	Ground
9	A12	XPU	MC68000/68010/Z80 Address Line 12
10	MEM/IO*	XMM	MC68000/68010 Memory or I/O Cycle
11	IOREQ*	XPU	Z80 I/O Request Control Line
12	AS*	XPU	MC68000/68010 Address Strobe Control Line
13	GND	BOTH	Ground
14	A21	XPU	MC68000/68010 Address Line 21
15	XMM-ACTIVE*	XMM	XMM turned on and mapping
16	A20	XPU	MC68000/68010 Address Line 20
17	A19	XPU	MC68000/68010 Address Line 19
18	A18	XPU	MC68000/68010 Address Line 18
19	A17	XPU	MC68000/68010 Address Line 17
20	A16	XPU	MC68000/68010 Address Line 16
21	A23	XPU	MC68000/68010 Address Line 23
22	GND	BOTH	Ground
23	R/W*	XPU	MC68000/68010 Read/Write Cycle Control Line
24	A22	XPU	MC68000/68010 Address Line 22
25	ZRDY	XMM	Z80 Cycle may proceed (delayed during mapping)
26	GND	BOTH	Ground
27	GND	XMM	Ground
28			Unused
29	FC1	XPU	MC68000/68010 Function Code Bit 1 Control Line
30	FC2	XPU	MC68000/68010 Function Code Bit 2 Control Line
31	FC0	XPU	MC68000/68010 Function Code Bit 0 Control Line
32	GND	BOTH	Ground
33	AOK	XMM	MC68000/68010 address translation permitted and complete
34	EN68010	XPU	Control will transfer from Z80 to MC68000/68010

Signals for MC68000/68010 Mapping

Clock - The **10MHZ** clock signal from the XPU is used to synchronize the XMM and XPU boards. This signal provides the basic timing for all operations on the XMM board.

CPU Transfer Enable - The **EN68000/68010** signal notifies the XMM board that the XPU is about to switch from the Z80 processor to the MC68000/68010 processor.

MC68000/68010 Control Signals - **AS*, R/W*** and **FC0-2** are the Address Strobe, Read/Write and Function code control signals from the MC68000/68010 processor. These signals describe the type of cycle being performed.

XMM Active - The **XMM-ACTIVE*** signal is true whenever the XMM board has been enabled. This signal forces the XPU to disable the address drivers for address lines A12 through A23 and examine the AOK and MEM/IO* signals to determine the type and validity of the cycle being executed.

Memory/IO - The **MEM/IO*** signal from the XMM defines whether the XPU is to run a memory cycle or an I/O cycle when address translation is enabled.

Address OK - The **AOK** signal from the XMM prevents the XPU from beginning an S-100 bus cycle until the address translation has been performed and proven valid. This signal occurs only when the XMM has been enabled.

I/O PORT CHARACTERISTICS

MC68000/68010/Z80 Switch

Port Address: FFh (write only)

The MC68000/68010/Z80 Switch output byte enables either the MC68000/68010 or the Z80 microprocessor on the XPU. When one is enabled, the other is disabled. Refer to the section "Microprocessor Selection" in Chapter 1.

D7-D1 - not used; should be set to 0 when writing to port.

D0 - When this bit is 1, the MC68000/68010 is on; when this bit is 0 the Z80 is on.

INTERRUPT VECTOR TRANSLATION

The interrupt vectors supplied by system devices must be translated into vectors that can be properly interpreted by the MC68000/68010. The following equation shows the mathematical relationship between the device vector and the vector that is received by the MC68000/68010. After translation, all device-generated vectors fall within the user-interrupt area of the MC68000/68010 vector table.

$$Vi = INT\ (Vo/2) + 40h$$

Where:

Vi = the hexadecimal equivalent of the binary vector input to the MC68000/68010,

INT = the integer part (whole number without the fraction) of the portion of the equation within the parentheses,

Vo = the hexadecimal vector output by the board or device within the system, and received on the DI bus of the XPU,

40h = hexadecimal 40.

The following table shows vector translation examples.

If Vo is:	then Vi is:
0h or 1h	40h
Ch or Dh	46h
7Eh or 7Fh	7Fh
FEh or FFh	BFh

Appendix A

XPU Parts List

Integrated Circuits

Designation	Cromemco Description	Part No.
IC1	74F10	010-0376
IC2	74S373	010-0085
IC3	PROM #1	502-0107-2
IC4	PROM #2	502-0108-2
IC5	PROM #3	502-0109-2
IC3-5	sckt 8 pin	017-0000
	sckt 16 pin	017-0002
IC6	74LS14	010-0061
IC7	74LS74	010-0055
IC8	74F08	010-0375
IC9	74LS00	010-0069
IC10	74LS32	010-0058
IC11	74LS51	010-0106
IC12	PAL16R8A	502-0132-1
IC13	74ALS04	010-0345
IC14-15	7472	010-0177
IC16	74LS148	010-0189
IC17	74LS11	010-0062
IC18	74LS05	010-0065
IC19	74S02	010-0122
IC20	74LS51	010-0106
IC21	74LS00	010-0069
IC22	74LS14	010-0061
IC23-25	74S151	010-0156
IC26	74LS74	010-0055
IC27-28	74LS04 (non-TI)	010-0066
IC29	74LS02	010-0068
IC30	74LS32	010-0058
IC31	74LS125	010-0127
IC32	74LS169	010-0144
IC33	74LS30	010-0059
IC34	74LS169	010-0144
IC35	74LS112	010-0126

Integrated Circuits (Continued)

Designation	Cromemco Description	Part No.
IC36	74F08	010-0375
IC37	74LS74	010-0055
IC38	74F32	010-0377
IC39	74LS00	010-0069
IC40	7425	010-0032
IC41	74LS125	010-0127
IC42	74F11	010-0414
IC43	74LS02	010-0068
IC44	74F08	010-0375
IC45	68000R10/	011-0115/
	68010R10	011-0116
	sckt 68 pin grid	017-0361
IC46	Z80B/MK3880-6	011-0113
	sckt 40 pin	017-0006
IC47	74LS133	010-0327
IC48-49	REG 7805/340T-5	012-0001
	sil-pad reg.	021-0109
IC50	7406	010-0028
IC51	74938 PAL16R8	502-0038
	sckt 20 pin	017-0004
IC52-54	74S257	010-0131
IC55	74LS373	010-0102
IC56	74LS244	010-0100
IC57	AM8304	010-0322
IC58	74S373	010-0085
IC59	PROM	502-0027
	sckt 20 pin	017-0004
IC60	AM8304	010-0322
IC61	74LS240	010-0038
IC62	PAL	502-0037
	sckt 20 pin	017-0004
IC63	74LS157	010-0046
IC64	74LS164	010-0043

Diodes/ Transistors

Designation	Cromemco Description	Part No.
D1	LED green TIL-211	008-0020
D2-4	1N5711	008-0033
D5	1N5225	008-0014
Q1	2N3640	009-0023

Capacitors

Designation	Cromemco Description	Part No.
C1	18 pf crdc	004-0002
C2	.1 uf crdc 10V	004-0143
C3	47uf/20V tant	004-0075
C4	10 uf tant 20V	004-0032
C5	220 pf crdc	004-0138
C6	75 pf crdc 1000V	004-0136
C7	47 pf mono	004-0152
C8-9	10 uf tant 20V	004-0032
C14-15	47 pf mono	004-0152
C16-18	220 pf crdc	004-0138
-o-	.047/50V	004-0061-1

Capacitor Networks

Designation	Cromemco Description	Part No.
CN1	47 pf 8 pin	005-0000

Resistors

Designation	Cromemco Description	Part No.
R1	1 kohm 1/4	001-0018-1
R2	330 ohm 1/4	001-0012-1
R3-4	680 ohm 1/4	001-0016-1
R6	560 ohm 1/4	001-0015-1
R7	1 kohm 1/4	001-0018-1
R8	2 kohm 1/4	001-0054-1
R9	560 ohm 1/4	001-0015-1
R10	680 ohm 1/4	001-0016-1
R11	39 ohm 1/4	001-0002-1
R12	1 kohm 1/4	001-0018-1
R13	330 ohm 1/4	001-0012-1
R14	1 kohm 1/4	001-0018-1
R15	2 kohm 1/4	001-0054-1
R16	1 kohm 1/4	001-0018-1
R17	100 ohm 1/4	001-0007-1
R18-21	20 ohm 3.0	001-0046
R22	75 ohm 1/4	001-0006-1
R23	150 ohm 1/4	001-0008-1
R24-26	100 ohm 1/4	001-0007-1

Resistor Networks

Designation	Cromemco Description	Part No.
RN1	1 kohm 10 pin	003-0011
RN2	4.7 kohm 8 pin	003-0009
RN3	1 kohm 8 pin	003-0007
RN4	10 kohm 8 pin	003-0025
RN5	4.7 kohm 8 pin	003-0009
RN6	4.7 kohm 10 pin	003-0014
RN7	1 kohm 8 pin	003-0007
RN8	560 ohm 8 pin	003-0006
RN9	1 kohm 8 pin	003-0007
RN10	560 ohm 8 pin	003-0006
RN11	1 kohm 8 pin	003-0007
RN12	4.7 kohm 8 pin	003-0009
RN13	4.7 kohm 10 pin	003-0014
RN14	1 kohm 10 pin	003-0011
RN15	4.7 kohm 8 pin	003-0009
RN16	1 kohm 10 pin	003-0011

Miscellaneous

Designation	Cromemco Description	Part No.
L1	choke 3.9 uH	007-0003
Y1	crystal 20MHz	026-0002
	#6 lock washer cad	015-0020
	spacer 1/4 hex 6-32 al	015-0169
J1	conn 34 pin R/A amp	017-0013
	XPU PC board	020-0141
	dual T0220 heatsink	021-0165

LIMITED WARRANTY

Cromemco, Inc. ("Cromemco") warrants this equipment against defects in material and workmanship to the original purchaser for ninety (90) days from the date of purchase, subject to the following terms and conditions.

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During the ninety (90) day warranty period Cromemco will, at its option, repair or replace this Cromemco product or repair or replace with new or used parts any parts or components, manufactured by Cromemco, which prove to be defective, provided the product is returned to your Dealer as set forth below.

How To Obtain Warranty Service:

You should immediately notify IN WRITING your Dealer or Cromemco of problems encountered during the warranty period in order to obtain warranty service; first obtain a return authorization number by contacting the Dealer from whom you purchased the product. Then attach to the product:

1. Your name, address, and telephone number,
2. the return authorization number
3. a description of the problem, and
4. proof of the date of retail purchase

Ship or otherwise return the product, transportation and insurance costs prepaid, to your Dealer. If you are unable to receive warranty repair from the Dealer from whom you purchased the product, you should contact Cromemco Customer Support at: Cromemco, Inc., 280 Bernardo Ave., Mountain View, Ca. 94043.

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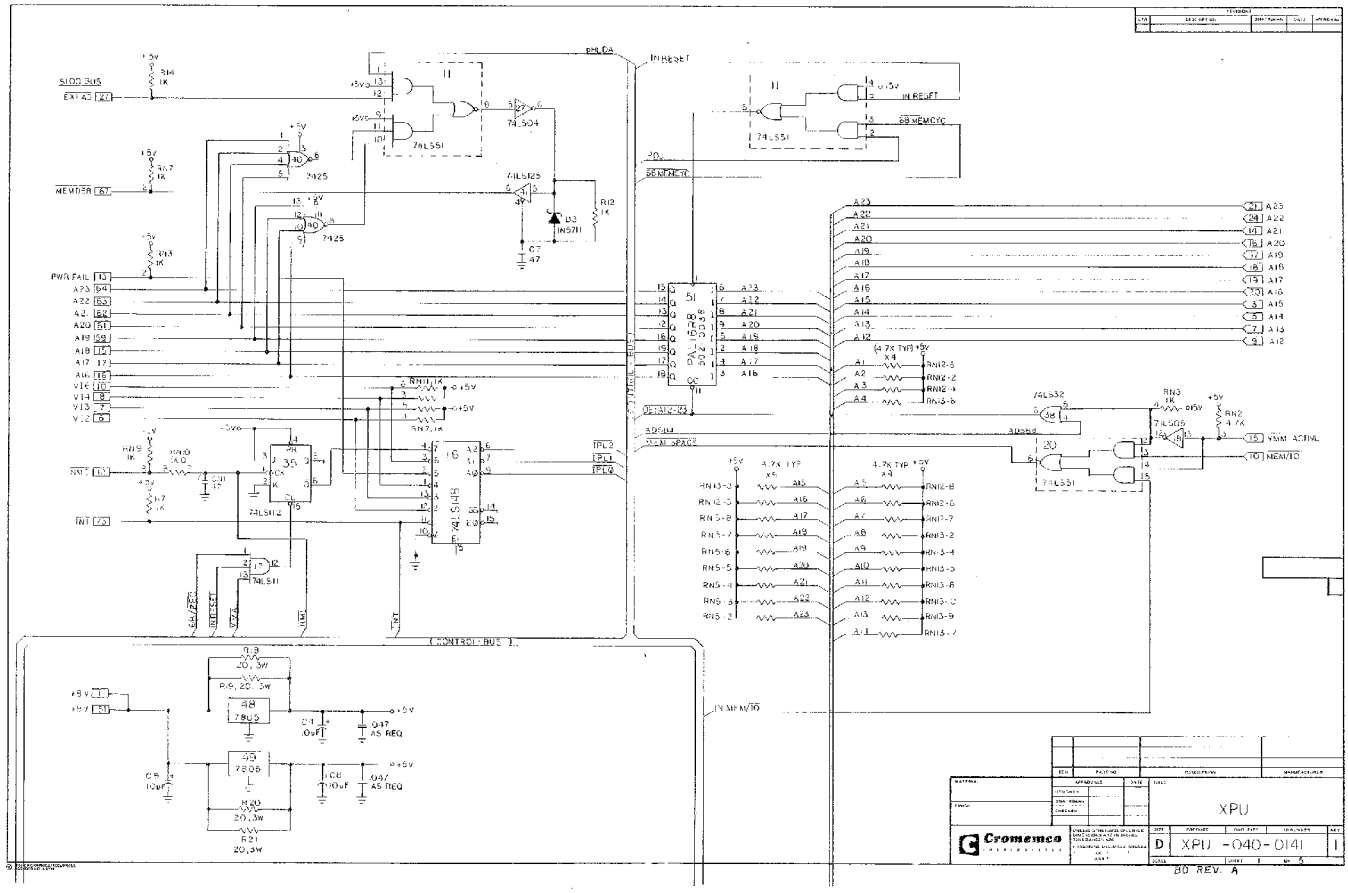
Rev. D 6/14/84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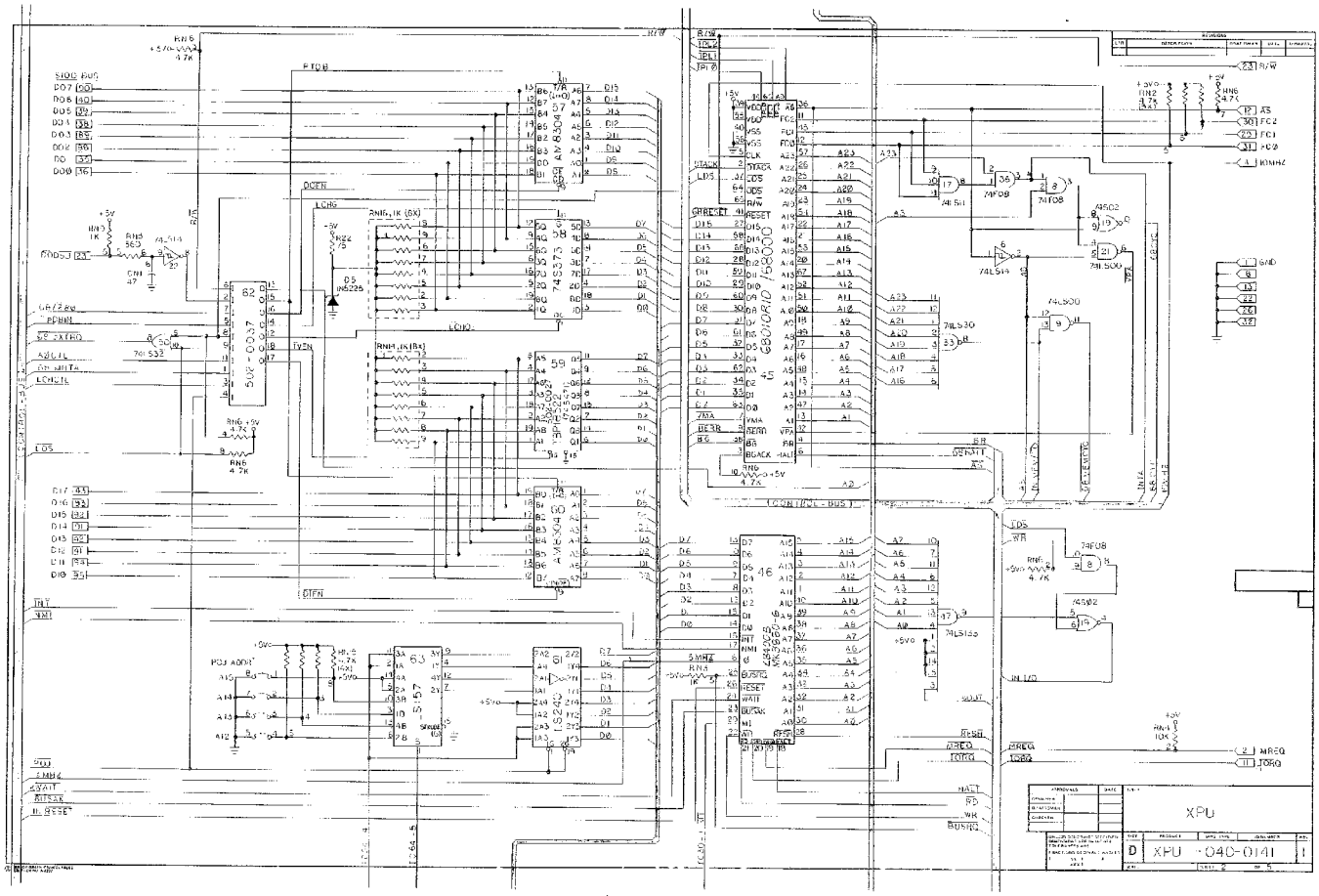
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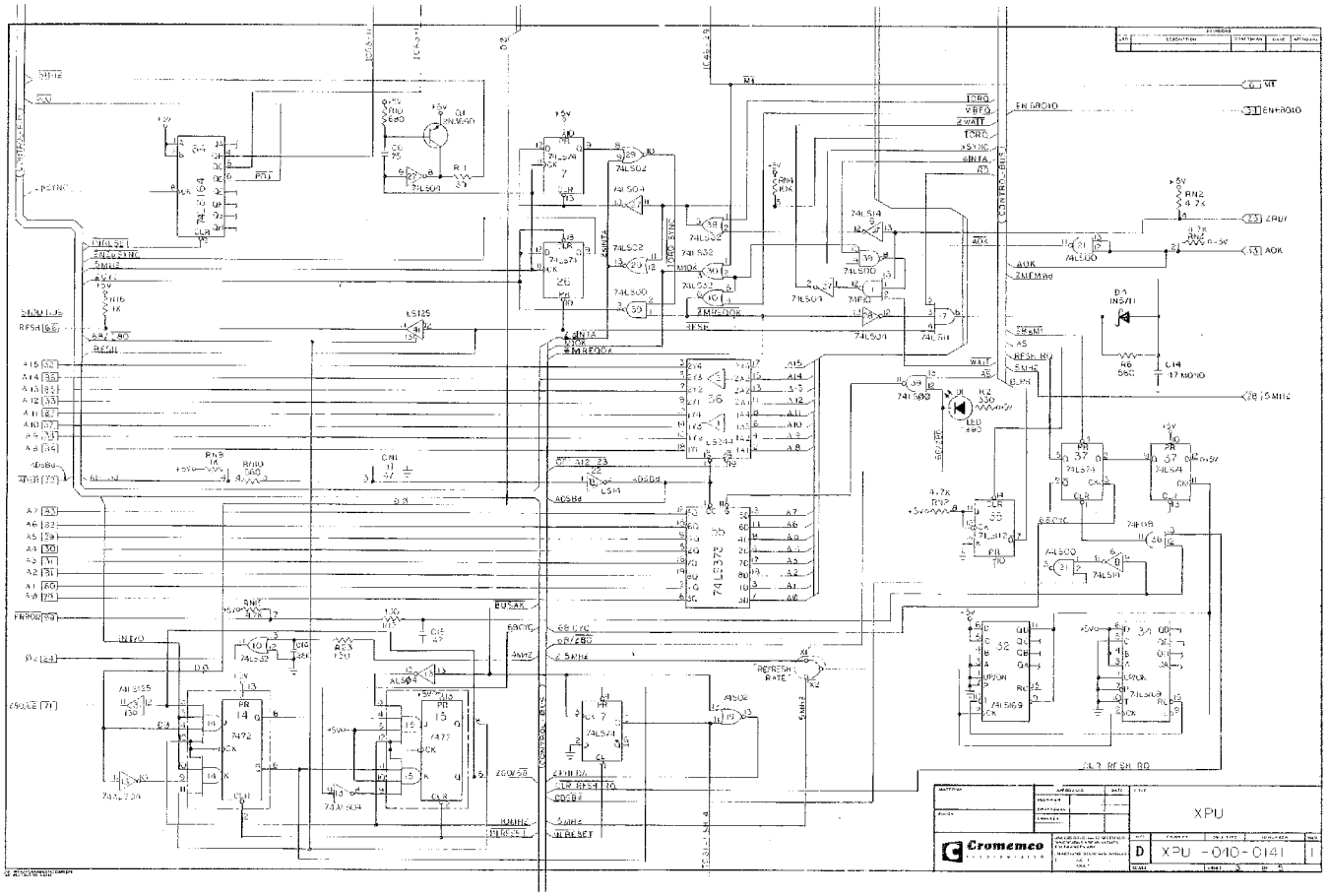
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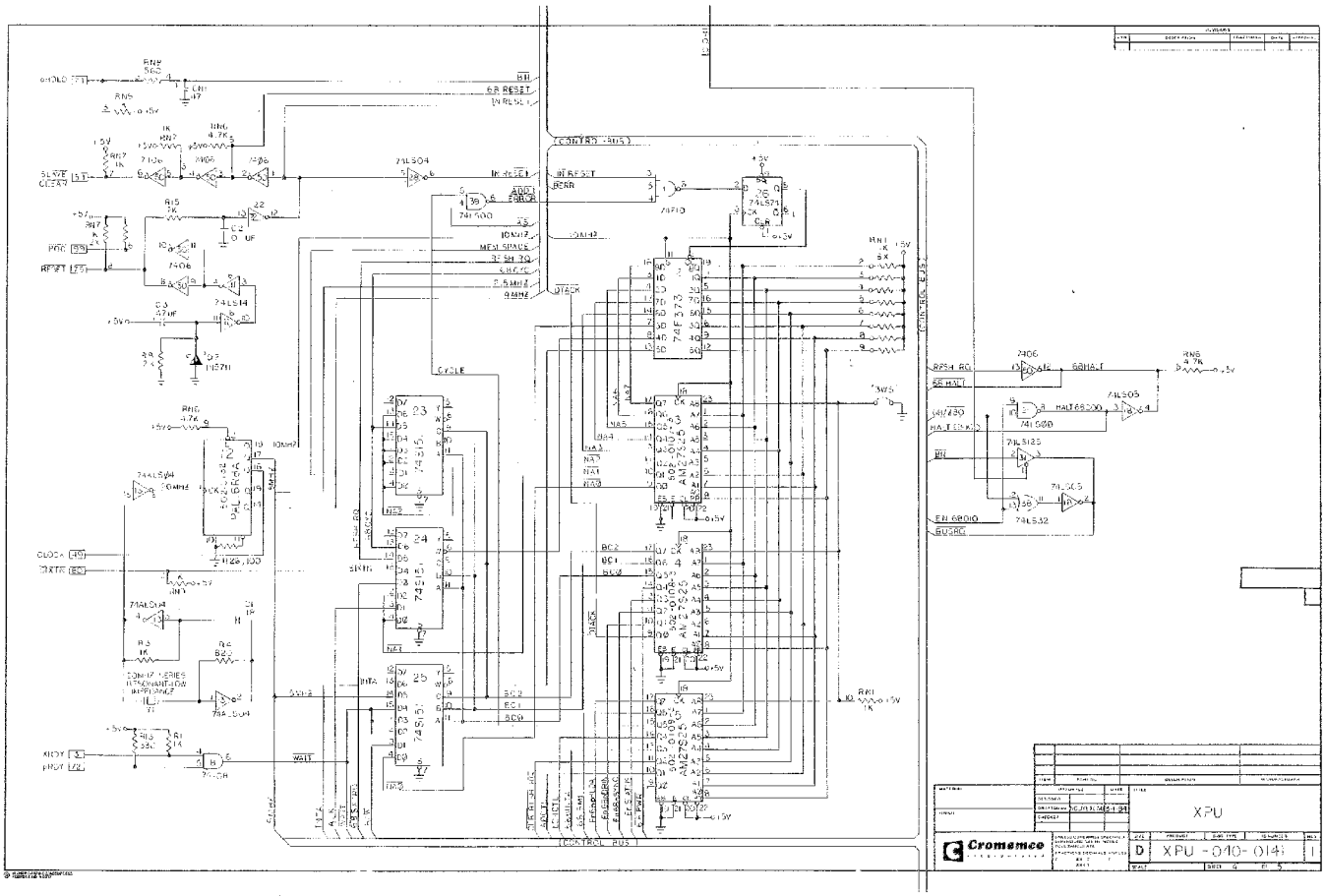
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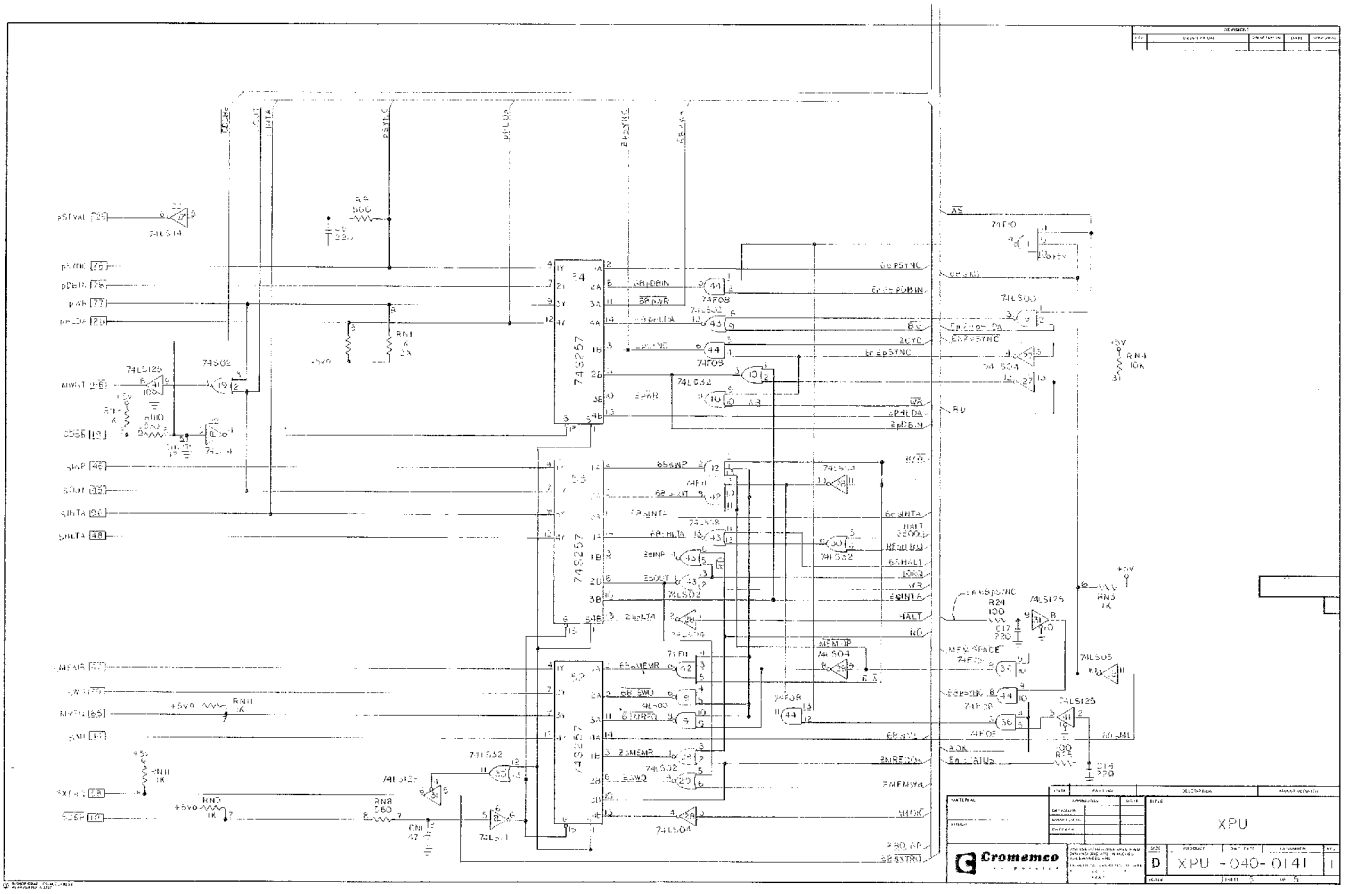
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280 Bernardo Ave.
P.O. Box 7400
Mountain View, CA 94039