DIGITAL RESEARCH CORP.

INTRODUCTION

The 16K Static RAM you have just purchased is one of the best RAM barsains on the market today. We have sone to sreat lensths to combine the risht mix of features that are most often required on Hish Density RAM boards for S-100 systems.

FEATURES:

Fully S-100 Compatible !

Uses the very popular 2114 4K Static RAM

Addressable as four separate 4K blocks.

On board bank select (Cromemco standard) is provided!

On board selectable wait states !

Board Access time under 500 NS.

PC Board is solder masked and silk screened.

Gold plated contact finsers for lons life.

All address and data lines fully buffered.

Phantom is Jumperable to buss pin #67.

LOW POWER dissipation (<2 amps typical).

Kit includes ALL parts and sockets.

PDBIN strobe is used for reliable operation.

Blank PC board may be populated as any multiple of 4K

PARTS LIST

1	4 Pin Low Profile Socket
13	14 Pin Low Profile Sockets
9	16 Pin Low Profile Sockets
32	18 Pin Low Profile Sockets
1	24 Pin Low Profile Sockets
4	Heatsinks (with hardware) for resulators.
53	Disc Bypass Capacitors
8	Tantalum Capacitors for resulators
1	1K ohm Resistor
5	2.2K ohm Resistors
4	7805 5VDC Resulators
32	2114 1K X 4 Static RAM's
5	74LS367 Buffers (8T97 or 74367)
1	74LS138 3 to 8 Decoder
1	74LS154 4 to 16 Decoder
3	74LS04 Hex Inverters
4	74LS32 Quad 2 Input OR
2	74LS05 Hex Inverter (O.C)
1	74LS10 Triple 3 Input Nand
1	74LS20 Dual 4 Input Nand
1	74LS30 8 Input Nand
1	74LS74 Dual D FF
1	74LS175 Quad D FF
1	Red LED

GENERAL CONSTRUCTION HINTS

For soldering we recommend a 32 Watt soldering pencil . DO NOT use a soldering gun !!! Use small diameter (such as 22 ga.) rosin core 60/40 alloy solder.

Keep the soldering pencil CLEAN with a wet sponge or cloth.

After such components as resistors or capacitors have been soldered, use a small pair of diagonal cutters to remove the excess lead length.

Observe polarities of all tantalum caps and the LED.

If you notice any discrepencies between the parts received and those listed please notify us immediately.

LIMITED WARRANTY

Digital Research Corp. of Texas warrants all components in this kit to be free from defects in material and workmanship for a period of 90 days. Any defective parts must be returned to us and will be replaced at no charge. Any board purchased as a kit which malfunctions during the warranty period which has not been subjected to abuse and that has been assembled with reasonable care will be repaired or replaced at no charge.

Any unassembled kit purchased from us may be returned within 14 days of receipt for a FULL "no questions asked" refund. No reason is necessary. The above warranties also apply to kits assembled by Digital Research Corp.

Any board which is not covered by the above warrants will be repaired at a cost commensurate with the work required. This charge will not exceed $20 without prior approval.

This warranty is made in lieu of any other warranty expressed or implied and is limited in all cases to the repair or replacement of the kit involved.

ASSEMBLY INSTRUCTIONS

( ) Give the PC board a good visual inspection for any obvious shorts or opens. There should be none, but a few minutes spent here could save hours later.

( ) Using an ohm meter, insure that there are no shorts between buss pins 1 and 50.

( ) Install and solder 18 pin sockets for IC locations 1 through 32. Note that there is a notch or indentation on each of the IC sockets. This should be oriented in the same direction as the notch on the silk screened component legend for each IC location.

( ) Install and solder a 24 pin socket in IC location 44.

( ) Install and solder a 16 pin IC socket in each of the followins locations: 33, 39, 40, 45, 49, 50 and 51. Also install 16 pin sockets for the "Bank Select" and "Address Select" locations.

( ) Install and solder 14 pin sockets in the followins locations: 34, 35, 36, 37, 38, 41, 42, 43, 46, 47, 48, 52, and 53.

( ) Install and solder the 4 pin socket in the location marked "DCBA".

( ) Install and solder the 53 bypass caps in locations C1 through C53 . Note that these are disc ceramic capacitors.

( ) Install and solder the one 1K resistor in location R4.

( ) Install and solder 2.2K resistors in locations R1, R2, R3, R5 and R6.

( ) Install and solder the four 7805 voltage regulators with heatsinks using the hardware provided.

( ) Install and solder the LED in the upper right hand corner of the board, near the word "ENABLED". The flat side of the LED is to the right.

( ) Install and solder the 8 tantalum caps as follows: C54 + down, C55 + up, C56 + down, C57 + up, C58 + down, C59 + up, C60 + down, and C61 + to the right. Note that "down" is toward the gold fingers. WARNING : Double check that the tantalums are installed properly.

( ) Using any of the regulator mounting tabs as ground, measure the output of each 7805 under power in your system. The output pin of the regulators is the uppermost pin. The measured outputs should be between 4.75 and 5.25 VDC. Any regulator not meeting these requirements must be replaced before any further steps are taken.

( ) Insert 74LS367's in the following locations: 39, 40, 49, 50, and 51. Be extremely careful to match the dot on each socket with pin 1 of each IC denoted by a small notch or indentation.

( ) Insert 74LS32 in locations 34, 35, 36, 37.

( ) Insert 74LS04 in locations 42, 47, and 48.

( ) Insert 7405's in locations 52 and 53.

( ) Insert a 74LS10 in location 41.

( ) Insert a 74LS20 in location 38.

( ) Insert a 74LS30 in location 46.

( ) Insert a 74LS74 in location 43.

( ) Insert a 74LS138 in location 33.

( ) Insert a 74LS154 in location 44.

( ) Insert a 74LS175 in location 45.

( ) Insert 2114's in locations 1 through 32. WARNING: All pin #1's are UP !!!

( ) Now that all IC's have been installed in sockets you should again check the regulators for proper operation.

16K SET UP AND USE

There are several options available to the user. These include "ADDRESS SELECTION", "WAIT STATES", "PHANTOM", and "BANK SELECT".

ADDRESS SELECTION

The DIGITAL RESEARCH CORP. 16K Static RAM is confisured as four indevendent 4K blocks. Each 4K block can be addressed on any of the sixteen available 4K areas of the S-100 buss. The four 4K blocks on the board are desisnated by the letters A,B,C,D. The sixteen system 4K areas are desisnated by 0 throush 15. It is necessary to place jumpers between each 4K block (A,B,C,D) and the desired 4K area (0 throush 15). The address select area is located at the lower left-hand side of the board.

If your board is not fully popvlated then the pins corresponding to the unused 4K blocks should be pvlled up to +5 VDC. This is accomplished as shown

4K Block not used	2.2K on back of PC (pin 1 to pin 14)
A	IC 34
B	IC 35
C	IC 36
D	IC 37

WAIT STATES

Wait states are normally not required however they can be jumpered if your system needs them. To select wait states place a jumper between "W" and the number desired (1 throush 4). With no jumper, no wait states are inserted.

PHANTOM

If your computer requires PHANTOM it is easily jumperable to buss pin 67 by placing a jumper at the location marked PHANTOM.

BANK SELECT

This board supports CROMEMCO standard bank select which is a feature of some of their software. Bank select is a method of interchansing up to eisht 64K blocks of RAM under software control. This is accomplished by outputins a byte of data to Port 40H. Each bit (when hish) determines which bank is enabled. Bit 0 is Bank 1 and Bit 7 is Bank 8.

To select which bank this board is part of, place a jumper from the left side to the risht side at the point desisnated by the BANK # stenciled on the PC board. This socket for jumperins is at the lower risht side of the board.

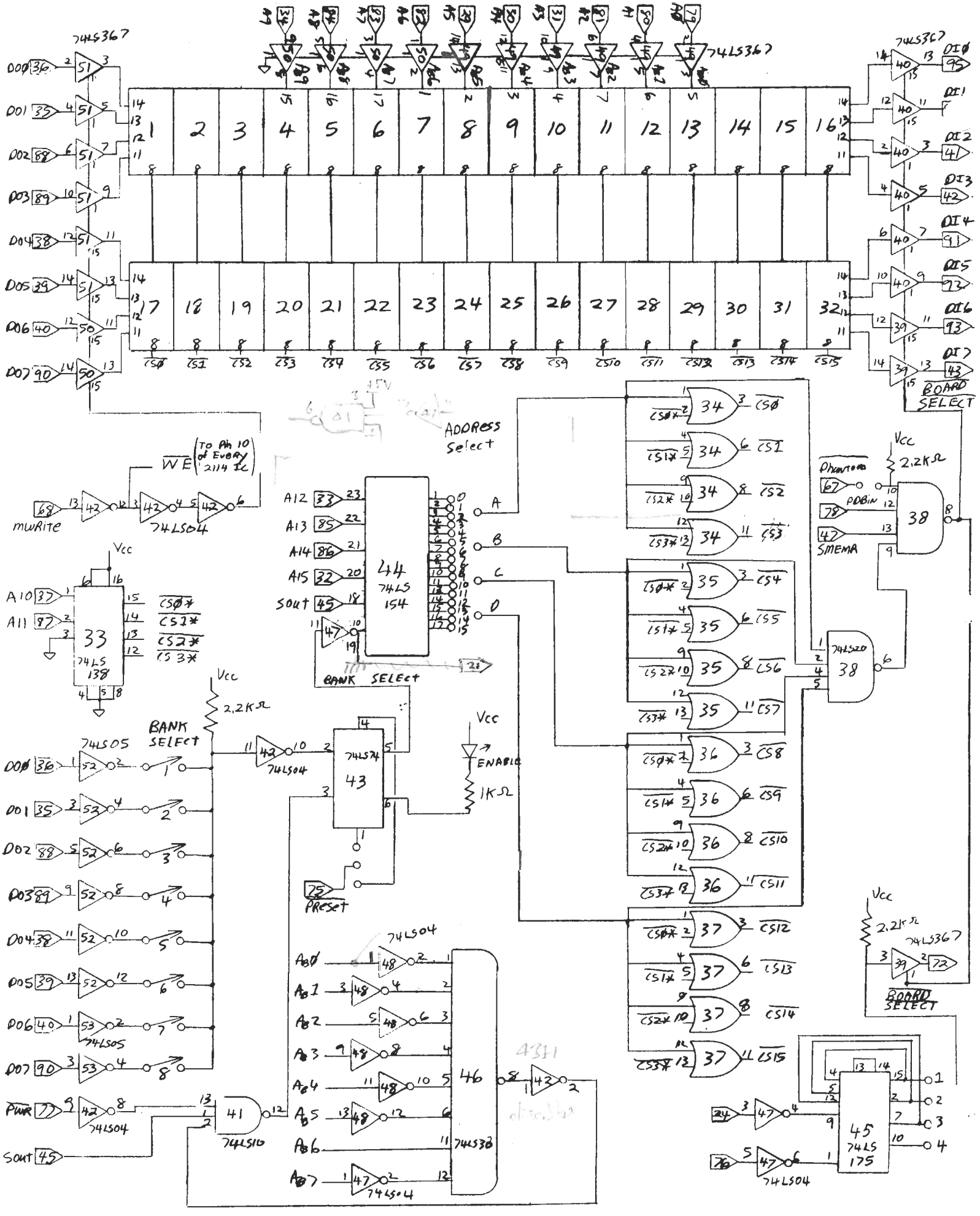
Also in the lower risht of the board is an area labeled RESET. A Jumper must be installed in this location such that a system reset will either enable or disable the board. Normally a jumper is placed from the ENABLE to the RESET pads. This will enable the board after a system reset. If, for example, the board is jumpered to be Bank 5 and it is not desired that BANK 5 be enabled after a system reset then the a jumper would placed between DISABLE and RESET. Now the only way the board could be enabled would be via software. Only one bank of upto 64K is enabled at one time.

THEORY OF OPERATION

This 16K board can reside in any of four 16K Ram areas available on the S-100 buss. IC 44 (74LS154) is used to decode the four hish order address (A12-A15) and senerates the outputs (0-15) brousht out to the address jumper area. IC 33 (74LS138) is used to decode addresses A10 and A11. The outputs of IC33 and IC44 are ORed (nesative losic AND) tosether to form the 16 Ram Chip Select sisnals. Addresses A0-A9 are buffered by IC's 49 and 50. The Write Enable sisnal required by the 2114 is senerated by invertins MWRITE from the buss (pin 68).
D00-D07 are buffered by IC's 50,51 which are enabled by the inverted MWRITE sisnal. This is data out of the CPU and in to the Ram board. D00-D07 are also inverted by IC52 and 53 the outputs of which are selected by the Bank Select Jumper area (Wired ORed) then inverted (by IC42) and fed into the Data input of FF IC43. IC's 46,47, 48, 42 and 41 decode output port 40 as the clock input of ic 43. The active hish output of IC43 is the Bank Select sisnal and is used to enable IC 44. The active low output is used to drive the Board Enable LED. The preset and clear inputs of IC 43 are jumperable to buss pin 75 (PRESET).

IC45 is confisured as a ripple counter which counts 02 and is cleared by PSYNC. IC45'S outputs are brousht out to jumpers. This allows sou to select how many 02's are counted before PSYNC clears the counter.

DI0-DI7 (data in to the CPU) are buffer by IC39 and 40. These are enabled by the output of IC38. The inputs of IC38 are comprised SMEMR,PDBIN, PHANTOM, and Board Select. Board Select is derived from the Jumpered outputs of IC 44.


74LS367
74LS367
74LS367
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
BOARD SELECT
ADDRESS Select
WE (TO Pin 10 of Every 2114 IC)
mWRite
74LS04
Vcc
2.2KΩ
Phantom
PDBIN
SMEMA
38
74LS20
38
A10
A11
33
74LS 138
A12
A13
A14
A15
SOUT
44
74LS 154
A
B
C
D
BANK SELECT
74LS05
74LS74
43
ENABLE
1KΩ
PRESET
74LS04
41
74LS10
46
74LS30
PWR
SOUT
74LS04
45
74LS 175
74LS04
BOARD SELECT

APPLICATIONS EXCHANGE

ALTAIR 8800 MEMORY CHECK PROGRAM

It seems that many of the members of S.C.C.S. are owners or soon to be owners of ALTAIR'S (myself included) and are in the first stages of going through the learning curve(s) of this "new" microcomputer technology. Building the hardware is only a small part of this hobby, because once everything is soldered together you're done. Software is where the real challenge and excitement come in. There is no "done" in software where you may sit back and say "I've done all the programs". There is no such point, as software can keep you occupied for years (I hope not on the same program). So to those members still in their learning curve I offer two basic programs for ALTAIR owners.

The first is a memory check program, of which there are several running around. This one is useful when you've just finished that new 4k board you bought from so-n-so and you're wondering if it's OK (memory chips do have a *small* failure rate).

The second is a cassette tape read and write program so you can dump all those programs you were playing with before you put your 8800 to bed and it forgets all it learned. This program was written to operate through the MITS Inc. Audio Cassette Interface, although any I/O parallel to serial modem operating around 2kHz should work Any medium quality recorder can be used.

The tape I/O port is addressed for control channel - 6 and data channel - 7 Put the bootstrap in manually, it will load the tape input program, which must be the first program recorded Make sure that the starting address of where the bootstrap is to start loading into memory is four addresses lower than where the body of the program being loaded is to start. This is because the boot is a dump type program and will load into memory the 4 preamble words that the output program places before each program it writes After the programs are initially entered the output program can be used to write itself onto tape.

SCOTT WILCOX
405-B No. Monterey
Alhambra, CA 91801

DESCRIPTION: This program checks any block of directly addressable memory for read/write data errors All possible bit patterns are read in and out of each memory location The program stops (enters a futile loop) and stores the address of the "bad" memory location and the data byte that execution failed on for three situations

1. a faulty memory location was encountered (data read did not equal data written)
2. a protected block of memory was encountered.
3. the program "stop memory check" address was set higher than the amount of memory actually in the machine

ADDRESS	MNEMONIC		COMMENT
000	LXI H,L	041	Load stop address of memory check
001		XXX	377 Example: Shows stopping at
002		XXX	037 end of 1st 8K block.
003	LXI D,E	021	Load start address of memory check
004		XXX	060 Start test just above
005		XXX	000 this program.
006	MVI A	076	
007		377	Initial check data
010	MOV A,B	107	Save data for comparison to memory read data
011	STAX D,E	022	
012	STA	062	Store data in case memory fails
013		056	
014		000	
015	LDAX D,E	032	Read data for comparison
016	CMP B	270	compare read/write data
017	JZ	312	Loop if no memory error
020		031	
021		000	

022	XCHG	353	
023	SHLD	042	Store address of bad memory
024		054	
025		000	
026	JMP	303	end of program futile loop
027		023	
030		000	
031	SUI	326	decrement check data
032		001	
033	JNC	322	loop if not final data case (000)
034		010	
035		000	
036	INX D,E	023	increment to next memory address
037	MOV D,A	172	
040	CMP H	274	
041	JNZ	302	loop if not last memory check address
042		006	
043		000	
044	MOV E,A	173	
045	CMP L	275	
046	JNZ	302	loop if not last memory check address
047		006	
050		000	
051	JMP	303	loop to store stop address
052		023	
053		000	
054		XXX	lo address of bad memory
055		XXX	hi address of bad memory
056		XXX	data case that memory failed on

LIMITATIONS: The program requires 46 bytes of known good memory and must not be located in a protected block of memory. Running time is approximately 30 sec. for each 4k of memory being checked

RUNNING THE MEMORY TEST

When the test is running properly most of the address lights on the front of the computer will be lit.You will be able to observe that several of the lights will be brighter than the others and will be working their way across from right to left as the program proceeds through the memory. If you are testing,for example, one 4K board in your system then you would use the start and stop addresses shown in the example. When the program is finished most of the address lights will go out and locations 54 and 55 will hold the address of the bad byte of memory or the address of the next byte above the stopping address.(i.e., the stopping address that you specified in the program)

64K MEMORY CHART

The chart below identifies (in hex and octal) the high order portion of the address for any given 1/4K of memory. Each 1/4K begins with low order address 00_{16} (000_8) and ends with FF_{16} (377_8). Each K is sectioned off for easy identification. Examples:

Section:	Begins with HX	Begins with OCT	Ends with HX	Ends with OCT
The 8th K	1C00	034 000	1FFF	037 377
The 3rd quarter of all 64K	8000	200 000	BFFF	277 377
The 2nd quarter of the 2nd K	0600	006 000	06FF	006 377
The 38th & 39th K	9400	224 000	9BFF	233 377

HX	OCT	K	HX	OCT	K	HX	OCT	K	HX	OCT	K	HX	OCT	K	HX	OCT	K	HX	OCT	K	HX	OCT	K
00	000	1	20	040	1	40	100	1	60	140	1	80	200	1	A0	240	1	C0	300	1	E0	340	1
01	001	2	21	041	2	41	101	2	61	141	2	81	201	2	A1	241	2	C1	301	2	E1	341	2
02	002	3	22	042	3	42	102	3	62	142	3	82	202	3	A2	242	3	C2	302	3	E2	342	3
03	003	1	23	043	9	43	103	17	63	143	25	83	203	33	A3	243	41	C3	303	49	E3	343	57
04	004	1	24	044	1	44	104	1	64	144	1	84	204	1	A4	244	1	C4	304	1	E4	344	1
05	005	2	25	045	2	45	105	2	65	145	2	85	205	2	A5	245	2	C5	305	2	E5	345	2
06	006	3	26	046	3	46	106	3	66	146	3	86	206	3	A6	246	3	C6	306	3	E6	346	3
07	007	2	27	047	10	47	107	18	67	147	26	87	207	34	A7	247	42	C7	307	50	E7	347	58
08	010	1	28	050	1	48	110	1	68	150	1	88	210	1	A8	250	1	C8	310	1	E8	350	1
09	011	2	29	051	2	49	111	2	69	151	2	89	211	2	A9	251	2	C9	311	2	E9	351	2
0A	012	3	2A	052	3	4A	112	3	6A	152	3	8A	212	3	AA	252	3	CA	312	3	EA	352	3
0B	013	3	2B	053	11	4B	113	19	6B	153	27	8B	213	35	AB	253	43	CB	313	51	EB	353	59
0C	014	1	2C	054	1	4C	114	1	6C	154	1	8C	214	1	AC	254	1	CC	314	1	EC	354	1
0D	015	2	2D	055	2	4D	115	2	6D	155	2	8D	215	2	AD	255	2	CD	315	2	ED	355	2
0E	016	3	2E	056	3	4E	116	3	6E	156	3	8E	216	3	AE	256	3	CE	316	3	EE	356	3
0F	017	4	2F	057	12	4F	117	20	6F	157	28	8F	217	36	AF	257	44	CF	317	52	EF	357	60
10	020	1	30	060	1	50	120	1	70	160	1	90	220	1	B0	260	1	D0	320	1	F0	360	1
11	021	2	31	061	2	51	121	2	71	161	2	91	221	2	B1	261	2	D1	321	2	F1	361	2
12	022	3	32	062	3	52	122	3	72	162	3	92	222	3	B2	262	3	D2	322	3	F2	362	3
13	023	5	33	063	13	53	123	21	73	163	29	93	223	37	B3	263	45	D3	323	53	F3	363	61
14	024	1	34	064	1	54	124	1	74	164	1	94	224	1	B4	264	1	D4	324	1	F4	364	1
15	025	2	35	065	2	55	125	2	75	165	2	95	225	2	B5	265	2	D5	325	2	F5	365	2
16	026	3	36	066	3	56	126	3	76	166	3	96	226	3	B6	266	3	D6	326	3	F6	366	3
17	027	6	37	067	14	57	127	22	77	167	30	97	227	38	B7	267	46	D7	327	54	F7	367	62
18	030	1	38	070	1	58	130	1	78	170	1	98	230	1	B8	270	1	D8	330	1	F8	370	1
19	031	2	39	071	2	59	131	2	79	171	2	99	231	2	B9	271	2	D9	331	2	F9	371	2
1A	032	3	3A	072	3	5A	132	3	7A	172	3	9A	232	3	BA	272	3	DA	332	3	FA	372	3
1B	033	7	3B	073	15	5B	133	23	7B	173	31	9B	233	39	BB	273	47	DB	333	55	FB	373	63
1C	034	1	3C	074	1	5C	134	1	7C	174	1	9C	234	1	BC	274	1	DC	334	1	FC	374	1
1D	035	2	3D	075	2	5D	135	2	7D	175	2	9D	235	2	BD	275	2	DD	335	2	FD	375	2
1E	036	3	3E	076	3	5E	136	3	7E	176	3	9E	236	3	BE	276	3	DE	336	3	FE	376	3
1F	037	8	3F	077	16	5F	137	24	7F	177	32	9F	237	40	BF	277	48	DF	337	56	FF	377	64

1024x4 Static Random Access Memory

SY2114

MEMORY PRODUCTS

Synertek®

MAY 1977

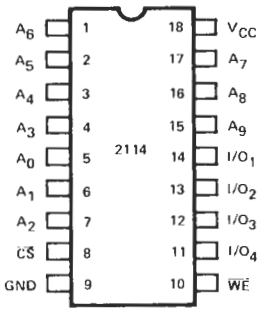
- 300 ns Maximum Access
- Low Operating Power Dissipation 0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clocks or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of bus oriented systems, and can drive 2 TTL loads.

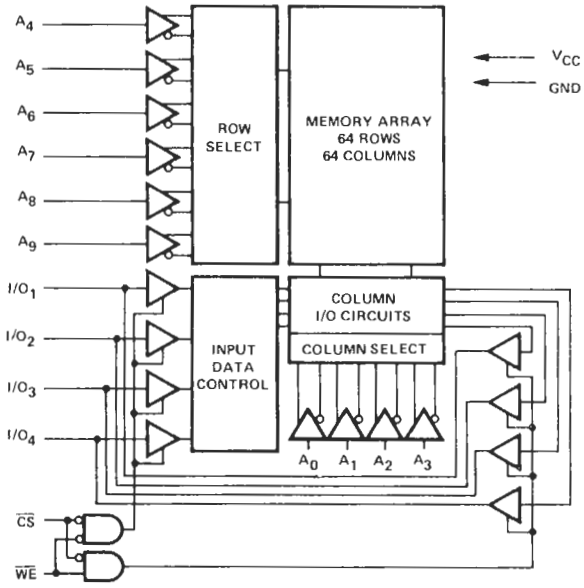
The SY2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.

PIN CONFIGURATION



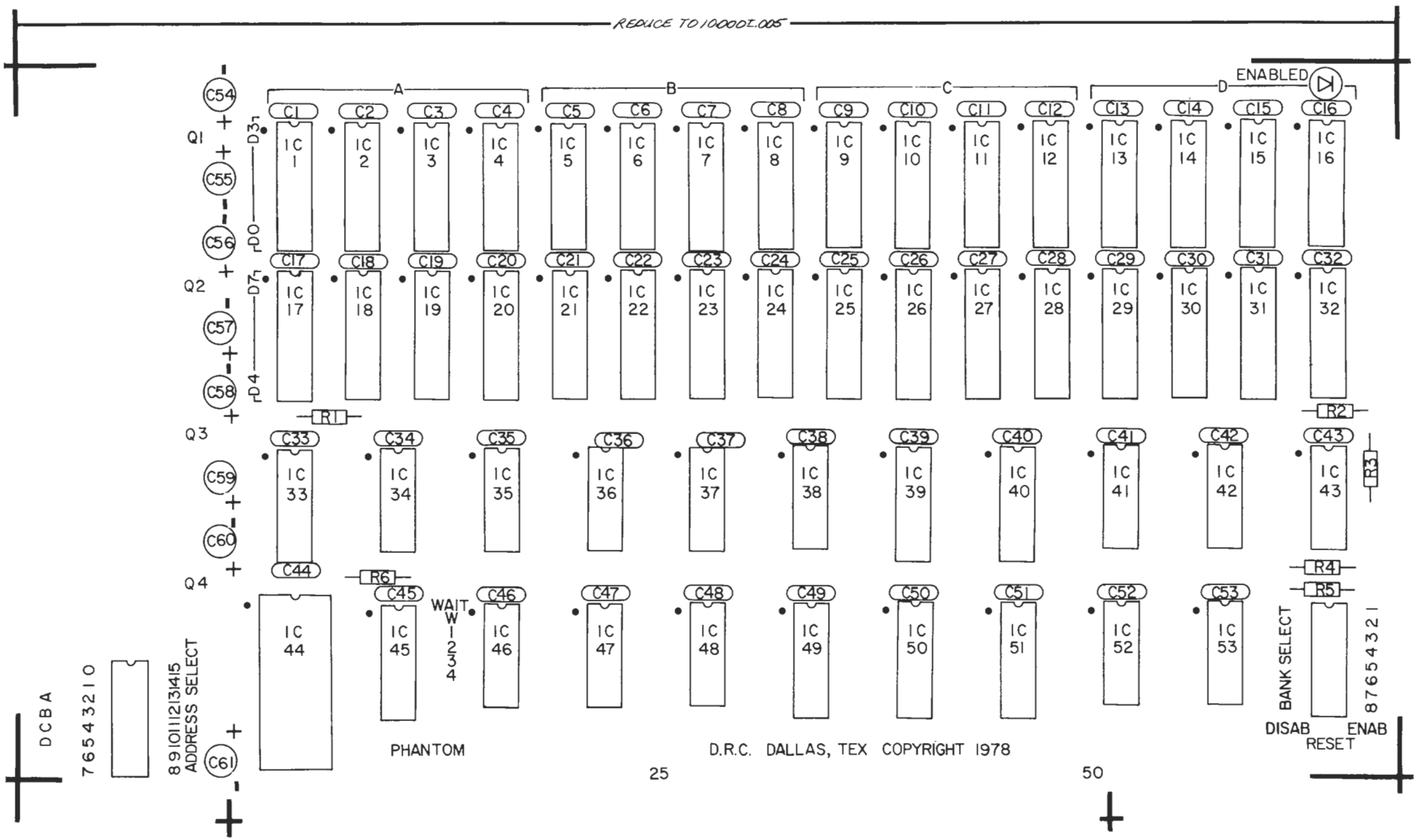
BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYC2114	Ceramic	450nsec	115mamp	0°C to 70°C
SYP2114	Molded	450nsec	115mamp	0°C to 70°C
SYC2114-3	Ceramic	300nsec	115mamp	0°C to 70°C
SYC2114L	Ceramic	450nsec	70mamp	0°C to 70°C
SYP2114L	Molded	450nsec	70mamp	0°C to 70°C

Synertek • P.O. Box 552 • Santa Clara, CA 95051 • Telephone (408) 984-8900 • TWX: 910-338-0135


REDUCE TO 10000I.005
A
B
C
D
ENABLED
C54
C55
C56
C57
C58
C59
C60
C61
Q1
Q2
Q3
Q4
D3
D0
D7
D4
C1 IC 1
C2 IC 2
C3 IC 3
C4 IC 4
C5 IC 5
C6 IC 6
C7 IC 7
C8 IC 8
C9 IC 9
C10 IC 10
C11 IC 11
C12 IC 12
C13 IC 13
C14 IC 14
C15 IC 15
C16 IC 16
C17 IC 17
C18 IC 18
C19 IC 19
C20 IC 20
C21 IC 21
C22 IC 22
C23 IC 23
C24 IC 24
C25 IC 25
C26 IC 26
C27 IC 27
C28 IC 28
C29 IC 29
C30 IC 30
C31 IC 31
C32 IC 32
R1
R2
R3
R4
R5
R6
C33 IC 33
C34 IC 34
C35 IC 35
C36 IC 36
C37 IC 37
C38 IC 38
C39 IC 39
C40 IC 40
C41 IC 41
C42 IC 42
C43 IC 43
C44 IC 44
C45 IC 45
C46 IC 46
C47 IC 47
C48 IC 48
C49 IC 49
C50 IC 50
C51 IC 51
C52 IC 52
C53 IC 53
WAIT
W
1
2
3
4
DCBA
7654321 0
8 9 10 11 12 13 14 15
ADDRESS SELECT
BANK SELECT
8 7 6 5 4 3 2 1
DISAB ENAB
RESET
PHANTOM
D.R.C. DALLAS, TEX COPYRIGHT 1978
25
50