IMSAI

PIC 8

PIC-8

FUNCTIONAL DESCRIPTION

The PIC-8 Priority Interrupt-Programmable Clock board provides the IMSAI 8080 Microcomputer System an eight level Priority Interrupt capability and a software-controlled interval clock.

The Priority Interrupt system utilizes the Intel 8214 Priority interrupt control unit and monitors the 8 Priority Interrupt lines on the 8080 back plane. The PIC-8 has the capability to service either single or multiple interrupt requests. When enabled and receiving an interrupt request, the Pic-8 determines if the request priority is higher than the software-controlled current priority, and if necessary issues a restart instruction that directs the 8080 system to one of eight priority controlled restart locations. For multiple interrupt requests, the 8214 determines the highest priority request, and processes it normally. It should be noted that the system does not store inactive requests, and that a peripheral device must hold an interrupt request until it is serviced by the microprocessor.

The current priority status register may be software set to any value desired to prevent low priority interrupts from being generated until the priority status register is reset to a lower value. The status register may be set to 0 if it is desired for all levels of interrupt to always occur.

The PIC-8 board also includes a clock circuit which provides programmed control at intervals ranging from .1 millisecond to 1 second. The program can select from among 3 jumper selected interval rates, or it can turn all three off. The 3 rates are jumper-selectable to any of the following values: .1 ms, .2 ms, 1 ms, 2 ms, 10 ms, 20 ms, 100 ms, 200 ms, or 1000 ms. Additionally, one bit of the DATA OUTPUT port is connected to a transistor and jumper pads for a special-purpose programmer-controlled output. Room is provided on the circuit board for a small speaker or other user-supplied circuitry. Also provided are 5 16-pin IC hole patterns with power and ground decoupling for special purpose user circuits. These hole patterns are drilled to accept wire wrap sockets.

Power on the board is regulated by an integrated circuit power regulator with current limiting protection. Tantalum ceramic bypass capacitors are supplied with the board. The board is G10-type double-sided laminate with plated through holes and contact fingers are gold-plated over nickel for reliable contact and long life.

PIC-8

THEORY OF OPERATION

Program control of the PIC-8 board is done entirely through one output port location. The address of this output port is jumper-selected in socket positions E4 and E5, and forms the input to the 8 input NAND gate (741s30). The output of this address select is ANDed with the Processor Write Strobe and Phase II clock and provides an output strobe which is used to latch the lower 4 bits of output data into the 8214 priority interrupt chip, and the upper 4 bits into the 7475 4 bit latch.

When the 8214 is ENABLED and one of the priority request lines is low the 8214 sets the output of a 2 GATE Flip-Flop low to request an interrupt from the 8080 processor. When the processor acknowledges the interrupt the Flip-Flop reset and 3 buffer drivers of the 8T98 are enabled to put interrupt request address on bits 3, 4, and 5 of the DATA IN bus. The remaining bits of the DATA are not driven, and remain high via pullup resistors on the MPU Board. The byte thus formed on the DATA IN bus is a restart instruction. with bits 3, 4, and 5 disecting the processor to one of eight restart locators.

Further details on the theory of operation of the 8214 chip can be found in the Intel Data Book.

The PIC-8 board also includes a software controlled interval clock. The clock circuit takes the Phase II clock running at two megahertz and divides it by 200 using a divide-by-two (7474) followed by two divide-by-10 sections (7490) to provide the .1 millisecond intervals.

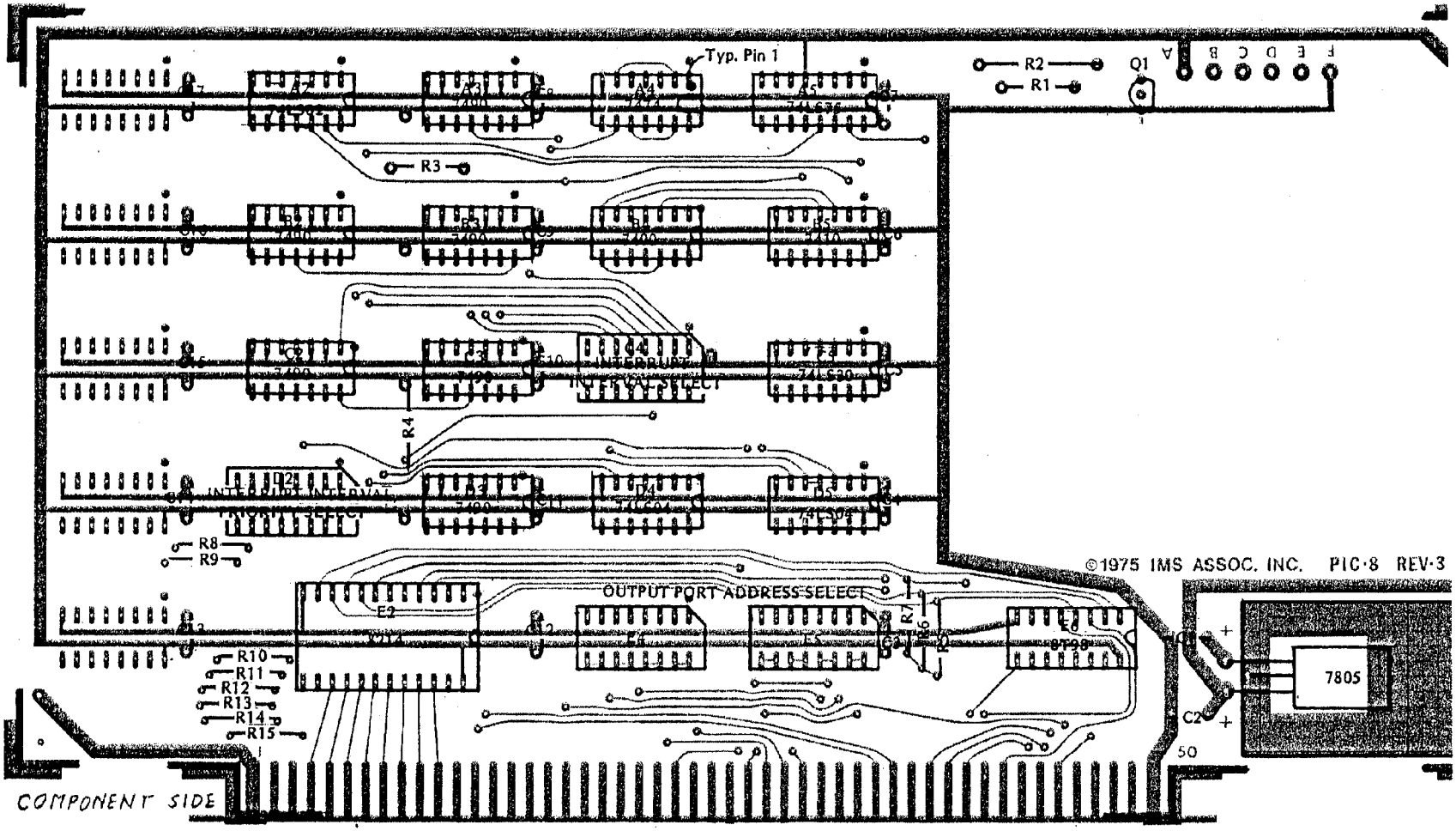
Four consecutive divide-by-10 7490's are then used to produce the other interval rates up to the longest rate of one second. Jumper selection is made from among these rates and ANDed with the output port bits 4, 5 and 6 and the output from the AND gate is used to drive the clock on the other half of the 7474 D type flip-flop. This section of the flip-flop is connected so that on successive clocks it will shift states and thus alternately request and remove the request for an interrupt.

When the processor system is running, and replying to the interrupts, shortly after the request is issued, the interrupt acknowledge line will become active in the low state and set this flip-flop to remove the interrupt

request so that the next time the clock line rises, the flip flop is again reset to request another interrupt. The interrupt request from this circuit is jumper-connected to any one of the priority interrupt lines and is handled by the 8214 circuitry exactly the same as any other peripheral board requesting an interrupt through the back plane would be.

Output bit 7 is used to drive the base of the transistor through a 1K resistor for current limiting, and the user supplied circuit to be driven is connected between the positive voltage and the collector current limiting resistor. Should just a voltage level be desired, as an output from this circuit, a resistor from 220 ohms to 1K ohm can be inserted in the collector circuit in the holes provided and a jumper placed between pads A and C to connect the top of the resistor to +5 volts. The output may be taken from point B which will be low when the bit is written as a 1 and will be high when the bit is written as a 0.

For a high impedance load, voltage swing will be nearly a full 5 volts for the high level and .3 volts for the low level. If a direct TTL level output is desired, it can be obtained from solder pad E if the 1K resistor in the base lead is removed and a jumper placed in its location and the transistor removed so as not to provide undesired load for a high level output.

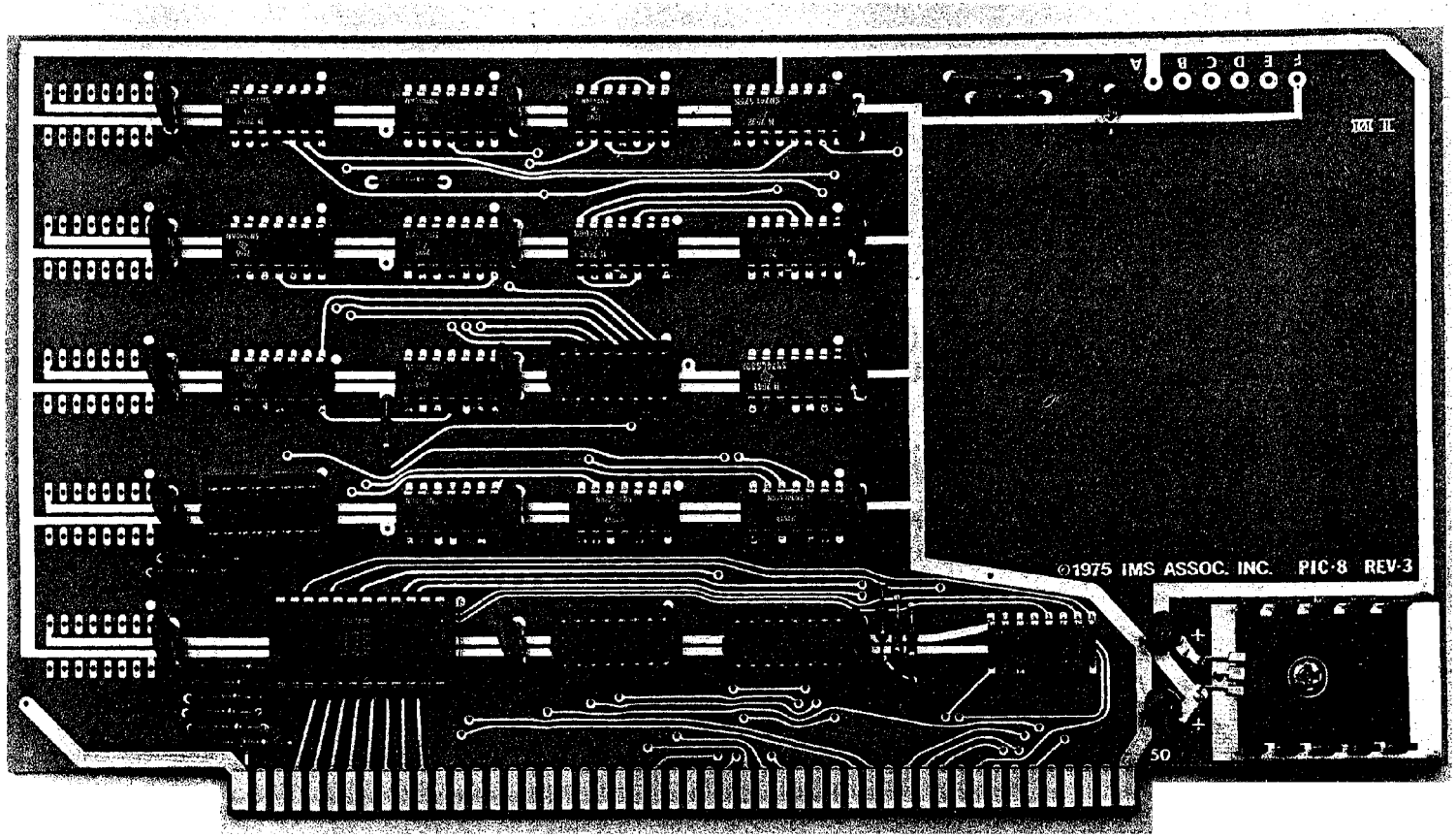


IMS Associates Inc.

ASSEMBLY DIAGRAM

PIC 8 REV 3 2/76

2/27/76



PIC 8 REV. 3

BOARD: PIC-8

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
7400	36-0740001	1	Quad 2 Input NAND/SN7400N
74LS02	36-0740202	1	Quad 2 Input NOR (Low Power Schottky)/ SN7402N
74LS04	36-0740402	2	Hex Inverter (LPS)/SN74LS04N
7410	36-0741001	1	Triple 3 Input NAND/SN7410N
74LS30	36-0743002	1	8 Input NAND (LPS)/SN74LS30N
7474	36-0747401	1	Dual D Flip-Flop, Preset and Clear/ SN7474N
74LS75	36-0747501	1	Quad Bistable Latch (LPS)/SN74LS75N
7490	36-0749001	6	Decode Counter/SN7490AN
7805	36-0780501	1	5V Positive Voltage Regulator/MC7805CP
8214	36-0821401	1	Priority Interrupt Control Unit/ P8214/S1260
Transistor	35-2000002	1	NPN Transistor/2N3904
8T98	36-0089801	1	Hex Tri-State Buffer/8T98
Capacitor	32-2010010	15	.1uF Disk Ceramic Capacitor
Heat Sink	16-0100002	1	Thermalloy/6106B-14
Header	23-4000001	4	16 Pin Integrated Circuit Header
PC Board	92-0000012	1	PIC-8, Rev. 1
Resistor	30-3220362	1	220 Ohm, ¼ Watt/red, red, brown
Resistor	30-4100362	14	1K Ohm, ¼ Watt/brown, black, red
Socket	23-0800001	4	16 Pin Solder Tail Socket
Socket	23-0800002	1	24 Pin Solder Tail Socket

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Capacitor	32-2233070	2	33-25 Tantalum Capacitor
Screw	20-3402001	1	6-32x3/8" Phillips Pan Head Machine
Nut	21-3120001	1	6-32 Hex Nut
Lockwasher	21-3350001	1	#6 Internal Star Lockwasher
Solder	15-0000001	5'	

ASSEMBLY INSTRUCTIONS

1) Unpack your board and check all parts against the parts lists enclosed in the package.

2) If gold contacts on the edge connector appear to be corroded, use pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any abrasive material as it will remove the gold plating.

RESISTOR INSTALLATION

3) Insert and solder each of the fourteen 1K ohm 1/4 watt resistors (brown/black/red) R1, R3 through R15. See Assembly Diagram for locations.

4) Insert and solder the one 220 ohm 1/4 watt resistor (red/red/brown) R2. See Assembly Diagram for location.

IC INSTALLATION

NOTE: When looking at component side of the board with edge connector down, all IC pin 1's point to the right hand side of the board and are indicated by small dots on the board.

5) Insert and solder the one 7400 at location B4.

6) Insert and solder the one 74LS02 at location A2.

7) Insert and solder each of the two 74LS04's at location D4 and D5.

8) Insert and solder the one 7410 at location B5.

9) Insert and solder the one 74LS30 at location C5.

10) Insert and solder the one 7474 at location A4.

11) Insert and solder the one 74LS75 at location A5.

12) Insert and solder each of the six 7490's at locations A3, B2, B3, C2, C3, and D3.

13) Insert and solder the one 8T98 at location E6.

DISCRETE COMPONENT INSTALLATION

14) Insert and solder each of the four 16 pin IC sockets at locations C4, D2, E4, and E5.

15) Insert and solder the one 24 pin IC socket at location E2.

16) Plug in each of the four 16 pin IC jumper headers in the four

16 pin IC sockets.

17) Insert and solder each of the fifteen .1 uf disk capacitors C3 through C17. See Assembly Diagram for locations.

18) Insert and solder each of the two 33uf tantalum capacitors C1 and C2. See Assembly Diagram for locations. Observe polarity as indicated on board.

19) Insert and solder the one 2N3904 NPN transistor Q1, orient as indicated on Assembly Diagram.

HEAT SINK AND REGULATOR INSTALLATION

20) Bend the leads of the 7805 regulator at 90° angles approximately 1/4" from the bottom edge of the regulator to facilitate insertion on top of the heat sink.

21) Insert the #6 screw through the regulator and heat sink and attached washer and nut from back side of board. NOTE: Be sure to hold the heat sink in proper vertical position while tightening the screw in order to prevent shorting to adjacent traces. Solder regulator leads.

22) Finally, plug the one 8214 24 pin IC into the 24 pin IC socket located at E2.

NOTE:

1) The 16 pin IC socket and header located at C4 is to be used for interrupt interval select.

2) The 16 pin IC socket and header located at D2 is to be used for interval priority select.

3) The two 16 pin IC sockets and header located at E4 and E5 are to be used for output port address select.

USER GUIDE

Request for an interrupt appears at the PIC-8 board in the form of one of the eight priority interrupt request lines being pulled to a logic 0 level. The 8214 chip will recognize that one or more interrupts are being requested and it will determine which multiple request has the highest priority.

The eight priority levels are numbered 0 through 7, with 7 being the highest priority. The priority level of the highest current interrupt request is then compared against the value stored in the current priority status register in bits 0, 1 and 2. If the currently-requested priority level is equal to or lower than the value stored in the current priority status register, no interrupt will be generated.

If the priority interrupt being requested is 0 and the current priority status register contains a 0, no interrupt will be generated. Thus, if a 5 were stored in the current priority status register, then only interrupt levels 6 and 7 would generate an interrupt. Interrupt levels 5 and lower would not be acted upon at this time.

If the priority interrupt being requested is 0, and the current priority status register contains a 0, no interrupt would be generated as the priority level is not greater than that stored in the current priority status register. If the current priority status register data bit 3 is written as a 1, the compare to the current priority status register is overridden, and the request for an interrupt priority 0 is acted upon and an interrupt to restart position 0 is generated.

If other priority level interrupts are requested during the time that data bit 3 has been written as a 1 in the current priority status level, then the highest priority interrupt requested will be acted upon.

At any time, if there is more than one priority level of interrupt being requested, only the highest priority level is acted upon, and any interrupt requests not serviced must be held present until the system can return to them.

After each interrupt has been generated, and the processor has responded to it, it is necessary that the current priority status register be restored to either the same or a different value; otherwise, no further interrupts will be generated.

When interrupts are initially enabled in a system, the current priority status register should also be initialized to insure that the interrupt generating system will respond to an interrupt.

It should be noted that the current priority status register inputs data bits 0, 1, and 2, are input in the complement form. Further information on the operation of the 8214 priority interrupt and coding can be located in the Intel Data Book.

The program controlled clock's functions are selected by both user jumpers and software. After jumpers have been installed in the interval selection and priority select sockets, writing to the PIC-8's output port address can enable the clock circuitry. Data bits 4, 5, and 6 control the user-selected intervals.

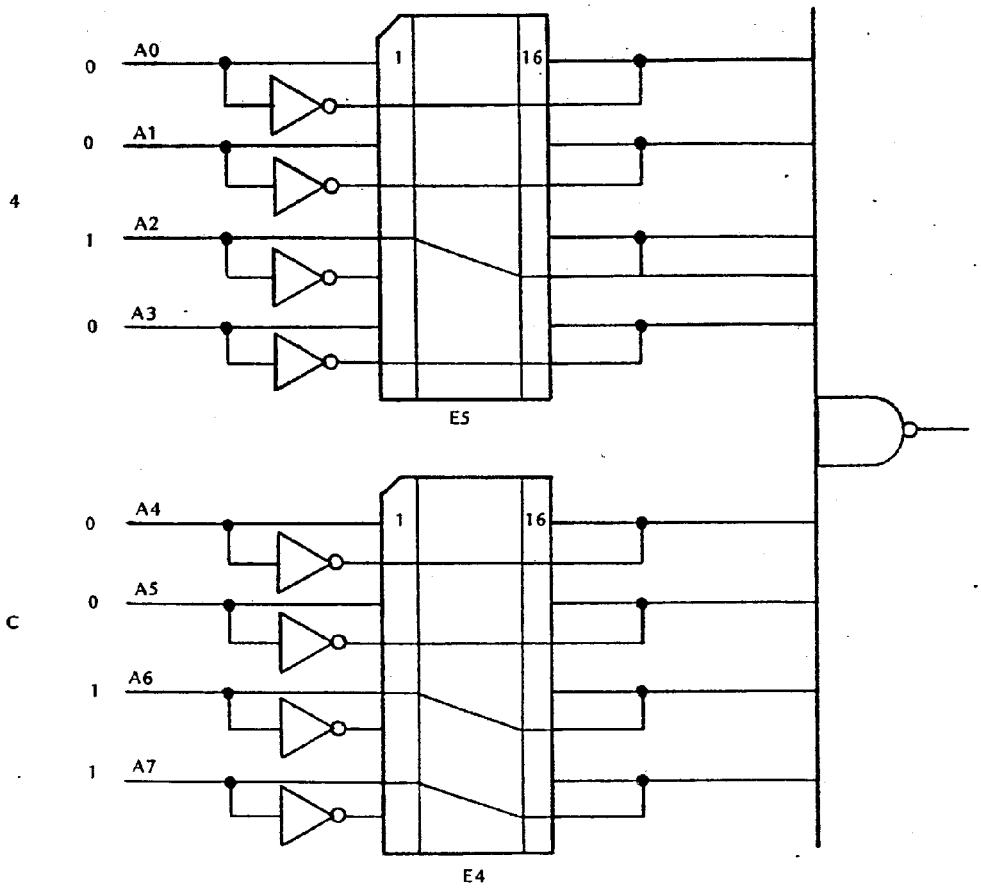
In normal use, only one interval will be selected at a time; thus, only one of the three bits, 4, 5, and 6 in the output port will be 1 at a given time. If two or more of these bits are written 1 at the same time, then the different rates will interact and interrupts will not occur continuously at the highest rate, but will occur at the highest rate for only portions of the time and not at all during other portions of the time as determined by the specific rates selected. For example, if both the rates 1 millisecond and 1 second are selected at the same time, one millisecond interrupts will be received for 1/2 of one second and then no interrupts will be received for the second half of that second and this pattern will repeat every second.

Should an interval interrupt not be acted upon in the time remaining between it's occurrence and the occurrence of the following interval interrupt request, the interrupt request will be taken away at the following pulse, and the request will again be asserted on the second interval following the first. This pattern of requesting an interrupt every other interval will continue until the system is able to respond to the interrupts within the time period required.

Whenever a byte is output to select or change the selection of the interrupt interval, it must be remembered that the lower 4 bits of the same output byte affect the interrupt generating circuitry, and will set it so that it is ready to respond to the next interrupt. The desired value for the current priority status register, must be present in the output bytes lower 4 bits every time a bit is output

for any purpose, whether it is to select or change the selection of the interrupt interval desired, or whether it is to change the current priority status register, or to output a bit 7 to the special purpose circuitry supplied by the user. Similarly, any time the output byte is used to set or change the current priority status level, bits 4, 5, and 6 must be also output according to the desired interrupt interval selected. Any bit which is written without changing does not cause any momentary glitches or other effects.

BOARD ADDRESSING



Positions E4 and E5 contain the user-jumpered 16-pin address selection sockets. These jumpers allow the PIC-8 board to respond to any 1 of the 256 possible I/O port addresses.

As shown on the schematic, to enable the CRI board it is necessary to have all eight inputs to the 74LS30 (C5) high. The user should select the desired address, and then jumper the address selection sockets so that when that address appears on address lines A0 through A7, all the NAND inputs are high, and the board is then enabled.

Each socket contains values of 4 lines and their complements. Socket E5 controls lines A0 through A3. Socket E4 controls lines A4 through A7. If the user-selected address presents a 1 on an address line, that line should be directly connected to the NAND input via a short wire jumper on the socket header. Conversely, if the user selected address presents a 0 on an address line, the inverted address line value should be connected to the NAND.

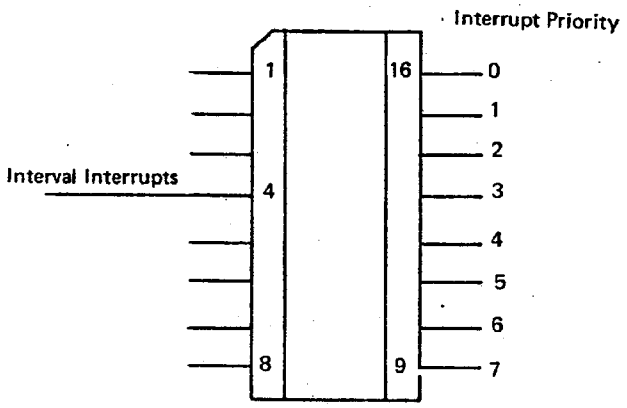
It is suggested that for lines jumpered to enable on a 1 value that the jumpers be placed diagonally across the socket (i.e., Pin 1 to Pin 15) and for lines jumpered for a 0 value, the jumper be placed straight across the header (i.e., Pin 2 to Pin 15). This convention allows easy visual determination of the selected address, for 1's appear as diagonals and 0's as horizontals. An example of a correctly jumpered socket pair for the address C4 hex or 304 octal is shown above.

If desired, very frequent address changes may be easily implemented through the exchange of an 8 pole DIP switch for each socket.

All 8 of the NAND inputs should be jumpered to respond to either a 1 or a 0. While any input left unconnected will appear to act as a 1, open inputs are very susceptible to noise pulses.

PRIORITY SELECT FOR THE INTERVAL GENERATING CIRCUIT

In position D2, the jumper socket permits the selection of the priority level at which the interrupts generated by the interval clock circuit will occur. The interrupt request level from the interval clock circuit appears on pin 4 of the jumper socket, and the eight available priority levels inputs appear on pins 9 through 16 of the jumper socket. A jumper should be placed between pin 4 and the pin corresponding to the priority level desired for the interval clock's interrupts.



CLOCK INTERVAL SELECTION

While 3 interrupt intervals may be program selected on the PIC-8 board, jumper selection from among the nine available interrupt intervals must be made in the jumper socket in position C4 to choose with three interrupt intervals the program is capable of selecting among. As indicated in the diagram, Pins 12, 13, and 14 on the jumper socket are the three inputs to the interrupt generating circuitry from among which port bits 4, 5, and 6 are used to select one or more of the levels to be active. A high level on

A transistor is provided to permit bit 7 to drive small loads such as a speaker or relay, and space is provided on the end of the board for such a device to be mounted. Connections to the driving transistor are made through solder paths available at the top of the board. If a small flat speaker is attached to the board here, and connected to the driving transistor, it will permit program control of audio pulses or tones which, in connection with the interrupt intervals available, allows for precise control of such things as musical notes rather than the empirical methods such as setting a small receiver beside the system and trying various different loops just to see what one gets. Since the program would have positive control of such a speaker, the output may be precisely calculated, and any modifications made with the assurance of the desired results.

The maximum current drawn by this output transistor should be held to 200 milliamperes or below. Provision is made on the board for a resistor in series with the open collector of this output transistor to limit the current to the desired value. A small speaker may be driven audibly by inserting a 220 ohm resistor in series with the collector and connecting the speaker between this resistor and the +8 volts on the board, using solder pads B and C.